

UR6515C

LINEAR INTEGRATED CIRCUIT

2A DDR BUS TERMINATION REGULATOR

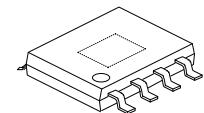
■ DESCRIPTION

The **UR6515C** is a linear regulator providing up to 2A transient peak current sourcing and sinking capability for DDR SDRAM bus terminator applications while regulating an output voltage to within 40mV. It contains a high speed operational amplifier which provides fast load transient response.

The **UR6515C** output termination voltage tracks the reference voltage applied at V_{REF} pin. A resistor divider connected to V_{IN} , GND and V_{REF} pins is used to force the reference voltage to V_{REF} pin. Additional features include current limiting protection and thermal shutdown protection.

■ FEATURES

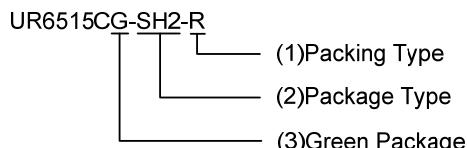
- * DDR1/ DDR2/DDR3 termination voltage applications
- * Sink and Source Current
- 2A Contious Current
- * Adjustable output voltage by external resistors
- * Integrated power MOS devices
- * Suspend to RAM(STR) functionality
- * Current Limiting Protection
- * Thermal Shutdown Protection
- * Cost-effective and easy to use



HSOP-8

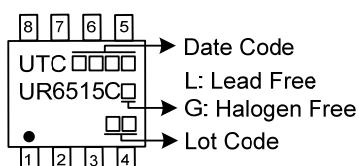
■ ORDERING INFORMATION

| Ordering Number | | Package | Packing |
|-----------------|----------------|---------|-----------|
| Lead Free | Halogen Free | | |
| UR6515CG-SH2-R | UR6515CG-SH2-R | HSOP-8 | Tape Reel |

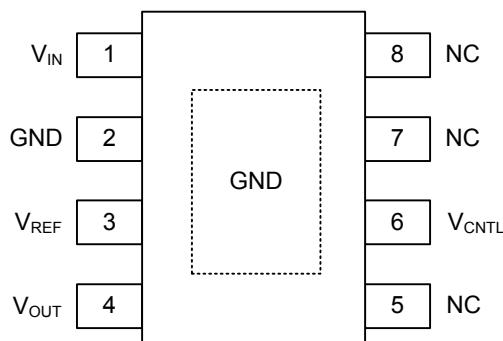


- (1)R: Tape Reel
- (2)SH2: HSOP-8
- (3)G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



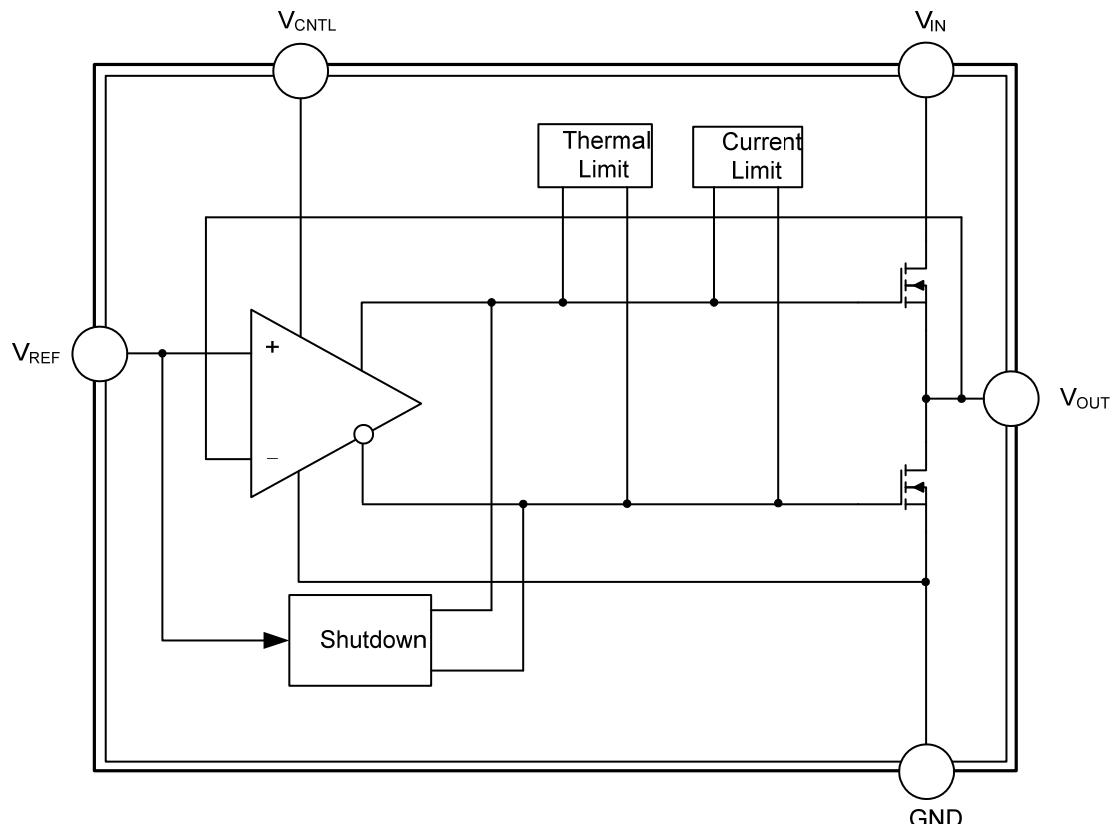
■ PIN CONFIGURATIONS



■ PIN DESCRIPTION

| PIN NO | PIN NAME | PIN DESCRIPTION |
|-------------|-------------------|---|
| 1 | V _{IN} | Power supply pin for the V _{OUT} output |
| 2 | GND | Ground pin |
| 3 | V _{REF} | Reference voltage input and active-low shutdown control pin |
| 4 | V _{OUT} | Output voltage pin |
| 5, 7, 8 | NC | No connect |
| 6 | V _{CNTL} | Power supply pin for the internal control circuits |
| Exposed Pad | GND | Ground pin |

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

| PARAMETER | SYMBOL | RATINGS | UNIT |
|--|-------------------|------------|------------------|
| V_{CNTL} Control Voltage | V_{CNTL} | +6 | V |
| V_{IN} Supply Voltage | V_{IN} | +6 | V |
| Power Dissipation ($T_A=25^\circ\text{C}$) | P_D | 1.33 | W |
| Junction Temperature | T_J | +125 | $^\circ\text{C}$ |
| Storage Temperature | T_{STG} | -65 ~ +150 | $^\circ\text{C}$ |

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

| PARAMETER | SYMBOL | RATINGS | UNIT |
|------------------------------|---------------|---------|---------------------------|
| Junction to Ambient (Note 1) | θ_{JA} | 75 | $^\circ\text{C}/\text{W}$ |
| Junction to Case | θ_{JC} | 28 | $^\circ\text{C}/\text{W}$ |

Note: θ_{JA} is measured in the natural convection at $T_A = 25^\circ\text{C}$ on a high effective thermal conductivity test board of JEDEC 51-7 thermal measurement standard.

■ RECOMMENDED OPERATING CONDITIONS (Note 1)

| PARAMETER | SYMBOL | RATINGS | UNIT |
|-----------------------------------|-------------------|--------------------------|------------------|
| V_{CNTL} Control Voltage | V_{CNTL} | 5 or $3.3 \pm 5\%$ | V |
| V_{IN} Supply Voltage | V_{IN} | $2.5 \sim 1.5 \pm 3\%$ | V |
| V_{REF} Input Voltage | V_{REF} | $1.25 \sim 0.75 \pm 3\%$ | V |
| Junction Temperature | T_J | -40 ~ +125 | $^\circ\text{C}$ |

Notes: 1. All voltage values are with respect to the network ground terminal unless otherwise noted.

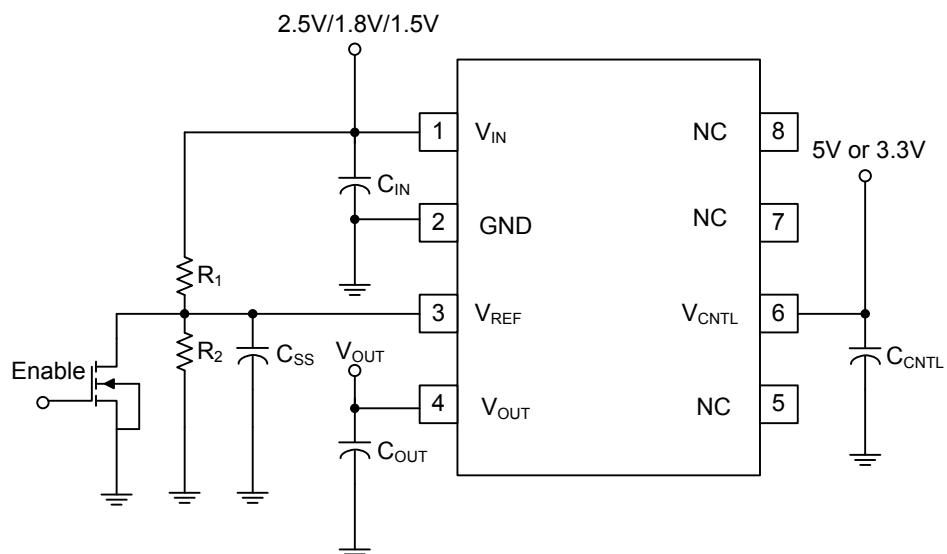
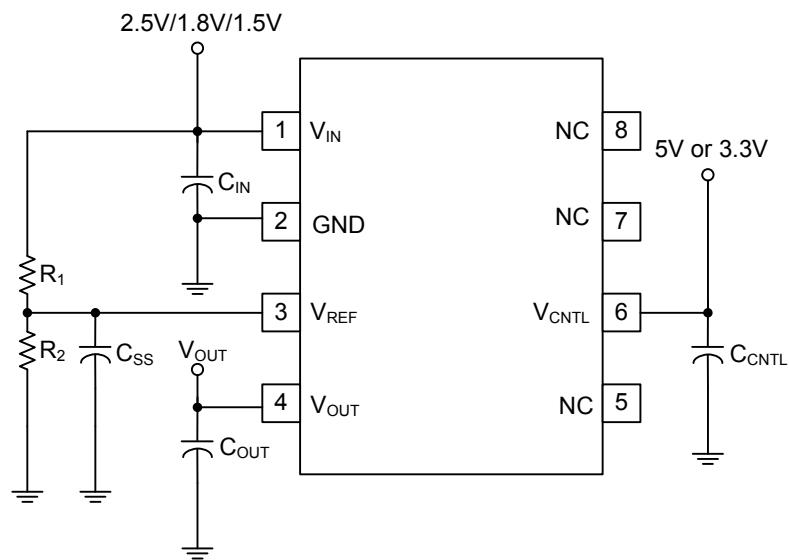
2. The V_{OUT} tracks the V_{REF} with additional voltage offset and load regulation.

■ ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$, unless otherwise specified)

($V_{\text{IN}}=2.5\text{V}/1.8\text{V}/1.5\text{V}$, $V_{\text{CNTL}}=3.3\text{V}$, $V_{\text{REF}}=1.25\text{V}/0.9\text{V}/0.75\text{V}$, $C_{\text{OUT}} = 10\mu\text{F}$ (Ceramic))

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--------------------------|--|-----|-----|-----|------------------|
| INPUT CURRENT | | | | | | |
| Operation Current of V_{CNTL} | I_{CNTL} | $I_{\text{OUT}} = 0\text{A}$ | | 1 | 2.5 | mA |
| Standby Current | I_{STB} | $V_{\text{REF}} < 0.2\text{V}$, $R_{\text{LOAD}} = 180\Omega$ | | 50 | 90 | μA |
| OUTPUT VOLTAGE (DDR/DDR II/DDR III) | | | | | | |
| Output Voltage Offset ($V_{\text{REF}} - V_{\text{OUT}}$) | V_{OS} | $I_{\text{OUT}} = 0\text{A}$ | -20 | | 20 | mV |
| Load Regulation | ΔV_{LOAD} | $I_{\text{OUT}} = \pm 2\text{A}$ | -20 | | 20 | mV |
| PROTECTION | | | | | | |
| Current Limit | I_{LIMIT} | $V_{\text{IN}} = 2.5\text{V}/1.8\text{V}/1.5\text{V}$ | 2.2 | | | A |
| Thermal Shutdown Temperature | T_{SD} | $V_{\text{CNTL}} = 3.3\text{V} \sim 5\text{V}$ | 125 | 170 | | $^\circ\text{C}$ |
| Thermal Shutdown Hysteresis | ΔT_{SD} | $V_{\text{CNTL}} = 3.3\text{V} \sim 5\text{V}$ | | 35 | | $^\circ\text{C}$ |
| V_{REF} Shutdown | | | | | | |
| Shutdown Threshold | V_{IH} | Enable | 0.6 | | | V |
| | V_{IL} | Shutdown | | | 0.2 | V |

■ TYPICAL APPLICATIONS CIRCUITS

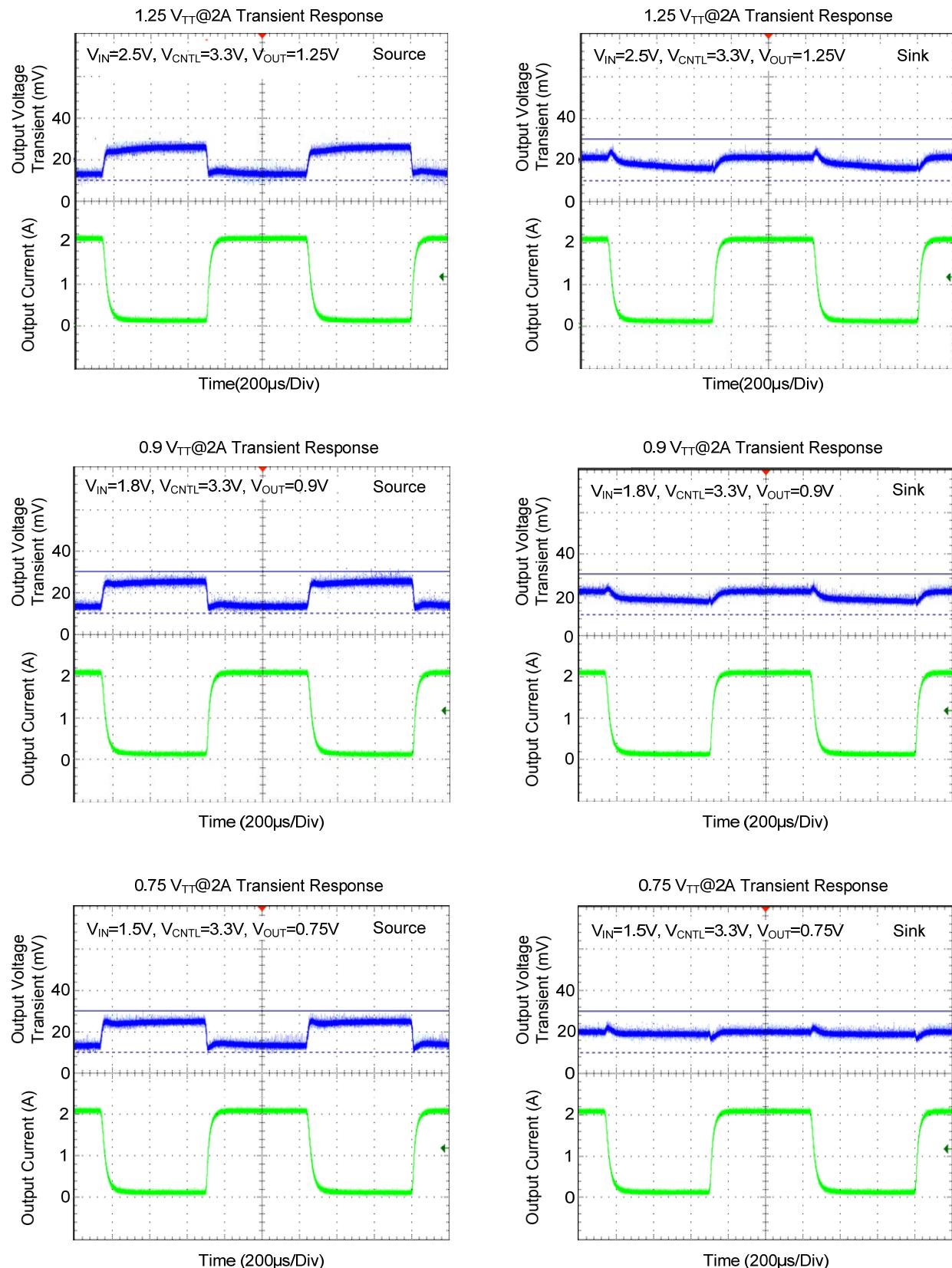


$R_1 = R_2 = 100\text{K}\Omega$, $C_{\text{OUT}} = 10\mu\text{F}$ (Ceramic)+ $1000\mu\text{F}$ under the worst case testing condition

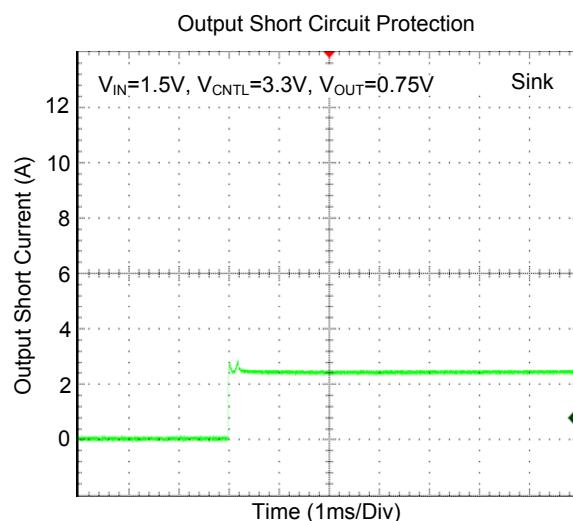
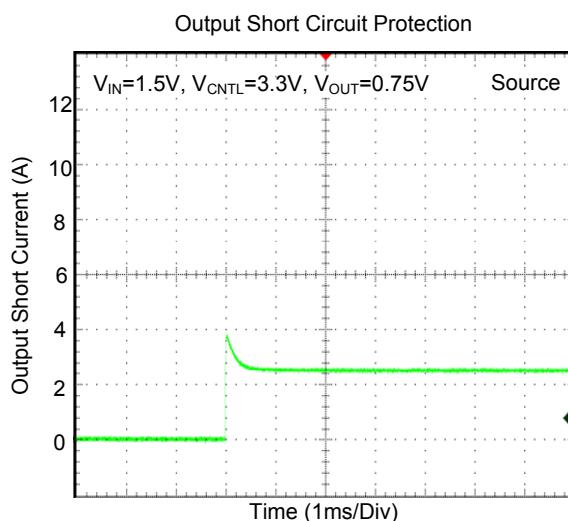
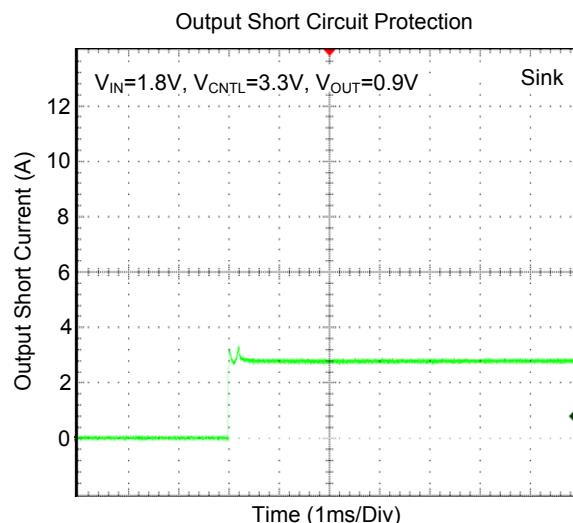
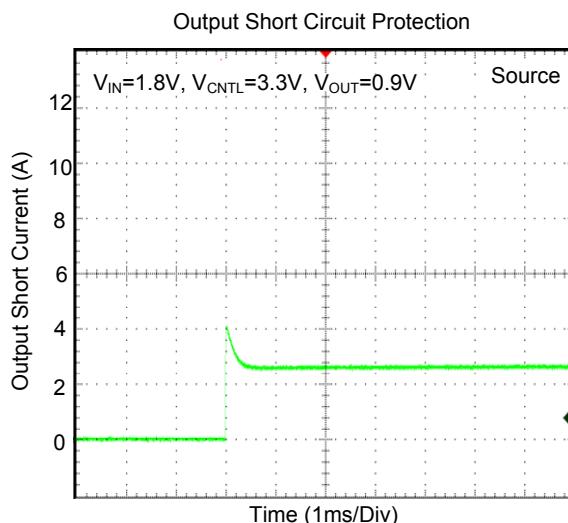
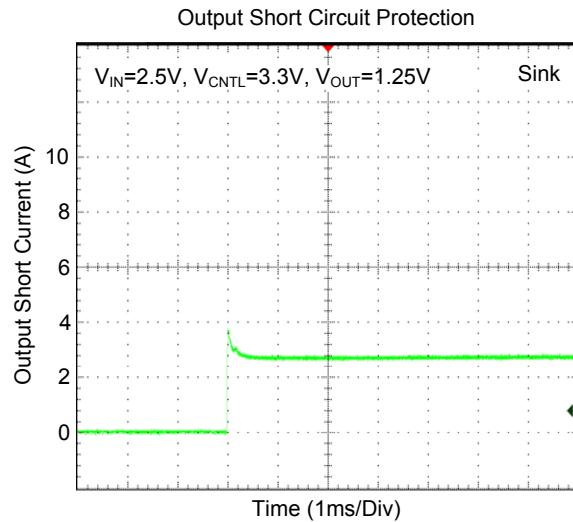
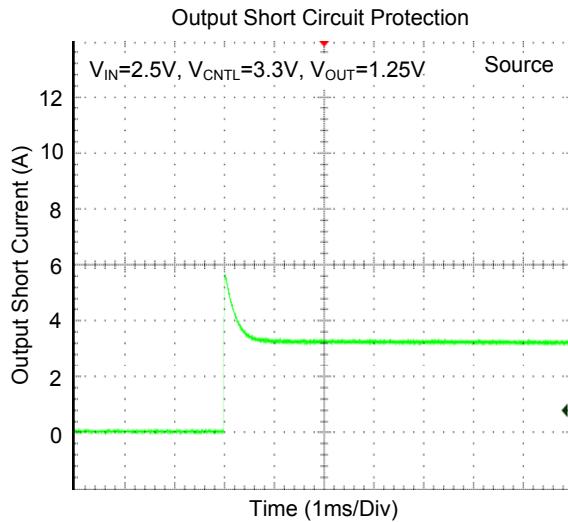
$C_{\text{SS}} = 1\mu\text{F}$, $C_{\text{IN}} = 470\mu\text{F}$ (Low ESR), $C_{\text{CNTL}} = 47\mu\text{F}$

$$V_{\text{REF}} = \frac{R_2}{R_1 + R_2} V_{\text{IN}}(\text{V}), \text{ V}_{\text{OUT}} \text{ track } V_{\text{REF}}$$

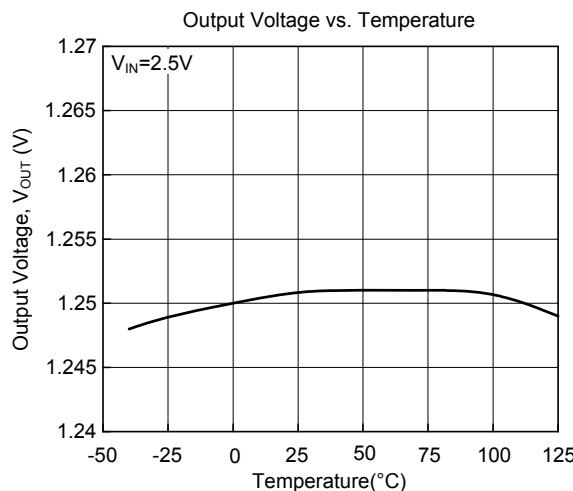
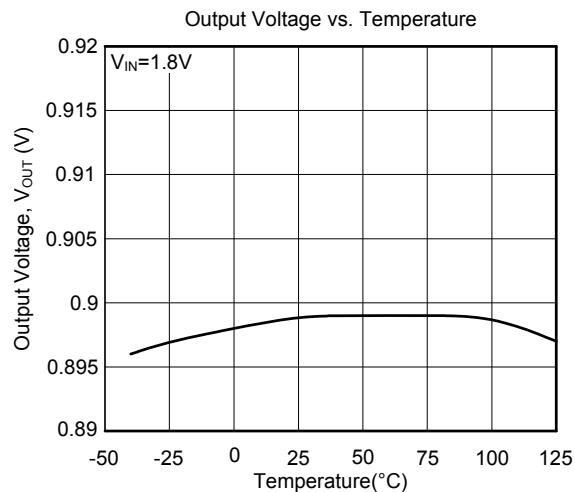
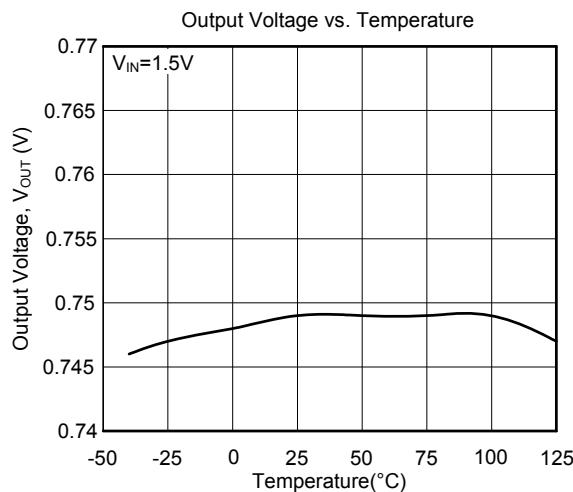
■ TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS (Cont.)



■ TYPICAL CHARACTERISTICS (Cont.)



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