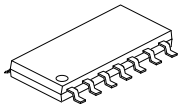
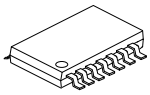
2-CHANNEL I²C BUS SWITCH WITH INTERRUPT LOGIC AND RESET



SOP-14



TSSOP-14

■ DESCRIPTION

The UTC **UCA9543** is a dual bidirectional translating switch controlled by the I²C bus. The SCL/SDA upstream pair fans out to two downstream pairs, or channels. Either individual SCn/SDn channel or both channels can be selected, determined by the contents of the programmable control register. Two interrupt inputs ($\overline{INT1}$ - $\overline{INT0}$), one for each of the downstream pairs, are provided. One interrupt output ($\overline{INT}$) acts as an AND of the two interrupt inputs.

An active-low reset ($\overline{RESET}$) input allows the UTC **UCA9543** to recover from a situation where one of the downstream I²C buses is stuck in a low state. Pulling $\overline{RESET}$ low resets the I²C state machine and causes both of the channels to be deselected, as does the internal power-on reset function.

The pass gates of the switches are constructed such that the V_{CC} pin can be used to limit the maximum high voltage, which will be passed by the UTC **UCA9543**. This allows the use of different bus voltages on each pair, so that 1.8V, 2.5V, or 3.3V parts can communicate with 5V parts without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O pins are 5.5V tolerant.

■ FEATURES

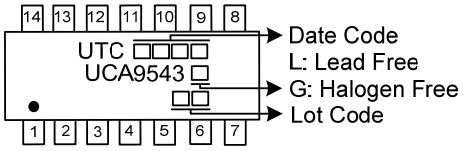
* 1-of-2 Bidirectional Translating Switches
* I²C Bus and SMBus Compatible
* Two Active-Low Interrupt Inputs
* Active-Low Interrupt Output
* Active-Low Reset Input
* Two Address Pins Allowing up to Four UTC **UCA9543** Devices on the I²C Bus
* Channel Selection Via I²C Bus, in Any Combination
* Power-up With All Switch Channels Deselected
* Low R_{ON} Switches
* Allows Voltage-Level Translation Between 1.8V, 2.5V, 3.3V and 5V Buses
* No Glitch on Power-up
* Supports Hot Insertion
* Low Standby Current
* Operating Power-Supply Voltage Range of 2.3V to 5.5V
* 5.5-V Tolerant Inputs
* 0 to 400-kHz Clock Frequency

■ ORDERING INFORMATION

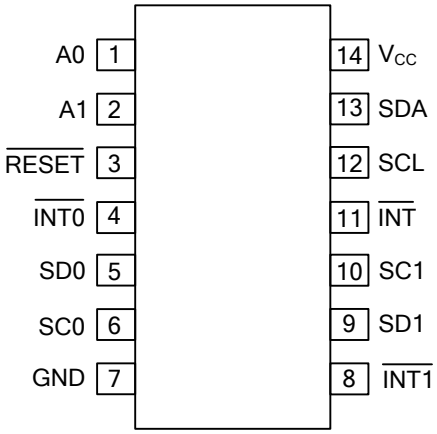
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UCA9543L-S14-R	UCA9543G-S14-R	SOP-14	Tape Reel
UCA9543L-P14-R	UCA9543G-P14-R	TSSOP-14	Tape Reel

UCA9543G-S14-R (1)Packing Type (2)Package Type (3)Green Package	 (1) R: Tape Reel (2) S14: SOP-14, P14: TSSOP-14 (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ PIN CONFIGURATION

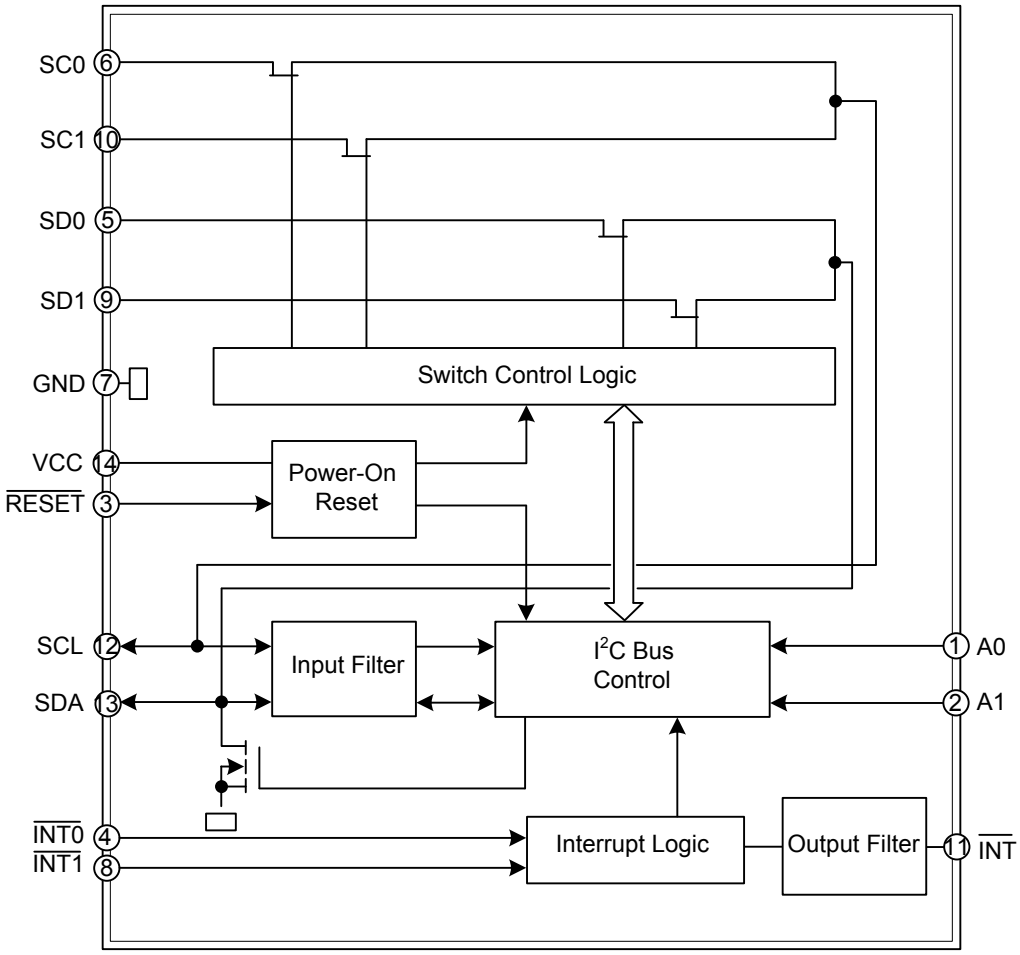


■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	A0	Address input 0. Connect directly to V_{CC} or ground.
2	A1	Address input 1. Connect directly to V_{CC} or ground.
3	$\overline{\text{RESET}}$	Active-low reset input. Connect to V_{CC} or V_{DPUM} (Note 1) through a pull-up resistor, if not used.
4	$\overline{\text{INT0}}$	Active-low interrupt input 0. Connect to V_{DPU0} (Note 1) through a pull-up resistor.
5	SD0	Serial data 0. Connect to V_{DPU0} (Note 1) through a pull-up resistor.
6	SC0	Serial clock 0. Connect to aV_{DPU0} (Note 1) through a pull-up resistor.
7	GND	Ground
8	$\overline{\text{INT1}}$	Active-low interrupt input 1. Connect to V_{DPU1} (Note 1) through a pull-up resistor.
9	SD1	Serial data 1. Connect to V_{DPU1} (Note 1) through a pull-up resistor.
10	SC1	Serial clock 1. Connect to V_{DPU1} (Note 1) through a pull-up resistor.
11	$\overline{\text{INT}}$	Active-low interrupt output. Connect to V_{DPUM} (Note 1) through a pull-up resistor.
12	SCL	Serial clock line. Connect to V_{DPUM} (Note 1) through a pull-up resistor.
13	SDA	Serial data line. Connect to V_{DPUM} (Note 1) through a pull-up resistor.
14	V_{CC}	Supply power

Note: V_{DPUX} is the pull-up reference voltage for the associated data line. V_{DPUM} is the master I^2C reference voltage while V_{DPU0} and V_{DPU1} are the slave channel reference voltages

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

over operating free-air temperature range (unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
Input Voltage Range (Note 2)	V_I	-0.5 ~ 7	V
Input Current	I_I	±20	mA
Output Current	I_O	±25	mA
Continuous Current through V_{CC}		±100	mA
Continuous Current through GND		±100	mA
Operating Free-Air Temperature Range	T_A	-40 ~ +85	°C
Storage Temperature	T_{STG}	-60 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOP-14	θ_{JA}	86	°C/W
	TSSOP-14		113	°C/W

■ RECOMMENDED OPERATING CONDITIONS (NOTE 1)

PARAMETER			SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage			V_{CC}	2.3		5.5	V
High-Level Input Voltage	SCL, SDA		V_{IH}	0.7 × V_{CC}		6	V
	A1, A0, $\overline{INT1}$, $\overline{INT0}$, $\overline{RESET}$	V_{CC}=2.3V~3.6V		0.7 × V_{CC}		V_{CC}+0.5	V
		V_{CC}=3.6V~4.5V		0.7 × V_{CC}		V_{CC}+0.5	V
		V_{CC}=4.5V~5.5V		0.7 × V_{CC}		V_{CC}+0.5	V
Low-Level Input Voltage	SCL, SDA		V_{IL}	-0.5		0.3×V_{CC}	V
	A1, A0, $\overline{INT1}$, $\overline{INT0}$, $\overline{RESET}$			-0.5		0.3×V_{CC}	V

Note: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

■ ELECTRICAL CHARACTERISTICS (NOTE 1)

over recommended operating free-air temperature range (unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Power-On Reset Voltage		V_{POR}	No Load: V_I=V_{CC} or GND (Note 2)			1.6	2.1	V
Switch Output Voltage		V_{pass}	V_{CC}=5V	V_{SWin}=V_{CC}, I_{SWout} =-100μA		3.6		V
			V_{CC}=4.5V~ 5.5V		2.6		4.5	V
			V_{CC}=3.3V			1.9		V
			V_{CC}=3V~3.6V		1.6		2.8	V
			V_{CC}=2.5V			1.5		V
			V_{CC}=2.3V~2.7V		1.1		2	V
High-Level Output Current	$\overline{INT}$	I_{OH}	V_{CC}=2.3V~2.7V, V_O=V_{CC}				100	μA
Low-Level Output Current	SDA	I_{OL}	V_{CC}=2.3V~5.5V	V_{OL}=0.4V	3	7		mA
				V_{OL}=0.6V	6	10		mA
	$\overline{INT}$			V_{OL}=0.4V	3			mA

■ ELECTRICAL CHARACTERISTICS (NOTE 1) (Cont.)

over recommended operating free-air temperature range (unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input Leakage	SCL, SDA	$I_{I(LEAK)}$	V_{CC}=2.3V~ 5.5V	V_I=V_{CC} or GND	-1		1	μA
	SC1-SC0		V_{CC}=2.3V~ 3.6V		-1		1	μA
			V_{CC}=4.5V~ 5.5V		-1		100	μA
	A1, A0		V_{CC}=2.3V~ 3.6V		-1		1	μA
			V_{CC}=4.5V~ 5.5V		-1		50	μA
	$\overline{INT1}$ - $\overline{INT0}$		V_{CC}=2.3V~ 3.6V		-1		1	μA
			V_{CC}=4.5V~ 5.5V		-1		50	μA
	$\overline{RESET}$		V_{CC}=2.3V~ 3.6V		-1		1	μA
			V_{CC}=4.5V~ 5.5V		-1		50	μA
Operating Mode	f_{SCL}=100kHz	I_{CC}	V_{CC}=5.5V	V_I=V_{CC} or GND, I_O=0		17	50	μA
			V_{CC}=3.6V			6	20	μA
			V_{CC}=2.7V			3	16	μA
Standby Mode	Low Inputs		V_{CC}=5.5V	V_I=GND, I_O=0		0.3	1	μA
			V_{CC}=3.6V			0.1	1	μA
			V_{CC}=2.7V			0.1	1	μA
	High Inputs		V_{CC}=5.5V	V_I=V_{CC}, I_O=0		0.3	1	μA
			V_{CC}=3.6V			0.1	1	μA
			V_{CC}=2.7V			0.1	1	μA
Supply-Current Change	$\overline{INT1}$ - $\overline{INT0}$	ΔI_{CC}	V_{CC}=2.3V~ 5.5V One $\overline{INT1}$ - $\overline{INT0}$ Input at 0.6V, Other Inputs at V_{CC} or GND			8	20	μA
			V_{CC}=2.3V~ 5.5V One $\overline{INT1}$ - $\overline{INT0}$ Input at V_{CC}-0.6V, Other Inputs at V_{CC} or GND			8	20	μA
	SCL, SDA		V_{CC}=2.3V~ 5.5V, SCL or SDA Input at 0.6V, Other Inputs at V_{CC} or GND			8	20	μA
			V_{CC}=2.3V~ 5.5V, SCL or SDA Input at V_{CC}-0.6V, Other Inputs at V_{CC} or GND			8	20	μA
Input Capacitance	A1, A0	C_I	V_{CC}=2.3V~3.6V	V_I=V_{CC} or GND		4	5	pF
			V_{CC}=4.5V~5.5V			4	5	pF
	$\overline{INT1}$ - $\overline{INT0}$		V_{CC}=2.3V~3.6V			4	6	pF
			V_{CC}=4.5V~5.5V			4	6	pF
	$\overline{RESET}$		V_{CC}=2.3V~3.6V			4	5	pF
			V_{CC}=4.5V~5.5V			4	5	pF
	SCL		V_{CC}=2.3V~5.5V			9	12	pF
Output Capacitance	SDA	$C_{IO(OFF)}$ (Note 3)	V_{CC}=2.3V~5.5V, V_I=V_{CC} or GND, Switch OFF			11	13	pF
	SC1-SC0, SD1-SD0					6	8	pF
Switch On-State Resistance		R_{ON}	V_{CC}=4.5V~5.5V	V_O=0.4V, I_O=15mA	4	9	20	Ω
			V_{CC}=3V~3.6V		5	11	25	Ω
			2.3V~ 2.7V , V_O=0.4V, I_O=10mA		7	16	50	Ω

Notes: 1. For operation between published voltage ranges, refer to the worst-case parameter in both ranges.

2. To reset the part, either $\overline{RESET}$ must be low or V_{CC} must be lowered to 0.2V.

3. $C_{IO(ON)}$ depends on the device capacitance and load that is downstream from the device.

■ I²C INTERFACE TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise specified) (see Figure 1)

PARAMETER		SYMBOL	STANDARD MODE I²C BUS			FAST MODE I²C BUS			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	UNIT
I²C Clock Frequency		f_{scl}	0		100	0		400	kHz
I²C Clock High Time		t_{sch}	4			0.6			μs
I²C Clock Low Time		t_{scl}	4.7			1.3			μs
I²C Spike Time		t_{sp}			50			50	ns
I²C Serial-Data Setup Time		t_{sds}	250			100			ns
I²C Serial-Data Hold Time		t_{sdh}	0 (Note 1)			0 (Note 1)			μs
I²C Input Rise Time		t_{icr}			1000	20 +0.1Cb (Note 2)		300	ns
I²C Input Fall Time		t_{icf}			300	20 +0.1Cb (Note 2)		300	ns
I²C Output Fall Time	10-pF to 400-pF Bus	t_{ocf}			300	20 +0.1Cb (Note 2)		300	ns
I²C Bus Free Time between Stop and Start		t_{buf}	4.7			1.3			μs
I²C Start or Repeated Start Condition Setup		t_{sts}	4.7			0.6			μs
I²C Start or Repeated Start Condition Hold		t_{sth}	4			0.6			μs
I²C Stop Condition Setup		t_{sps}	4			0.6			μs
Valid-Data Time (High to Low) (Note 3)	SCL Low to SDA Output Low Valid	$t_{vdL(Data)}$			1			1	μs
Valid-Data Time (Low to High) (Note 3)	SCL Low to SDA Output High Valid	$t_{vdH(Data)}$			0.6			0.6	μs
Valid-Data Time of ACK Condition	ACK Signal from SCL Low to SDA Output Low	$t_{vd(ack)}$			1			1	μs
I²C bus capacitive load		C_b			400			400	pF

Notes: 1. A device internally must provide a hold time of at least 300 ns for the SDA signal (referred to as the V_{IH} min of the SCL signal), in order to bridge the undefined region of the falling edge of SCL.

2. C_b = total bus capacitance of one bus line in pF.

3. Data taken using a 1kΩ pull-up resistor and 50-pF load (see Figure 1)

■ SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L \leq 100pF$ (unless otherwise specified) (see Figure 3)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay Time input (SDA or SCL) to output(SDn or SCn)	t_{pd} (Note 1)	R_{ON}=20Ω, C_L=15pF			0.3	ns
		R_{ON}=20Ω, C_L=50pF			1	ns
Interrupt Valid Time (Note 2) input ($\overline{INTn}$) to output($\overline{INT}$)	t_{iv}				4	μs
Interrupt Reset Delay Time(Note 2) input ($\overline{INTn}$) to output($\overline{INT}$)	t_{ir}				2	μs

Notes: 1. The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
2. Data taken using a 4.7-kΩ pull-up resistor and 100-pF load (see Figure 3)

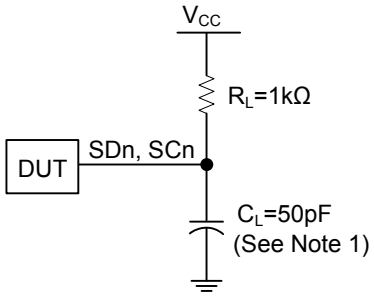
■ INTERRUPT AND RESET TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise specified) (see Figure 3)

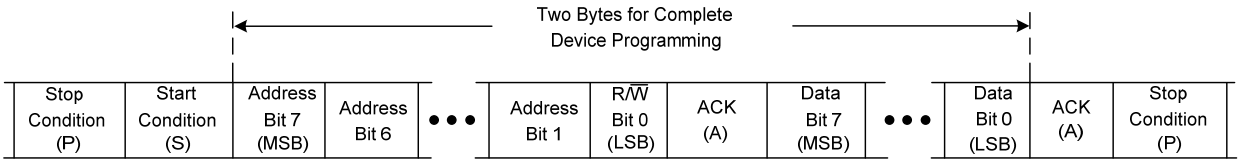
PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Required Low-Level Pulse Duration of $\overline{INTn}$ Inputs (Note 1)	t_{PWRL}	1			μs
Required High-Level Pulse Duration of $\overline{INTn}$ Inputs (Note 1)	t_{PWRH}	0.5			μs
Pulse Duration, $\overline{RESET}$ Low	t_{WL}	4			ns
$\overline{RESET}$ Time (SDA Clear)	t_{rst} (Note 2)			500	ns
Recovery Time from $\overline{RESET}$ to Start	t_{REC}	0			ns

Notes: 1. The device has interrupt input rejection circuitry for pulses less than the listed minimum.
2. t_{rst} is the propagation delay measured from the time the $\overline{RESET}$ pin is first asserted low to the time the SDA pin is asserted high, signaling a stop condition. It must be a minimum of t_{WL}.

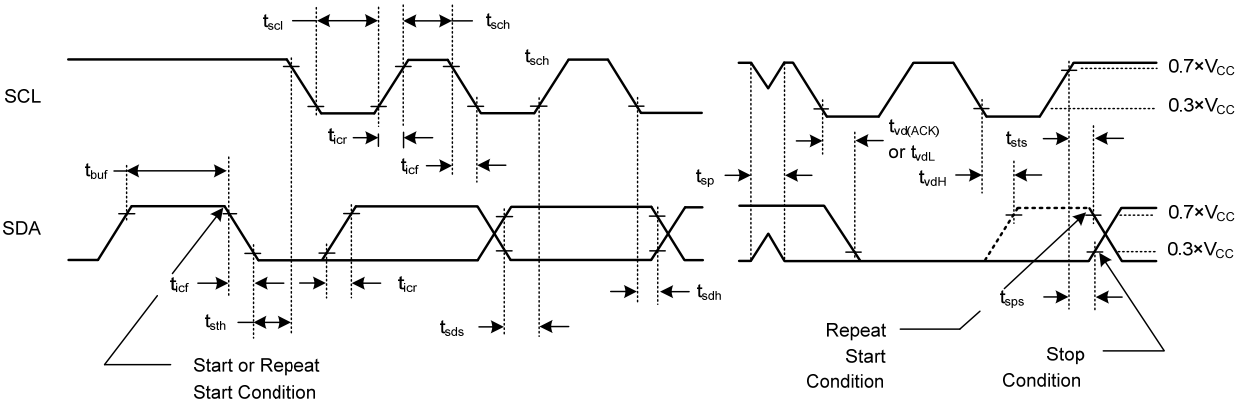
■ PARAMETER MEASUREMENT INFORMATION



I^2C PORT LOAD CONFIGURATION



BYTE	DESCRIPTION
1	I^2C address + R/$\overline{W}$
2	Control register data



VOLTAGE WAVEFORMS

Notes: 1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, Z_O=50Ω, t_r/t_f=30ns.
3. The outputs are measured one at a time, with one transition per measurement.

Figure 1. I^2C Interface Load Circuit, Byte Descriptions, and Voltage Waveforms

■ PARAMETER MEASUREMENT INFORMATION (Cont.)

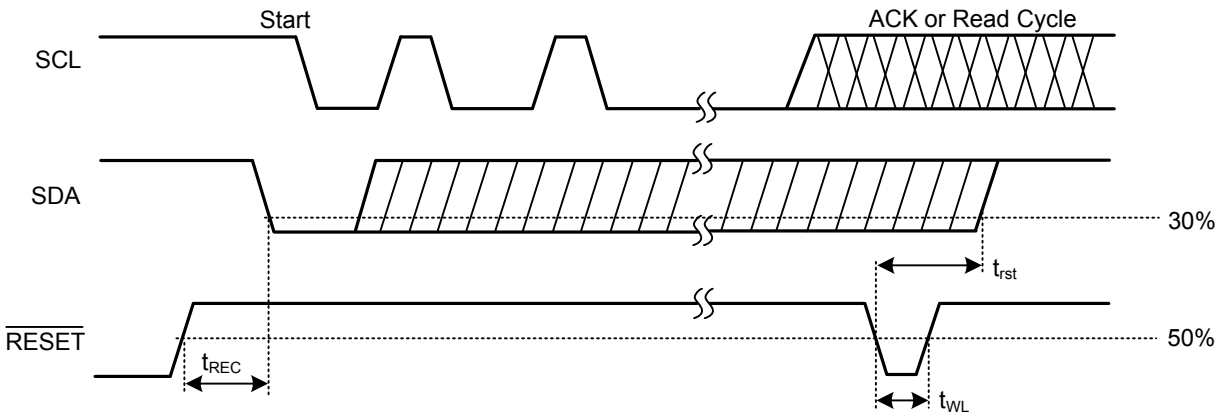
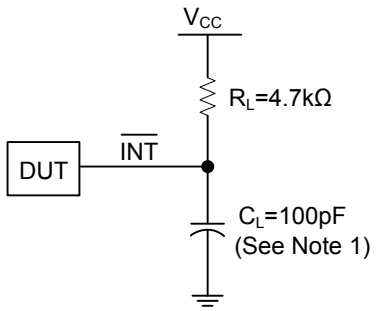
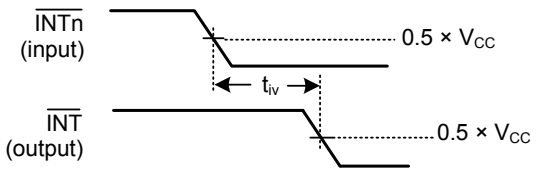


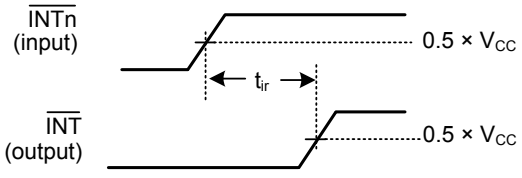
Figure 2. Reset Timing



INTERRUPT LOAD CONFIGURATION



VOLTAGE WAVEFORMS (t_{iv})



VOLTAGE WAVEFORMS (t_{ir})

Notes: 1. C_L includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics: PRR ≤1MHz, Z_O= 50Ω,tr≤3ns,tf≤3ns.

Figure 3. Interrupt Load Circuit and Voltage Waveforms

■ FEATURE DESCRIPTION

The UTC **UCA9543** is a dual channel bidirectional translating switch for I^2C buses that supports Standard-Mode (100 kHz) and Fast-Mode (400 kHz) operation. The UTC **UCA9543** features I^2C control using a single 8-bit control register in which bits 1 and 0 control the enabling and disabling of the two switch channels of I^2C data flow. The UTC **UCA9543** also supports interrupt signals for each slave channel and this data is held in bits 5 and 4 of the control register. Depending on the application, voltage translation of the I^2C bus can also be achieved using the UTC **UCA9543** to allow 1.8-V, 2.5-V, or 3.3-V parts to communicate with 5-V parts. Additionally, in the event that communication on the I^2C bus enters a fault state, the UTC **UCA9543** can be reset to resume normal operation using the $\overline{\text{RESET}}$ pin feature or by a power-on reset which results from cycling power to the device.

■ DEVICE FUNCTIONAL MODES

$\overline{\text{RESET}}$ Input

The $\overline{\text{RESET}}$ input can be used to recover the UTC **UCA9543** from a bus-fault condition. The registers and the I^2C state machine within this device initialize to their default states if this signal is asserted low for a minimum of t_{WL}. Both channels also are deselected in this case. $\overline{\text{RESET}}$ must be connected to V_{CC} through a pull-up resistor.

Power-On Reset

When power is applied to V_{CC}, an internal power-on reset holds the UTC **UCA9543** in a reset condition until V_{CC} has reached V_{PORR}. At this point, the reset condition is released and the UTC **UCA9543** registers and I^2C state machine are initialized to their default states, all zeroes, causing all the channels to be deselected. Thereafter, V_{CC} must be lowered below V_{PORF} to reset the device.

■ PROGRAMMING

I^2C Interface

The I^2C bus is for two-way, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high period of the clock pulse as changes in the data line at this time is interpreted as control signals (see Figure 4).

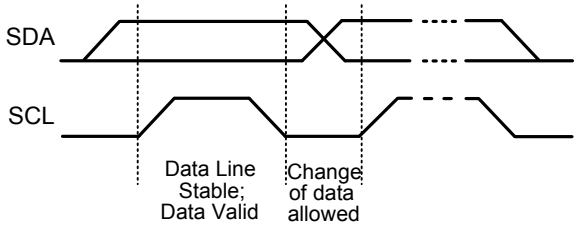


Figure 4. Bit Transfer

Both data and clock lines remain high when the bus is not busy. A high-to-low transition of the data line while the clock is high is defined as the start condition (S). A low-to-high transition of the data line while the clock is high is defined as the stop condition (P) (see Figure 5).

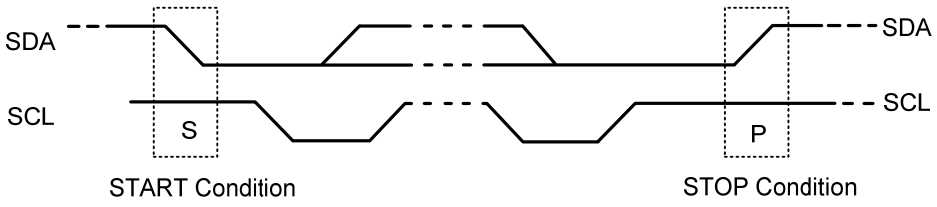


Figure 5. Definition of Start and Stop Conditions

■ PROGRAMMING (Cont.)

A device generating a message is a transmitter; a device receiving a message is the receiver. The device that controls the message is the master and the devices that are controlled by the master are the slaves (see Figure 6).

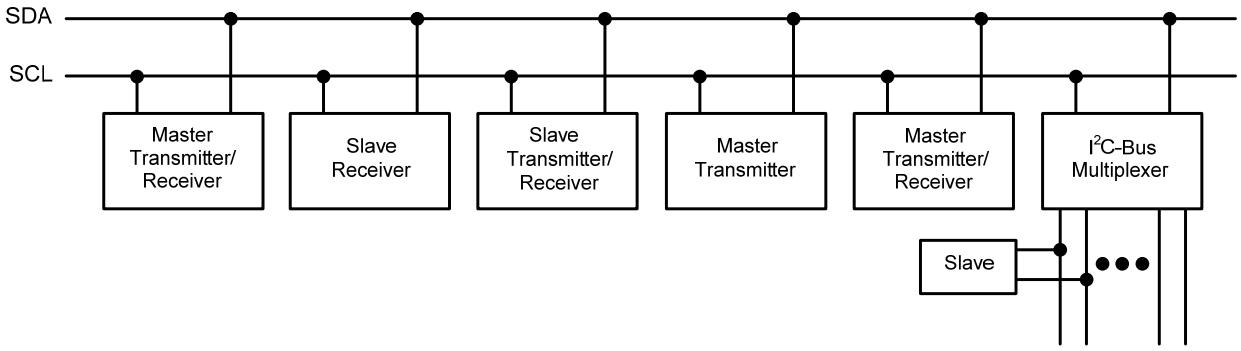


Figure 6. System Configuration

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge (ACK) bit. The transmitter must release the SDA line before the receiver can send an ACK bit.

When a slave receiver is addressed, it must generate an ACK after the reception of each byte. Also, a master must generate an ACK after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 7). Setup and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a stop condition.

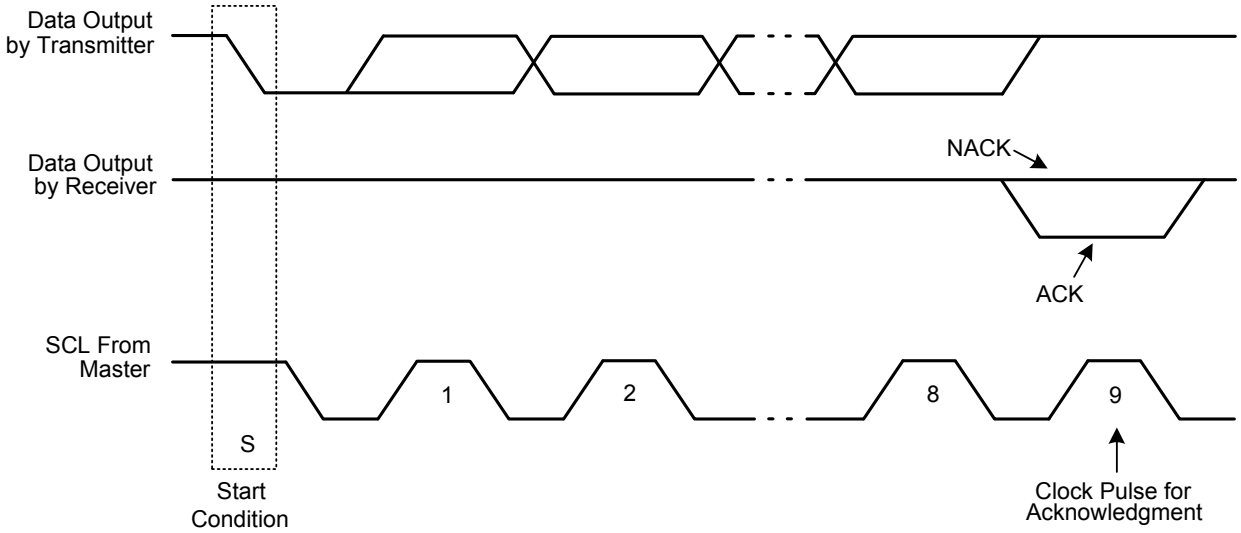


Figure 7. Acknowledgment on I²C Bus

Data is transmitted to the UTC **UCA9543** control register using the write mode shown in Figure 8.

■ PROGRAMMING (Cont.)

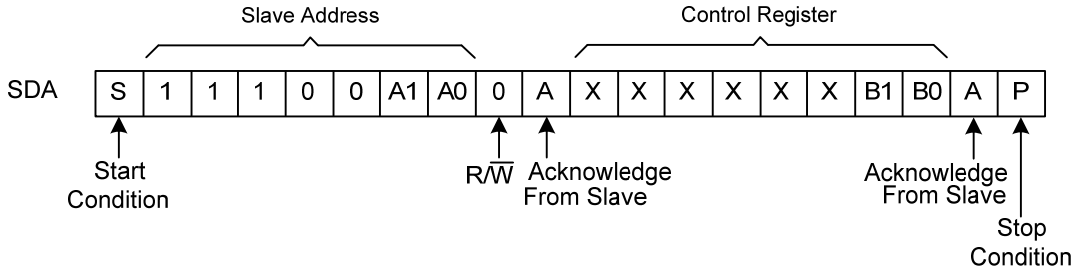


Figure 8. Write Control Register

Data is read from the UTC **UCA9543** control register using the read mode shown in Figure 9.

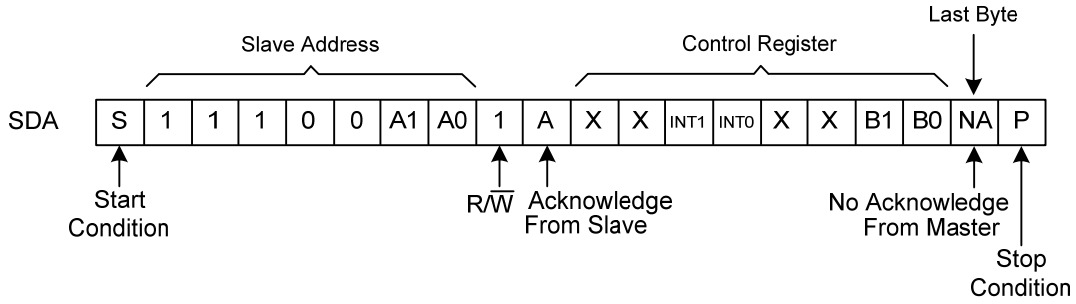


Figure 9. Read Control Register

■ CONTROL REGISTER

Device Address

Following a start condition, the bus master must output the address of the slave it is accessing. The address of the UTC **UCA9543** is shown in Figure 10. To conserve power, no internal pull-up resistors are incorporated on the hardware-selectable address pins and they must be pulled high or low.

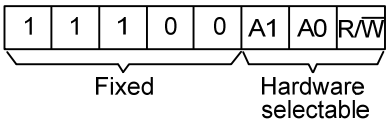


Figure 10. Slave Address UTC **UCA9543**

The last bit of the slave address defines the operation to be performed. When set to a logic 1, a read is selected, while a logic 0 selects a write operation.

Control Register Description

Following the successful acknowledgment of the slave address, the bus master sends a byte to the UTC **UCA9543**, which is stored in the control register (see Figure 11). If multiple bytes are received by the UTC **UCA9543**, it saves the last byte received. This register can be written and read via the I^2C bus.

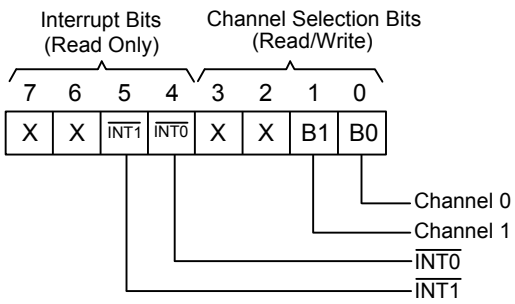


Figure 11. Control Register

■ CONTROL REGISTER (Cont.)

Control Register Definition

One or both SCn/SDn downstream pairs, or channels, are selected by the contents of the control register (see Table 1). After the UTC **UCA9543** has been addressed, the control register is written. The two LSBs of the control byte are used to determine which channel or channels are to be selected. When a channel is selected, the channel becomes active after a stop condition has been placed on the I^2C bus. This ensures that all SCn/SDn lines are in a high state when the channel is made active, so that no false conditions are generated at the time of connection. A stop condition must occur always right after the acknowledge cycle.

Table 1. Control Register Write (Channel Selection), Control Register Read (Channel Status)

D7	D6	$\overline{INT1}$	$\overline{INT0}$	D3	D2	B1	B0	COMMAND
X	X	X	X	X	X	X	0	Channel 0 disabled
							1	Channel 0 disabled
X	X	X	X	X	X	0	X	Channel 1 disabled
						1		Channel 1 disabled
0	0	0	0	0	0	0	0	No channel selected; power-up/reset default state

Note: Channel 0 and channel 1 can be enabled at the same time. Care should be taken not to exceed the maximum bus capacitance.

Interrupt Handling

The UTC **UCA9543** provides two interrupt inputs (one for each channel) and one open-drain interrupt output (see Table 2). When an interrupt is generated by any device, it is detected by the UTC **UCA9543** and the interrupt output is driven low. The channel does not need to be active for detection of the interrupt. A bit also is set in the control register.

Bit 4 and Bit 5 of the control register correspond to the $\overline{INT0}$ and $\overline{INT1}$ inputs of the UTC **UCA9543**, respectively. Therefore, if an interrupt is generated by any device connected to channel 1, the state of the interrupt inputs is loaded into the control register when a read is accomplished. Likewise, an interrupt on any device connected to channel 0 would cause bit 4 of the control register to be set on the read. The master then can address the UTC **UCA9543** and read the contents of the control register to determine which channel contains the device generating the interrupt. The master then can reconfigure the UTC **UCA9543** to select this channel, and locate the device generating the interrupt and clear it.

It should be noted that more than one device can provide an interrupt on a channel, so it is up to the master to ensure that all devices on a channel are interrogated for an interrupt.

The interrupt inputs may be used as general-purpose inputs if the interrupt function is not required.

If unused, interrupt input(s) must be connected to V_{CC} through a pull-up resistor.

Table 2. Control Register Read (Interrupt)

D7	D6	$\overline{INT1}$	$\overline{INT0}$	D3	D2	B1	B0	COMMAND
X	X	X	0	X	X	X	X	No interrupt on channel 0
			1					Interrupt on channel 0
X	X	0	X	X	X	X	X	No interrupt on channel 1
		1						Interrupt on channel 1
0	0	0	0	0	0	0	0	No channel selected; power-up/reset default state

Note: Two interrupts can be active at the same time.

■ TYPICAL APPLICATION CIRCUIT