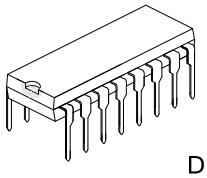
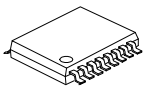
# U74HCT4094

**CMOS IC**

## 8-STAGE SHIFT&STORE BUS REGISTER



DIP-16



TSSOP-16

## ■ DESCRIPTION

The **U74HCT4094** consists of an 8-stage shift register and 8-stage D-type latch with 3-stage parallel outputs. Data is shifted serially through the shift register on the positive going transition of the clock input singal. The output of the last stage QS1 can be used to cascade several devices.

The output of QS1 is transferred to a second output(QS2) on the following negative transition of the clock input singal. The data of each stage of the shift register is provided with a latch which latches data on the negative going transition of the Strobe input signal. When the strobe input is held high, data propagates through the latch to a 3-state output buffer.

The buffer is enabled when Output Enable input is taken high.

## ■ FEATURES

* Operate from 4.5V to 5.5V
* Low Input Current: 0.1μA
* High Noise Immunity Characteristic of CMOS Devices
* Inputs are TTL Voltage Compatible

## ■ ORDERING INFORMATION

| Ordering Number | | Package | Packing |
|---|---|---|---|
| Lead Free | Halogen Free | | |
| U74HCT4094L-D16-T | U74HCT4094G-D16-T | DIP-16 | Tube |
| U74HCT4094L-P16-R | U74HCT4094G-P16-R | TSSOP-16 | Tape Reel |

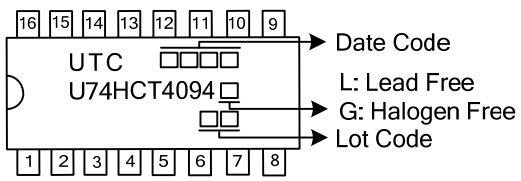
U74HCT4094G-D16-T

(1)Packing Type
(2)Package Type
(3)Green Package

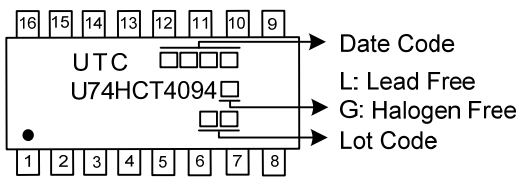
(1) T: Tube, R: Tape Reel
(2) D16: DIP-16, P16: TSSOP-16
(3) G: Halogen Free and Lead Free, L: Lead Free

## ■ MARKING

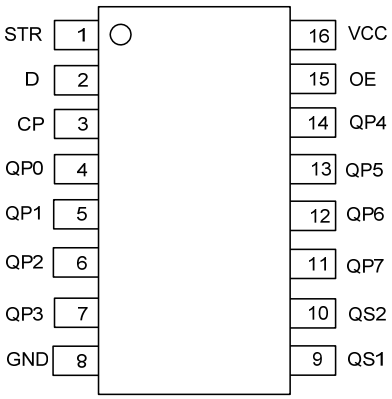
DIP-16




TSSOP-16



## ■ PIN CONFIGURATION

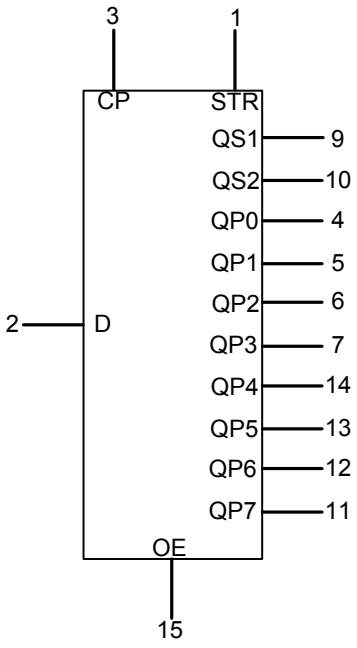



## ■ FUNCTION TABLE

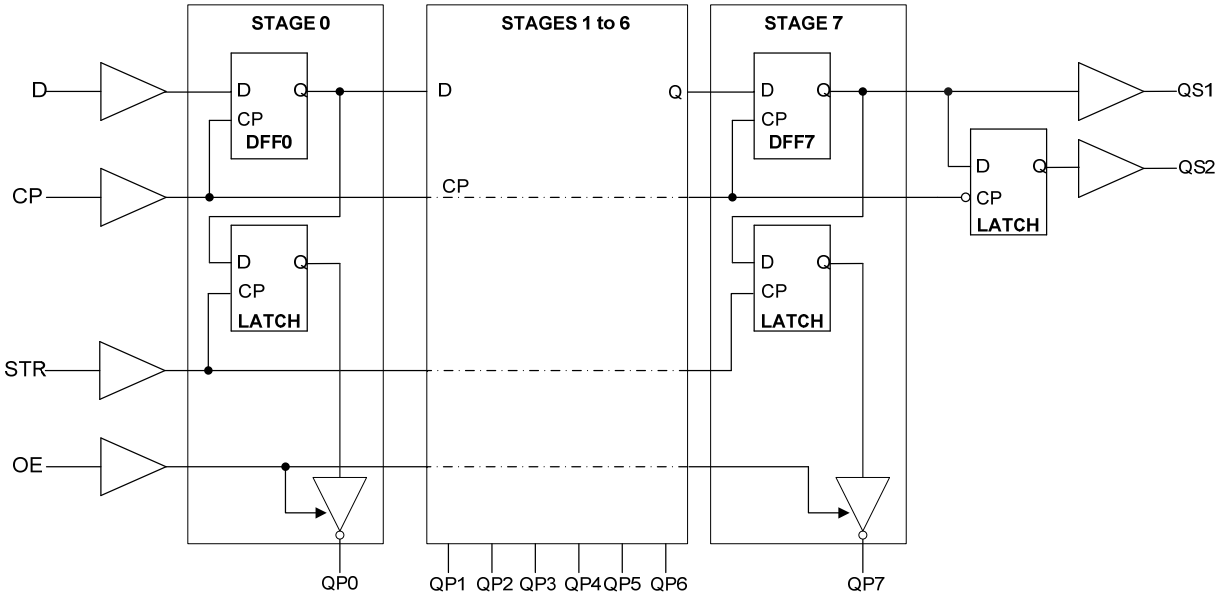
| INPUTS | | | | PARALLEL OUTPUTS | | SERIAL OUTPUTS | |
|---|---|---|---|---|---|---|---|
| CP | OE | STR | D | QP0 | QPn | QS1 | QS2 |
| ↑ | L | X | X | Z | Z | Q'6 | NC |
| ↓ | L | X | X | Z | Z | NC | QP7 |
| ↑ | H | L | X | NC | NC | Q'6 | NC |
| ↑ | H | H | L | L | QPn-1 | Q'6 | NC |
| ↑ | H | H | H | H | QPn-1 | Q'6 | NC |
| ↓ | H | H | H | NC | NC | NC | QP7 |

Note:H : HIGH voltage level; L : LOW voltage level.
X : Don't care.High impedance OFF-state.
NC: No change.
↑ : Low-to-High CP transition.
↓ : High-to-Low CP transition.
Q'6: the information in the seventh register stage is transferred to the 8th register stage and QSn output at the positive clock edge

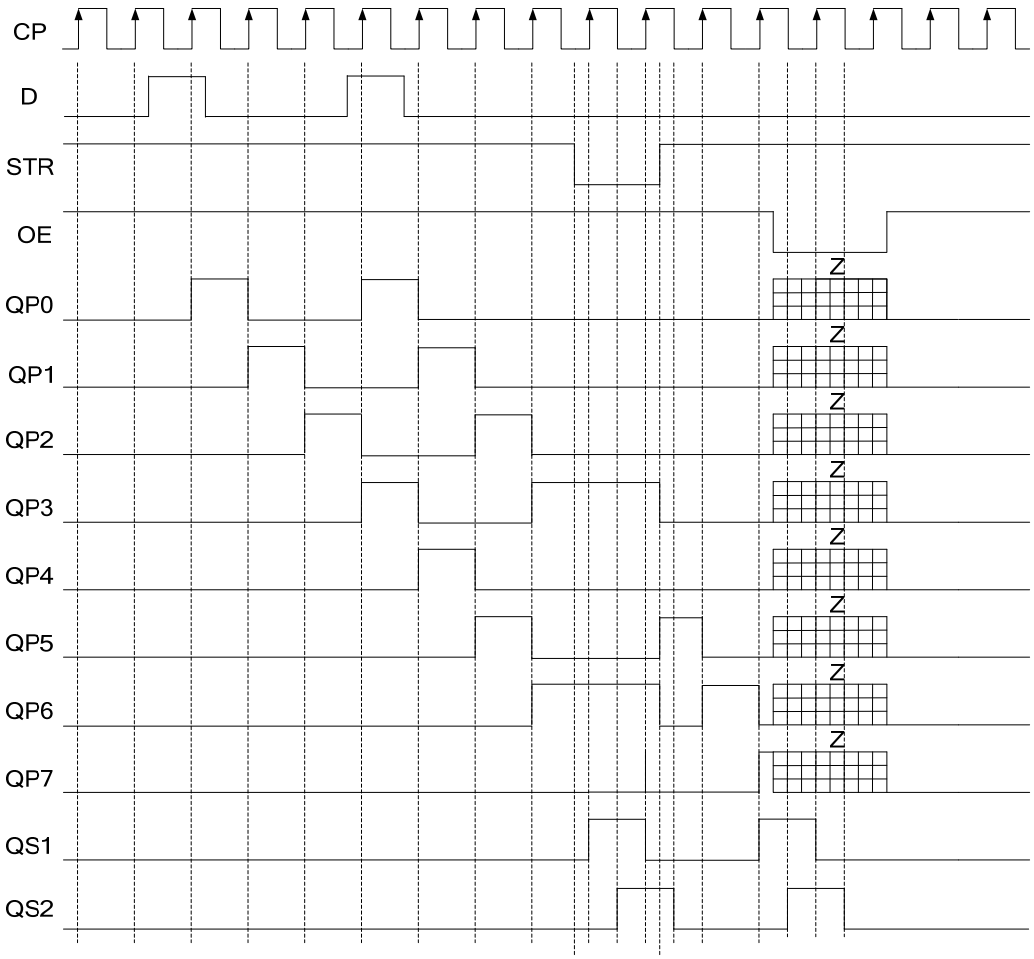
## ■ LOGIC SYMBOL



## ■ LOGIC DIAGRAM




## ■ TIMING DIAGRAM



## ■ ABSOLUTE MAXIMUM RATING

| PARAMETER | SYMBOL | RATINGS | UNIT |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | -0.5 ~ 7.0 | V |
| Input Voltage | $V_{IN}$ | -0.5 ~ $V_{CC}$ +1.5 | V |
| Output Voltage | $V_{OUT}$ | -0.5 ~ $V_{CC}$ +0.5 | V |
| Input Clamp Current | $I_{IK}$ | ±20 | mA |
| Output Clamp Current | $I_{OK}$ | ±20 | mA |
| Output Current | $I_{OUT}$ | ±25 | mA |
| $V_{CC}$ or GND Current | $I_{CC}$ | ±50 | mA |
| Storage Temperature | $T_{STG}$ | -65 ~ + 150 | °C |

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

## ■ RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | Operating | 4.5 | | 5.5 | V |
| Input Voltage | $V_{IN}$ | | 0 | | $V_{CC}$ | V |
| Output Voltage | $V_{OUT}$ | | 0 | | $V_{CC}$ | V |
| Operating Temperature | $T_A$ | | -40 | | +125 | °C |
| Input Rise and Fall Times | $t_R$, $t_F$ | $V_{CC}$=4.5V to 5.5V | | | 500 | ns |

## ■ ELECTRICAL CHARACTERISTICS ($T_A$=25°C, unless otherwise specified)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | $V_{CC}$=4.5V to 5.5V | 2.0 | 1.6 | | V |
| Low-lever output voltage | $V_{IL}$ | $V_{CC}$=4.5V to 5.5V | | 1.2 | 0.8 | V |
| High-Level Output Voltage, | $V_{OH}$ | $V_{CC}$=4.5V, $I_{OH}$=-20μA | 4.4 | | | V |
| | | $V_{CC}$=4.5V, $I_{OH}$=-4mA | 3.98 | | | V |
| Low-Level Output Voltage, | $V_{OL}$ | $V_{CC}$=4.5V, $I_{OL}$=20μA | | | 0.1 | V |
| | | $V_{CC}$=4.5V, $I_{OL}$=4mA | | | 0.26 | V |
| Input Leakage Current | $I_{I(LEAK)}$ | $V_{CC}$=5.5V, $V_{IN}$=$V_{CC}$ or GND | | | ±0.1 | μA |
| Output OFF -state current | $I_{OZ}$ | $V_{CC}$=5.5V, $V_{OUT}$=$V_{CC}$ or GND | | | ±0.5 | μA |
| Quiescent Supply Current | $I_{CC}$ | $V_{CC}$=5.5V, $V_{IN}$=$V_{CC}$ or GND, $I_{OUT}$=0 | | | 4 | μA |
| Additional Quiescent Supply Current | $\triangle I_{CC}$ | One input=$V_{CC}$-2.1V, other inputs at $V_{CC}$ or GND | | 100 | 500 | μA |

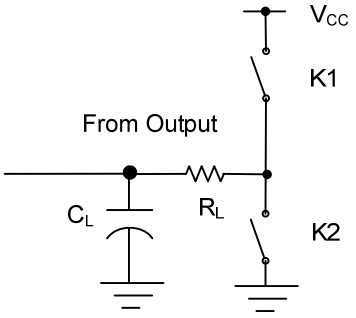
## ■ SWITCHING CHARACTERISTICS ($T_A$=25°C, see TEST CIRCUIT AND WAVEFORMS)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Propagation Delay from Input (CP) to Output(QS1) | $t_{PHL}/t_{PLH}$ | $V_{CC}$=4.5V | | 23 | 39 | ns |
| Propagation Delay from Input (CP) to Output(QS2) | $t_{PHL}/t_{PLH}$ | $V_{CC}$=4.5V | | 21 | 36 | ns |
| Propagation Delay from Input (CP) to Output (QPn) | $t_{PHL}/t_{PLH}$ | $V_{CC}$=4.5V | | 25 | 43 | ns |
| Propagation Delay from Input (STR) to Output (QPn) | $t_{PHL}/t_{PLH}$ | $V_{CC}$=4.5V | | 22 | 39 | ns |
| 3-state Output Enable Time from Input (OE) to Output(QPn) | $t_{PZH}/t_{PZL}$ | $V_{CC}$=4.5V | | 20 | 35 | ns |
| 3-State Output Disable Time from Input (OE) to Output(QPn) | $t_{PHZ}/t_{PLZ}$ | $V_{CC}$=4.5V | | 21 | 35 | ns |
| Output Transition Time(QSn、QPn) | $t_{TLH}$/ $t_{THL}$ | $V_{CC}$=4.5V | | 7 | 15 | ns |
| Clock Pulse Width HIGH or LOW(CP) | $t_W$ | $V_{CC}$=4.5V | 16 | 7 | | ns |
| Strobe Pulse Width HIGH(STR) | $t_W$ | $V_{CC}$=4.5V | 16 | 5 | | ns |
| Set-up Time(D to CP) | $t_{SU}$ | $V_{CC}$=4.5V | 10 | 4 | | ns |
| Set-up Time(D to STR) | $t_{SU}$ | $V_{CC}$=4.5V | 20 | 9 | | ns |
| Hold Time(D to CP) | $t_H$ | $V_{CC}$=4.5V | 4 | 0 | | ns |
| Hold Time(D to STR) | $t_H$ | $V_{CC}$=4.5V | 0 | -4 | | ns |
| Maximum Clock Pulse Frequency | $f_{(MAX)}$ | $V_{CC}$=4.5V | 30 | 80 | | MHz |

## ■ OPERATING CHARACTERISTICS

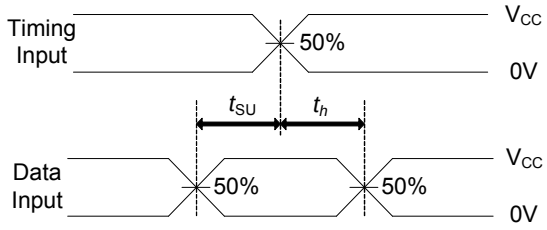
| PARAMETER | SYMBOL | TEST CONDITIONS | RATINGS | UNIT |
|---|---|---|---|---|
| Power Dissipation Capacitance | $C_{PD}$ | No Load | 92 | pF |

## ■ TEST CIRCUIT AND WAVEFORMS

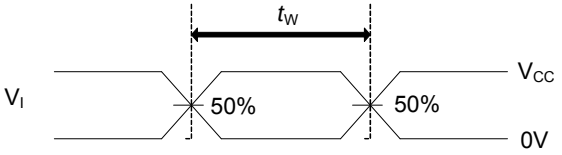



| TEST | K1 | K2 |
|---|---|---|
| $t_{PLH}/t_{PHL}$ | Open | Open |
| $t_{PHZ}/t_{PZH}$ | Open | Close |
| $t_{PLZ}/t_{PZL}$ | Close | Open |

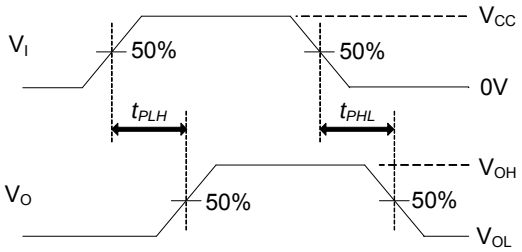
Note: $C_L$ =50pF, $R_L$ =1kΩ



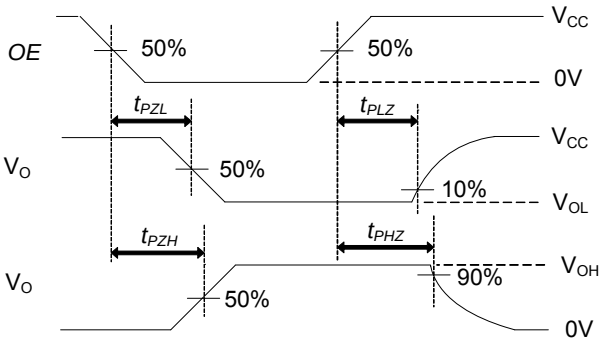

Setup Time and Hold Time




Pulse Width




Propagation Delay Times




Enable and Disable Times

Note: $C_L$ includes probe and jig capacitance.
$P_{RR}$ ⩽10MHz, Zo = 50Ω, $t_R$ ⩽6ns, $t_F$ ⩽6ns.