HV9910C

Universal High-Brightness LED Driver

Features

- Switch Mode Controller for Single Switch LED Drivers
- Enhanced Drop-In Replacement to the HV9910B
- Open Loop Peak Current Controller
- Internal 15 to 450V Linear Regulator
- Constant Frequency or Constant Off-Time Operation
- Linear and PWM Dimming Capability
- Requires Few External Components for Operation
- Over-Temperature Protection

Applications

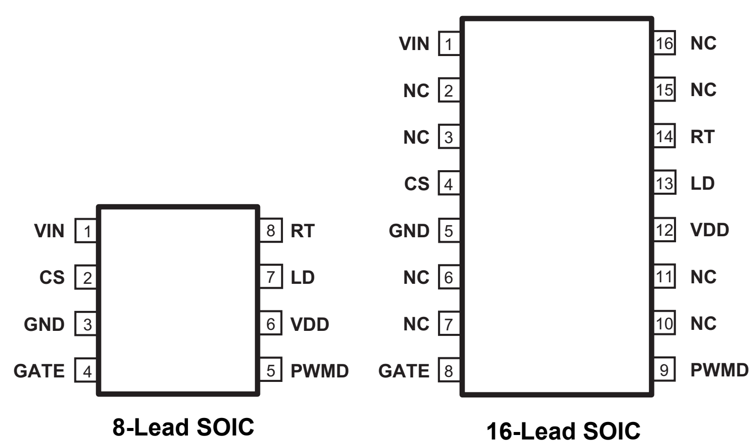
- DC/DC or AC/DC LED Driver Applications
- RGB Back-Lighting LED Driver
- Back Lighting of Flat Panel Displays
- General Purpose Constant Current Source
- Signage and Decorative LED Lighting
- Chargers

Description

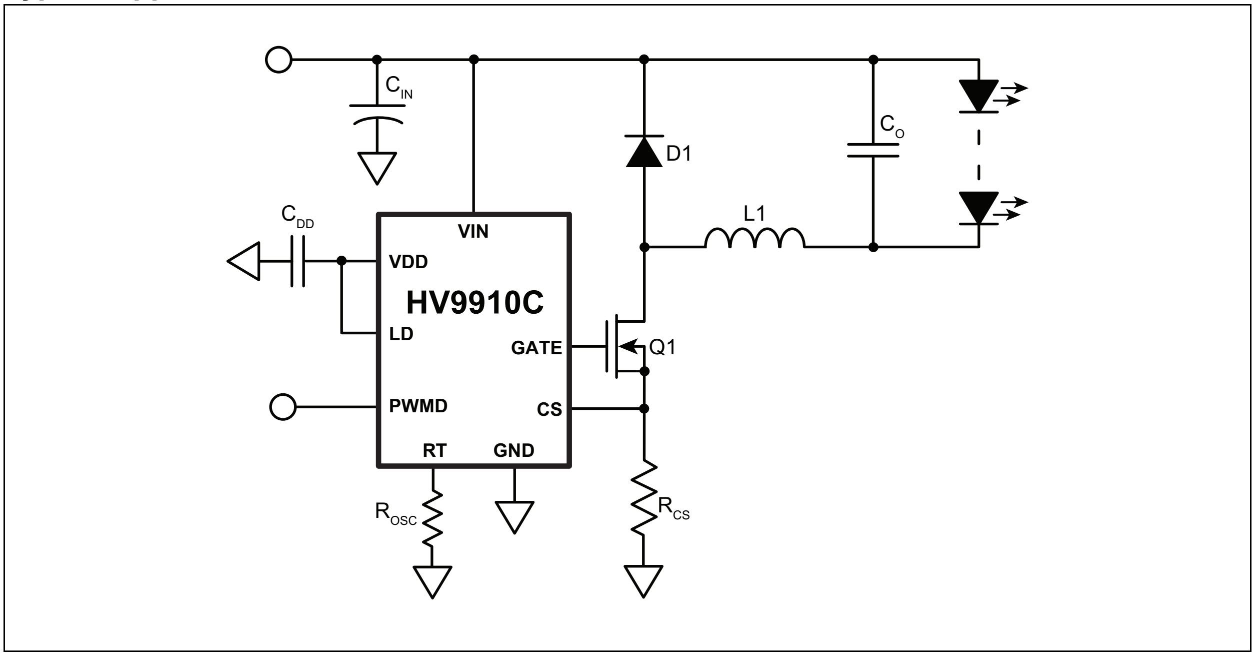
HV9910C is an open-loop, current-mode control, LED driver IC. This IC can be programmed to operate in either a constant frequency or constant off-time mode. It includes a 15-450V linear regulator which allows it to work with a wide range of input voltages without the need for an external low voltage supply. HV9910C includes a TTL-compatible, PWM-dimming input that can accept an external control signal with a duty ratio of 0-100% and a frequency of up to a few kilohertz. It also includes a 0-250 mV linear-dimming input which can be used for linear dimming of the LED current. Unlike the HV9910B, the HV9910C is equipped with built-in thermal-shutdown protection.

HV9910C is ideally suited for buck LED drivers. Since the HV9910C operates in open-loop current mode control, the controller achieves good output current regulation without the need for any loop compensation. Also, being an open-loop controller, PWM-dimming response is limited only by the rate of rise of the inductor current, enabling a very fast rise and fall times of the LED current. HV9910C requires only three external components (apart from the power stage) to produce a controlled LED current. This makes HV9910C an ideal solution for low-cost LED drivers.

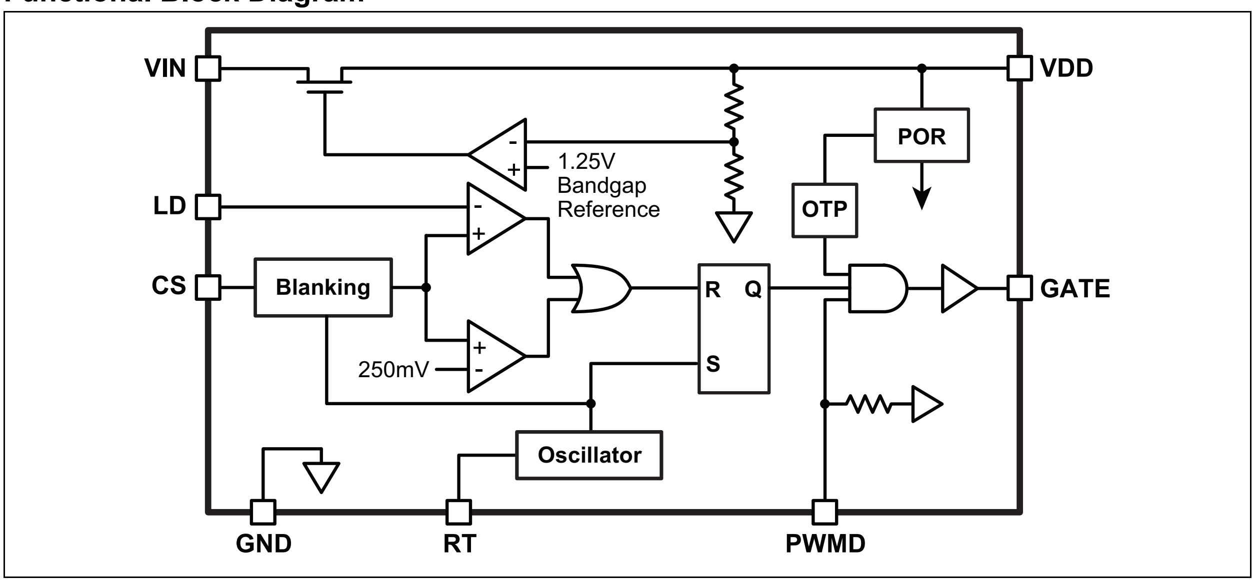
Package Types



Typical Application Circuit



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS†

V_{IN} to GND .... -0.5V to +470V
V_{DD} to GND 12V
CS, LD, PWMD, GATE .... -0.3V to (V_{DD} + 0.3V)
Junction temperature .... -40°C to +125°C
Storage temperature .... -65°C to +150°C
Continuous power dissipation (T_A = +25°C)
8-lead SOIC .... 650 mW
16-lead SOIC .... 1300 mW
8-lead SOIC with heat slug .... 1300 mW

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operational listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1.1 ELECTRICAL SPECIFICATIONS

TABLE 1-1: ELECTRICAL CHARACTERISTICS (Note 1)

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Input						
Input DC Supply Voltage Range, (Note 2)	V_{INDC}	15	—	450	V	DC input voltage, (Note 3)
Supply Current	$I_{IN(MAX)}$	—	0.8	1.5	mA	Pin PWMD to V_{DD}, no capacitance at GATE
Shut-down Mode Supply Current	I_{INSD}	—	0.5	1.0	mA	Pin PWMD to GND
Internal Regulator						
Internally Regulated Voltage	V_{DD}	7.20	7.50	7.75	V	V_{IN} = 15V, $I_{DD(ext)}$ = 0, PWMD = V_{DD}, 500 pF at GATE; R_{OSC} = 249 kΩ
Line Regulation of V_{DD}	ΔV_{DD}, line	0	—	1.0	V	V_{IN} = 15 - 450V, $I_{DD(ext)}$ = 0, PWMD = V_{DD}, 500 pF at GATE; R_{OSC} = 249 kΩ
Load Regulation of V_{DD}	ΔV_{DD}, load	0	—	0.1	V	$I_{DD(ext)}$ = 0 - 1.0 mA, PWMD = V_{DD}, 500 pF at GATE; ROSC = 249 kΩ
V_{DD} Under Voltage Lockout Threshold	UVLO	6.45	6.70	6.95	V	V_{DD} rising, (Note 3)
V_{DD} Under Voltage Lockout Hysteresis	ΔUVLO	—	500	—	mV	V_{DD} falling
Maximum Regulator Current	$I_{IN(MAX)}$	5.0	—	—	mA	V_{DD} = UVLO - ΔUVLO, (Note 4)
PWM Dimming						
PWMD Input Low Voltage	$V_{EN(lo)}$	—	—	1.0	V	V_{IN} = 15 - 450V, (Note 3)
PWMD Input High Voltage	$V_{EN(hi)}$	2.4	—	—	V	V_{IN} = 15 - 450V, (Note 3)
Internal Pull-down Resistance at PWMD	R_{EN}	50	100	150	kΩ	V_{PWMD} = 5.0V
Current Sense Comparator						
Current Sense Pull-in Threshold Voltage	V_{CST}	217	250	275	mV	-40°C < T_A < +125°C
Offset Voltage for LD Comparator	V_{OFFSET}	–20	—	+20	mV	Note 3

Note 1: Specifications apply at T_A = 25°C, V_{IN} = 15V unless otherwise noted.
2: Also limited by package-power dissipation limit; Whichever is lower.
3: Applies over the full operating ambient temperature range of –40°C < T_A < +125°C.
4: For design guidance only.

TABLE 1-1: ELECTRICAL CHARACTERISTICS (Note 1) (CONTINUED)

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Current Sense Blanking Interval	T_{BLANK}	175	215	317	ns	0°C < T_A < +85°C, V_{LD} = V_{DD}, V_{CS} = $V_{CS,TH}$ + 50 mV after T_{BLANK}
		175	215	350		-40°C < T_A < +125°C, V_{LD} = V_{DD}, V_{CS} = $V_{CS,TH}$ + 50 mV after T_{BLANK}
Delay to Output	t_{DELAY}	—	80	150	ns	V_{IN} = 15V, V_{LD} = 0.15V, V_{CS} = 0V to 0.22V after t_{BLANK}
Oscillator						
Oscillator Frequency	f_{OSC}	20	25	30	kHz	R_{OSC} = 1.00 MΩ
		80	100	120		R_{OSC} = 249 kΩ
Gate Driver						
Maximum GATE Sourcing Current	I_{SOURCE}	0.165	—	—	A	V_{GATE} = 0V
Maximum GATE Sinking Current	I_{SINK}	0.165	—	—	A	V_{GATE} = V_{DD}
GATE Output Rise Time	t_{RISE}	—	30	50	ns	C_{GATE} = 500 pF, (Note 4)
GATE Output Fall Time	t_{FALL}	—	30	50	ns	C_{GATE} = 500 pF, (Note 4)
Over-Temperature Protection						
Shut-down Temperature	T_{SD}	128	—	150	°C	
Hysteresis	ΔT_{SD}	10	—	30	°C	
T_{SD}-mode V_{IN} Current	I_{SD}	—	—	350	µA	

Note 1: Specifications apply at T_A = 25°C, V_{IN} = 15V unless otherwise noted.
2: Also limited by package-power dissipation limit; Whichever is lower.
3: Applies over the full operating ambient temperature range of -40°C < T_A < +125°C.
4: For design guidance only.

TABLE 1-2: THERMAL RESISTANCE

Package	Symbol	Min	Typ	Max	Units	Conditions
8-Lead SOIC	θ_{JA}	—	101	—	°C/W	
16-Lead SOIC	θ_{JA}	—	83	—	°C/W	
8-Lead SOIC (with heat slug)	θ_{JA}	—	84	—	°C/W	

2.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN DESCRIPTION

Pin #		Function	Description
8-Lead SOIC	16-Lead SOIC		
1	1	VIN	Input of an 15-450V linear regulator.
2	4	CS	Current sense pin used to sense the FET current by means of an external sense resistor. When this pin exceeds the lower of either the internal 250 mV or the voltage at the LD pin, the GATE output goes low.
3	5	GND	Ground return for all internal circuitry. Must be electrically connected to the power ground.
4	8	GATE	Output GATE driver for an external N-channel power MOSFET.
5	9	PWMD	TTL-compatible, PWM-dimming input of the IC. When this pin is pulled to GND or left open, the GATE driver is turned off. When the pin is pulled high, the GATE driver operates normally.
6	12	VDD	Power supply pin for all internal circuits. It must be bypassed with a low-ESR capacitor to GND (≥ 0.1 µF).
7	13	LD	Linear-dimming input and sets the current sense threshold as long as the voltage at the pin is less than 250 mV (typ).
8	14	RT	Sets the oscillator frequency. When a resistor is connected between RT and GND, the HV9910C operates in constant frequency mode. When the resistor is connected between RT and GATE, the IC operates in constant off-time mode.
—	2, 3, 6, 7, 10, 11, 15, 16	NC	No connection

3.0 APPLICATION INFORMATION

HV9910C is optimized to drive buck LED drivers using open-loop, peak-current mode control. This method of control enables fairly accurate LED current control without the need for high side current sensing or the design of any closed loop controllers. The IC uses very few external components and enables both Linear and PWM-dimming of the LED current.

A resistor connected to the RT pin programs the frequency of operation (or the off-time). The oscillator produces pulses at regular intervals. These pulses set the SR flip-flop in the HV9910C which causes the GATE driver to turn on. The same pulses also start the blanking timer, which inhibits the reset input of the SR flip flop and prevents false turn-offs due to the turn-on spike. When the FET turns on, the current through the inductor starts ramping up. This current flows through the external sense resistor, R_{CS}, and produces a ramp voltage at the CS pin. The comparators are constantly comparing the CS pin voltage to both the voltage at the LD pin and the internal 250 mV. Once the blanking timer is complete, the output of these comparators is allowed to reset the flip-flop. When the output of either one of the two comparators goes high, the flip-flop is reset and the GATE output goes low. The GATE goes low until the SR flip-flop is set by the oscillator. Assuming a 30% ripple in the inductor, the current sense resistor R_{CS} can be set using:

$$R_{CS} = \frac{0.25V(or V_{LD})}{1.15 \bullet I_{LED}}$$

Constant frequency peak current mode control has an inherent disadvantage – at duty cycles greater than 0.5, the control scheme goes into subharmonic oscillations. To prevent this, an artificial slope is typically added to the current sense waveform. This slope compensation scheme will affect the accuracy of the LED current in the present form. However, a constant off-time peak current control scheme does not have this problem and can easily operate at duty cycles greater than 0.5. This control scheme also gives inherent input voltage rejection, making the LED current almost insensitive to input voltage variations. However, this scheme leads to variable frequency operation and the frequency range depends greatly on the input and output voltage variation. Using HV9910C, it is easy to switch between the two modes of operation by changing one connection (see **Section 3.3 “Oscillator”**).

3.1 Input Voltage Regulator

HV9910C can be powered directly from its V_{IN} pin and can work from 15-450 VDC at its V_{IN} pin. When a voltage is applied at the V_{IN} pin, HV9910C maintains a constant 7.5V at the V_{DD} pin. This voltage is used to power the IC and any external-resistor dividers needed to control the IC. The V_{DD} pin must be bypassed by a low-ESR capacitor to provide a low impedance path for the high frequency current of the output GATE driver.

HV9910C can also be operated by supplying a voltage at the V_{DD} pin greater than the internally regulated voltage. This will turn off the internal linear regulator of the IC and the HV9910C will operate directly off the voltage supplied at the V_{DD} pin. This external voltage at the V_{DD} pin should not exceed 12V.

Although the V_{IN} pin of the HV9910C is rated up to 450V, the actual maximum voltage that can be applied is limited by the power dissipation in the IC. For example, if an 8-lead SOIC HV9910C (junction to ambient thermal resistance $R_{\theta j\text{-}a}$ = 101°C/W) draws about I_{IN} = 2.0 mA from the V_{IN} pin, and has a maximum allowable temperature rise of the junction temperature limited to ΔT = 75°C, the maximum voltage at the V_{IN} pin would be:

$$\begin{aligned} V_{IN(MAX)} &= \frac{\Delta T}{R_{\theta ja}} \bullet \frac{1}{I_{IN}} \\ &= \frac{75\,°C}{101\,°C/W} \bullet \frac{1}{2mA} \\ &= 371V \end{aligned}$$

In these cases, to operate HV9910C from higher input voltages, a Zener diode can be added in series with the V_{IN} pin to divert some of the power loss from HV9910C to the Zener diode. In the above example, using a 100V Zener diode will allow the circuit to easily work up to 450V.

Note:	The Zener diode will increase the minimum input voltage required to turn on the HV9910C to 115V.

The input current drawn from the V_{IN} pin is a sum of the 1.5 mA (maximum) current drawn by the internal circuit and the current drawn by the GATE driver. The GATE driver depends on the switching frequency and the GATE charge of the external FET.

$$I_{IN} = 1.5mA + Q_g \bullet f_s$$

In the above equation, f_s is the switching frequency and Q_g is the GATE charge of the external FET, which can be obtained from the data sheet of the FET.

3.2 Current Sense

The current sense input of HV9910C goes to the non-inverting inputs of two comparators. The inverting terminal of one comparator is tied to an internal 250 mV reference, whereas the inverting terminal of the other comparator is connected to the LD pin. The outputs of both these comparators are fed into an OR GATE and the output of the OR GATE is fed into the reset pin of the flip-flop. Thus, the comparator which has the lowest voltage at the inverting terminal determines when the GATE output is turned off.

The outputs of the comparators also include a 150-280 ns blanking time which prevents spurious turn-offs of the external FET due to the turn-on spike normally present in peak-current mode control. In rare cases, this internal blanking might not be enough to filter out the turn-on spike. In these instances, an external RC filter needs to be added between the external sense resistor (RCS) and the CS pin.

Please note that the comparators are fast (with a typical 80 ns response time). A proper layout minimizing external inductances will prevent false triggering of these comparators.

3.3 Oscillator

The oscillator in HV9910C is controlled by a single resistor connected at the RT pin. The equation governing the oscillator time period T_{osc} is given by:

$$T_{OSC}(\mu s) = \frac{R_{OSC}(k\Omega)}{25}$$

If the resistor is connected between RT and GND, HV9910C operates in a constant frequency mode and the above equation determines the time period. If the resistor is connected between RT and GATE, HV9910C operates in a constant off-time mode and the above equation determines the off-time.

3.4 Gate Output

The gate output of the HV9910C is used to drive an external FET. It is recommended that the GATE charge of the external FET be less than 25 nC for switching frequencies ≤ 100 kHz and less than 15 nC for switching frequencies > 100 kHz.

3.5 Linear Dimming

The Linear Dimming pin is used to control the LED current. There are two cases when it may be necessary to use the Linear Dimming pin.

1. In some cases, when using the internal 250 mV, it may not be possible to find the exact R_{CS} value required to obtain the LED current. In these cases, an external voltage divider from the V_{DD} pin can be connected to the LD pin to obtain a voltage (less than 250 mV) corresponding to the desired voltage across R_{CS}.
2. Linear dimming may be desired to adjust the current level to reduce the intensity of the LEDs. In these cases, an external 0-250 mV voltage can be connected to the LD pin to adjust the LED current during operation.

To use the internal 250 mV, the LD pin can be connected to V_{DD}.

Note:	Although the LD pin can be pulled to GND, the output current will not go to zero. This is due to the presence of a minimum on-time, which is equal to the sum of the blanking time and the delay to output time, or about 450 ns. This minimum on-time causes the FET to be on for a minimum of 450 ns, and thus the LED current when LD = GND is not zero. This current is also dependent on the input voltage, inductance value, forward voltage of the LEDs, and circuit parasitics. To get zero LED current, the PWMD pin has to be used.

3.6 PWM Dimming

PWM Dimming can be achieved by driving the PWMD pin with a low frequency square wave signal. When the PWM signal is zero, the GATE driver is turned off; when the PWMD signal if high, the GATE driver is enabled. The PWMD signal does not turn off the other parts of the IC, therefore, the response of HV9910C to the PWMD signal is almost instantaneous. The rate of rise and fall of the LED current is thus determined solely by the rise and fall times of the inductor current.

To disable PWM Dimming and enable the HV9910C permanently, connect the PWMD pin to V_{DD}.

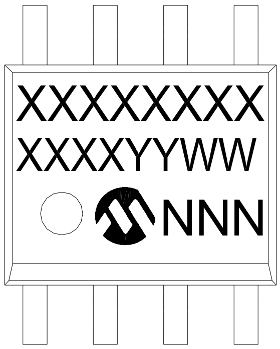
3.7 Over-Temperature Protection

The auto-recoverable thermal shutdown at 140°C (typ.) junction temperature with 20°C hysteresis is featured to avoid thermal runaway. When the junction temperature reaches T_{SD} = 140°C (typ.), HV9910C enters a low power consumption shut-down mode with I_{IN} < 350 µA.

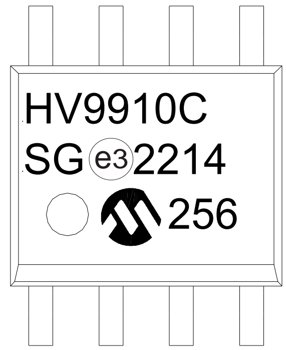
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

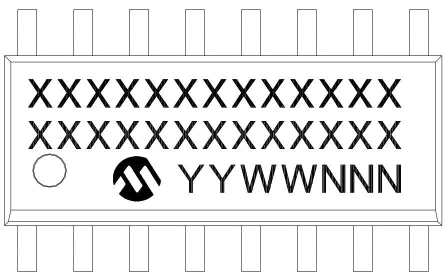
8-Lead SOIC



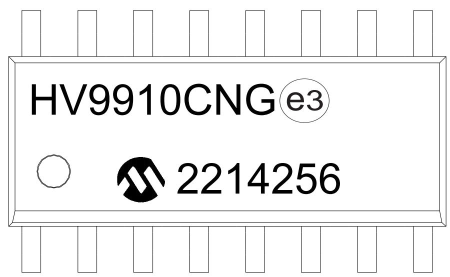
Example



16-Lead SOIC



Example



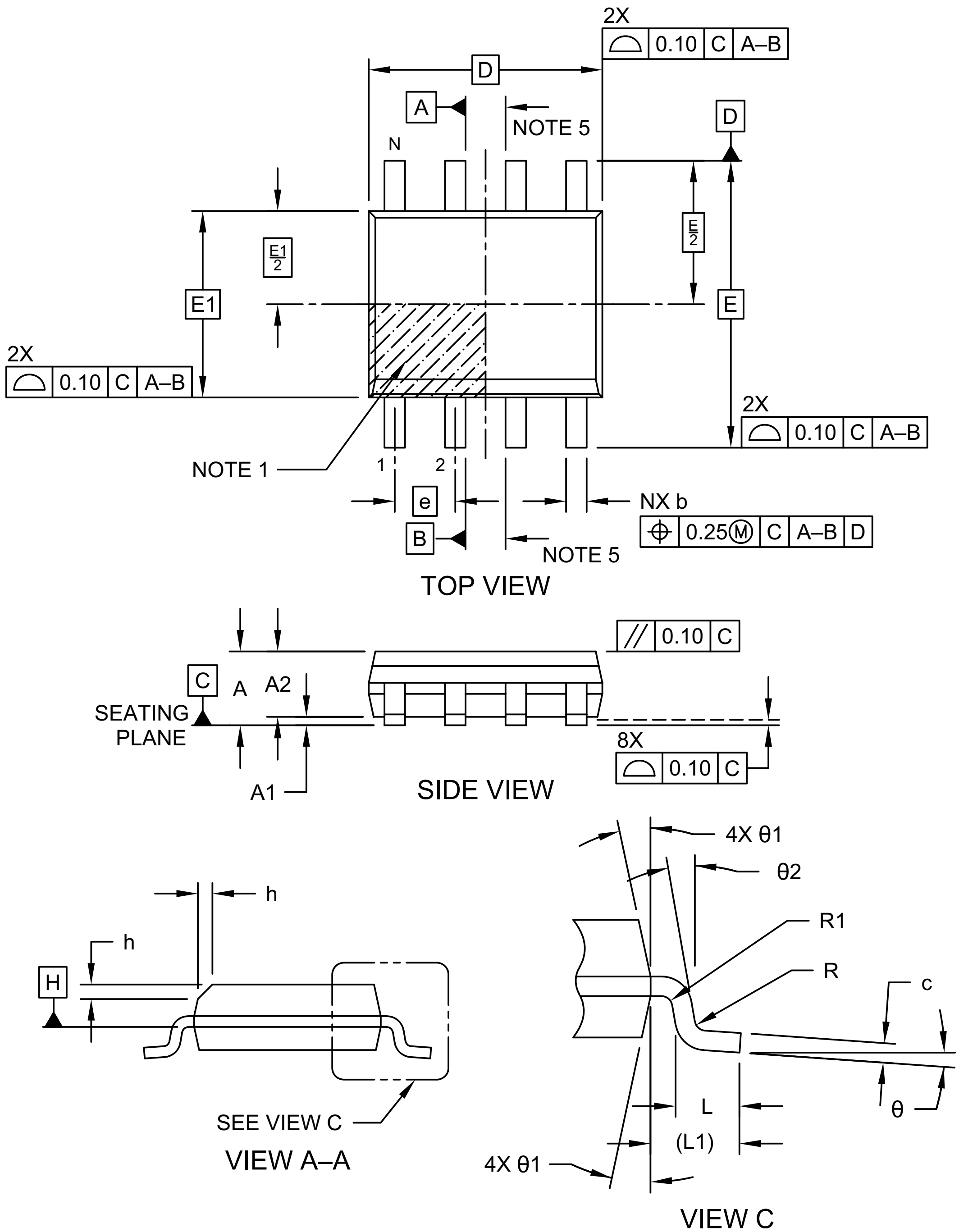
Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (‾) symbol may not be to scale.

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

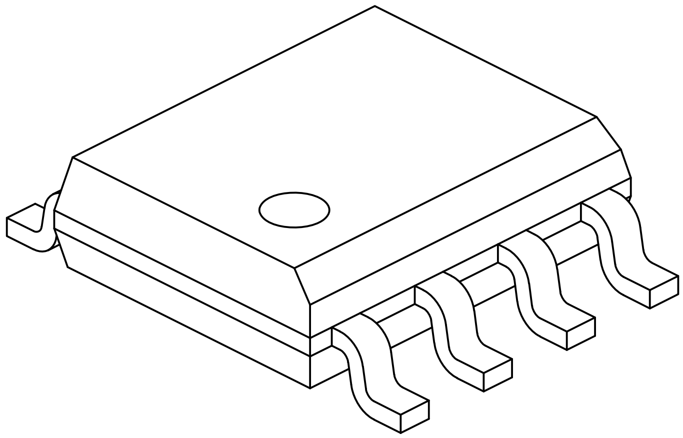
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057-SN Rev J Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	-
Standoff §	A1	0.10	–	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (Optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1	1.04 REF		
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°
Lead Angle	θ2	0°	–	8°

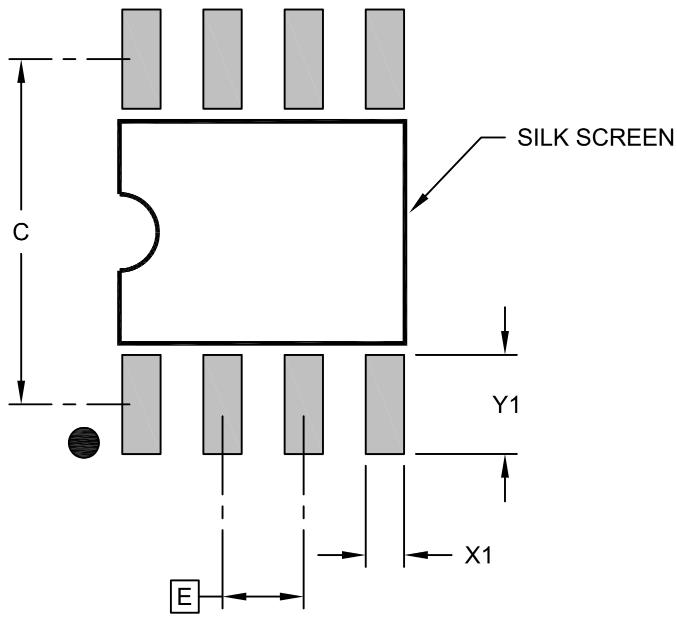
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev J Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

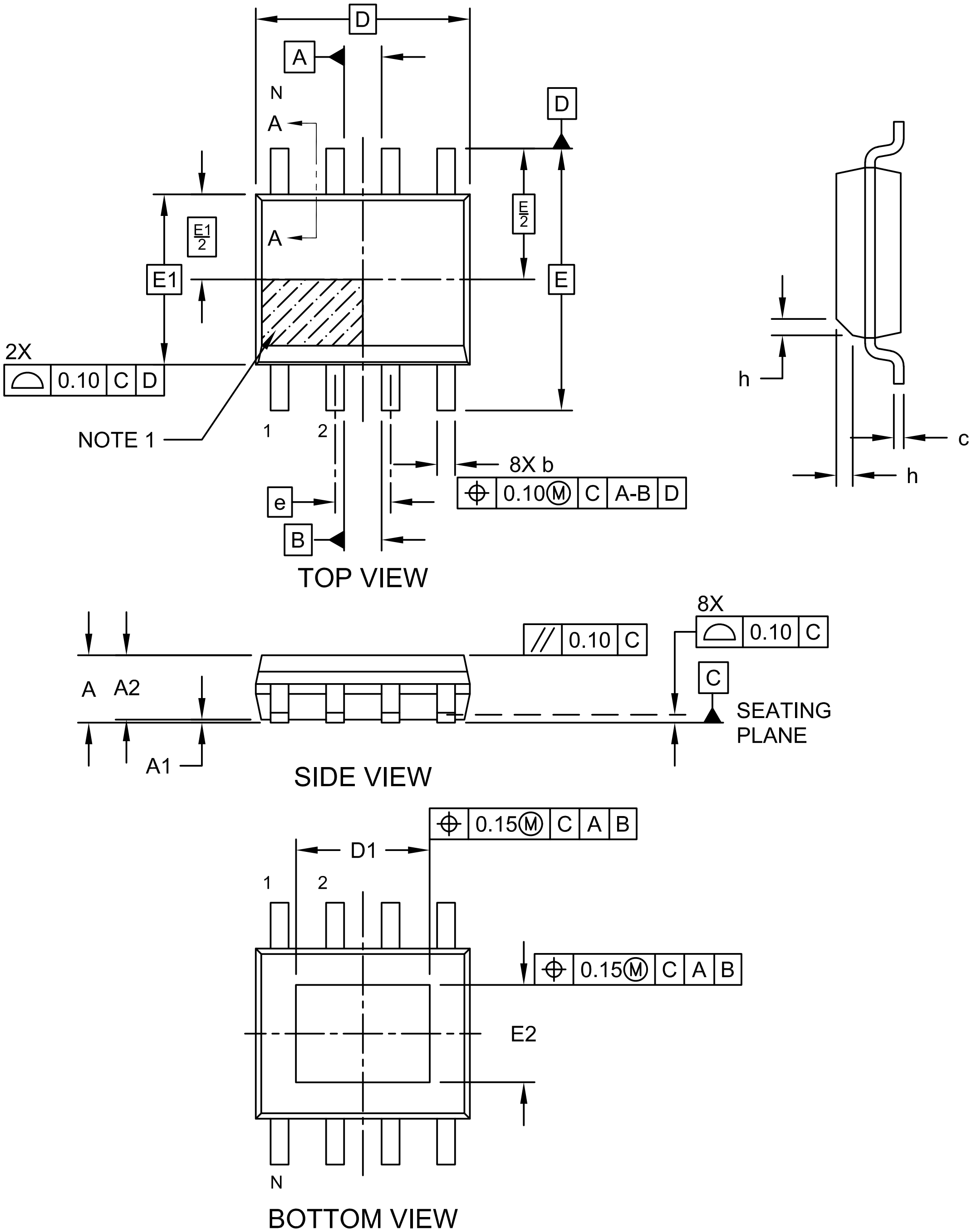
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev J

8-Lead Thermally Enhanced Plastic Small Outline (SE) - Narrow, 3.90 mm Body [SOIC] With 2.2 x 3.0 mm Exposed Pad

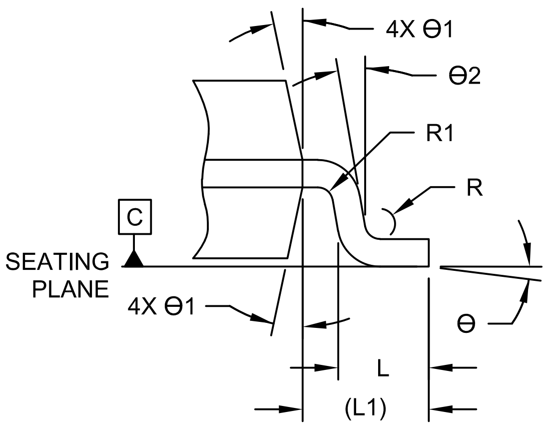
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



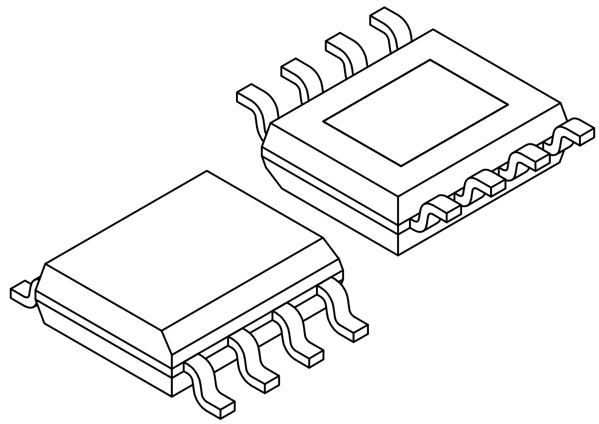
Microchip Technology Drawing C04-162-SE Rev D Sheet 1 of 2

8-Lead Thermally Enhanced Plastic Small Outline (SE) - Narrow, 3.90 mm Body [SOIC] With 2.2 x 3.0 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



SECTION A-A



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.00	-	0.15
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Exposed Pad Width	E2	2.05	2.23	2.41
Exposed Pad Length	D1	2.81	3.06	3.30
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Lead Bend Radius	R	0.07	-	-
Lead Bend Radius	R1	0.07	-	-
Foot Angle	Θ	0°	-	8°
Lead Angle	Θ2	0°	-	-
Mold Draft Angle Top and Bottom	Θ1	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

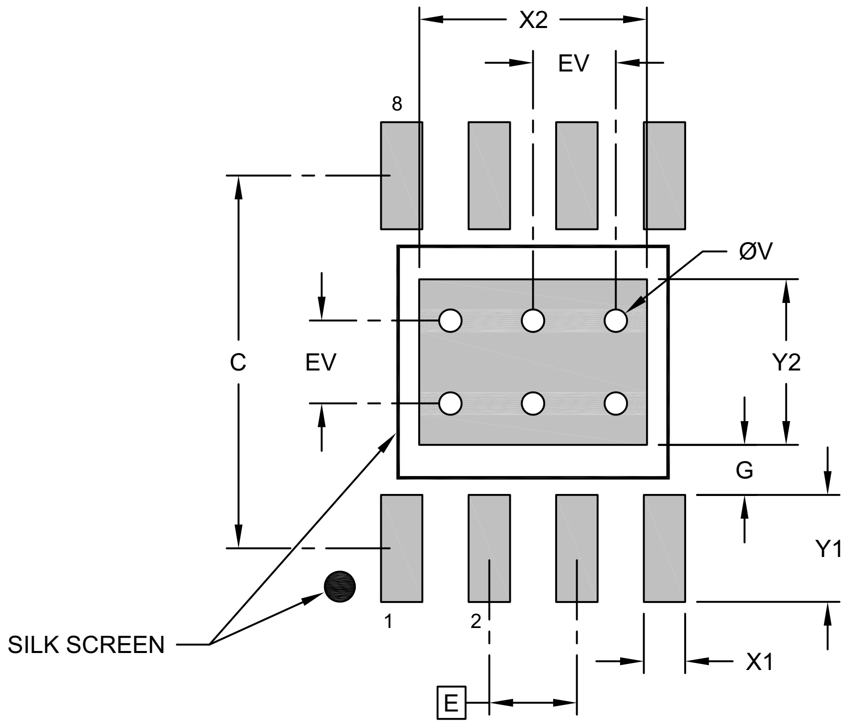
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-162-SE Rev D Sheet 2 of 2

8-Lead Thermally Enhanced Plastic Small Outline (SE) - Narrow, 3.90 mm Body [SOIC] With 2.2 x 3.0 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Center Pad Width	X2			3.30
Center Pad Length	Y2			2.40
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55
Contact Pad to Center Pad (X8)	G	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

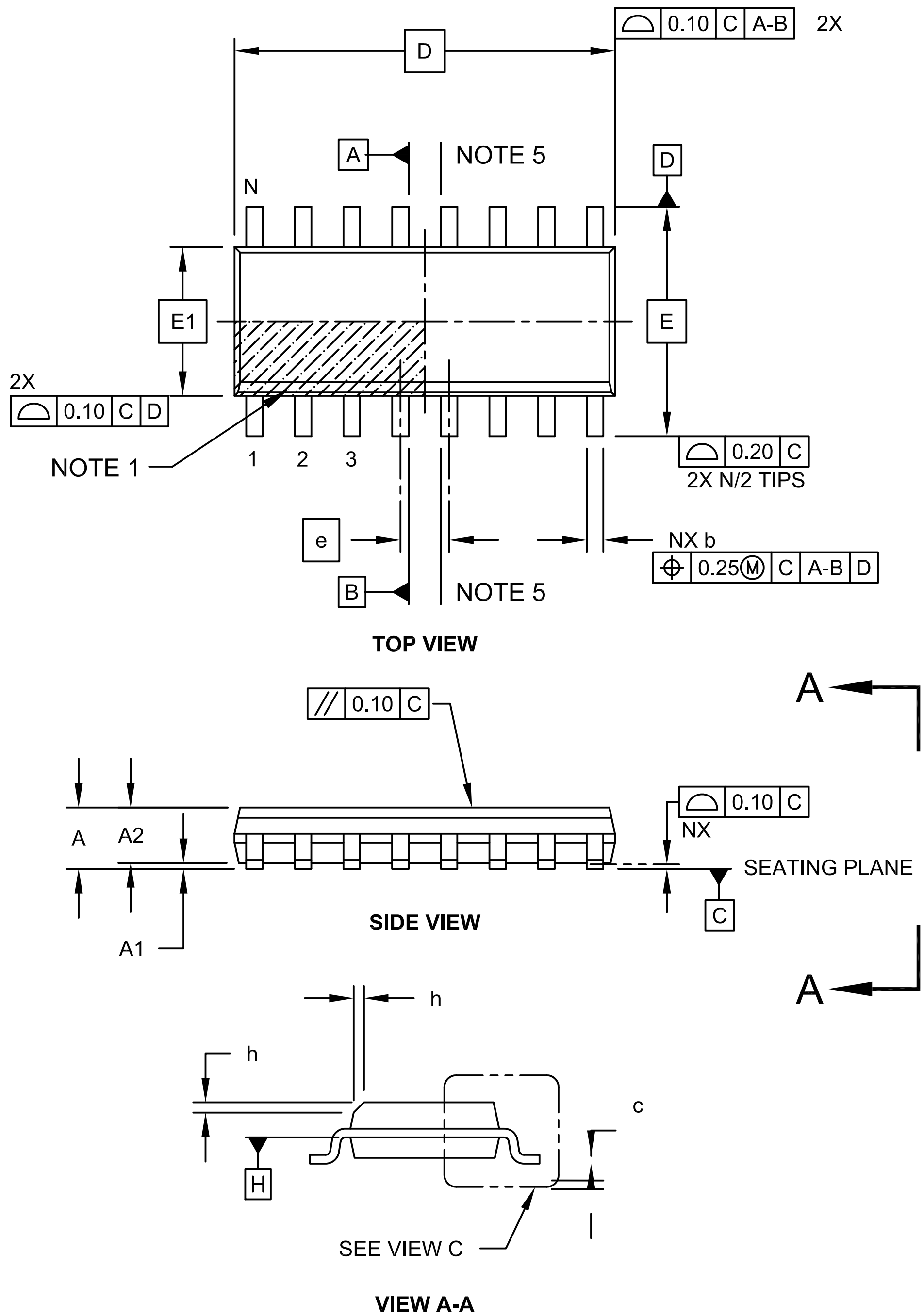
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing No. C04-2162-SE Rev D

16-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

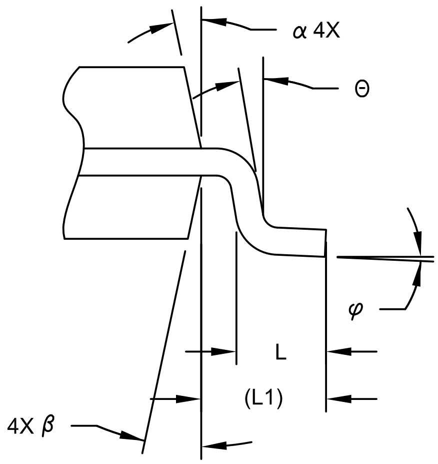
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



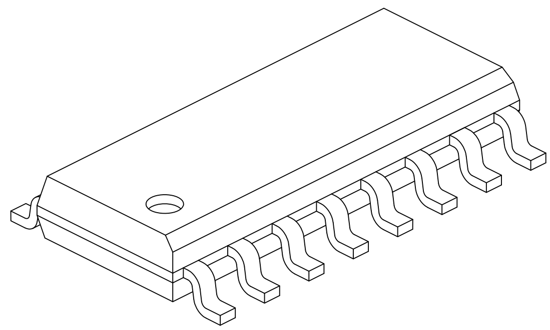
Microchip Technology Drawing No. C04-108C Sheet 1 of 2

16-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW C



	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	16		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	9.90 BSC		
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1	1.04 REF		
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.10	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

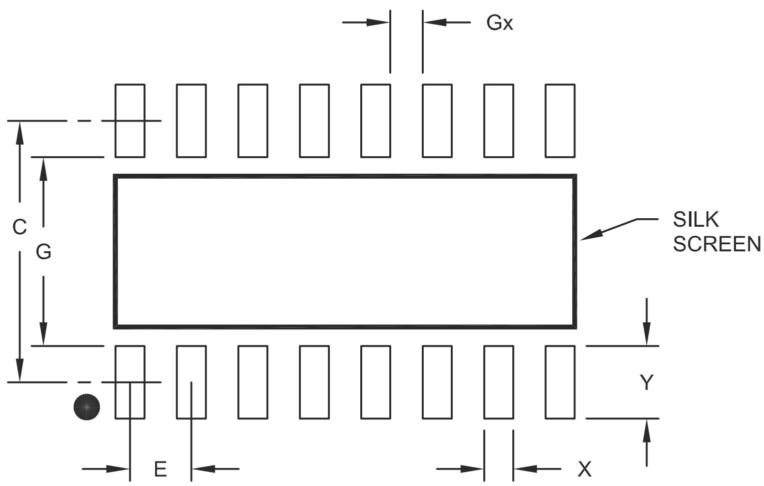
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-108C Sheet 2 of 2

16-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width	X			0.60
Contact Pad Length	Y			1.50
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	3.90		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2108A

APPENDIX A: REVISION HISTORY

Revision B (July 2022)

- Modified values in sections Internal Regulator and Current Sense Comparator in Table 1-1.
- Updated **Section 4.0 "Packaging Information"** with the latest package markings and drawings.
- Minor text and format changes throughout.

Revision A (August 2014)

- Original Release of this Document.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XX	-X	-XXXX[1]
Device	Package Options	Environmental	Reel

Device:	HV9910C=	Universal High-Brightness LED Driver
Package:	LG	= 8-Lead SOIC
	NG	= 16-Lead SOIC
	SG	= 8-Lead SOIC with heat slug
Environmental:	G	= Lead (Pb)-free/RoHS-compliant package
Reel:	Blank	= Reel for LG and SG packages, Tube for NG package
	M934	= Reel for NG package

Examples:

a) HV9910CLG-G: 8-Lead SOIC package, Lead (Pb)-free, RoHS-compliant, 3300/Reel.

b) HV9910CNG-G: 16-Lead SOIC package, Lead (Pb)-free, RoHS-compliant, 45/Tube

c) HV9910CNG-G-M934: 16-Lead SOIC package, Lead (Pb)-free, RoHS-compliant, 2600/Reel.

d) HV9910CSG-G: 8-Lead SOIC package with heat slug, Lead (Pb)-free, RoHS-compliant, 3300/Reel.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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