EMC1422

1°C Temperature Sensor with Hardware Thermal Shutdown

Features

- Hardware Thermal Shutdown
  - Triggers dedicated $\overline{SYS\_SHDN}$ pin
  - Hardware configured range +77°C to +112°C in +1°C steps
  - Cannot be disabled or modified by software
- Support for diodes requiring the BJT/transistor model
  - Supports 45 nm, 65 nm and 90 nm CPU thermal diodes
- Pin compatible with ADM1032, MAX6649 and LM99
- Automatically determines external diode type and optimal settings
- Resistance Error Correction
- External Temperature Monitors
  - ±1°C Accuracy (+60°C < T_{DIODE} < +100°C)
  - 0.125°C Resolution
  - Supports up to 2.2 nF diode filter capacitor
- Internal Temperature Monitor
  - ±2°C Accuracy
- 3.3V Supply Voltage
- Programmable temperature limits for $\overline{ALERT}$
- Available in Small 8-pin MSOP Lead-free RoH Compliant Package

Applications

- Notebook Computers
- Desktop Computers
- Industrial
- Embedded Applications

Description

The EMC1422 is a high-accuracy, low-cost, System Management Bus (SMBus) temperature sensor. Advanced features such as Resistance Error Correction (REC), Beta Compensation (to support CPU diodes requiring the BJT/transistor model including 45 nm, 65 nm and 90 nm processors) and automatic diode type detection combine to provide a robust solution for complex environmental monitoring applications.

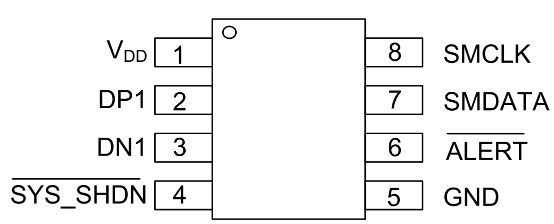
Additionally, the EMC1422 provides a hardware programmable system shutdown feature that is programmed at part power-up via two pull-up resistor values and that cannot be masked or corrupted through the SMBus.

Each device provides ±1° accuracy for external diode temperatures and ±2°C accuracy for the internal diode temperature. The EMC1422 monitors two temperature channels (one external and one internal).

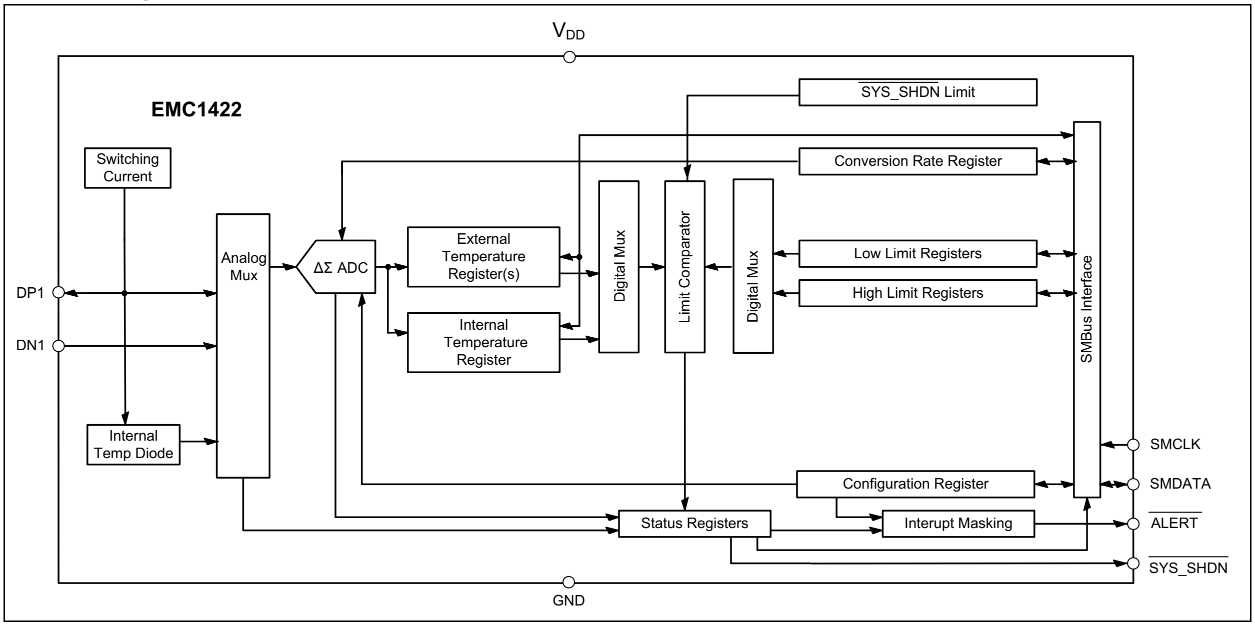
Resistance Error Correction automatically eliminates the temperature error caused by series resistance allowing greater flexibility in routing thermal diodes. Beta Compensation eliminates temperature errors caused by low, variable beta transistors common in today's fine geometry processors. The automatic beta detection feature monitors the external diode/transistor and determines the optimum sensor settings for accurate temperature measurements regardless of processor technology. This frees the user from providing unique sensor configurations for each temperature monitoring application. These advanced features plus ±1°C measurement accuracy provide a low-cost, highly flexible and accurate solution for critical temperature monitoring applications.

Package Types

EMC1422
8-pin MSOP



Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

1.1 Electrical Specifications

Absolute Maximum Ratings(†)

Supply Voltage (V_{DD}) .... -0.3V to +4.0V

Voltage on 5V tolerant pins (V_{5VT_pin}) .... -0.3 to 5.5V

Voltage on 5V tolerant pins ($|V_{5VT\_pin} - V_{DD}|$) (**Note**) .... -0.3 to 3.6V

Voltage on any other pin to Ground .... -0.3 to V_{DD} +0.3V

Operating Temperature Range .... -40 to +125°C

Storage Temperature Range .... -55 to +150°C

Lead Temperature Range .... Refer to JEDEC Spec. J-STD-020

Package Thermal Characteristics for 8-pin MSOP

Thermal Resistance (θ_{j-a}) .... 140.8°C/W

ESD Rating, All pins HBM 2000V

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

Note: For the 5V tolerant pins that have a pull-up resistor (SMCLK, SMDATA, $\overline{\text{SYS\_SHDN}}$ and $\overline{\text{ALERT}}$), the pull-up voltage must not exceed 3.6V when the device is unpowered.

TABLE 1-1: ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise specified V_{DD} = 3.0V to 3.6V, T_A = -40°C to +125°C, all typical values at T_A = +27°C

Characteristic	Sym.	Min.	Typ.	Max.	Units	Conditions
DC Power						
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	
Supply Current	I_{DD}	—	430	850	µA	One conversion/second, dynamic averaging disabled
		—	930	1200	µA	Four conversions/second, dynamic averaging enabled
		—	1120	—	µA	≥16 conversions/second, dynamic averaging enabled
Internal Temperature Monitor						
Temperature Accuracy	—	—	±0.25	±1	°C	-5°C < T_A < +100°C
		—		±2	°C	-40°C < T_A < +125°C
Temperature Resolution	—	—	0.125	—	°C	

Note: During the power up time, SMBus communication is permitted, however the $\overline{\text{SYS\_SHDN}}$ and $\overline{\text{ALERT}}$ pins must not be pulled low.

TABLE 1-1: ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise specified V_{DD} = 3.0V to 3.6V, T_A = -40°C to +125°C, all typical values at T_A = +27°C

Characteristic	Sym.	Min.	Typ.	Max.	Units	Conditions
External Temperature Monitor						
Temperature Accuracy	—	—	±0.25	±1	°C	+20°C < T_{DIODE} < +110°C 0°C < T_A < +100°C
		—	±0.5	±2	°C	-40°C < T_{DIODE} < +127°C
Temperature Resolution	—	—	0.125	—	°C	
Conversion Time all Channels	t_{CONV}	—	190	—	ms	EMC1422, default settings
Capacitive Filter	C_{FILTER}	—	2.2	2.5	nF	Connected across external diode
ALERT and SYS_SHDN Pins						
Output Low Voltage	V_{OL}	0.4	—	—	V	I_{SINK} = 8 mA
Leakage Current	I_{LEAK}	—	—	±5	µA	$\overline{\text{ALERT}}$ and $\overline{\text{SYS\_SHDN}}$ pins Device powered or unpowered T_A < +85°C Pull-up voltage < 3.6V
Power up time	—	—	—	15	ms	Temp selection read (**Note**)

Note: During the power up time, SMBus communication is permitted, however the $\overline{\text{SYS\_SHDN}}$ and $\overline{\text{ALERT}}$ pins must not be pulled low.

1.2 SMBus Electrical Characteristics

TABLE 1-2: SMBUS ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise specified V_{DD} = 3.0V to 3.6V, T_A = -40°C to +125°C, all typical values at T_A = +27°C

Characteristic	Sym.	Min.	Typ.	Max.	Units	Conditions
SMBus Interface						
Input High Voltage	V_{IH}	2.0	—	V_{DD}	V	5V Tolerant
Input Low Voltage	V_{IL}	-0.3	—	0.8	V	5V Tolerant
Input High/Low Current	I_{IH}/I_{IL}	—	—	±5	µA	Powered or unpowered T_A < +85°C
Hysteresis	—	—	420	—	mV	
Input Capacitance	C_{IN}	—	5	—	pF	
Output Low Sink Current	I_{OL}	8.2	—	15	mA	SMDATA = 0.4V
SMBus Timing						
Clock Frequency	f_{SMB}	10	—	400	kHz	
Spike Suppression	t_{SP}	—	—	50	ns	
Bus free time Start to Stop	t_{BUF}	1.3	—	—	µs	
Hold Time: Start	$t_{HD:STA}$	0.6	—	—	µs	
Setup Time: Start	$t_{SU:STA}$	0.6	—	—	µs	
Setup Time: Stop	$t_{SU:STP}$	0.6	—	—	µs	
Data Hold Time	$t_{HD:DAT}$	0	—	—	µs	When transmitting to the host
Data Hold Time	$t_{HD:DAT}$	0.3	—	—	µs	When receiving from the host
Data Setup Time	$t_{SU:DAT}$	100	—	—	ns	

TABLE 1-2: SMBUS ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise specified V_{DD} = 3.0V to 3.6V, T_A = -40°C to +125°C, all typical values at T_A = +27°C						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Clock Low Period	t_{LOW}	1.3	—	—	µs	
Clock High Period	t_{HIGH}	0.6	—	—	µs	
Clock/Data Fall Time	t_{FALL}	—	—	300	ns	Min = 20+0.1C_{LOAD} ns
Clock/Data Rise Time	t_{RISE}	—	—	300	ns	Min = 20+0.1C_{LOAD} ns
Capacitive Load	C_{LOAD}	—	—	400	pF	Per bus line

2.0 TYPICAL OPERATING CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

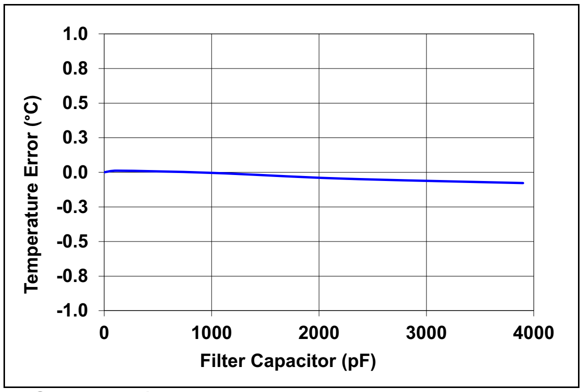


FIGURE 2-1: *Temperature Error vs. Filter Capacitor (V_{DD} = 3.3V, T_A = T_{DIODE} = +27°C, 2N3904).*

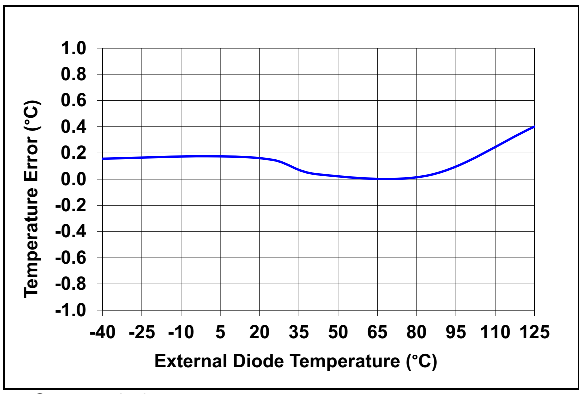


FIGURE 2-2: *Temperature Error vs. External Diode Temperature (T_A = +42.5°C, V_{DD} = 3.3V, 2N3904).*

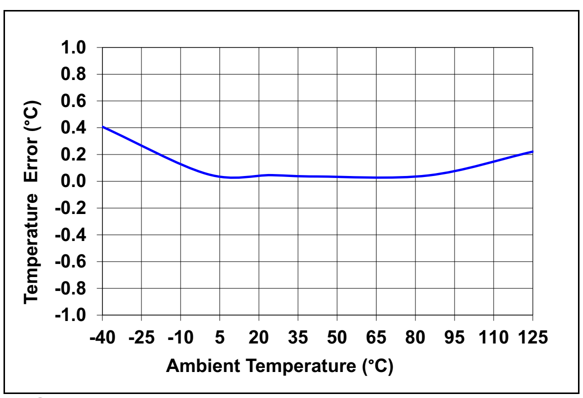


FIGURE 2-3: *Temperature Error vs. Ambient Temperature (T_{DIODE} = +42.5°C, V_{DD} = 3.3V, 2N3904).*

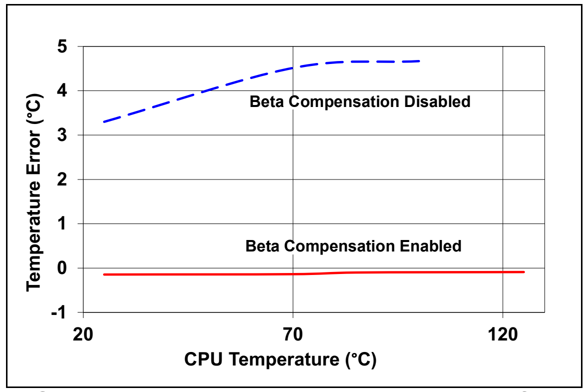


FIGURE 2-4: *Temperature Error vs. CPU Temperature (T_A = +27°C, V_{DD} = 3.3V, BETA = 011, C_{FILTER} = 470 pF).*

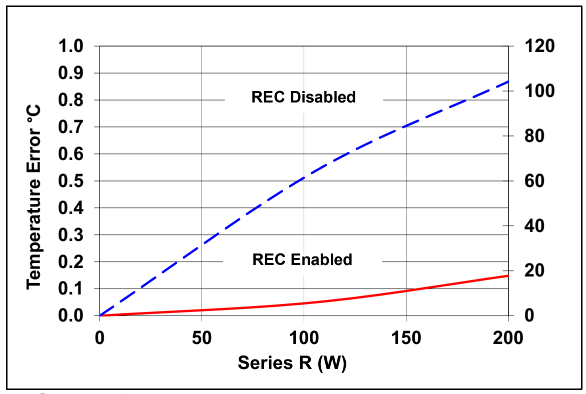


FIGURE 2-5: *Temperature Error vs. Series Resistance.*

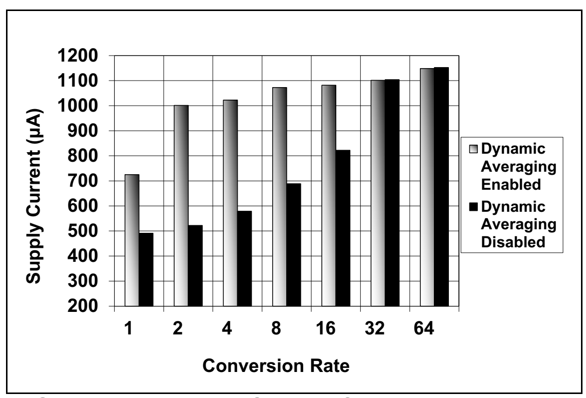


FIGURE 2-6: *Supply Current vs. Conversion Rate.*

3.0 SYSTEM MANAGEMENT BUS INTERFACE PROTOCOL

3.1 System Management Bus Interface Protocol

The EMC1422 communicates with a host controller through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 3-1.

For the first 15 ms after power-up the device may not respond to SMBus communications.

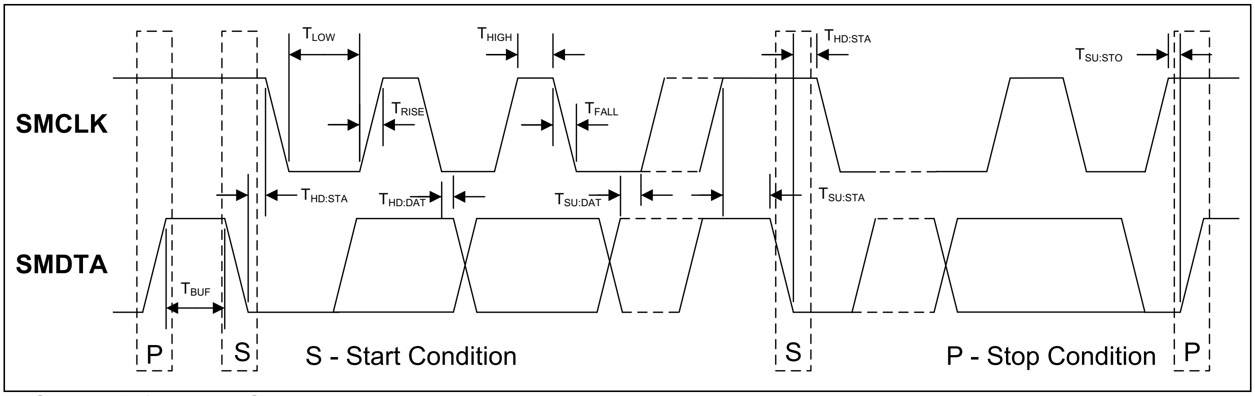


FIGURE 3-1: SMBus Timing Diagram.

The EMC1422 is SMBus 2.0 compatible and support Send Byte, Read Byte, Write Byte, Receive Byte, and the Alert Response Address as valid protocols as shown below.

All of the below protocols use the convention in Table 3-1.

TABLE 3-1: PROTOCOL FORMAT

Data Sent to Device	Data Sent to the Host
# of bits sent	# of bits sent

Attempting to communicate with the EMC1422 SMBus interface with an invalid client address or invalid protocol will result in no response from the device and will not affect its register contents. Stretching of the SMCLK signal is supported, provided other devices on the SMBus control the timing.

3.2 Write Byte

The Write Byte is used to write one byte of data to the registers as shown below Table 3-2.

TABLE 3-2: WRITE BYTE PROTOCOL

START	Client Address	WR	ACK	Register Address	ACK	Register Data	ACK	STOP
1 → 0	1001_100	0	0	XXh	0	XXh	0	0 → 1

3.3 Read Byte

The Read Byte protocol is used to read one byte of data from the registers as shown in Table 3-3.

TABLE 3-3: READ BYTE PROTOCOL

START	Client Address	WR	ACK	Register Address	ACK	
1 → 0	1001_100	0	0	XXh	0	
START	**Client Address**	**RD**	**ACK**	**Register Data**	**NACK**	**STOP**
1 → 0	1001_100	1	0	XXh	1	0 → 1

3.4 Send Byte

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol as shown in Table 3-4.

TABLE 3-4: SEND BYTE PROTOCOL

START	Client Address	WR	ACK	Register Address	ACK	STOP
1 → 0	1001_100	0	0	XXh	0	0 → 1

3.5 Receive Byte

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g. set via Send Byte). This is used for consecutive reads of the same register as shown in Table 3-5.

TABLE 3-5: RECEIVE BYTE PROTOCOL

START	Client Address	RD	ACK	Register Data	NACK	STOP
1 → 0	1001_100	1	0	XXh	1	0 → 1

3.6 Alert Response Address

The $\overline{\text{ALERT}}$ output can be used as a processor interrupt or as an SMBus Alert.

When it detects that the $\overline{\text{ALERT}}$ pin is asserted, the host will send the Alert Response Address (ARA) to the general address of 0001_100xb. All devices with active interrupts will respond with their client address as shown in Table 3-6.

TABLE 3-6: ALERT RESPONSE ADDRESS PROTOCOL

START	ALERT Response Address	RD	ACK	Device Address	NACK	STOP
1 → 0	0001_100	1	0	1001_1000	1	0 → 1

The EMC1422 will respond to the ARA in the following way:

- Send client Address and verify that full client address was sent (i.e. the SMBus communication from the device was not prematurely stopped due to a bus contention event).
- Set the MASK bit to clear the $\overline{\text{ALERT}}$ pin.

The ARA does not clear the Status Register and if the MASK bit is cleared prior to the Status Register being cleared, the $\overline{\text{ALERT}}$ pin will be reasserted.

3.7 SMBus Address

The EMC1422 responds to hard-wired SMBus client address.

3.8 SMBus Timeout

The EMC1422 supports SMBus Timeout. If the clock line is held low for longer than 30 ms, the device will reset its SMBus protocol. This function can be enabled by setting the TIMEOUT bit in the Consecutive Alert Register (Register 6-22).

4.0 PIN DESCRIPTIONS

The description of the pins is listed in Table 4-1.

TABLE 4-1: EMC1422 PIN DESCRIPTION

8-pin MSOP	Pin Name	Pin Type	Description
1	V_{DD}	Power	Power supply
2	DP	AIO	External diode positive (anode) connection
3	DN	AIO	External diode negative (cathode) connection
4	$\overline{\text{SYS\_SHDN}}$	OD (5V)	Active low System Shutdown output signal – requires pull-up resistor which selects the Hardware Thermal Shutdown Limit
5	GND	Power	Ground
6	$\overline{\text{ALERT}}$	OD (5V)	Active low digital ALERT output signal – requires pull-up resistor
7	SMDATA	DIOD (5V)	SMBus Data input/output – requires pull-up resistor
8	SMCLK	DI (5V)	SMBus Clock input – requires pull-up resistor

For the 5V tolerant pins that have a pull-up resistor (SMCLK, SMDATA, $\overline{\text{SYS\_SHDN}}$ and $\overline{\text{ALERT}}$), the voltage difference between V_{DD} and the pull-up voltage must never exceed 3.6V.

The pin types are described in Table 4-2.

TABLE 4-2: PIN TYPES

Power	These pins are used to supply either V_{DD} or GND to the device
AIO	Analog Input/Output
DI	Digital Input
OD	Open Drain Digital Output
DIOD	Digital Input/Open Drain Output

5.0 PRODUCT DESCRIPTION

The EMC1422 is an SMBus temperature sensor with Hardware Thermal Shutdown. The EMC1422 monitors one internal diode and one externally connected temperature diode.

Thermal management is performed in cooperation with a host device. This consists of the host reading the temperature data of both the external and internal temperature diodes of the EMC1422 and using that data to control the speed of one or more fans.

The EMC1422 has two levels of monitoring. The first provides a maskable ALERT signal to the host when measured temperatures meet or exceed user programmable limits. This allows the EMC1422 to be used as an independent thermal watchdog to warn the host of temperature hot spots without direct control by the host.

The second level of monitoring asserts the SYS_SHDN pin when the External Diode temperature exceeds a hardware specified threshold temperature. Additionally, the internal diode can be configured to assert the SYS_SHDN pin when the measured temperature exceeds user programmable limits.

Since the EMC1422 automatically corrects for temperature errors due to series resistance in temperature diode lines, there is greater flexibility in where external diodes are positioned and better measurement accuracy than previously available with non-resistance error correcting devices. The automatic beta detection feature means that there is no need to program the device according to which type of diode is present. This also includes CPU diodes that require the transistor or BJT model for monitoring their temperature. Therefore, the EMC1422 can power up ready to operate for any system configuration.

Figure 5-1 shows a system level block diagram of the EMC1422.

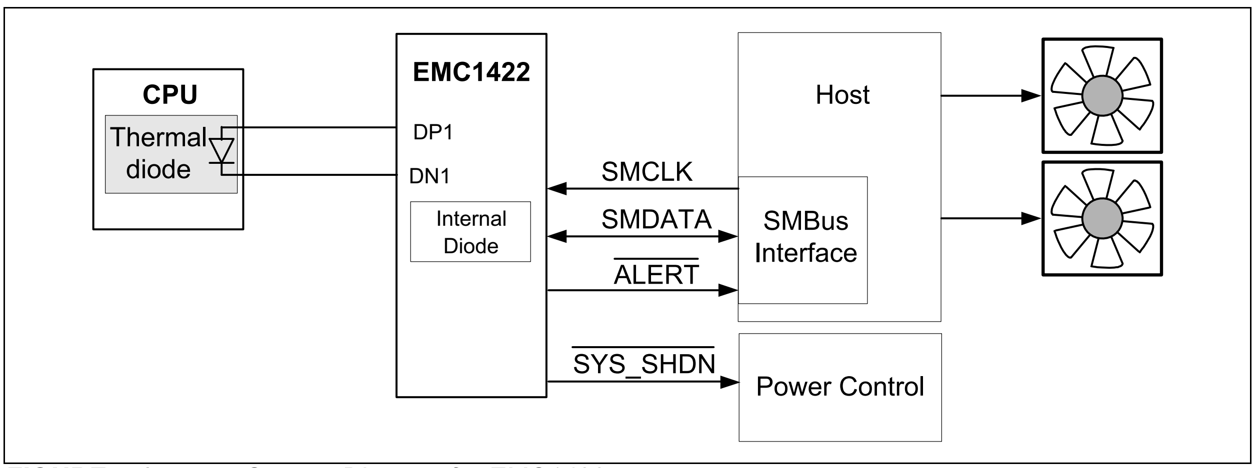


FIGURE 5-1: *System Diagram for EMC1422.*

5.1 Conversion Rates

The EMC1422 may be configured for different conversion rates based on the system requirements. The conversion rate is configured as described in Register 6-7. The default conversion rate is 4 conversions per second.

5.2 Dynamic Averaging

Dynamic averaging causes the EMC1422 to measure the external diode channels for an extended time based on the selected conversion rate. This functionality can be disabled for increased power savings at the lower conversion rates (see Register 6-6). When dynamic averaging is enabled, the device will automatically adjust the sampling and measurement time for the external diode channels. This allows the device to average 2x or 16x longer than the normal 11 bit operation (nominally 21ms per channel) while still maintaining the selected conversion rate. The benefits of dynamic averaging are improved noise rejection due to the longer integration time as well as less random variation of the temperature measurement.

When enabled, the dynamic averaging will affect the average supply current based on the chosen conversion rate as shown in Table 5-1 for the EMC1422.

TABLE 5-1: SUPPLY CURRENT VS. CONVERSION RATE FOR EMC1422

Conversion Rate	Average Supply Current		Averaging Factor (Based on 11-bit Operation)	
	Enabled (Default)	Disabled	Enabled (Default)	Disabled
1/sec	660 µA	430 µA	16x	1x
2/sec	930 µA	475uA µA	16x	1x
4/sec (default)	950 µA	510 µA	8x	1x
8/sec	1010 µA	630 µA	4x	1x
16/sec	1020 µA	775 µA	2x	1x
32/sec	1050 µA	1050 µA	1x	1x
64/sec	1100 µA	1100 µA	0.5x	0.5x

5.3 SYS_SHDN Output

The SYS_SHDN output is asserted independently of the ALERT output and cannot be masked. If the External Diode temperature exceeds the Hardware Thermal Shutdown Limit for the programmed number of consecutive measurements, then the SYS_SHDN pin is asserted.

The Hardware Thermal Shutdown Limit is defined at power-up via the pull-up resistors on the SYS_SHDN and ALERT pins as shown in Table 5-2. This limit cannot be modified or masked via software.

In addition to External Diode channel triggering the SYS_SHDN pin when the measured temperature exceeds to the Hardware Thermal Shutdown Limit, each of the measurement channels can be configured to assert the SYS_SHDN pin when they exceed the corresponding THERM Limit.

When the SYS_SHDN pin is asserted, it will not release until the External Diode temperature drops below the Hardware Thermal Shutdown Limit minus 10°C and all other measured temperatures drop below the THERM Limit minus the THERM Hysteresis value (when linked to SYS_SHDN).

Figure 5-2 shows a block diagram of the interaction between the input channels and the SYS_SHDN pin.

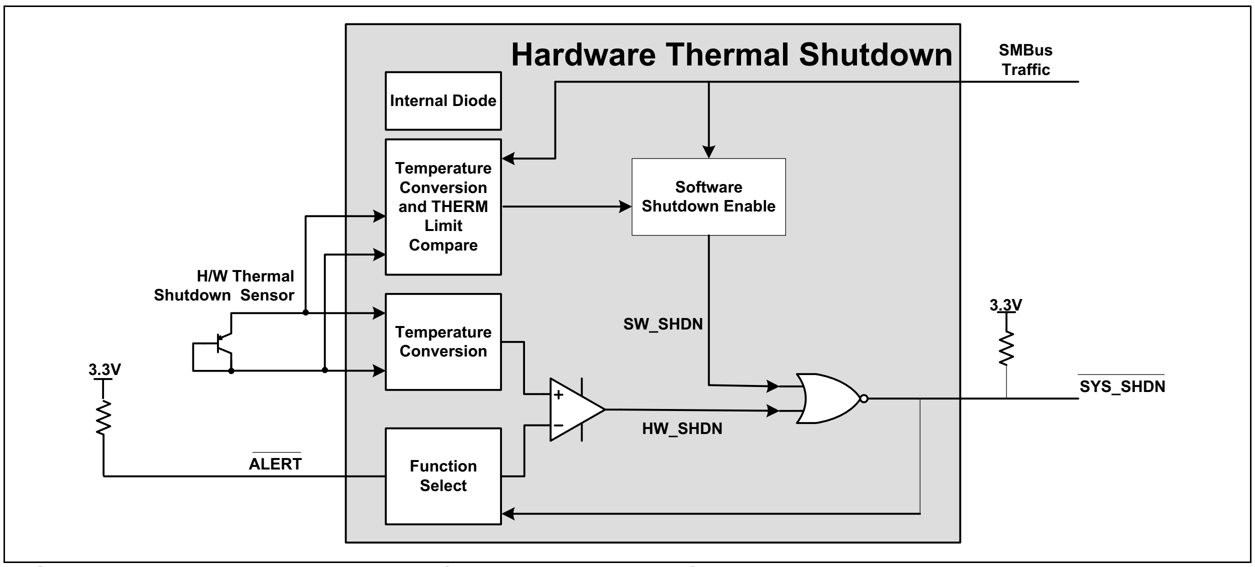


FIGURE 5-2: Block Diagram of Hardware Thermal Shutdown.

5.4 Hardware Thermal Shutdown Limit

The Hardware Thermal Shutdown Limit temperature is determined by pull-up resistors on the SYS_SHDN and ALERT pins shown in Table 5-2.

TABLE 5-2: SYS_SHDN THRESHOLD TEMPERATURE

SYS_SHD Pull-up / ALERT Pull-up	4.7 kΩ ±10%	6.8 kΩ ±10%	10 kΩ ±10%	15 kΩ ±10%	22 kΩ ±10%	33 kΩ ±10%
4.7 kΩ ±10%	77°C	83°C	89°C	95°C	101°C	107°C
6.8 kΩ ±10%	78°C	84°C	90°C	96°C	102°C	108°C
10 kΩ ±10%	79°C	85°C	91°C	97°C	103°C	109°C
15 kΩ ±10%	80°C	86°C	92°C	98°C	104°C	110°C
22 kΩ ±10%	81°C	87°C	93°C	99°C	105°C	111°C
33 kΩ ±10%	82°C	88°C	94°C	100°C	106°C	112°C

5.5 ALERT Output

The ALERT pin is an open drain output and requires a pull-up resistor to V_{DD} and has two modes of operation: interrupt mode and comparator Mode. The mode of the ALERT output is selected via the AT/COMP bit in the Configuration Register (see Register 6-6).

5.5.1 ALERT PIN INTERRUPT MODE

When configured to operate in interrupt mode, the ALERT pin asserts low when an out of limit measurement (≥ high limit or < low limit) is detected on any diode or when a diode fault is detected. The ALERT pin will remain asserted as long as an out-of-limit condition remains. Once the out-of-limit condition has been removed, the ALERT pin will remain asserted until the appropriate status bits are cleared.

The ALERT pin can be masked by setting the MASK bit. Once the ALERT pin has been masked, it will be de-asserted and remain deasserted until the MASK bit is cleared by the user. Any interrupt conditions that occur while the ALERT pin is masked will update the Status Register normally.

The ALERT pin is used as an interrupt signal or as an SMBus Alert signal that allows an SMBus client to communicate an error condition to the host. One or more ALERT outputs can be hard-wired together.

5.5.2 ALERT PIN COMPARATOR MODE

When the ALERT pin is configured to operate in comparator mode it will be asserted if any of the measured temperatures exceeds the respective high limit. The ALERT pin will remain asserted until all temperatures drop below the corresponding high limit minus the THERM Hysteresis value.

When the ALERT pin is asserted in comparator mode, the corresponding high limit status bits will be set. Reading these bits will not clear them until the ALERT pin is deasserted. Once the ALERT pin is deasserted, the status bits will be automatically cleared.

The MASK bit will not block the ALERT pin in this mode, however the individual channel masks (see Register 6-21) will prevent the respective channel from asserting the ALERT pin.

5.6 ALERT and SYS_SHDN Pin Considerations

Because of the decode method used to determine the Hardware Thermal Shutdown Limit, it is important that the pull-up resistance on both the ALERT and SYS_SHDN pins be within the tolerances shown in Table 5-2. Additionally, the pull-up resistor on the ALERT and SYS_SHDN pins must be connected to the same 3.3V supply that drives the V_{DD} pin.

For 1 5ms after power up, the ALERT and SYS_SHDN pins must not be pulled low or the Hardware Thermal Shutdown Limit will not be decoded properly. If the system requirements do not permit these conditions, then the ALERT and SYS_SHDN pins must be isolated from their respective buses during this time.

One method of isolating this pin is shown in Figure 5.3.

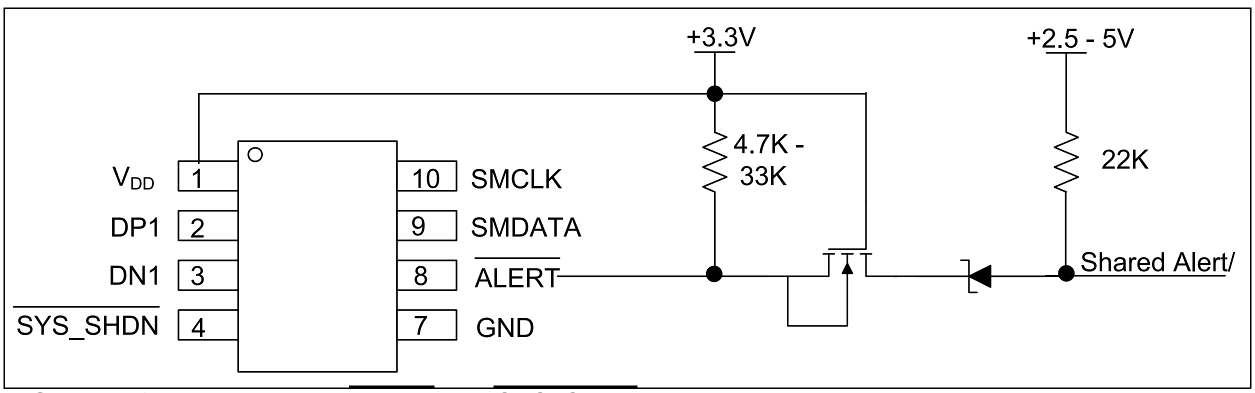


FIGURE 5-3: *Isolating ALERT and SYS_SHDN Pins.*

5.7 Beta Compensation

The EMC1422 is configured to monitor the temperature of basic diodes (e.g. 2N3904), or CPU thermal diodes. It automatically detects the type of external diode (CPU diode or diode connected transistor) and determines the optimal setting to reduce temperature errors introduced by beta variation.Compensating for this error is also known as implementing the transistor or BJT model for temperature measurement.

For discrete transistors configured with the collector and base shorted together, the beta is generally sufficiently high such that the percent change in beta variation is very small. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 50 would contribute approximately 0.25°C error at 100°C. However for substrate transistors where the base-emitter junction is used for temperature measurement and the collector is tied to the substrate, the proportional beta variation will cause large error. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 0.5 would contribute approximately 8.25°C error at 100°C.

5.8 Resistance Error Correction (REC)

Parasitic resistance in series with the external diodes will limit the accuracy obtainable from temperature measurement devices. The voltage developed across this resistance by the switching diode currents cause the temperature measurement to read higher than the true temperature. Contributors to series resistance are Printed Circuit Board (PCB) trace resistance, on die (i.e. on the processor) metal resistance, bulk resistance in the base and emitter of the temperature transistor. Typically, the error caused by series resistance is +0.7°C per ohm. The EMC1422 automatically corrects up to 100 ohms of series resistance.

5.9 Diode Faults

The EMC1422 detects an open on the DP and DN pins, and a short across the DP and DN pins. For each temperature measurement made, the device checks for a diode fault on the external diode channel(s). When a diode fault is detected, the $\overline{\text{ALERT}}$ pin asserts (unless masked, see Section 5.10, Consecutive Alerts) and the temperature data reads 00h in the MSb and LSb registers (note: the low limit will not be checked). A diode fault is defined as one of the following: an open between DP and DN, a short from V_{DD} to DP or a short from V_{DD} to DN.

If a short occurs across DP and DN or a short occurs from DP to GND, the low limit status bit is set and the $\overline{\text{ALERT}}$ pin asserts (unless masked). This condition is indistinguishable from a temperature measurement of 0.000°C (-64°C in extended range) resulting in temperature data of 00h in the MSb and LSb registers.

If a short from DN to GND occurs (with a diode connected), temperature measurements will continue as normal with no alerts.

5.10 Consecutive Alerts

The EMC1422 contains multiple consecutive alert counters. One set of counters applies to the $\overline{\text{ALERT}}$ pin and the second set of counters applies to the $\overline{\text{SYS\_SHDN}}$ pin. Each temperature measurement channel has a separate consecutive alert counter for each of the $\overline{\text{ALERT}}$ and $\overline{\text{SYS\_SHDN}}$ pins. All counters are user programmable and determine the number of consecutive measurements that a temperature channel(s) must be out-of-limit or reporting a diode fault before the corresponding pin is asserted.

See Register 6-22 for more details on the consecutive alert function.

5.11 Digital Filter

To reduce the effect of noise and temperature spikes on the reported temperature, the External Diode channel uses a programmable digital filter. This filter can be configured as Level 1, Level 2 or Disabled. The typical filter performance is shown in Figure 5-4 and Figure 5-5.

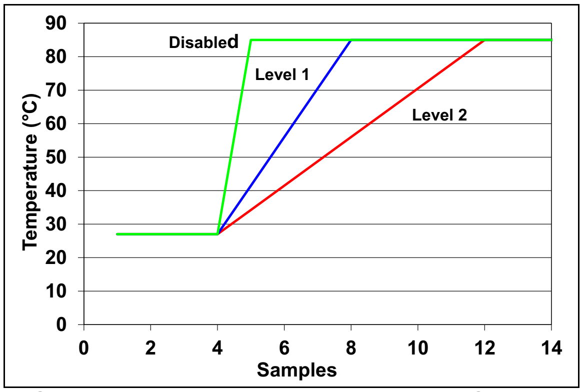


FIGURE 5-4: *Temperature Filter Step Response.*

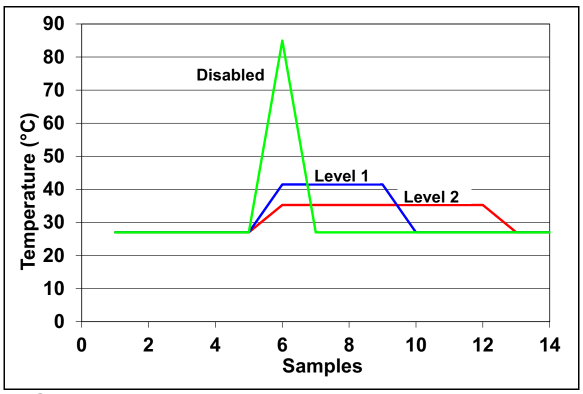


FIGURE 5-5: *Temperature Filter Impulse Response.*

5.12 Temperature Monitors

In general, thermal diode temperature measurements are based on the change in forward bias voltage of a diode when operated at two different currents. This ΔV_{BE} is proportional to absolute temperature as shown in Equation 5-1.

EQUATION 5-1:

$$\Delta V_{BE} = \frac{\eta k T}{q} \ln\left(\frac{I_{HIGH}}{I_{LOW}}\right)$$

Where:

k	=	Boltzmann's constant
T	=	Absolute temperature in Kelvin
q	=	Electron charge
η	=	Diode ideality factor

Figure 5-6 shows a block diagram of the temperature measurement circuit. The negative terminal for the remote temperature diode, DN, is internally biased with a forward diode voltage referenced to ground.

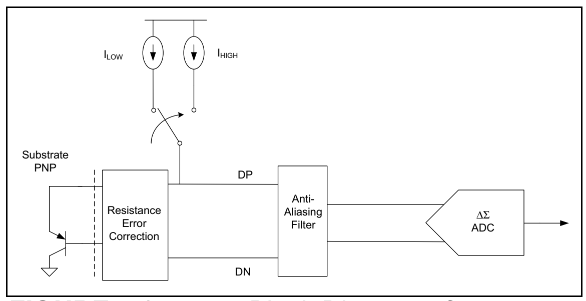


FIGURE 5-6: *Block Diagram of Temperature Monitoring Circuit.*

5.13 Temperature Measurement Results and Data

The temperature measurement results are stored in the internal and external temperature registers. These are then compared with the values stored in the high and low limit registers. Both external and internal temperature measurements are stored in 11-bit format with the eight (8) most significant bits stored in a high byte register and the three (3) least significant bits stored in the three (3) MSB positions of the low byte register. All other bits of the low byte register are set to zero.

The EMC1422 has two selectable temperature ranges. The default range is from 0°C to +127°C and the temperature is represented as binary number able to report a temperature from 0°C to +127.875°C in 0.125°C steps.

The extended range is an extended temperature range from -64°C to +191°C. The data format is a binary number offset by 64°C. The extended range is used to measure temperature diodes with a large known offset (such as AMD processor diodes) where the diode temperature plus the offset would be equivalent to a temperature higher than +127°C.

Table 5-3 shows the default and extended range formats.

TABLE 5-3: TEMPERATURE DATA FORMAT

Temperature (°C)	Default Range 0°C to +127°C	Extended Range -64°C to +191°C
Diode Fault	000 0000 0000	000 0000 0000
-64	000 0000 0000	000 0000 0000 (Note 2)
-1	000 0000 0000	001 1111 1000
0	000 0000 0000 (Note 1)	010 0000 0000
0.125	000 0000 0001	010 0000 0001
1	000 0000 1000	010 0000 1000
64	010 0000 0000	100 0000 0000
65	010 0000 1000	100 0000 1000
127	011 1111 1000	101 1111 1000
127.875	011 1111 1111	101 1111 1111
128	011 1111 1111 (Note 3)	110 0000 0000
190	011 1111 1111	111 1111 0000
191	011 1111 1111	111 1111 1000
≥ 191.875	011 1111 1111	111 1111 1111 (Note 4)

Note 1: In default mode, all temperatures < 0°C will be reported as 0°C

2: In the extended range, all temperatures less than -64°C will be reported as -64°C.

3: For the default range, all temperatures greater than +127.875°C will be reported as +127.875°C.

4: For the extended range, all temperatures greater than +191.875°C will be reported as +191.875°C.

5.14 External Diode Connections

The EMC1422 is hard-wired to measure a specific kind of thermal diode and none of the measurement options can be changed by software. Figure 5-7 shows the different diode configurations.

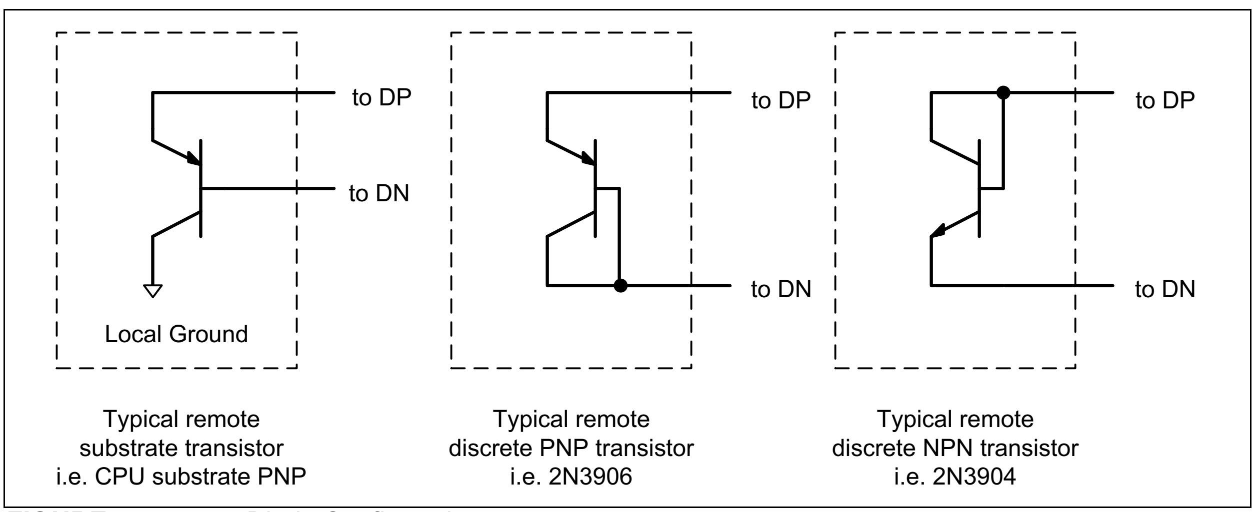


FIGURE 5-7: Diode Configurations.

6.0 REGISTER DESCRIPTION

The registers shown in Table 6-1 are accessible through the SMBus. An entry of '-' indicates that the bit is not used and will always read '0'.

TABLE 6-1: REGISTER SET IN HEXADECIMAL ORDER

Register Address	R/W	Register Name	Function	Default Value
00h	R	Internal Diode Data High Byte	Stores the integer data for the Internal Diode	00h
01h	R	External Diode Data High Byte	Stores the integer data for External Diode	00h
02h	R	Status	Stores the status bits for the Internal Diode and External Diodes	00h
03h	R/W	Configuration	Controls the general operation of the device (mirrored at address 09h)	00h
04h	R/W	Conversion Rate	Controls the conversion rate for updating temperature data (mirrored at address 0Ah)	06h (4/sec)
05h	R/W	Internal Diode High Limit	Stores the 8-bit high limit for the Internal Diode (mirrored at address 0Bh)	55h (+85°C)
06h	R/W	Internal Diode Low Limit	Stores the 8-bit low limit for the Internal Diode (mirrored at address 0Ch)	00h (0°C)
07h	R/W	External Diode High Limit High Byte	Stores the integer portion of the high limit for External Diode (mirrored at register 0Dh)	55h (+85°C)
08h	R/W	External Diode Low Limit High Byte	Stores the integer portion of the low limit for External Diode (mirrored at register 0Eh)	00h (0°C)
09h	R/W	Configuration	Controls the general operation of the device (mirrored at address 03h)	00h
0Ah	R/W	Conversion Rate	Controls the conversion rate for updating temperature data (mirrored at address 04h)	06h (4/sec)
0Bh	R/W	Internal Diode High Limit	Stores the 8-bit high limit for the Internal Diode (mirrored at address 05h)	55h (+85°C)
0Ch	R/W	Internal Diode Low Limit	Stores the 8-bit low limit for the Internal Diode (mirrored at address 06h)	00h (0°C)
0Dh	R/W	External Diode High Limit High Byte	Stores the integer portion of the high limit for External Diode (mirrored at register 07h)	55h (+85°C)
0Eh	R/W	External Diode Low Limit High Byte	Stores the integer portion of the low limit for External Diode (mirrored at register 08h)	00h (0°C)
10h	R	External Diode Data Low Byte	Stores the fractional data for External Diode	00h
11h	R/W	Scratchpad	Scratchpad register for software compatibility	00h
12h	R/W	Scratchpad	Scratchpad register for software compatibility	00h
13h	R/W	External Diode High Limit Low Byte	Stores the fractional portion of the high limit for External Diode	00h

TABLE 6-1: REGISTER SET IN HEXADECIMAL ORDER (CONTINUED)

Register Address	R/W	Register Name	Function	Default Value
14h	R/W	External Diode Low Limit Low Byte	Stores the fractional portion of the low limit for External Diode	00h
19h	R/W	External Diode THERM Limit	Stores the 8-bit critical temperature limit for External Diode	55h (+85°C)
1Dh	R/W	SYS_SHDN Configuration	Controls which software channels, if any, are linked to the SYS_SHDN pin	00h
1Eh	R	Hardware Thermal Shutdown Limit	When read, returns the selected Hardware Thermal Shutdown Limit	N/A
1Fh	R/W	Channel Mask Register	Controls the masking of individual channels	00h
20h	R/W	Internal Diode THERM Limit	Stores the 8-bit critical temperature limit for the Internal Diode	55h (+85°C)
21h	R/W	THERM Hysteresis	Stores the 8-bit hysteresis value that applies to all THERM limits	0Ah (+10°C)
22h	R/W	Consecutive ALERT	Controls the number of out-of-limit conditions that must occur before an interrupt is asserted	70h
29h	R	Internal Diode Data Low Byte	Stores the fractional data for the Internal Diode	00h
35h	R-C	High Limit Status	Status bits for the High Limits	00h
36h	R-C	Low Limit Status	Status bits for the Low Limits	00h
37h	R	THERM Limit Status	Status bits for the THERM Limits	00h
40h	R/W	Filter Control	Controls the digital filter setting for the External Diode channel	00h
FDh	R	Product ID	Stores a fixed value that identifies each product	Register 6-27
FEh	R	Microchip ID	Stores a fixed value that represents Microchip	5Dh
FFh	R	Revision	Stores a fixed value that represents the revision number	01h or 04h

6.1 Data Read Interlock

When any temperature channel high byte register is read, the corresponding low byte is copied into an internal ‘shadow’ register. The user is free to read the low byte at any time and be guaranteed that it will correspond to the previously read high byte. Regardless if the low byte is read or not, reading from the same high byte register again will automatically refresh this stored low byte data.

6.2 Temperature Data Registers

All temperatures are stored as an 11-bit value with the high byte representing the integer value and the low byte representing the fractional value left justified to occupy the MSBits.

REGISTER 6-1: INTERNAL DIODE HIGH BYTE REGISTER (ADDRESS 00h)

R	R	R	R	R	R	R	R
128	64	32	16	8	4	2	1
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **IHB[7:0]**: 2’s complement integer value of the internal diode temperature reading

REGISTER 6-2: INTERNAL DIODE LOW BYTE REGISTER (ADDRESS 29h)

R	R	R	U-0	U-0	U-0	U-0	U-0
0.5	0.25	0.125	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-5 **ILB[7:5]**: Fractional portion of the Internal Diode Temperature to be added to the value at register 00h.

bit 4-0 **Unimplemented**: Read as ‘0’

REGISTER 6-3: EXTERNAL DIODE HIGH BYTE REGISTER (ADDRESS 01h)

R	R	R	R	R	R	R	R
128	64	32	16	8	4	2	1
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **EXT_HB[7:0]**: 2’s complement integer value of the External Diode n temperature reading, where n = 1 to 3, depending on the device.

REGISTER 6-4: EXTERNAL DIODE LOW BYTE REGISTER (ADDRESS 10h)

R	R	R	U-0	U-0	U-0	U-0	U-0
0.5	0.25	0.125	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **EXT_LB[7:5]**: Fractional portion of the Internal Diode Temperature to be added to the value at register 01h.

bit 4-0 **Unimplemented**: Read as '0'

6.3 Status Register

The Status Register reports general error conditions. To identify specific channels, refer to Register 6-18, Register 6-23, Register 6-24 and Register 6-25. The individual Status Register bits are cleared when the appropriate High Limit, Low Limit, or THERM Limit register has been read or cleared.

REGISTER 6-5: STATUS REGISTER (ADDRESS 02h)

R	U-0	U-0	R	R	R	R	R
BUSY	—	—	HIGH	LOW	FAULT	THERM	HWSD
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **BUSY**: This bit indicates that the ADC is currently converting. This bit does not cause the $\overline{\text{ALERT}}$ pin to be asserted.

bit 6-5 **Unimplemented**: Read as '0'

bit 4 **HIGH**: This bit is set when any of the temperature channels exceeds its programmed high limit. See the High Limit Status Register for specific channel information (Register 6-23). When set, this bit will assert the $\overline{\text{ALERT}}$ pin.

bit 3 **LOW**: This bit is set when any of the temperature channels drops below its programmed low limit. See the Low Limit Status Register for specific channel information (Register 6-24). When set, this bit will assert the $\overline{\text{ALERT}}$ pin.

bit 2 **FAULT**: This bit is asserted when a diode fault is detected on any of the external diode channels. See the External Diode Fault Register for specific channel information (Register 6-18). When set, this bit will assert the $\overline{\text{ALERT}}$ pin.

bit 1 **THERM**: This bit is set when the any of the temperature channels exceeds its programmed THERM limit. See the THERM Limit Status Register for specific channel information (Register 6-25).

bit 0 **HWSD**: This bit is set when the External Diode Temperature exceeds the Hardware Thermal Shutdown Limit set by the pull-up resistors on the $\overline{\text{ALERT}}$ and $\overline{\text{SYS\_SHDN}}$ pins. When set, this bit will assert the $\overline{\text{SYS\_SHDN}}$ pin.

6.4 Configuration Register

The Configuration Register controls the basic operation of the device. This register is fully accessible at either address.

REGISTER 6-6: CONFIGURATION REGISTER (ADDRESSES 03H AND 09h)

RW	U-0	RW	U-0	U-0	RW	RW	U-0
MSKAL	—	AT/COMP	—	—	RANGE	DA_DIS	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7	**MSKAL**: Masks the $\overline{\text{ALERT}}$ pin from asserting. 1 = The $\overline{\text{ALERT}}$ pin is masked. It will not be asserted for any interrupt condition unless it is configured to act in comparator mode. The Status Registers will be updated normally. 0 = The $\overline{\text{ALERT}}$ pin is not masked. If any of the appropriate status bits are set the $\overline{\text{ALERT}}$ pin will be asserted.
bit 6	**Unimplemented**: Read as ‘0’
bit 5	**AT/COMP**: Controls the operation of the $\overline{\text{ALERT}}$ pin. 1 = The $\overline{\text{ALERT}}$ pin acts in comparator mode as described in Section 5.5.2, ALERT Pin Comparator Mode. In this mode the MSKAL bit is ignored. 0 = The $\overline{\text{ALERT}}$ pin acts as described in Section 5.5, ALERT Output.
bit 4-3	**Unimplemented**: Read as ‘0’
bit 2	**RANGE**: Configures the measurement range and data format of the temperature channels 1 = The temperature measurement range is -64°C to +191.875°C and the data format is offset binary (see Table 5-3) 0 = The temperature measurement range is 0°C to +127.875°C and the data format is binary
bit 1	**DA_DIS**: Disables the dynamic averaging feature on all temperature channels 1 = The dynamic averaging feature is disabled. All temperature channels will be converted with a maximum averaging factor of 1x (equivalent to 11-bit conversion). For higher conversion rates, this averaging factor will be reduced as shown in Table 5-1. 0 = The dynamic averaging feature is enabled. All temperature channels will be converted with an averaging factor that is based on the conversion rate as shown in Table 5-1.
bit 0	**Unimplemented**: Read as ‘0’

6.5 Conversion Rate Register

The Conversion Rate Register controls how often the temperature measurement channels are updated and compared against the limits. This register is fully accessible at either address.

REGISTER 6-7: CONVERSION RATE REGISTER (ADDRESS 04h, 0Ah)

U-0	U-0	U-0	U-0	RW	RW	RW	RW
—	—	—	—	CONV[3:0]			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **Unimplemented**: Read as '0'

bit 3-0 **CONV[3:0]**: Determines the conversion rate as shown below:

CONV[3:0]					**Conversions/Second**
HEX	**3**	**2**	**1**	**0**	
0h	0	0	0	0	1
1h	0	0	0	1	1
2h	0	0	1	0	1
3h	0	0	1	1	1
4h	0	1	0	0	1
5h	0	1	0	1	2
6h	0	1	1	0	4 (default)
7h	0	1	1	1	8
8h	1	0	0	0	16
9h	1	0	0	1	32
Ah	1	0	1	0	64
Bh - Fh	All others				1

6.6 Limit Registers

The device contains both high and low limits for all temperature channels. If the measured temperature exceeds the high limit, then the corresponding status bit is set and the $\overline{\text{ALERT}}$ pin is asserted. Likewise, if the measured temperature is less than or equal to the low limit, the corresponding status bit is set and the $\overline{\text{ALERT}}$ pin is asserted.

The data format for the limits must match the selected data format for the temperature so that if the extended temperature range is used, the limits must be programmed in the extended data format.

The limit registers with multiple addresses are fully accessible at either address.

REGISTER 6-8: INTERNAL DIODE HIGH LIMIT TEMPERATURE REGISTER (ADDRESSES 05h AND 0Bh)

RW	RW	RW	RW	RW	RW	RW	RW
128	64	32	16	8	4	2	1
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **IDHL[7:0]**: 2’s complement integer value of the Internal Diode temperature reading.

REGISTER 6-9: INTERNAL DIODE LOW LIMIT TEMPERATURE REGISTER (ADDRESSES 06h AND 0Ch)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
128	64	32	16	8	4	2	1
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **IDHL[7:0]**: Fractional portion of the Internal Diode Low Limit Temperature to be added to the value at the respective high byte registers.

REGISTER 6-10: EXTERNAL DIODE HIGH TEMPERATURE LIMIT, HIGH BYTE REGISTER (ADDRESSES 07h AND 0Dh)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
128	64	32	16	8	4	2	1
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **EXT_HLH[7:0]**: Integer value of the External Diode temperature reading

REGISTER 6-11: EXTERNAL DIODE HIGH LIMIT TEMPERATURE, LOW BYTE REGISTER (ADDRESS 13h)

R/W	R/W	R/W	U-0	U-0	U-0	U-0	U-0
0.5	0.25	0.125	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-5 **EXT_HLL[2:0]**: Fractional portion of the High Limit Temperature to be added to the value at the respective high byte registers

bit 4-0 **Unimplemented**: Read as ‘0’

REGISTER 6-12: EXTERNAL DIODE LOW LIMIT, HIGH BYTE TEMPERATURE REGISTER (ADDRESSES 08h AND 0Eh)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
128	64	32	16	8	4	2	1
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **EXT_LLHB[7:0]**: Integer portion of External Diode Low temperature Limit

REGISTER 6-13: EXTERNAL DIODE LOW LIMIT, LOW BYTE TEMPERATURE REGISTER (ADDRESS 14h)

R/W	R/W	R/W	U-0	U-0	U-0	U-0	U-0
0.5	0.25	0.125	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-5 **EXT_LLLB[2:0]**: Fractional portion of the Low Limit Temperature to be added to the value at the respective high byte registers

bit 4-0 **Unimplemented**: Read as ‘0’

6.7 Scratchpad Registers

The Scratchpad Registers are Read Write registers that are used for place holders to be software compatible with legacy programs. Reading from the registers will return what is written to them.

REGISTER 6-14: SCRATCHPAD REGISTER (ADDRESSES 11h AND 12h)

RW	RW	RW	RW	RW	RW	RW	RW
SPD(N)[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **SPD(N)[7:0]**: User temporary storage registers, where N = 1 to 2

6.8 Therm Limit Registers

REGISTER 6-15: EXTERNAL DIODE $\overline{\text{THERM}}$ LIMIT REGISTER (ADDRESS 19h)

RW	RW	RW	RW	RW	RW	RW	RW
128	64	32	16	8	4	2	1
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **EXT_THL[7:0]**: External Diode THERM Limits

REGISTER 6-16: INTERNAL DIODE $\overline{\text{THERM}}$ LIMIT REGISTER (ADDRESS 20h)

RW	RW	RW	RW	RW	RW	RW	RW
128	64	32	16	8	4	2	1
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **IDTHL[7:0]**: Internal Diode THERM Limits

REGISTER 6-17: THERM LIMIT HYSTERESIS REGISTER (ADDRESS 21h)

RW	RW	RW	RW	RW	RW	RW	RW
128	64	32	16	8	4	2	1
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **THRMH[7:0]**: THERM Limit hysteresis.

6.9 External Diode Fault Register

The External Diode Fault Register indicates which of the external diodes caused the FAULT bit in the Status Register to be set. This register is cleared when it is read.

REGISTER 6-18: EXTERNAL DIODE FAULT STATUS REGISTER (ADDRESS 1Bh)

U-0	U-0	U-0	U-0	U-0	U-0	RC	U-0
—	—	—	—	—	—	FLT	—
bit 7							bit 0

Legend:			
RC = Read-then-clear bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-3 **Unimplemented**: Read as ‘0’

bit 1 **FLT**: This bit is set if the External Diode channel reported a diode fault.

bit 0 **Unimplemented**: Read as ‘0’

6.10 Software Thermal Shutdown Configuration Register

The Software Thermal Shutdown Configuration Register controls whether any of the software channels will assert the SYS_SHDN pin. If a channel is enabled, the temperature is compared against the corresponding THERM Limit. If the measured temperature exceeds the THERM Limit, then the SYS_SHDN pin is asserted. This functionality is in addition to the Hardware Shutdown circuitry.

REGISTER 6-19: SOFTWARE THERMAL SHUTDOWN CONFIGURATION REGISTER (ADDRESS 1Dh)

U-0	U-0	U-0	U-0	U-0	U-0	R/W	R/W
—	—	—	—	—	—	EXTSYS	INTSYS
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-2 **Unimplemented**: Read as ‘0’

bit 1 **EXTSYS**: This bit configures the External Diode channel to assert the SYS_SHDN pin based on its THERM Limit.
1 = The External Diode channel is linked to the SYS_SHDN pin. If the temperature exceeds its THERM Limit, the ETHERM status bit is set and the SYS_SHDN pin is asserted. It will remain asserted until the temperature drops below its THERM Limit minus the THERM Hysteresis.
0 = The External Diode channel is not linked to the SYS_SHDN pin. If the temperature exceeds its THERM Limit, the ETHERM status bit is set but the SYS_SHDN pin is not asserted.

bit 0 **INTSYS**: This bit configures the Internal Diode channel to assert the SYS_SHDN pin based on its THERM Limit.
1 = The Internal Diode channel is linked to the SYS_SHDN pin. If the temperature exceeds its THERM Limit, the ITHERM status bit is set and the SYS_SHDN pin is asserted. It will remain asserted until the temperature drops below its THERM Limit minus the THERM Hysteresis.
0 = The Internal Diode channel is not linked to the SYS_SHDN pin. If the temperature exceeds its THERM Limit, the ITHERM status bit is set but the SYS_SHDN pin is not asserted.

6.11 Hardware Thermal Shutdown Limit Register

This read only register returns the Hardware Thermal Shutdown Limit selected by the value of the pull-up resistors on the ALERT and SYS_SHDN pins. The data represents the hardware set temperature in °C using the active temperature setting set by the RANGE bit in the Configuration Register. See Register 6-7 for the data format.

When the External Diode Temperature exceeds this limit, the SYS_SHDN pin is asserted and will remain asserted until the External Diode Temperature drops below this limit minus 10°C.

REGISTER 6-20: HARDWARE THERMAL SHUTDOWN LIMIT REGISTER (ADDRESS 1Eh)

R	R	R	R	R	R	R	R
128	64	32	16	8	4	2	1
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **X[7:0]**: Hardware Thermal Shutdown Limit

6.12 Channel Mask Register

The Channel Mask Register controls individual channel masking. When a channel is masked, the ALERT pin will not be asserted when the masked channel reads a diode fault or out of limit error. The channel mask does not mask the SYS_SHDN pin.

REGISTER 6-21: CHANNEL MASK REGISTER (ADDRESS 1Fh)

U-0	U-0	U-0	U-0	U-0	U-0	RW	RW
—	—	—	—	—	—	EMASK	INTMASK
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-2 **Unimplemented**: Read as ‘0’

bit 1 **EMASK**: Masks the ALERT pin from asserting when the External Diode channel is out of limit or reports a diode fault.
1 = The External Diode channel will not cause the ALERT pin to be asserted if it is out of limit or reports a diode fault.
0 = The External Diode channel will cause the ALERT pin to be asserted if it is out of limit or reports a diode fault.

bit 0 **INTMASK**: Masks the ALERT pin from asserting when the Internal Diode temperature is out of limit.
1 = The Internal Diode channel will not cause the ALERT pin to be asserted if it is out of limit.
0 = The Internal Diode channel will cause the ALERT pin to be asserted if it is out of limit.

6.13 Consecutive ALERT Register

The Consecutive ALERT Register determines how many times an out-of-limit error or diode fault must be detected in consecutive measurements before the ALERT or SYS_SHDN pin is asserted. Additionally, the Consecutive ALERT Register controls the SMBus Timeout functionality.

An out-of-limit condition (i.e. HIGH, LOW, or FAULT) occurring on the same temperature channel in consecutive measurements will increment the consecutive alert counter. The counters will also be reset if no out-of-limit condition or diode fault condition occurs in a consecutive reading.

When the ALERT pin is configured as an interrupt, when the consecutive alert counter reaches its programmed value, the following will occur: the STATUS bit(s) for that channel and the last error condition(s) (i.e. EHIGH) will be set to '1', the ALERT pin will be asserted, the consecutive alert counter will be cleared, and measurements will continue.

When the ALERT pin is configured as a comparator, the consecutive alert counter will ignore diode fault and low limit errors and only increment if the measured temperature exceeds the High Limit. Additionally, once the consecutive alert counter reaches the programmed limit, the ALERT pin will be asserted, but the counter will not be reset. It will remain set until the temperature drops below the High Limit minus the THERM Hysteresis value.

For example, if the CALRT[2:0] bits are set for four consecutive alerts, the high limits are set at +70°C, and none of the channels are masked, then the ALERT pin will be asserted after the following four measurements:

1. Internal Diode reads +71°C and the external diode reads +69°C. Consecutive alert counter for INT is incremented to 1.
2. Both the Internal Diode and the External Diode read +71°C. Consecutive alert counter for INT is incremented to 2and for EXT is set to 1.
3. The External Diode reads +71°C and the Internal Diode reads 69°C. Consecutive alert counter for INT is cleared and EXT is incremented to 2.
4. The Internal Diode reads +71°C and the external diode reads +71°C. Consecutive alert counter for INT is set to 1 and EXT is incremented to 3.
5. The Internal Diode reads +71°C and the external diode reads +71°C. Consecutive alert counter for INT is incremented to 2 and EXT is incremented to 4. The appropriate status bits are set for EXT and the ALERT pin is asserted. EXT counter is reset to 0 and all other counters hold the last value until the next temperature measurement.

REGISTER 6-22: CONSECUTIVE ALERT REGISTER (ADDRESS 22h)

RW	RW	RW	RW	RW	RW	RW	U-0
TIMEOUT	CTHRM[2:0]			CALRT[2:0]			—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **TIMEOUT**: Determines whether the SMBus Timeout function is enabled.
1 = The SMBus Timeout feature is enabled. If the SMCLK line is held low for more than 30 ms, then the device will reset the SMBus protocol.
0 = The SMBus Timeout feature is disabled. The SMCLK line can be held low indefinitely without the device resetting its SMBus protocol.

REGISTER 6-22: CONSECUTIVE ALERT REGISTER (ADDRESS 22h) (CONTINUED)

bit 6-4	**CTHM<2:0>**: Determines the number of consecutive measurements that must exceed the corresponding THERM Limit and Hardware Thermal Shutdown Limit before the SYS_SHDN pin is asserted. All temperature channels use this value to set the respective counters. The consecutive THERM counter is incremented whenever any of the measurements exceed the corresponding THERM Limit or if the External Diode measurement exceeds the Hardware Thermal Shutdown Limit. If the temperature drops below the THERM limit or Hardware Thermal Shutdown Limit, then the counter is reset. If the programmed number of consecutive measurements exceed the THERM Limit or Hardware Thermal Shutdown Limit, and the appropriate channel is linked to the SYS_SHDN pin, then the SYS_SHDN pin will be asserted low. Once the SYS_SHDN pin is asserted, the consecutive THERM counter will not reset until the corresponding temperature drops below the appropriate limit minus the corresponding hysteresis. The default setting is 4 consecutive out of limit conversions. 000 = 1 001 = 2 011 = 3 111 = 4
bit 3-1	**CALRT<2:0>**: Determine the number of consecutive measurements that must have an out of limit condition or diode fault before the ALERT pin is asserted. All temperature channels use this value to set the respective counters. The default setting is 1 consecutive out of limit conversion. 000 = 1 001 = 2 011 = 3 111 = 4
bit 0	**Unimplemented**: Read as ‘0’

6.14 High Limit Status Register

The High Limit Status Register contains the status bits that are set when a temperature channel high limit is exceeded. If any of these bits are set, then the HIGH status bit in the Status Register is set. Reading from the High Limit Status Register will clear all bits if. Reading from the register will also clear the HIGH status bit in the Status Register.

The ALERT pin will be set if the programmed number of consecutive alert counts have been met and any of these status bits are set.

The status bits will remain set until read unless the ALERT pin is configured as a comparator output (see Section 5.5.2, ALERT Pin Comparator Mode).

REGISTER 6-23: HIGH LIMIT STATUS REGISTER (ADDRESS 35h)

U-0	U-0	U-0	U-0	U-0	U-0	RC	RC
—	—	—	—	—	—	EHIGH	IHIGH
bit 7							bit 0

Legend:			
RC = Read-then-clear bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-2	**Unimplemented**: Read as ‘0’
bit 1	**EHIGH**: This bit is set when the External Diode channel exceeds its programmed high limit.
bit 0	**IHIGH**: This bit is set when the Internal Diode channel exceeds its programmed high limit.

6.15 Low Limit Status Register

The Low Limit Status Register contains the status bits that are set when a temperature channel drops below the low limit. If any of these bits are set, then the LOW status bit in the Status Register is set. Reading from the Low Limit Status Register will clear all bits. Reading from the register will also clear the LOW status bit in the Status Register.

The ALERT pin will be set if the programmed number of consecutive alert counts have been met and any of these status bits are set.

The status bits will remain set until read unless the ALERT pin is configured as a comparator output (see Section 5.5.2, ALERT Pin Comparator Mode).

REGISTER 6-24: LOW LIMIT STATUS REGISTER (ADDRESS 36h)

U-0	U-0	U-0	U-0	U-0	U-0	RC	RC
—	—	—	—	—	—	ELOW	ILOW
bit 7							bit 0

Legend:			
RC = Read-then-clear bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-2	**Unimplemented**: Read as ‘0’
bit 1	**ELOW**: This bit is set when the External Diode channel drops below its programmed low limit.
bit 0	**ILOW**: This bit is set when the Internal Diode channel drops below its programmed low limit.

6.16 THERM Limit Status Register

The THERM Limit Status Register contains the status bits that are set when a temperature channel THERM Limit is exceeded. If any of these bits are set, then the THERM status bit in the Status Register is set. Reading from the THERM Limit Status Register will not clear the status bits. Once the temperature drops below the THERM Limit minus the THERM Hysteresis, the corresponding status bits will be automatically cleared. The THERM bit in the Status Register will be cleared when all individual channel THERM bits are cleared.

REGISTER 6-25: THERM LIMIT STATUS REGISTER (ADDRESS 37h)

U-0	U-0	U-0	U-0	U-0	U-0	R	R
—	—	—	—	—	—	ETHERM	ITHERM
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-2	**Unimplemented**: Read as ‘0’
bit 1	**ETHERM**: This bit is set when the External Diode channel exceeds its programmed THERM limit.
bit 0	**ITHERM**: This bit is set when the Internal Diode channel exceeds its programmed THERM limit.

6.17 Filter Control Register

The Filter Configuration Register controls the digital filter on the External Diode channel.

REGISTER 6-26: FILTER CONFIGURATION REGISTER (ADDRESS 40h)

U-0	U-0	U-0	U-0	U-0	U-0	R/W	R/W
—	—	—	—	—	—	FLTER[1:0]	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-2 **Unimplemented**: Read as ‘0’

bit 1-0 **FILTER**: Control the level of digital filtering that is applied to the External Diode temperature measurements as shown below. See Figure 5-4 and Figure 5-5 for examples on the filter behavior.

FILTER[1:0]		Averaging
1	**0**	
0	0	Disabled (default)
0	1	Level 1
1	0	Level 1
1	1	Level 2

6.18 Product ID Register

The Product ID Register holds a unique value that identifies the device (22h).

REGISTER 6-27: PRODUCT ID REGISTER (ADDRESS FDh)

R	R	R	R	R	R	R	R
0	0	1	0	0	0	1	0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 Product ID hardwired to `0010 0010`.

6.19 Microchip ID Register

The Manufacturer ID register contains an 8-bit word that identifies Microchip as the manufacturer of the EMC1422 (5Dh).

REGISTER 6-28: MANUFACTURER ID REGISTER (ADDRESS FEh)

R	R	R	R	R	R	R	R
0	1	0	1	1	1	0	1
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 8-bit manufacturer ID hardwired to be `0101 1101` (5Dh).

6.20 Revision Register

The Revision register contains an 8-bit word that identifies the die revision. It can be 01h or 04h.

REGISTER 6-29: REVISION REGISTER

(Address FFh, Default 01h)

R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	1
bit 7							bit 0

bit 7-0 Hardwired to be `0000 0001` (01h) depending on the revision of the die.

(Address FFh, Default 04h)

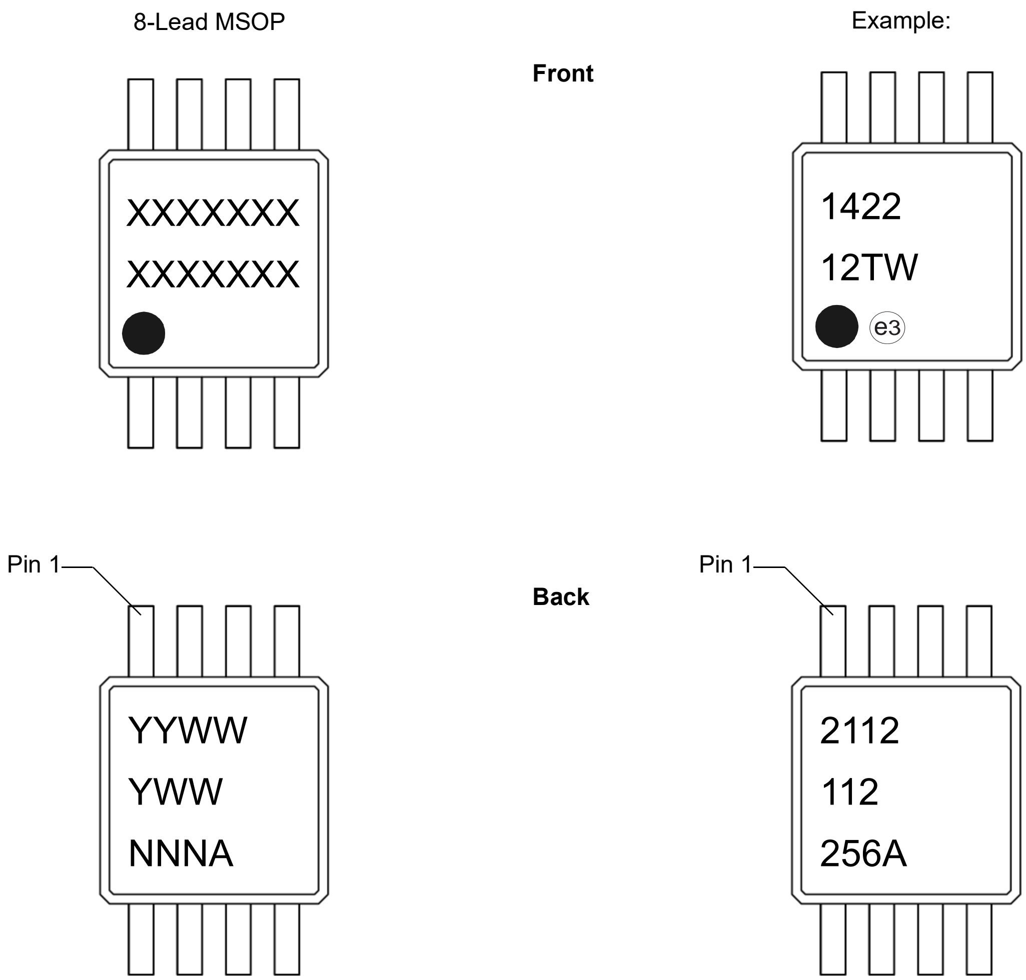
R	R	R	R	R	R	R	R
0	0	0	0	0	1	0	0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 Hardwired to be `0000 0100` (04h) depending on the revision of the die.

7.0 PACKAGING INFORMATION

7.1 Package Marking Information

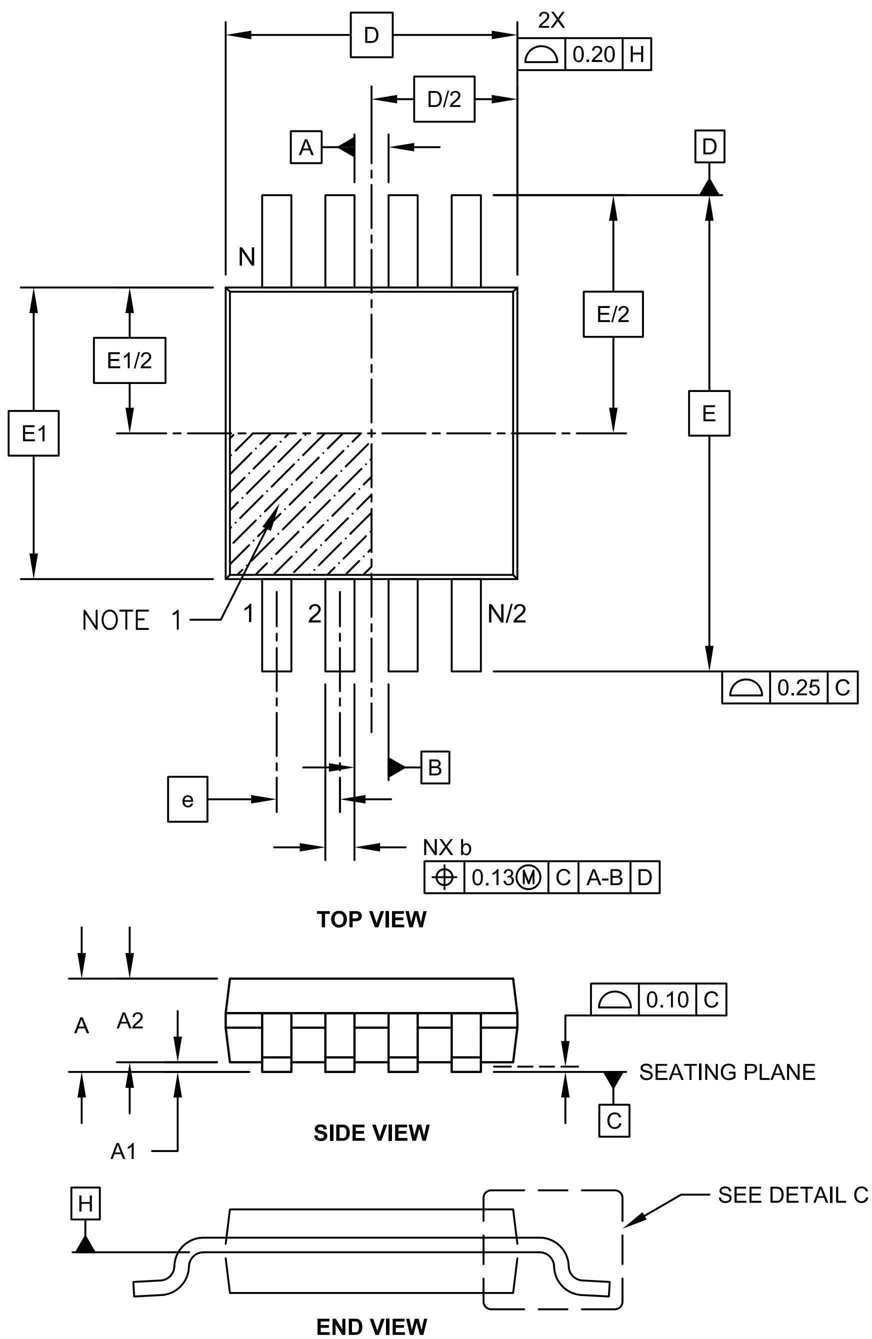


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Micro Small Outline Package (UA) [MSOP]

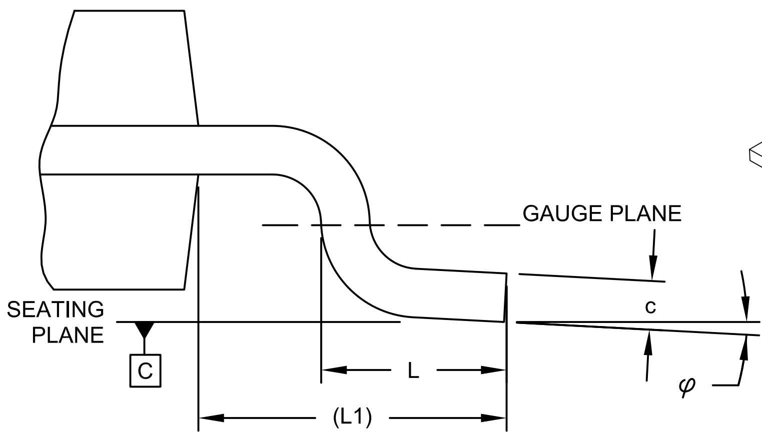
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



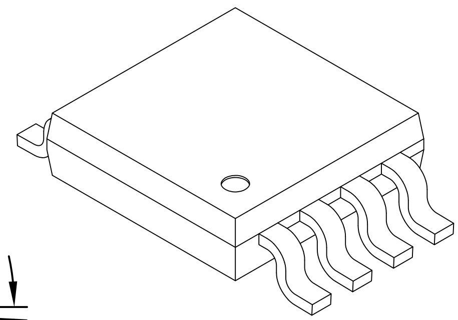
Microchip Technology Drawing C04-111C Sheet 1 of 2

8-Lead Plastic Micro Small Outline Package (UA) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL C



		Units	MILLIMETERS	
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	-	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.08	-	0.23
Lead Width	b	0.22	-	0.40

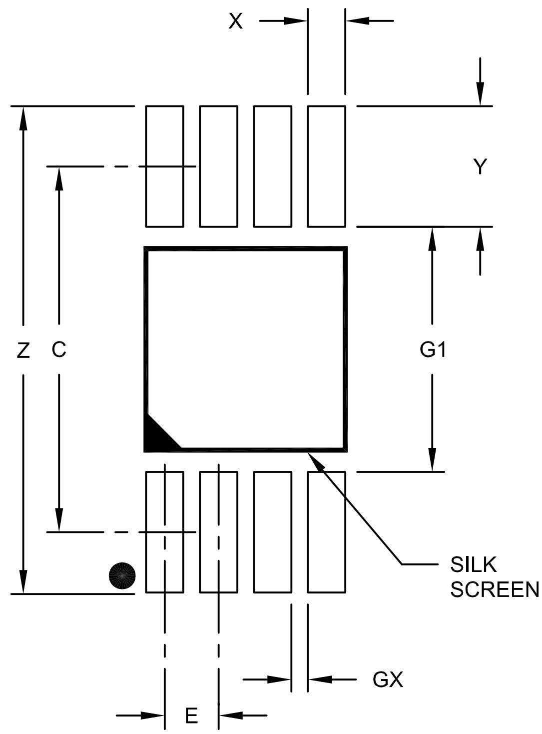
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111C Sheet 2 of 2

8-Lead Plastic Micro Small Outline Package (UA) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.85
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G1	2.95		
Distance Between Pads	GX	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2111A

APPENDIX A: REVISION HISTORY

Revision A (April 2021)

- Original release of this document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	–X	X	/XX
Device	Tape and Reel	SMBUS Address	Temperature Range	Package

Device:	EMC1422: High-Accuracy, Low-Cost, SMBus Temperature Sensor
Tape and Reel:	T = Tape and Reel
SMBus Address:	1 = `1001_100xb`
Temperature Range:	E = -40°C to +125°C (Extended)
Package:	UA = 8-Lead Plastic Micro Small Outline Package (MSOP)

Examples:

a) EMC1422-1-ACZL: Tape and reel, Extended temperature, 8L-MSOP package

NOTES:

ISBN: 978-1-5224-8124-9

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