# 34AA02/34LC02

## 2-Kbit I²C Serial EEPROM Software Write-Protect

### Device Selection Table

| Part Number | VCC Range | Max. Clock Frequency | Temp. Ranges | Packages |
|---|---|---|---|---|
| 34AA02 | 1.7V-5.5V | 400 kHz(1) | I, E | MS, P. SN, OT, MNY, ST |
| 34LC02 | 2.2V-5.5V | 1 MHz | I, E | MS, P. SN, OT, MNY, ST |

**Note 1:** 100 kHz for VCC <1.8V.

### Features

- Permanent and Resettable Software Write-Protect for Lower Half of the Array (00h-7Fh)
- Single Supply with Operation Down to 1.7V
- Low-Power CMOS Technology:
  - Read current: 1 mA, typical
  - Standby current: 100 nA, typical
- Two-Wire Serial Interface Bus, I²C Compatible
- Cascadable Up to Eight Devices
- Schmitt Trigger Inputs for Noise Suppression
- Output Slope Control to Eliminate Ground Bounce
- 100 kHz and 400 kHz Compatibility
- 1 MHz Clock for LC Versions
- Page Write Time: 5 ms, Maximum
- Self-Timed Erase/Write Cycle
- 16-Byte Page Write Buffer
- ESD Protection > 4,000V
- Software Write Protection for Lower 128 Bytes
- Hardware Write Protection for Entire Array
- More than 1 Million Erase/Write Cycles
- Data Retention > 200 Years
- RoHS Compliant
- Available for Extended Temperature Ranges:
  - Industrial (I): -40°C to +85°C
  - Extended (E): -40°C to +125°C
- Automotive AEC-Q100 Qualified

### Packages

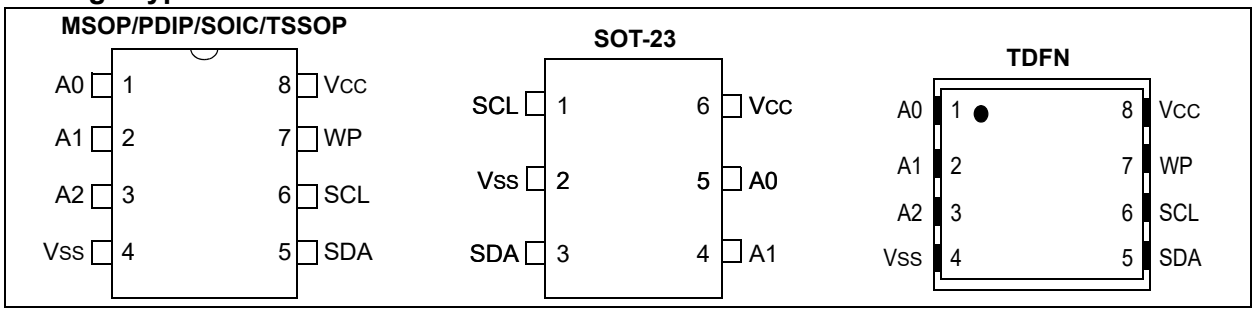
- 8-Lead MSOP, 8-Lead PDIP, 8-Lead SOIC, 6-Lead SOT-23, 8-Lead TDFN and 8-Lead TSSOP

### Description

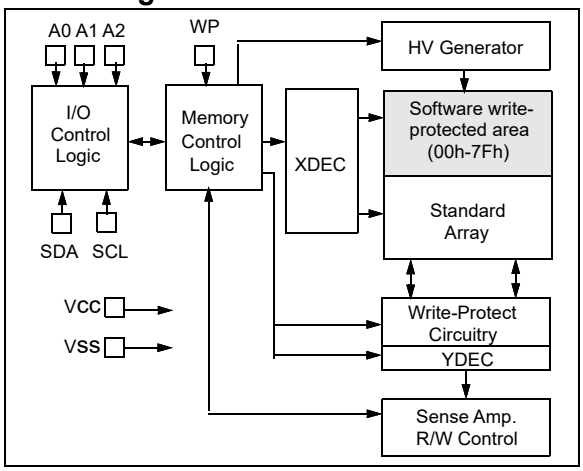
The Microchip Technology Inc. 34XX02(1) is a 2-Kbit Electrically Erasable PROM (EEPROM). This device has two software write-protect features for the lower half of the array, as well as an external pin that can be used to write-protect the entire array. This allows the system designer to protect none, half or all of the array, depending on the application. The device is organized as one block of 256 x 8-bit memory with a two-wire serial interface. Its low-voltage design permits operation down to 1.7V, with standby and active currents of only 100 nA and 1 mA, respectively. The 34XX02 also has a page write capability for up to 16 bytes of data.

**Note 1:** 34XX02 is used in this document as a generic part number for the 34AA02/34LC02 devices.

### Package Types



## Block Diagram



# 1.0 ELECTRICAL CHARACTERISTICS

## Absolute Maximum Ratings(†)

VCC.....6.5V

All inputs and outputs w.r.t. VSS .....-0.3V to VCC +1.0V

Storage temperature .....-65°C to +150°C

Ambient temperature with power applied.....-40°C to +125°C

ESD protection on all pins .....≥ 4 kV

**† NOTICE:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

**TABLE 1-1: DC SPECIFICATIONS**

| **DC CHARACTERISTICS** | | | **Electrical Characteristics:**<br>**Industrial (I): TA = -40°C to +85°C**<br>**Extended (E): TA = -40°C to +125°C** | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristic** | **Min.** | **Typical** | **Max.** | **Units** | **Conditions** |
| D1 | VIH | High-Level Input Voltage | 0.7 VCC | — | — | V | |
| D2 | VIL | Low-Level Input Voltage | — | — | 0.3 VCC | V | 0.2 VCC for VCC < 2.5V |
| D3 | VHYS | Hysteresis of Schmitt Trigger Inputs | 0.05 Vcc | — | — | V | **Note 1** |
| D4 | VOL | Low-Level Output Voltage | — | — | 0.40 | V | IOL = 3.0 mA, VCC = 2.5V |
| D5 | VHV | High-Voltage Detect | 7 | — | 10 | V | A0 Pin only, VCC < 2.2V |
| | | | VCC + 4.8 | — | 10 | V | A0 Pin only, VCC ≥ 2.2V |
| | | | 10 | — | VCC + 4.8 | V | A0 Pin only, VCC > 5.2V |
| D6 | ILI | Input Leakage Current | — | — | ±1 | µA | VIN = VSS or VCC |
| D7 | ILO | Output Leakage Current | — | — | ±1 | µA | VOUT = VSS or VCC |
| D8 | CIN, COUT | Pin Capacitance (all inputs/outputs) | — | — | 10 | pF | VCC = 5.5V (**Note 1**)<br>TA = +25°C, FCLK = 1 MHz |
| D9 | ICCWRITE | Operating Current | — | 0.1 | 3 | mA | VCC = 5.5V, SCL = 1 MHz |
| D10 | ICCREAD | | — | 0.05 | 1 | mA | VCC = 5.5V, SCL = 1 MHz |
| D11 | ICCS | Standby Current | — | 0.01 | 1 | µA | SDA = SCL = VCC,<br>A0, A1, A2, WP = VSS,<br>I-Temp. |
| | | | — | — | 5 | µA | SDA = SCL = VCC,<br>A0, A1, A2, WP = VSS,<br>E-Temp. |

**Note 1:** This parameter is periodically sampled and is not 100% tested.

**TABLE 1-2: AC SPECIFICATIONS**

| AC CHARACTERISTICS | | | Electrical Characteristics:<br>Industrial (I): TA = -40°C to +85°C<br>Extended (E): TA = -40°C to +125°C | | | |
|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristic** | **Min.** | **Max.** | **Units** | **Conditions** |
| 1 | FCLK | Clock Frequency | — | 100 | kHz | 1.7V ≤ VCC < 1.8V |
| | | | — | 400 | kHz | 1.8V ≤ VCC ≤ 5.5V |
| | | | — | 1000 | kHz | 2.5V ≤ VCC ≤ 5.5V (**34LC02**) |
| 2 | THIGH | Clock High Time | 4000 | — | ns | 1.7V ≤ VCC < 1.8V |
| | | | 600 | — | ns | 1.8V ≤ VCC ≤ 5.5V |
| | | | 500 | — | ns | 2.5V ≤ VCC ≤ 5.5V (**34LC02**) |
| 3 | TLOW | Clock Low Time | 4700 | — | ns | 1.7V ≤ VCC < 1.8V |
| | | | 1300 | — | ns | 1.8V ≤ VCC ≤ 5.5V |
| | | | 500 | — | ns | 2.5V ≤ VCC ≤ 5.5V (**34LC02**) |
| 4 | TR | SDA and SCL Rise Time | — | 1000 | ns | 1.7V ≤ VCC < 1.8V (**Note 1**) |
| | | | — | 300 | ns | 1.8V ≤ VCC ≤ 5.5V (**Note 1**) |
| | | | — | 300 | ns | 2.5V ≤ VCC ≤ 5.5V (**34LC02**) (**Note 1**) |
| 5 | TF | SDA and SCL Fall Time | — | 1000 | ns | 1.7V ≤ VCC < 1.8V (**Note 1**) |
| | | | — | 300 | ns | 1.8V ≤ VCC ≤ 5.5V (**Note 1**) |
| | | | — | 300 | ns | 2.5V ≤ VCC ≤ 5.5V (**34LC02**) (**Note 1**) |
| 6 | Thd:sta | Start Condition Hold Time | 4000 | — | ns | 1.7V ≤ VCC < 1.8V |
| | | | 600 | — | ns | 1.8V ≤ VCC ≤ 5.5V |
| | | | 250 | — | ns | 2.5V ≤ VCC ≤ 5.5V (**34LC02**) |
| 7 | TSU:STA | Start Condition Setup Time | 4700 | — | ns | 1.7V ≤ VCC < 1.8V |
| | | | 600 | — | ns | 1.8V ≤ VCC ≤ 5.5V |
| | | | 250 | — | ns | 2.5V ≤ VCC ≤ 5.5V (**34LC02**) |
| 8 | THD:DAT | Data Input Hold Time | 0 | — | ns | **Note 2** |
| 9 | TSU:DAT | Data Input Setup Time | 250 | — | ns | 1.7V ≤ VCC < 1.8V |
| | | | 100 | — | ns | 1.8V ≤ VCC ≤ 5.5V |
| | | | 100 | — | ns | 2.5V ≤ VCC ≤ 5.5V (**34LC02**) |
| 10 | TSU:STO | Stop Condition Setup Time | 4000 | — | ns | 1.7V ≤ VCC < 1.8V |
| | | | 600 | — | ns | 1.8V ≤ VCC ≤ 5.5V |
| | | | 250 | — | ns | 2.5V ≤ VCC ≤ 5.5V (**34LC02**) |
| 11 | TSU:WP | WP Setup Time | 4000 | — | ns | 1.7V ≤ VCC < 1.8V |
| | | | 600 | — | ns | 1.8V ≤ VCC ≤ 5.5V |
| | | | 600 | — | ns | 2.5V ≤ VCC ≤ 5.5V (**34LC02**) |
| 12 | THD:WP | WP Hold Time | 4700 | — | ns | 1.7V ≤ VCC < 1.8V |
| | | | 600 | — | ns | 1.8V ≤ VCC ≤ 5.5V |
| | | | 600 | — | ns | 2.5V ≤ VCC ≤ 5.5V (**34LC02**) |

**Note 1:** Not 100% tested. CB = total capacitance of one bus line in pF.

**2:** As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

**3:** The combined TSP and VHYS specifications are due to new Schmitt Trigger inputs, which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

**4:** This parameter is not tested but is ensured by characterization.

**TABLE 1-2: AC SPECIFICATIONS**

| AC CHARACTERISTICS | | | Electrical Characteristics: Industrial (I): $T_A$ = -40°C to +85°C Extended (E): $T_A$ = -40°C to +125°C | | | |
|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristic** | **Min.** | **Max.** | **Units** | **Conditions** |
| 13 | $T_{AA}$ | Output Valid from cloCk | — | 3500 | ns | 1.7V ≤ $V_{CC}$ < 1.8V (**Note 2**) |
| | | | — | 900 | ns | 1.8V ≤ $V_{CC}$ ≤ 5.5V (**Note 2**) |
| | | | — | 400 | ns | 2.5V ≤ $V_{CC}$ ≤ 5.5V (**34LC02**) (**Note 2**) |
| 14 | $T_{BUF}$ | Bus Free Time: The time the bus must be free before a new transmission can start | 4700 | — | ns | 1.7V ≤ $V_{CC}$ < 1.8V |
| | | | 1300 | — | ns | 1.8V ≤ $V_{CC}$ ≤ 5.5V |
| | | | 500 | — | ns | 2.5V ≤ $V_{CC}$ ≤ 5.5V (**34LC02**) |
| 15 | $T_{SP}$ | Input Filter Spike Suppression (SDA and SCL pins) | — | 50 | ns | **34AA02** (**Note 1** and **Note 3**) |
| 16 | $T_{WC}$ | Write Cycle Time (byte or page) | — | 5 | ms | |
| 17 | | Endurance | 1,000,000 | — | cycles | +25°C, 5.5V, Page Mode (**Note 4**) |

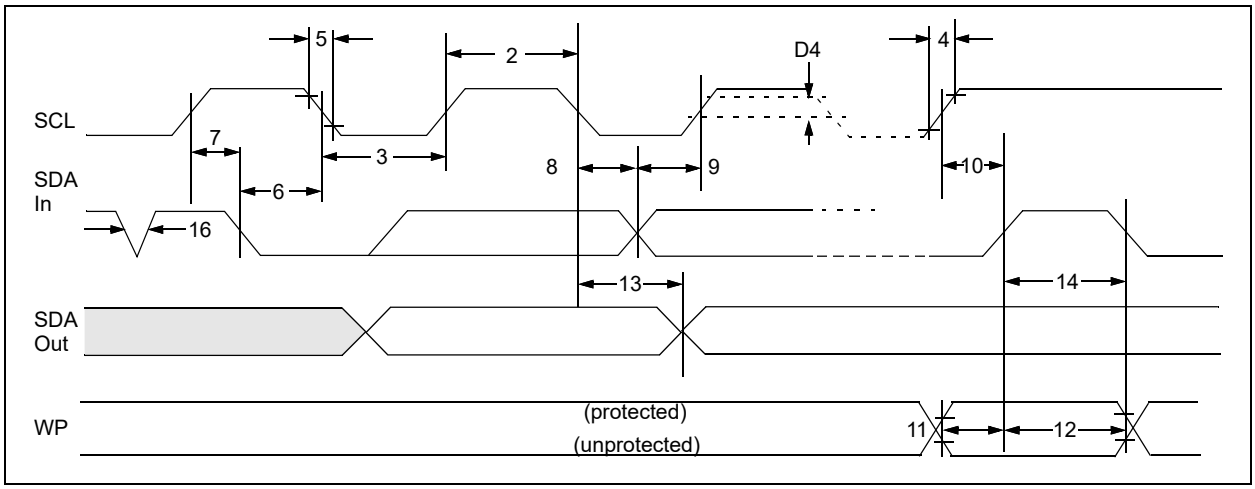
**Note 1:** Not 100% tested. $C_B$ = total capacitance of one bus line in pF.

**2:** As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

**3:** The combined $T_{SP}$ and $V_{HYS}$ specifications are due to new Schmitt Trigger inputs, which provide improved noise spike suppression. This eliminates the need for a $T_I$ specification for standard operation.

**4:** This parameter is not tested but is ensured by characterization.

**FIGURE 1-1: BUS TIMING DATA**



## 2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

**TABLE 2-1: PIN FUNCTION TABLE**

| Name | MSOP | PDIP | SOIC | SOT-23 | TDFN | TSSOP | Description |
|---|---|---|---|---|---|---|---|
| A0 | 1 | 1 | 1 | 5 | 1 | 1 | Chip Address Input |
| A1 | 2 | 2 | 2 | 4 | 2 | 2 | Chip Address Input |
| A2 | 3 | 3 | 3 | — | 3 | 3 | Chip Address Input |
| VSS | 4 | 4 | 4 | 2 | 4 | 4 | Ground |
| SDA | 5 | 5 | 5 | 3 | 5 | 5 | Serial Address/Data I/O |
| SCL | 6 | 6 | 6 | 1 | 6 | 6 | Serial Clock |
| WP | 7 | 7 | 7 | — | 7 | 7 | Write-Protect Input |
| VCC | 8 | 8 | 8 | 6 | 8 | 8 | Power Supply |

### 2.1 Chip Address Inputs (A0, A1, A2)

The levels on these inputs are compared with the corresponding bits in the client address. The chip is selected if the compare is true.

Up to eight 34XX02 devices (four for the SOT-23 package) may be connected to the same bus by using different Chip Select bit combinations. These inputs must be connected to either VSS or VCC. The A0 pin is also used to detect VHV.

### 2.2 Serial Address/Data Input/Output (SDA)

This is a bidirectional pin used to transfer addresses and data into and out of the device. It is an open-drain terminal. Therefore, the SDA bus requires a pull-up resistor to VCC (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz and 1 MHz).

For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the Start and Stop conditions.

### 2.3 Serial Clock (SCL)

This input is used to synchronize the data transfer to and from the device.

### 2.4 Write-Protect (WP)

This is the hardware write-protect pin. It can be tied to VCC or VSS. If tied to VCC, the hardware write protection is enabled. If the WP pin is tied to VSS, the hardware write protection is disabled.

## 3.0 FUNCTIONAL DESCRIPTION

The 34XX02 has two Software Write-Protect features that allow the user to protect half of the array from being written (Addresses 00h-7Fh). One command, Software Write-Protect (SWP), will prevent writes to half of the array and is resettable by using the Clear Software Write-Protect (CSWP) command. The other command is Permanent Software Write-Protect (PSWP), which is not resettable and will permanently lock half the array from being written to. The device still has an external pin (WP) that allows the user to protect the entire array if so desired.

The 34XX02 supports a bidirectional two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data, as a receiver. The bus must be controlled by a host device, which generates the Serial Clock (SCL), controls the bus access and generates the Start and Stop conditions, while the 34XX02 works as client. Both host and client can operate as transmitter or receiver, but the host device determines which mode is activated.

## 4.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition

Accordingly, the following bus conditions have been defined (Figure 4-1).

### 4.1 Bus Not Busy (A)

Both data and clock lines remain high.

### 4.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

### 4.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must be ended with a Stop condition.

### 4.4 Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal. The data on the line must be changed during the low period of clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of data bytes transferred between the Start and Stop conditions is determined by the host device and is, theoretically, unlimited; although only the last 16 bytes will be stored when doing a write operation. When an overwrite does occur, it will replace data in a First-In First-Out (FIFO) principle.

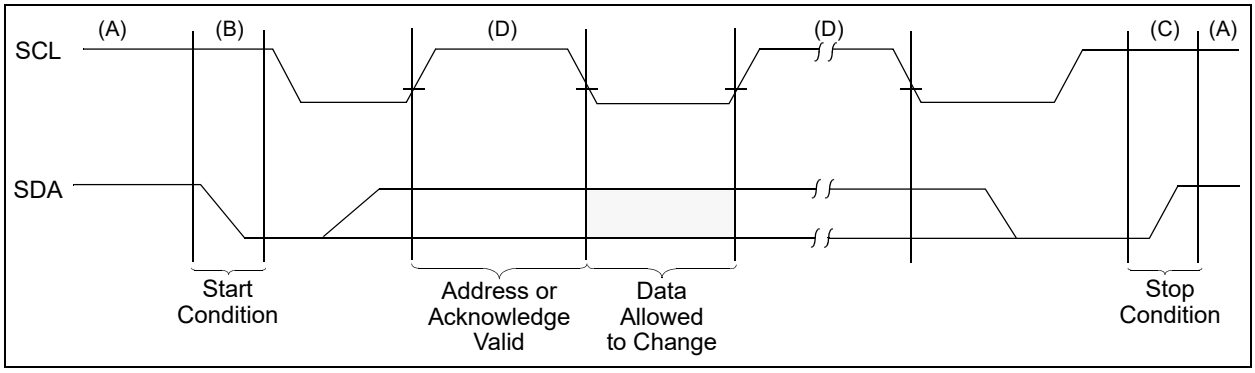
### 4.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an Acknowledge after the reception of each byte. Exceptions to this rule relating to software write protection are described in **Section 7.0 "Write Protection"**. The host device must generate an extra clock pulse which is associated with this Acknowledge bit.

| **Note:** | The 34XX02 does not generate any Acknowledge bits if an internal programming cycle is in progress. |
|---|---|

The device that acknowledges has to pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable-low during the high period of the Acknowledge-related clock pulse. Moreover, setup and hold times must be taken into account. During reads, a host must signal an end-of-data to the client by not generating an Acknowledge bit on the last byte that has been clocked out of the client. In this case, the client (34XX02) will leave the data line high to enable the host to generate the Stop condition.

**FIGURE 4-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS**



## 5.0 DEVICE ADDRESSING

A control byte is the first byte received following the Start condition from the host device. The first part of the control byte consists of a 4-bit control code which is set to '1010' for normal read and write operations and '0110' for writing to the write-protect register. The control byte is followed by three Chip Select bits (A2, A1, A0). The Chip Select bits allow the use of up to eight 34XX02 devices on the same bus and are used to determine which device is accessed. The Chip Select bits in the control byte must correspond to the logic levels on the corresponding A2, A1 and A0 pins for the device to respond. These bits are, in effect, the three Most Significant bits of the word address. The combination of the 4-bit control code and the next three bits are called the client address.

For the SOT-23 package, the A2 pin is not connected. During device addressing, the A2 Chip Select bit should be set to '0'. Only four 34XX02 SOT-23 packages can be connected to the same bus.

The last bit of the control byte is the Read/$\overline{\text{Write}}$ (R/$\overline{\text{W}}$) bit and it defines the operation to be performed. When set to a '1', a read operation is selected. When set to a '0', a write operation is selected. Following the Start condition, the 34XX02 monitors the SDA bus, checking the device type identifier being transmitted. Upon receiving a valid client address and the R/$\overline{\text{W}}$ bit, the client device outputs an Acknowledge signal on the SDA line. Depending on the state of the R/$\overline{\text{W}}$ bit, the 34XX02 will select a read or write operation.

The next byte received defines the address of the first data byte within the selected block (Figure 5-2). The word address byte uses all eight bits.

| Operation | Control Code | Chip Select | R/$\overline{\text{W}}$ |
|---|---|---|---|
| Read | 1010 | A2 A1 A0 | 1 |
| Write | 1010 | A2 A1 A0 | 0 |
| Write-Protect Register | 0110 | A2 A1 A0 | 0 |

**FIGURE 5-1: CONTROL BYTE FORMAT**

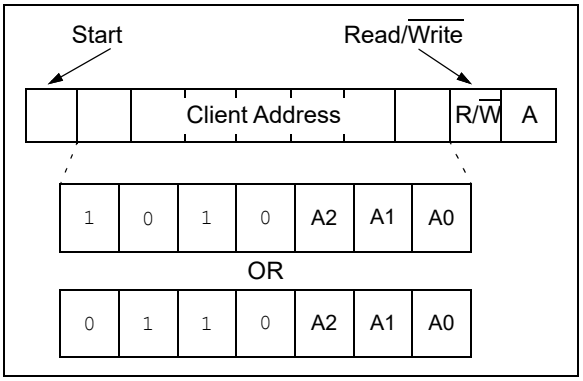
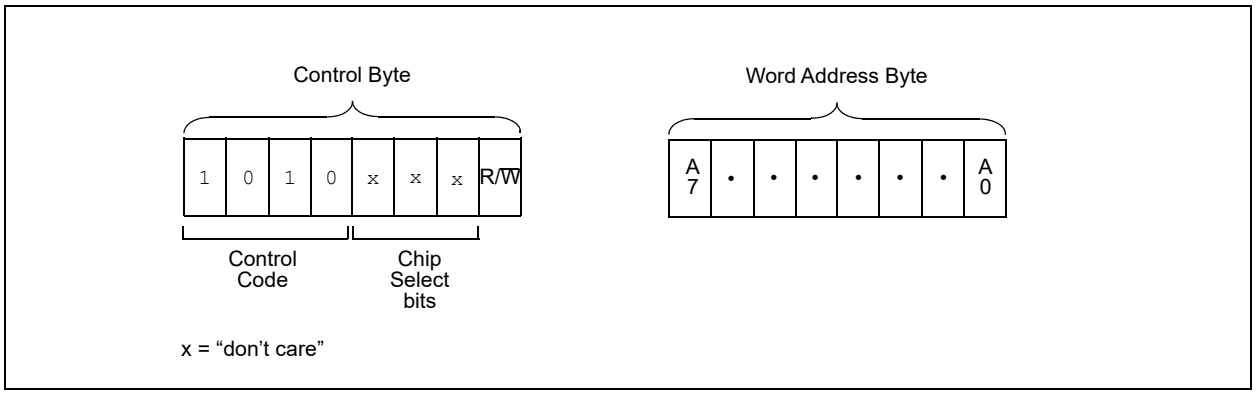



**FIGURE 5-2: ADDRESS SEQUENCE BIT ASSIGNMENTS**



## 6.0 WRITE OPERATIONS

### 6.1 Byte Write

Following the Start signal from the host, the device code(4 bits), the Chip Select bits (3 bits) and the R/$\overline{W}$ bit, which is a logic-low, are placed onto the bus by the host transmitter. This indicates to the addressed client receiver that a byte with a word address will follow, once it has generated an Acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the host is the word address and will be written into the Address Pointer of the 34XX02. After receiving another Acknowledge signal from the 34XX02, the host device will transmit the data word to be written into the addressed memory location. The 34XX02 acknowledges again and the host generates a Stop condition. This initiates the internal write cycle, which means that during this time, the 34XX02 will not generate Acknowledge signals (Figure 6-1).

If an attempt is made to write to the array when the software or hardware write protection has been enabled, the device will acknowledge the command, but no data will be written. The write cycle time must be observed even if the write protection is enabled.

### 6.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 34XX02 in the same way as in a byte write. Instead of generating a Stop condition, the host transmits up to 15 additional data bytes to the 34XX02, which are temporarily stored in the on-chip page buffer and will be written into the memory after the host has transmitted a Stop condition.

Upon receipt of each word, the four lower order Address Pointer bits, which form the byte counter, are internally incremented by one. The higher order four bits of the word address remain constant. If the host should transmit more than 16 bytes prior to generating the Stop condition, the Address Pointer will roll over and the previously received data will be overwritten. As with the byte write operation, once the Stop condition is received, an internal write cycle will begin (Figure 6-2).

If an attempt is made to write to the array when the hardware write protection has been enabled, the device will acknowledge the command, but no data will be written. The write cycle time must be observed even if the write protection is enabled.

**Note:** Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and end at addresses that are integer multiples of page size – 1. If a page write command attempts to write across a physical page boundary, the result is that the data wrap around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page, as might be expected. It is, therefore, necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

**FIGURE 6-1: BYTE WRITE**

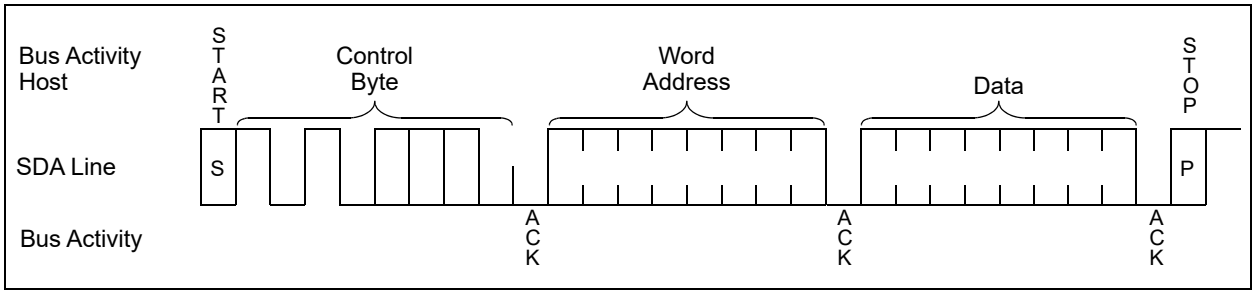
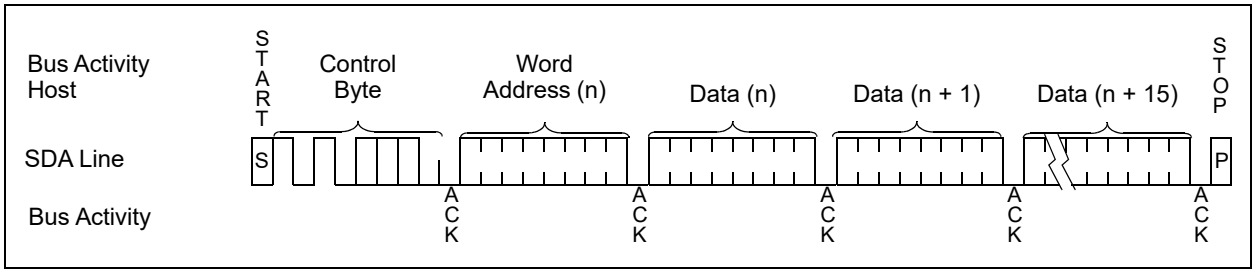



**FIGURE 6-2: PAGE WRITE**



## 7.0 WRITE PROTECTION

The 34XX02 has two software write-protect features (SWP and PSWP) that allow the lower half of the array (addresses 00h-7Fh) to be write-protected, as well as a WP pin that can be used to protect the entire array. The permanent software write-protect feature is enabled by sending the device a special command. Once this feature has been enabled, it cannot be reversed. The resettable software write-protect feature is also enabled by sending the device a special command but it can be reset by issuing another special command. In addition to the software protect features, there is a WP pin that can be used to write-protect the entire array, regardless of whether the software write-protect register has been written or not.

Table 7-2 and Table 7-3 describe how the 34XX02 will acknowledge specific commands under various circumstances.

### 7.1 Hardware Write Protection

The WP pin allows the user to write-protect the entire array (00-FF) when the pin is tied to VCC. If the pin is tied to VSS, the write protection is disabled.

### 7.2 Software Write Protection (SWP) and Clear Software Write Protection (CSWP)

In addition to hardware write-protect, the 34XX02 has a software write-protect feature that, when set, protects the first 128 bytes (00-7Fh) of the array from being written.

Setting the software write protection is done by sending the SWP instruction. SWP can also then be cleared by issuing a CSWP instruction (see Figure 7-1).

These two instructions follow the same format as the Byte Write instruction with the exception of the Device Type Identifier (typically '1010', instead changes to '0110'). Once this identifier is recognized by the device, the rest of the Byte Write command, address and data are "don't cares". In addition to the identifier, high voltage must be applied to the A0 pin of the device and specific levels must be present on A1 and A2. See Table 7-1 for the available commands.

### 7.3 Permanent Software Write-Protect (PSWP)

The Permanent Software Write Protect (PSWP) is another instruction that may be used to permanently protect the first 128 bytes of the array. Once this command is issued, the user will no longer have the ability to clear this feature regardless of instruction, power cycling or state of the WP pin. Also, once this instruction has been executed, the device will no longer acknowledge the device identifier '0110'.

**FIGURE 7-1: SOFTWARE WRITE PROTECTION FOR SWP, CSWP, PSWP OR CPSWP**

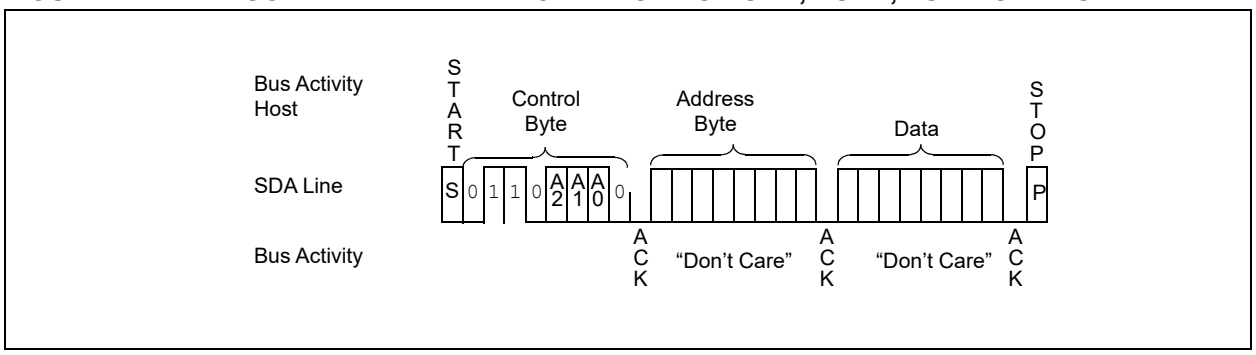


**TABLE 7-1: SOFTWARE WRITE PROTECTION INSTRUCTION SET WP = 0**

| Instruction | Address Pins | | | Device Type Identifier | | | | Chip Select Bits | | | R/$\overline{W}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | A2 | A1 | A0[1] | B7 | B6 | B5 | B4 | B3[2] | B2[2] | B1[2] | B0 |
| SWP | VSS | VSS | VHV | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| CSWP | VSS | VCC | VHV | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| PSWP | A2 | A1 | A0 | 0 | 1 | 1 | 0 | A2 | A1 | A0 | 0 |
| Read SWP | VSS | VSS | VHV | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| Read CSWP | VSS | VCC | VHV | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| Read PSWP | A2 | A1 | A0 | 0 | 1 | 1 | 0 | A2 | A1 | A0 | 1 |

**Note 1:** A0 is used to detect VHV for the SWP and CSWP commands.

**2:** B3, B2 and B1 are compared to the A2, A1 and A0 external pins, respectively.

**TABLE 7-2: ACKNOWLEDGE TABLE FOR WRITE OR WRITE PROTECTION WITH R/$\overline{W}$ = 0**

| Status | Write- Protect | Instruction | ACK | Address | ACK | Data Byte | ACK | Write Cycle |
|---|---|---|---|---|---|---|---|---|
| Permanently Protected | x | PSWP, SWP, CSWP | No ACK | Don't Care | No ACK | Don't Care | No ACK | No |
| | | Page or Byte Write in lower 128 bytes | ACK | Address | ACK | Data | No ACK | No |
| Protected with SWP | 0 | SWP | No ACK | Don't Care | No ACK | Don't Care | No ACK | No |
| | | CSWP | ACK | Don't Care | ACK | Don't Care | ACK | Yes |
| | | PSWP | ACK | Don't Care | ACK | Don't Care | ACK | Yes |
| | | Page or Byte Write in lower 128 bytes | ACK | Address | ACK | Data | No ACK | No |
| | 1 | SWP | No ACK | Don't Care | No ACK | Don't Care | No ACK | No |
| | | CSWP | ACK | Don't Care | ACK | Don't Care | No ACK | No |
| | | PSWP | ACK | Don't Care | ACK | Don't Care | No ACK | No |
| | | Page or Byte Write | ACK | Address | ACK | Data | No ACK | No |
| Not Protected | 0 | PSWP, SWP or CSWP | ACK | Don't Care | ACK | Don't Care | ACK | Yes |
| | | Page or Byte Write | ACK | Address | ACK | Data | ACK | Yes |
| | 1 | PSWP, SWP or CSWP | ACK | Don't Care | ACK | Don't Care | No ACK | No |
| | | Page or Byte Write | ACK | Address | ACK | Address | No ACK | No |

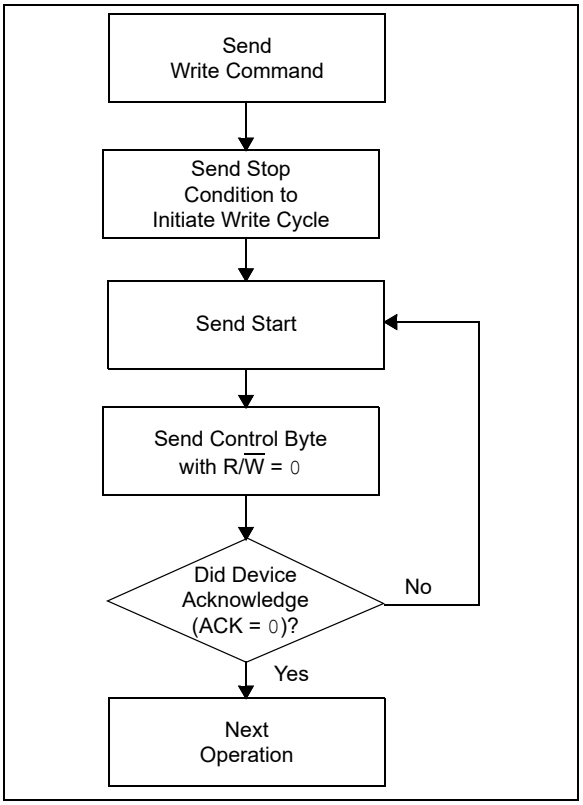
**TABLE 7-3: ACKNOWLEDGE TABLE FOR WRITE OR WRITE PROTECTION WITH R/$\overline{W}$ = 1**

| Status | Instruction | ACK |
|---|---|---|
| Permanently Protected | PSWP, SWP, CSWP | No ACK |
| Protected with SWP | SWP | No ACK |
| | CSWP | ACK |
| | PSWP | ACK |
| Not protected | PSWP, SWP, CSWP | ACK |

## 8.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, acknowledge polling can be used to determine when the cycle is complete. This feature can be used to maximize bus throughput. Once the Stop condition for a write command has been issued from the host, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the host sending a Start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the host can then proceed with the next read or write operation. See Figure 8-1 for flow diagram.

**FIGURE 8-1: ACKNOWLEDGE POLLING FLOW**



## 9.0 READ OPERATION

Read operations are initiated in the same way as write operations, with the exception that the R/$\overline{W}$ bit of the client address is set to '1'. There are three basic types of read operations: current address read, random read and sequential read.

### 9.1 Current Address Read

The 34XX02 contains an Address Pointer that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address 'n', the next current address read operation would access data from address n+1.

Upon receipt of the client address with R/$\overline{W}$ bit set to '1', the 34XX02 issues an Acknowledge and transmits the 8-bit data word. The host will not acknowledge the transfer, but does generate a Stop condition and the 34XX02 discontinues transmission (Figure 9-1).

### 9.2 Random Read

Random read operations allow the host to access any memory location in a random manner. To perform this type of read operation, the word address must first be set. This is done by sending the word address to the 34XX02 as part of a write operation. Once the word address is sent, the host generates a Start condition following the Acknowledge. This terminates the write operation, but not before the internal Address Pointer is set. The host then issues the control byte again, but with the R/$\overline{W}$ bit set to a '1'. The 34XX02 then issues an Acknowledge and transmits the 8-bit data word. The host will not acknowledge the transfer, but does generate a Stop condition and the 34XX02 discontinues transmission (Figure 9-2).

### 9.3 Sequential Read

Sequential reads are initiated in the same way as a random read, with the exception that after the 34XX02 transmits the first data byte, the host issues an Acknowledge, as opposed to a Stop condition in a random read. This directs the 34XX02 to transmit the next sequentially addressed 8-bit word (Figure 9-3).

To provide sequential reads, the 34XX02 contains an internal Address Pointer, which is incremented by one at the completion of each operation. This Address Pointer allows the entire memory contents to be serially read during one operation.

### 9.4 Contiguous Addressing Across Multiple Devices

The Chip Select bits (A2, A1, A0) can be used to expand the contiguous address space for up to 16K bits by adding up to eight 34XX02 devices on the same bus. In this case, the software can use A0 of the control byte as address bit A8, A1 as address bit A9 and A2 as address bit A10. It is not possible to sequentially read across device boundaries.

### 9.5 Noise Protection and Brown-Out

The 34XX02 employs a VCC threshold detector circuit which disables the internal erase/write logic if the VCC is below 1.35V at nominal conditions.

The SCL and SDA inputs have Schmitt Trigger and filter circuits which suppress noise spikes to assure proper device operation, even on a noisy bus.

**FIGURE 9-1: CURRENT ADDRESS READ**

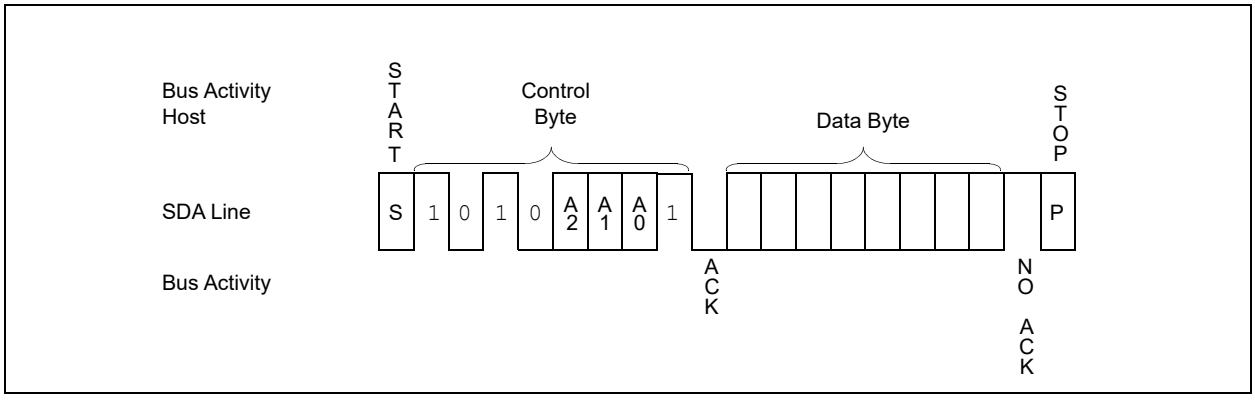


**FIGURE 9-2: RANDOM READ**

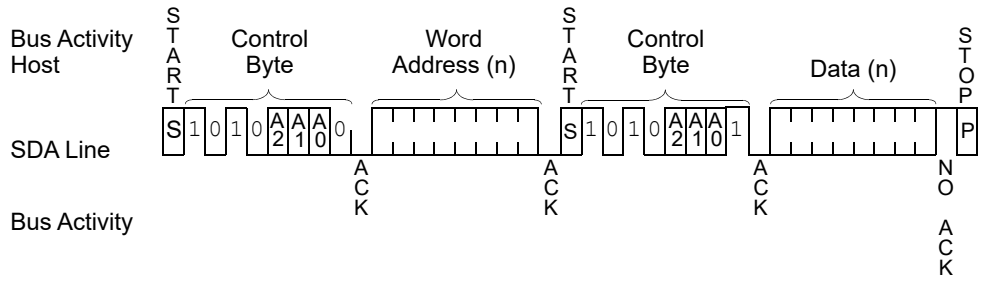
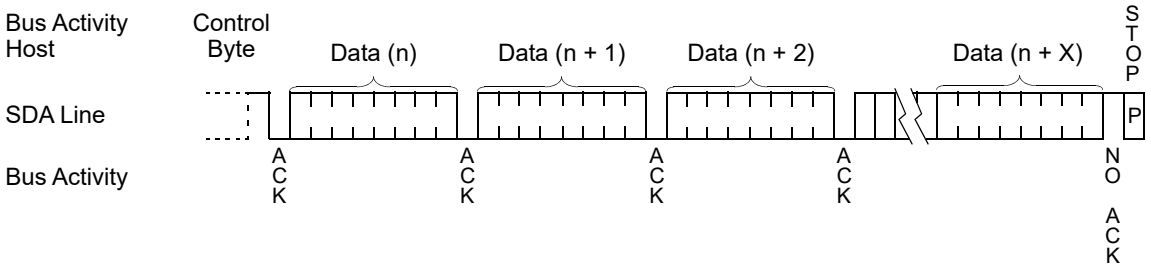


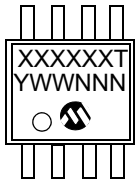

**FIGURE 9-3: SEQUENTIAL READ**



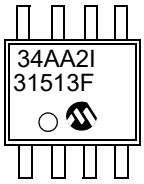
## 10.0 PACKAGING INFORMATION

### 10.1 Package Marking Information

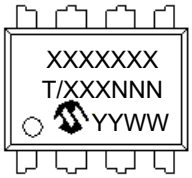
8-Lead MSOP



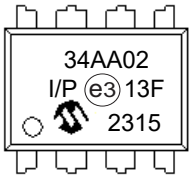

Example



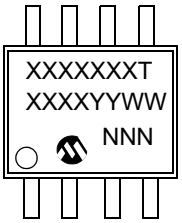

8-Lead PDIP (300 mil)



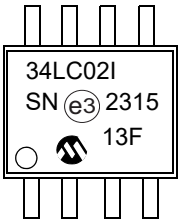

Example



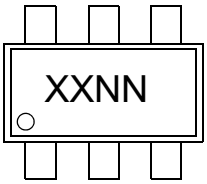

8-Lead SOIC



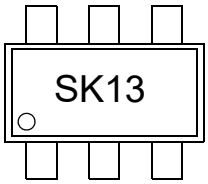

Example



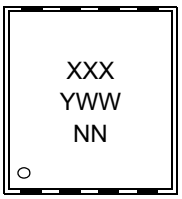

6-Lead SOT-23



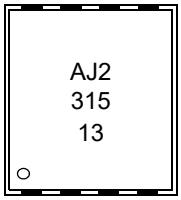

Example




8-Lead 2x3 TDFN

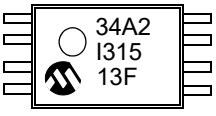



Example




8-Lead TSSOP


Example



| Part Number | 1st Line Marking Codes | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | MSOP | PDIP | SOIC | SOT-23 | | TDFN | | TSSOP |
| | | | | I-Temp. | E-Temp. | I-Temp. | E-Temp. | |
| 34AA02 | 34AA2T(1) | 34AA02 | 34AA02T(1) | SKNN(2) | SLNN(2) | AJ2 | AJ3 | 34A2 |
| 34LC02 | 34LC2T(1) | 34LC02 | 34LC02T(1) | STNN(2) | SUNN(2) | AJ5 | AJ6 | 34L2 |

**Note 1:** T = Temperature grade (I, E)

**2:** NN = Alphanumeric traceability code

| | | |
|---|---|---|
| **Legend:** | XX...X | Part number or part number code |
| | T | Temperature (I, E) |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code (2 characters for small packages) |
| | (e3) | JEDEC® designator for Matte Tin (Sn) |

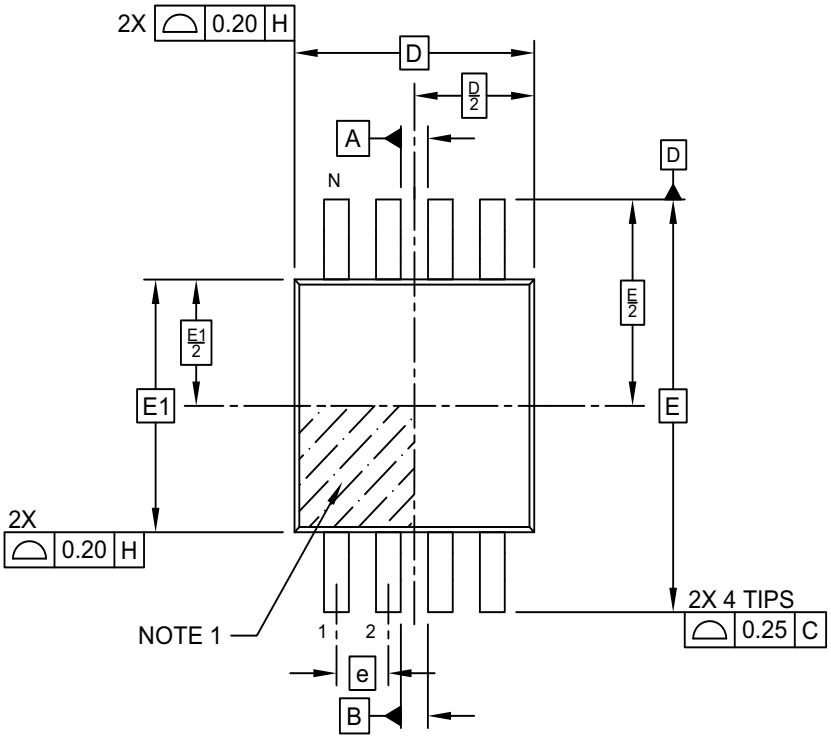
**Note:** Standard OTP marking consists of Microchip part number, year code, week code and traceability code.

**Note:** For very small packages with no room for the JEDEC® designator (e3), the marking will only appear on the outer carton or reel label.

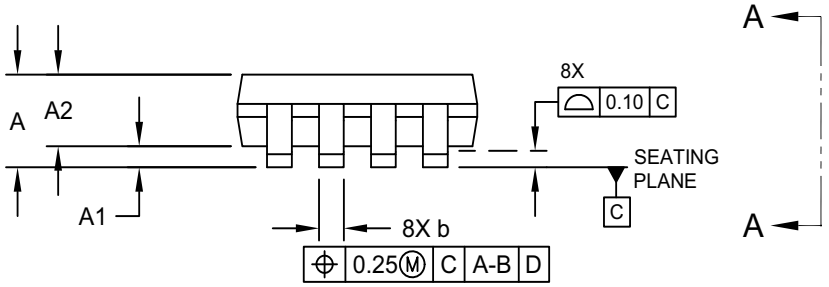
**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

### 8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

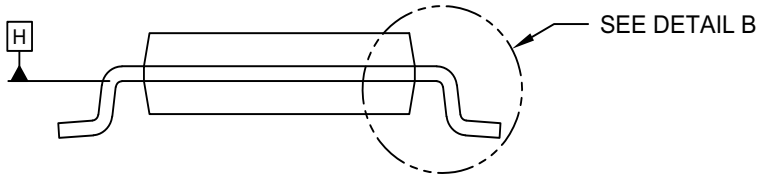
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




TOP VIEW




SIDE VIEW

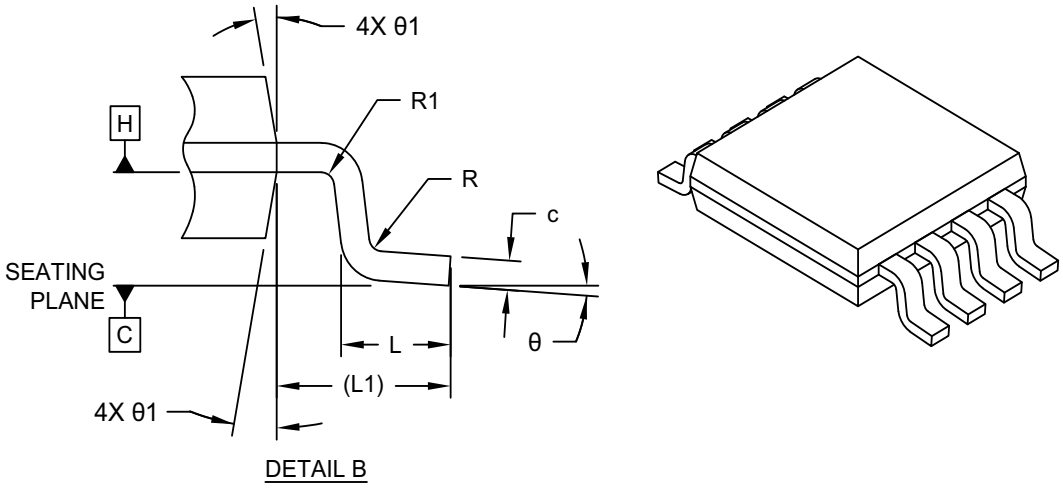



VIEW A–A

Microchip Technology Drawing C04-111-MS Rev F Sheet 1 of 2

### 8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Terminals | N | | 8 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | – | – | 1.10 |
| Standoff | A1 | 0.00 | – | 0.15 |
| Molded Package Thickness | A2 | 0.75 | 0.85 | 0.95 |
| Overall Length | D | | 3.00 BSC | |
| Overall Width | E | | 4.90 BSC | |
| Molded Package Width | E1 | | 3.00 BSC | |
| Terminal Width | b | 0.22 | – | 0.40 |
| Terminal Thickness | c | 0.08 | – | 0.23 |
| Terminal Length | L | 0.40 | 0.60 | 0.80 |
| Footprint | L1 | | 0.95 REF | |
| Lead Bend Radius | R | 0.07 | – | – |
| Lead Bend Radius | R1 | 0.07 | – | – |
| Foot Angle | θ | 0° | – | 8° |
| Mold Draft Angle | θ1 | 5° | – | 15° |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

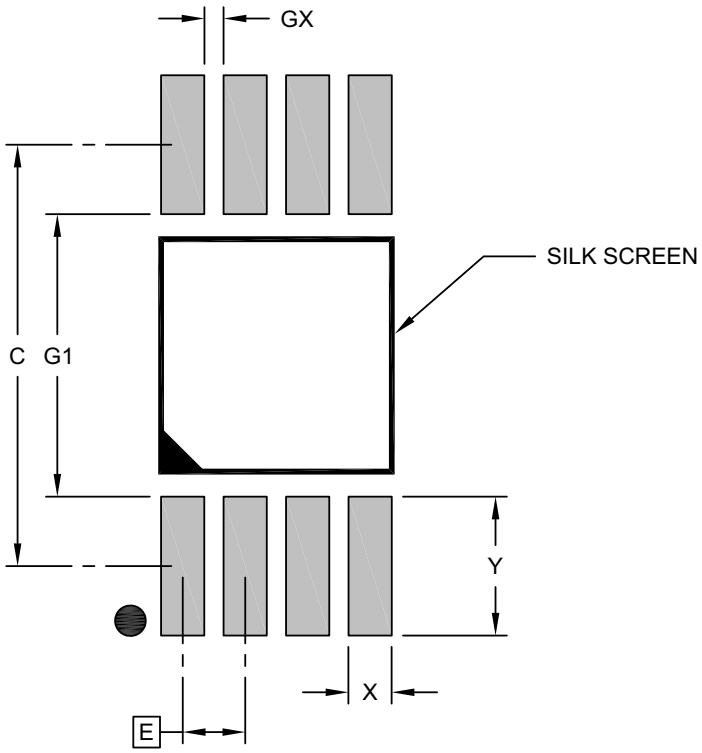
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111-MS Rev F Sheet 2 of 2

### 8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.65 BSC | |
| Contact Pad Spacing | C | | 4.40 | |
| Contact Pad Width (X8) | X | | | 0.45 |
| Contact Pad Length (X8) | Y | | | 1.45 |
| Contact Pad to Contact Pad (X4) | G1 | 2.95 | | |
| Contact Pad to Contact Pad (X6) | GX | 0.20 | | |

Notes:

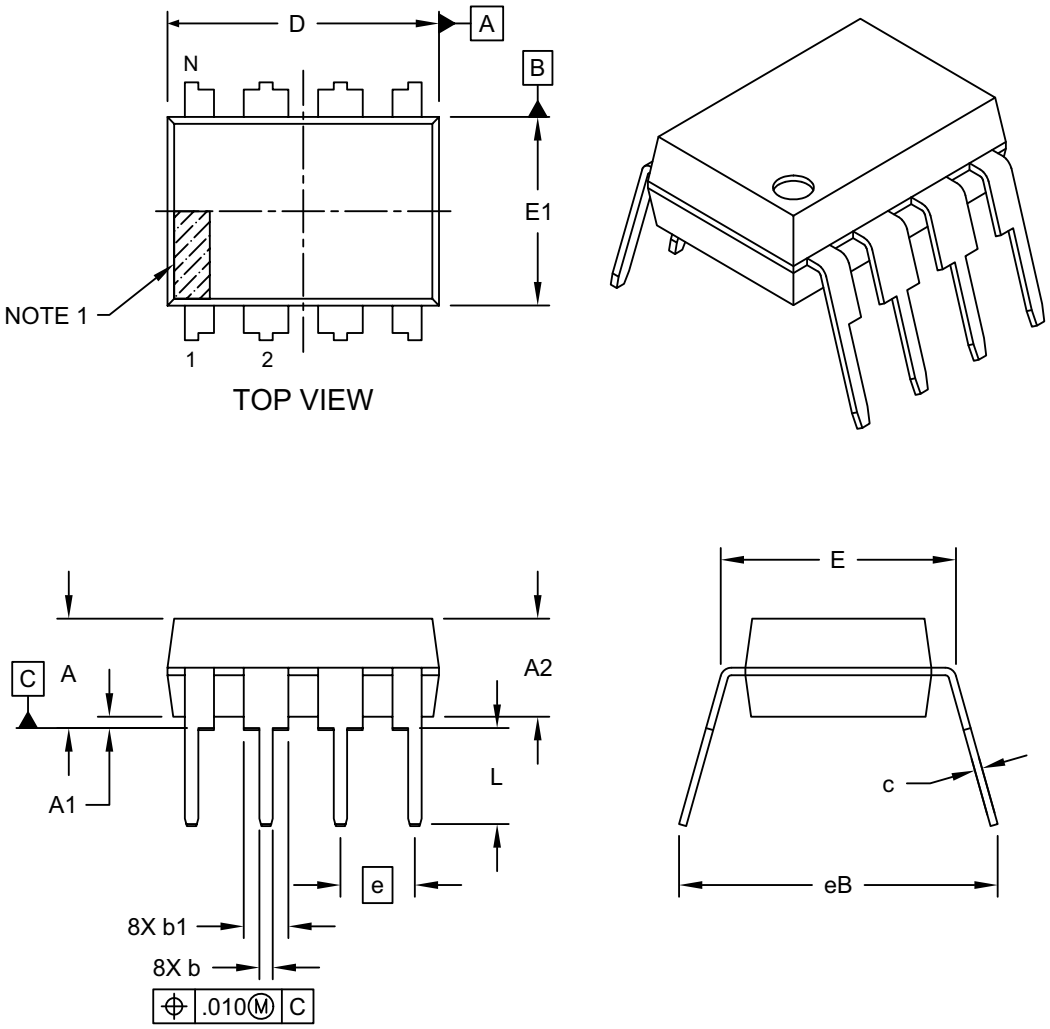
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2111-MS Rev F

### 8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

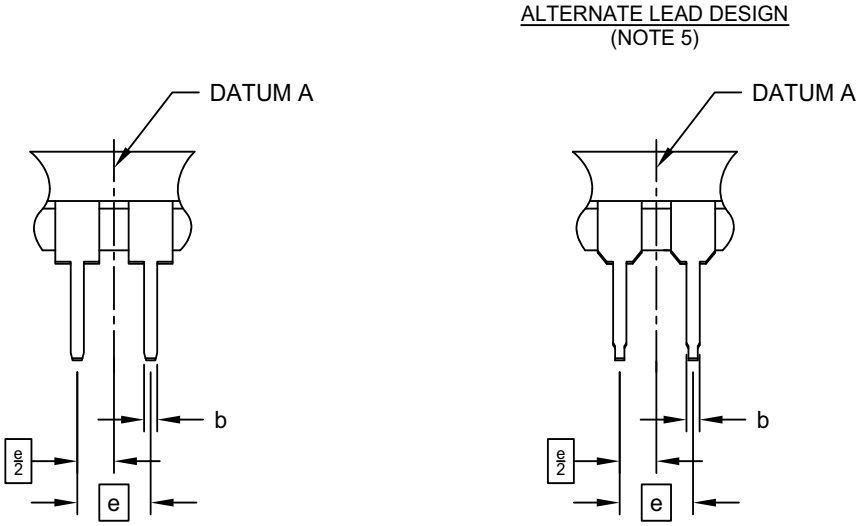
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing No. C04-018-P Rev F Sheet 1 of 2

### 8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | .100 BSC | |
| Top to Seating Plane | A | - | - | .210 |
| Molded Package Thickness | A2 | .115 | .130 | .195 |
| Base to Seating Plane | A1 | .015 | - | - |
| Shoulder to Shoulder Width | E | .290 | .310 | .325 |
| Molded Package Width | E1 | .240 | .250 | .280 |
| Overall Length | D | .348 | .365 | .400 |
| Tip to Seating Plane | L | .115 | .130 | .150 |
| Lead Thickness | c | .008 | .010 | .015 |
| Upper Lead Width | b1 | .040 | .060 | .070 |
| Lower Lead Width | b | .014 | .018 | .022 |
| Overall Row Spacing § | eB | - | - | .430 |

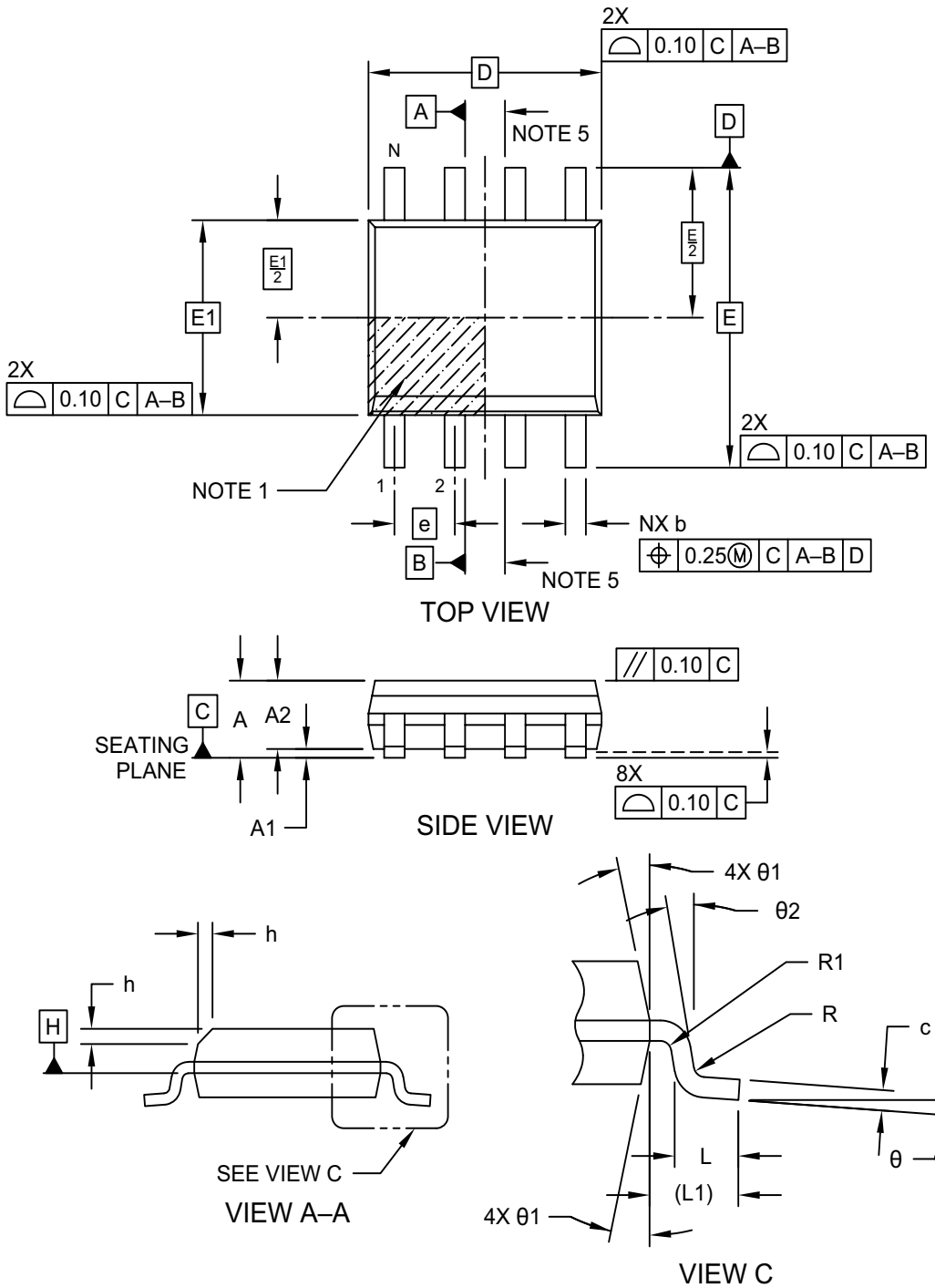
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
5. Lead design above seating plane may vary, based on assembly vendor.

Microchip Technology Drawing No. C04-018-P Rev F Sheet 2 of 2

### 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

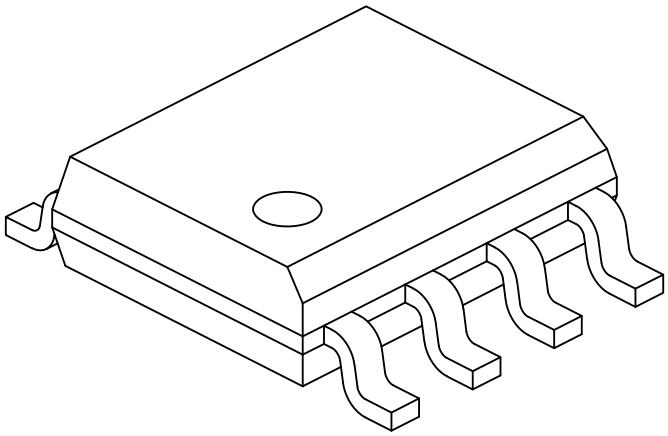
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing No. C04-057-SN Rev K Sheet 1 of 2

## 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 1.27 BSC | |
| Overall Height | A | – | – | 1.75 |
| Molded Package Thickness | A2 | 1.25 | – | - |
| Standoff § | A1 | 0.10 | – | 0.25 |
| Overall Width | E | | 6.00 BSC | |
| Molded Package Width | E1 | | 3.90 BSC | |
| Overall Length | D | | 4.90 BSC | |
| Chamfer (Optional) | h | 0.25 | – | 0.50 |
| Foot Length | L | 0.40 | – | 1.27 |
| Footprint | L1 | | 1.04 REF | |
| Lead Thickness | c | 0.17 | – | 0.25 |
| Lead Width | b | 0.31 | – | 0.51 |
| Lead Bend Radius | R | 0.07 | – | – |
| Lead Bend Radius | R1 | 0.07 | – | – |
| Foot Angle | θ | 0° | – | 8° |
| Mold Draft Angle | θ1 | 5° | – | 15° |
| Lead Angle | θ2 | 0° | – | – |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

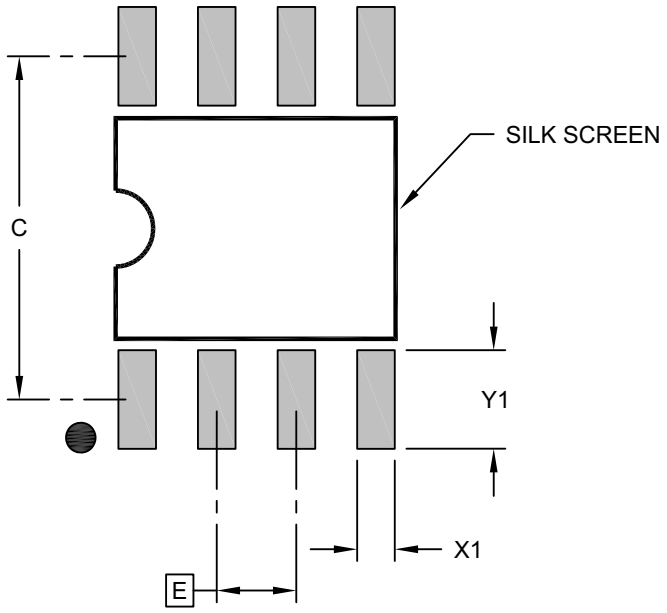
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev K Sheet 2 of 2

### 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 1.27 BSC | | |
| Contact Pad Spacing | C | | 5.40 | |
| Contact Pad Width (X8) | X1 | | | 0.60 |
| Contact Pad Length (X8) | Y1 | | | 1.55 |

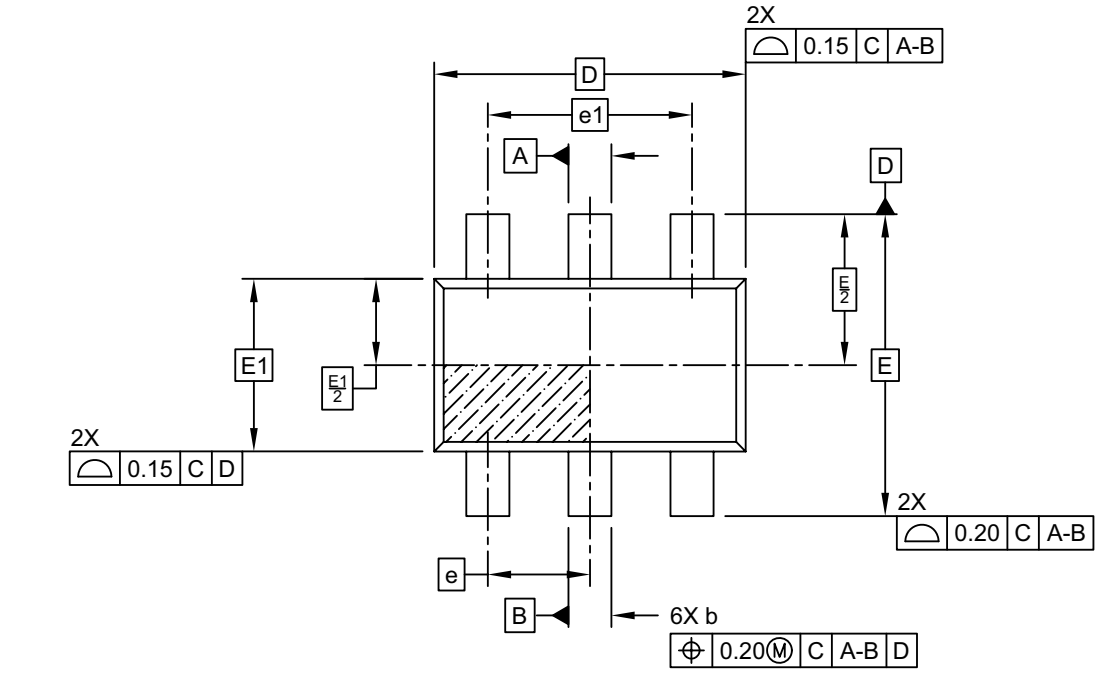
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

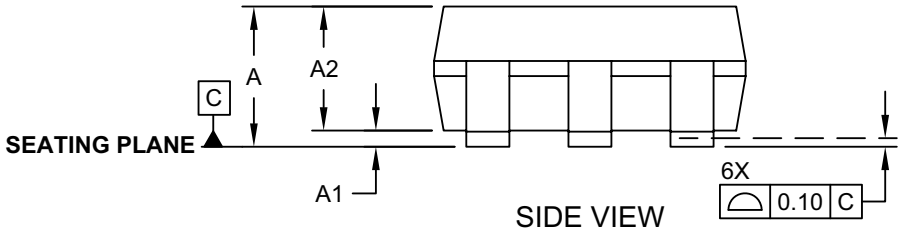
Microchip Technology Drawing C04-2057-SN Rev K

### 6-Lead Plastic Small Outline Transistor (OT, OTY) [SOT-23]

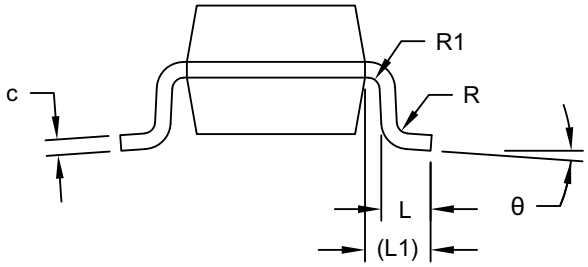
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




TOP VIEW




SIDE VIEW

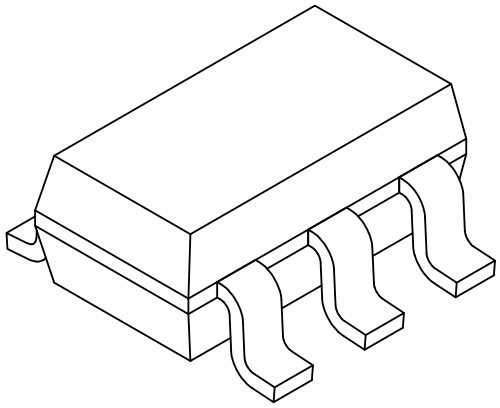



END VIEW

Microchip Technology Drawing C04-028-OT Rev E Sheet 1 of 2

### 6-Lead Plastic Small Outline Transistor (OT, OTY) [SOT-23]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Leads | N | | 6 | |
| Pitch | e | | 0.95 BSC | |
| Outside lead pitch | e1 | | 1.90 BSC | |
| Overall Height | A | 0.90 | - | 1.45 |
| Molded Package Thickness | A2 | 0.89 | 1.15 | 1.30 |
| Standoff | A1 | 0.00 | - | 0.15 |
| Overall Width | E | | 2.80 BSC | |
| Molded Package Width | E1 | | 1.60 BSC | |
| Overall Length | D | | 2.90 BSC | |
| Foot Length | L | 0.30 | 0.45 | 0.60 |
| Footprint | L1 | | 0.60 REF | |
| Foot Angle | θ | 0° | - | 10° |
| Lead Thickness | c | 0.08 | - | 0.26 |
| Lead Width | b | 0.20 | - | 0.51 |

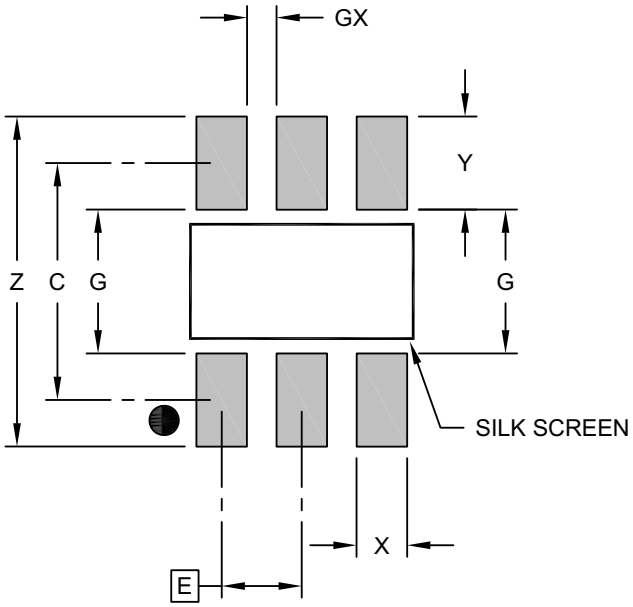
Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-028-OT Rev E Sheet 2 of 2

### 6-Lead Plastic Small Outline Transistor (OT, OTY) [SOT-23]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.95 BSC | |
| Contact Pad Spacing | C | | 2.80 | |
| Contact Pad Width (X3) | X | | | 0.60 |
| Contact Pad Length (X3) | Y | | | 1.10 |
| Distance Between Pads | G | 1.70 | | |
| Distance Between Pads | GX | 0.35 | | |
| Overall Width | Z | | | 3.90 |

Notes:

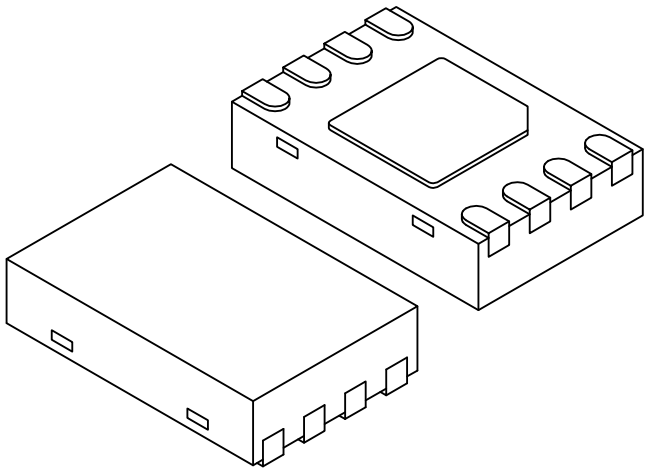
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2028-OT Rev E

### 8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.8 mm Body [TDFN] With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.70 | 0.75 | 0.80 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | | 0.20 REF | |
| Overall Length | D | | 2.00 BSC | |
| Overall Width | E | | 3.00 BSC | |
| Exposed Pad Length | D2 | 1.35 | 1.40 | 1.45 |
| Exposed Pad Width | E2 | 1.25 | 1.30 | 1.35 |
| Contact Width | b | 0.20 | 0.25 | 0.30 |
| Contact Length | L | 0.25 | 0.30 | 0.45 |
| Contact-to-Exposed Pad | K | 0.20 | - | - |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

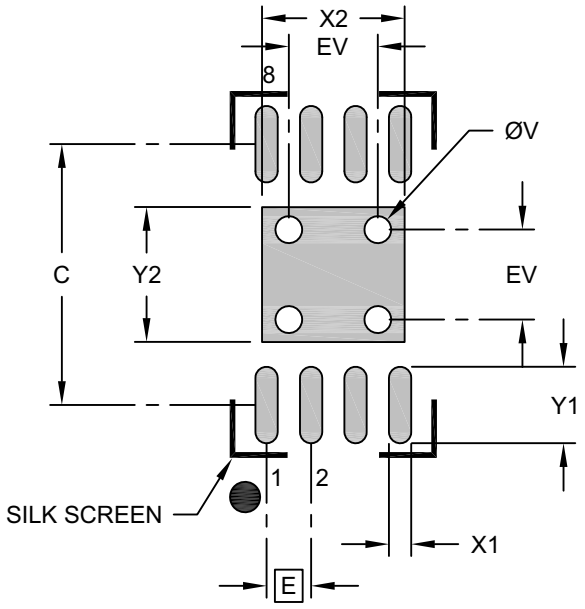
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-129-MN Rev E Sheet 2 of 2

### 8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.8 mm Body [TDFN] With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 0.50 BSC | | |
| Optional Center Pad Width | X2 | | | 1.60 |
| Optional Center Pad Length | Y2 | | | 1.50 |
| Contact Pad Spacing | C | | 2.90 | |
| Contact Pad Width (X8) | X1 | | | 0.25 |
| Contact Pad Length (X8) | Y1 | | | 0.85 |
| Thermal Via Diameter | V | | 0.30 | |
| Thermal Via Pitch | EV | | 1.00 | |

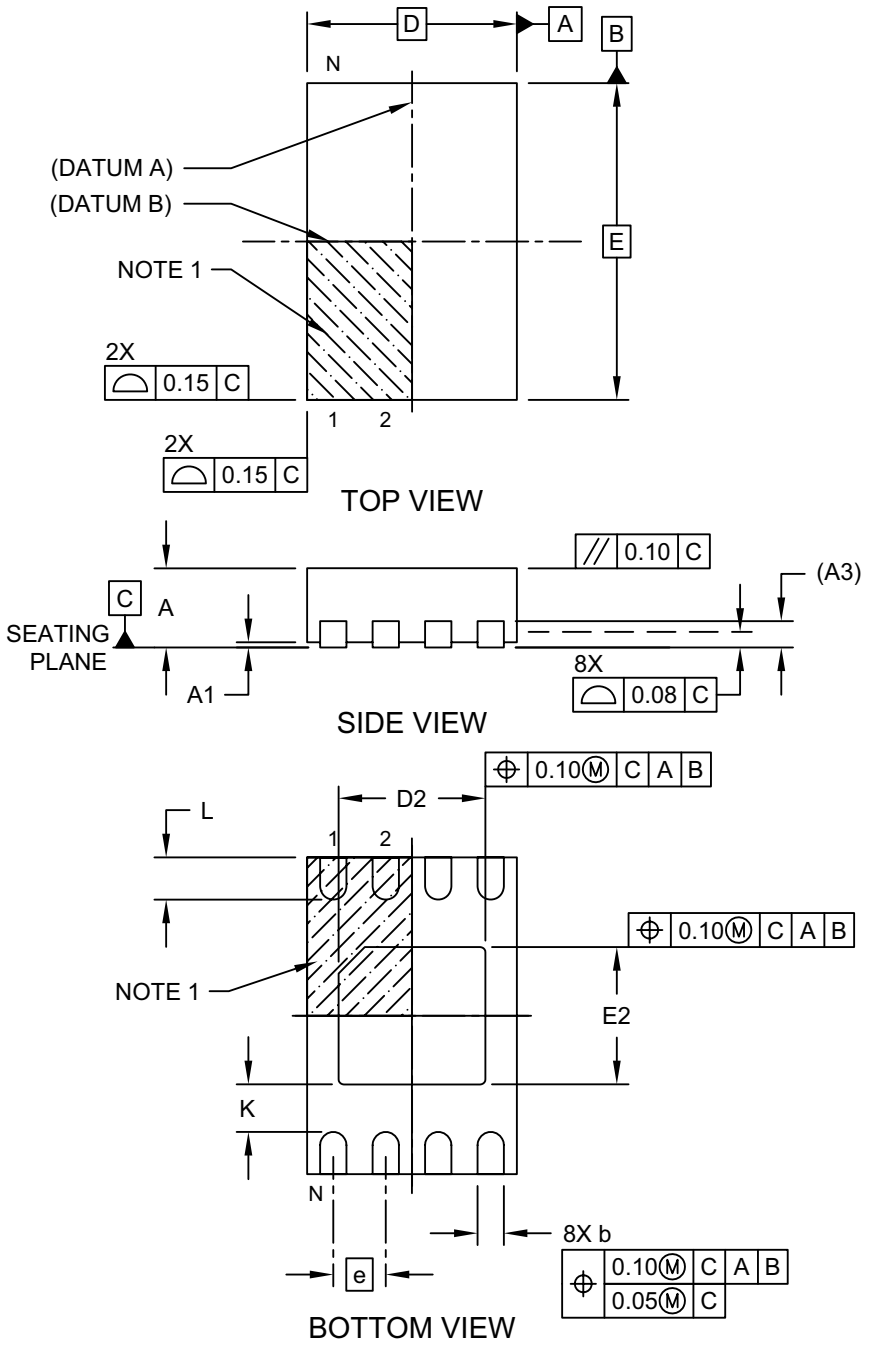
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing No. C04-129-MN Rev. B

**8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.8 mm Body [TDFN]**
**With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)**

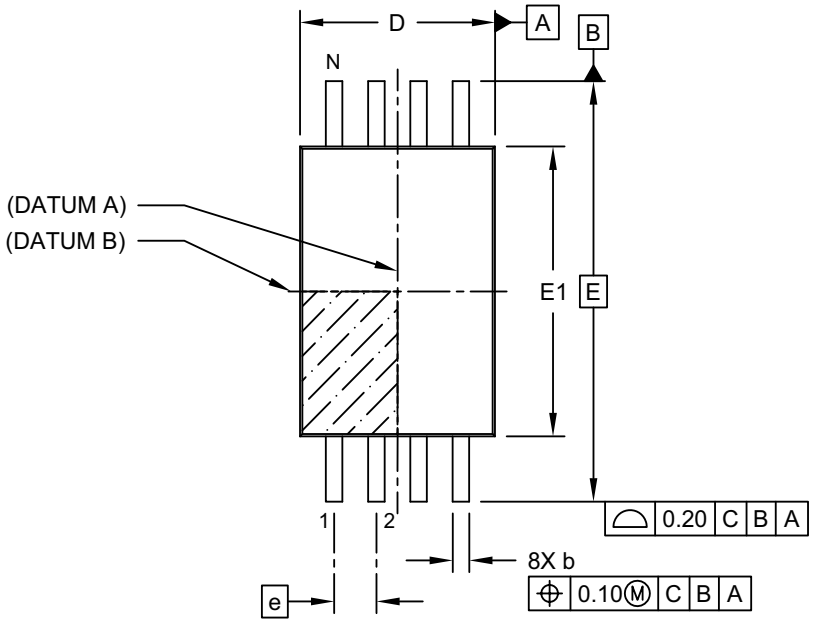
| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |
|---|---|



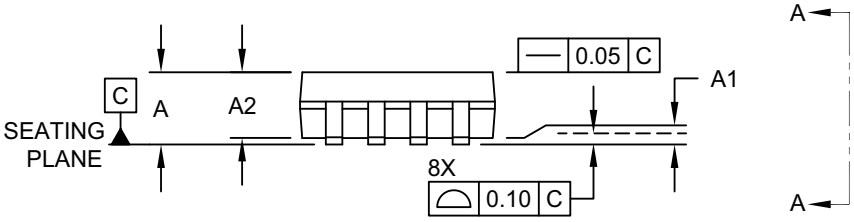

Microchip Technology Drawing No. C04-129-MN Rev E Sheet 1 of 2

### 8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

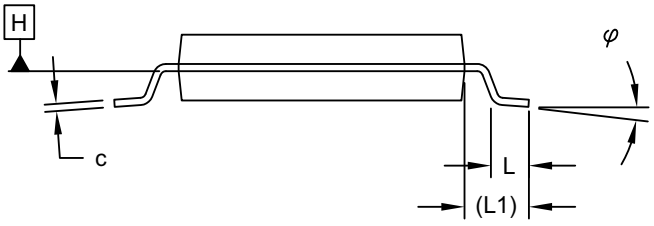
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




TOP VIEW




SIDE VIEW

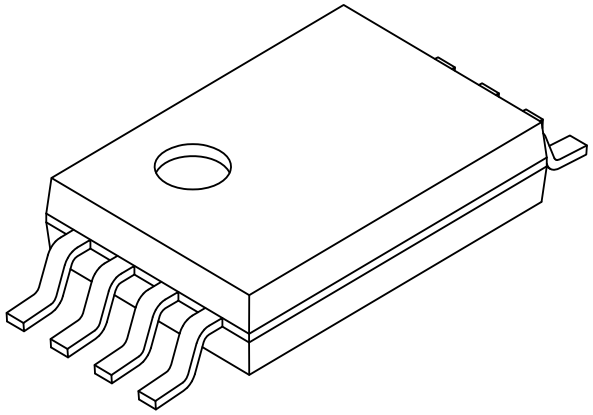



VIEW A-A

Microchip Technology Drawing C04-086 Rev C Sheet 1 of 2

### 8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | - | - | 1.20 |
| Molded Package Thickness | A2 | 0.80 | 1.00 | 1.05 |
| Standoff | A1 | 0.05 | - | - |
| Overall Width | E | | 6.40 BSC | |
| Molded Package Width | E1 | 4.30 | 4.40 | 4.50 |
| Overall Length | D | 2.90 | 3.00 | 3.10 |
| Foot Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | | 1.00 REF | |
| Lead Thickness | c | 0.09 | - | 0.25 |
| Foot Angle | φ | 0° | 4° | 8° |
| Lead Width | b | 0.19 | - | 0.30 |

Notes:

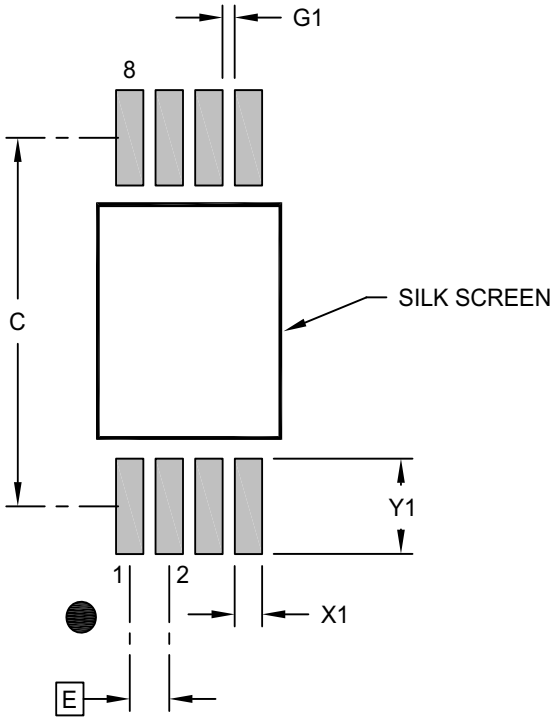
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086 Rev C Sheet 2 of 2

## 8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 0.65 BSC | | |
| Contact Pad Spacing | C | | 5.80 | |
| Contact Pad Width (X8) | X1 | | | 0.45 |
| Contact Pad Length (X8) | Y1 | | | 1.50 |
| Contact Pad to Center Pad (X6) | G1 | 0.20 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2086 Rev B

## APPENDIX A: REVISION HISTORY

### Revision H (06/2023)

Fixed the SOT-23 pinout descriptions on page 1 and in Product Identification System section. Pinout was in error and packages listed showed 5-pin that should be 6-pin.

### Revision G (04/2022)

Added Automotive Product Identification System section; Fixed $T_{BUF}$ typo and added 1 MHz spec; Updated MSOP, PDIP, SOIC, SOT-23, TDFN and TSSOP package drawings; Replaced terminology “Master” and “Slave” with “Host” and “Client”, respectively; Reformatted some sections for better readability.

### Revision F (03/2011)

Revised Section 3.6; Updated spec to new template.

### Revision E (01/2010)

Revised SOT-23 and TDFN marking codes.

### Revision D (04/2008)

Updated Product Identification System section.

### Revision C (02/2008)

Added TDFN and SOT-23 Package info; Removed “VL” Part.

### Revision B (02/2007)

Replaced Package Drawings.

### Revision A (01/2007)

Initial release of this document.

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## PRODUCT IDENTIFICATION SYSTEM (NON-AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | X [1] | –X | /XX |
|---|---|---|---|
| Device | Tape and Reel Option | Temperature Range | Package |

| | | | |
|---|---|---|---|
| **Device:** | 34AA02 | = | 1.7V, 2-Kbit $I^2C$ Serial EEPROM |
| | 34LC02 | = | 2.2V, 2-Kbit $I^2C$ Serial EEPROM |
| **Tape and Reel Option:** | Blank | = | Standard packaging (tube) |
| | T | = | Tape and Reel [1] |
| **Temperature Range:** | I | = | -40°C to +85°C (Industrial) |
| | E | = | -40°C to +125°C (Extended) |
| **Package:** | MS | = | Plastic Micro Small Outline – 8-Lead (MSOP) |
| | P | = | Plastic Dual In-Line – 300 mil Body, 8-Lead (PDIP) |
| | SN | = | Plastic Small Outline - Narrow, 3.90 mm Body, 8-Lead (SOIC) |
| | OT | = | Plastic Small Outline Transistor – 6-Lead (SOT-23) (Tape and Reel only) |
| | MNY | = | Plastic Dual Flat, No Lead Package – 2x3x0.8 mm Body, 8-Lead (TDFN) |
| | ST | = | Plastic Thin Shrink Small Outline – 4.4 mm Body, 8-Lead (TSSOP) |

**Examples**

a) 34AA02-I/P: 1.7V, 2-Kbit $I^2C$ Serial EEPROM, Industrial temp., PDIP package.

b) 34AA02-I/SN: 1.7V, 2-Kbit $I^2C$ Serial EEPROM, Industrial temp., SOIC package.

c) 34AA02T-E/MS: 1.7V, 2-Kbit $I^2C$ Serial EEPROM, Tape and Reel, Extended temp., MSOP package.

d) 34LC02-I/P: 2.2V, 2-Kbit $I^2C$ Serial EEPROM, Industrial temp., PDIP package.

e) 34LC02-I/MNY: 2.2V, 2-Kbit $I^2C$ Serial EEPROM, Industrial temp., TDFN package.

f) 34LC02T-E/MS: 2.2V, 2-Kbit, $I^2C$ Serial EEPROM, Tape and Reel, Extended temp., MSOP package.

g) 34AA02T-I/OT: 1.7V, 2-Kbit, $I^2C$ Serial EEPROM, Tape and Reel, Industrial temp., SOT-23 package.

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

## PRODUCT IDENTIFICATION SYSTEM (AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | X [1] | –X | /XX | XXX [2,3] |
|---|---|---|---|---|
| Device | Tape and Reel Option | Temperature Range | Package | Variant |

| | | | |
|---|---|---|---|
| **Device:** | 34AA02 | = | 2-Kbit $I^2C$ Serial EEPROM |
| | 34LC02 | = | 2-Kbit $I^2C$ Serial EEPROM |
| **Tape and Reel Option:** | Blank | = | Standard packaging (tube) |
| | T | = | Tape and Reel [1] |
| **Temperature Range:** | I | = | -40°C to +85°C (AEC-Q100 Grade 3) |
| | E | = | -40°C to +125°C (AEC-Q100 Grade 1) |
| **Package:** | OT | = | Plastic Small Outline Transistor – 6-Lead (SOT-23) (Tape and Reel only) |
| | MNY | = | Plastic Dual Flat, No Lead Package – 2x3x0.8 mm Body, 8-Lead (TDFN) |
| **Variant:** [2,3] | 16KVAO | = | Standard Automotive, 16K Process |
| | 16KVXX | = | Customer-Specific Automotive, 16K Process |

**Examples**

a) 34LC02T-I/MNY16KVAO: 2-Kbit $I^2C$ Serial EEPROM, Tape and Reel, Automotive Grade 3, TDFN package.

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

**2:** The VAO/VXX automotive variants have been designed, manufactured, tested and qualified in accordance with AEC-Q100 requirements for automotive applications.

**3:** For customers requesting a PPAP, a customer-specific part number will be generated and provided. A PPAP is not provided for VAO part numbers.

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