# LMC567 Low Power Tone Decoder

**Check for Samples: LMC567**

## FEATURES

- **Functionally Similar to LM567**
- **2V to 9V Supply Voltage Range**
- **Low Supply Current Drain**
- **No Increase in Current with Output Activated**
- **Operates to 500 kHz Input Frequency**
- **High Oscillator Stability**
- **Ground-referenced Input**
- **Hysteresis Added to Amplitude Comparator**
- **Out-of-band Signals and Noise Rejected**
- **20 mA Output Current Capability**

## DESCRIPTION

The LMC567 is a low power general purpose LMCMOS tone decoder which is functionally similar to the industry standard LM567. It consists of a twice frequency voltage-controlled oscillator (VCO) and quadrature dividers which establish the reference signals for phase and amplitude detectors. The phase detector and VCO form a phase-locked loop (PLL) which locks to an input signal frequency which is within the control range of the VCO. When the PLL is locked and the input signal amplitude exceeds an internally pre-set threshold, a switch to ground is activated on the output pin. External components set up the oscillator to run at twice the input frequency and determine the phase and amplitude filter time constants.

### Block Diagram

(with External Components)

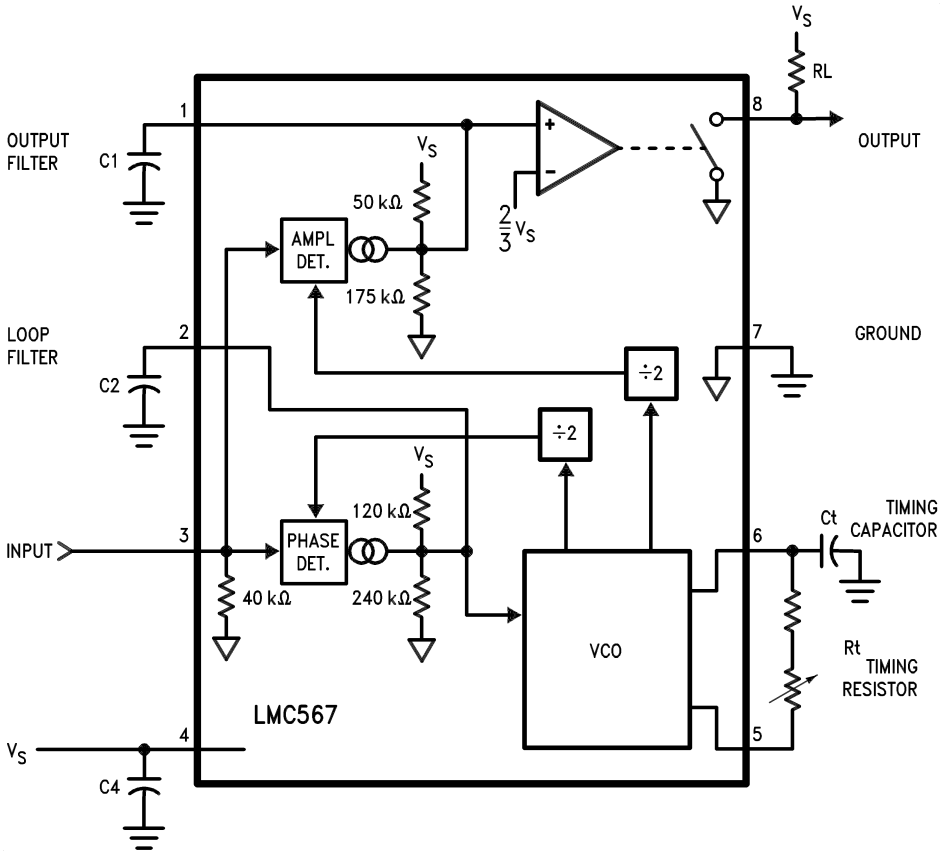


**Figure 1. See Package Number D0008A or P0008E**

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ABSOLUTE MAXIMUM RATINGS(1)(2)

| | MIN | MAX | UNIT |
|---|---|---|---|
| Input Voltage, Pin 3 | 2 | | $V_{p-p}$ |
| Supply Voltage, Pin 4 | | 10 | |
| Output Voltage, Pin 8 | | 13 | V |
| **Voltage at All Other Pins, Vs to Gnd** | | | |
| Output Current, Pin 8 | | 30 | mA |
| Package Dissipation | | 500 | mW |
| Operating Temperature Range ($T_A$) | −25 | 125 | |
| Storage Temperature Range | −55 | 150 | °C |
| **Soldering Information(3)**<br>**PDIP Package** | | | |
| Soldering (10 sec.) | | 260 | °C |
| **SOIC Package** | | | |
| Vapor Phase (60 sec.) | | 215 | |
| Infrared (15 sec.) | | 220 | °C |

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

(3) See http://www.ti.com for other methods of soldering surface mount devices.

## ELECTRICAL CHARACTERISTICS

Test Circuit, $T_A$ = 25°C, $V_s$ = 5V, RtCt #2, Sw. 1 Pos. 0, and no input, unless otherwise noted.

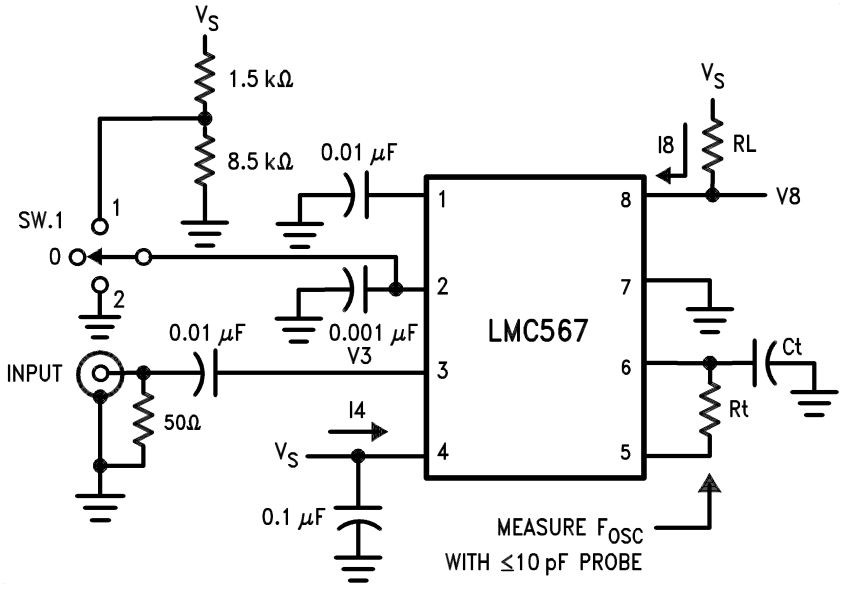
| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| I4 | Power Supply Current | RtCt #1, Quiescent or Activated | $V_s$ = 2V | | 0.3 | | mAdc |
| | | | $V_s$ = 5V | | 0.5 | 0.8 | |
| | | | $V_s$ = 9V | | 0.8 | 1.3 | |
| V3 | Input D.C. Bias | | | | 0 | | mVdc |
| R3 | Input Resistance | | | | 40 | | kΩ |
| I8 | Output Leakage | | | | 1 | 100 | nAdc |
| $f_0$ | Center Frequency, $F_{osc} \div 2$ | RtCt #2, Measure Oscillator Frequency and Divide by 2 | $V_s$ = 2V | | 98 | | kHz |
| | | | $V_s$ = 5V | 92 | 103 | 113 | |
| | | | $V_s$ = 9V | | 105 | | |
| $\Delta f_0$ | Center Frequency Shift with Supply | $\frac{f_0\|_{9V} - f_0\|_{2V}}{7\, f_0\|_{5V}} \times 100$ | | | 1.0 | 2.0 | %/V |
| $V_{in}$ | Input Threshold | Set Input Frequency Equal to $f_0$ Measured Above, Increase Input Level Until Pin 8 Goes Low. | $V_s$ = 2V | 11 | 20 | 27 | mVrms |
| | | | $V_s$ = 5V | 17 | 30 | 45 | |
| | | | $V_s$ = 9V | | 45 | | |
| $\Delta V_{in}$ | Input Hysteresis | Starting at Input Threshold, Decrease Input Level Until Pin 8 goes High. | | | 1.5 | | mVrms |
| V8 | Output "Sat' Voltage | Input Level > Threshold Choose RL for Specified I8 | I8 = 2 mA | | 0.06 | 0.15 | Vdc |
| | | | I8 = 20 mA | | 0.7 | | |

## ELECTRICAL CHARACTERISTICS (continued)

Test Circuit, $T_A$ = 25°C, $V_S$ = 5V, RtCt #2, Sw. 1 Pos. 0, and no input, unless otherwise noted.

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| L.D.B.W. | Largest Detection Bandwidth | Measure $F_{osc}$ with Sw. 1 in Pos. 0, 1, and 2; $L.D.B.W. = \frac{F_{osc\|P2} - F_{osc\|P1}}{F_{osc\|P0}} \times 100$ | $V_S$ = 2V | 7 | 11 | 15 | % |
| | | | $V_S$ = 5V | 11 | 14 | 17 | |
| | | | $V_S$ = 9V | | 15 | | |
| ΔBW | Bandwidth Skew | $Skew = \left(\frac{F_{osc\|P2} - F_{osc\|P1}}{2\,F_{osc\|P0}} - 1\right) \times 100$ | | | 0 | ±1.0 | % |
| $f_{max}$ | Highest Center Freq. | RtCt #3, Measure Oscillator Frequency and Divide by 2 | | | 700 | | kHz |
| $V_{in}$ | Input Threshold at $f_{max}$ | Set Input Frequency Equal to $f_{max}$ measured Above, Increase Input Level Until Pin 8 goes Low. | | | 35 | | mVrms |

## Test Circuit




| RtCt | Rt | Ct |
|---|---|---|
| #1 | 100k | 300 pF |
| #2 | 10k | 300 pF |
| #3 | 5.1k | 62 pF |

## TYPICAL PERFORMANCE CHARACTERISTICS

**Supply Current vs. Operating Frequency**

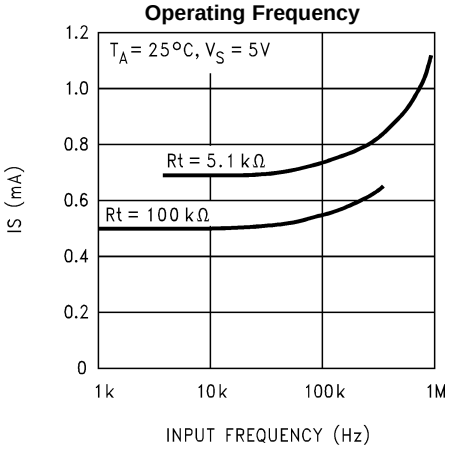



**Figure 2.**

**Bandwidth vs. Input Signal Level**

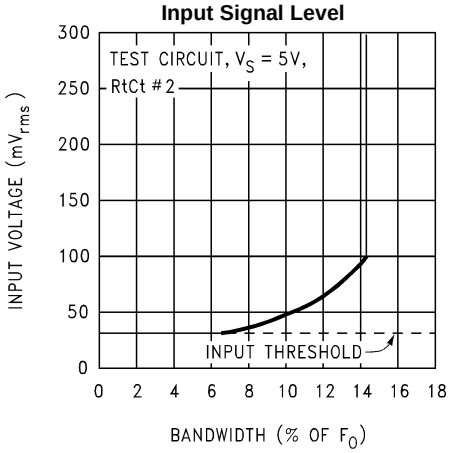



**Figure 3.**

**Largest Detection Bandwidth vs. Temp.**

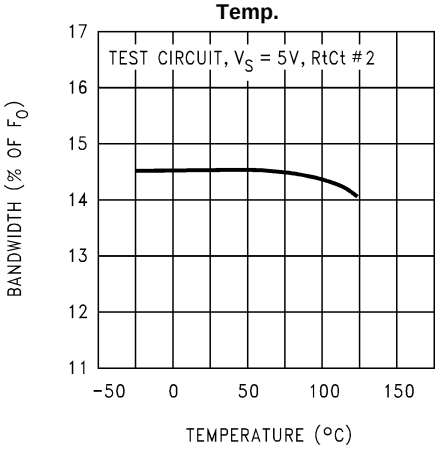



**Figure 4.**

**Bandwidth as a Function of C2**

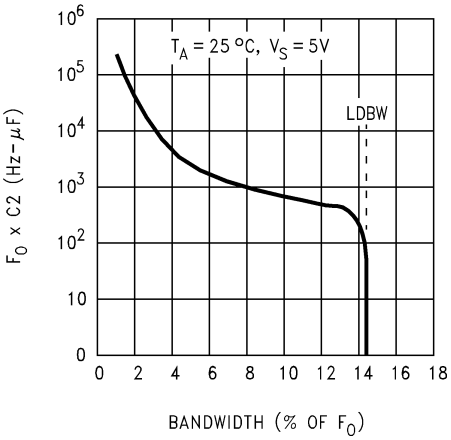



**Figure 5.**

**Frequency Drift with Temperature**

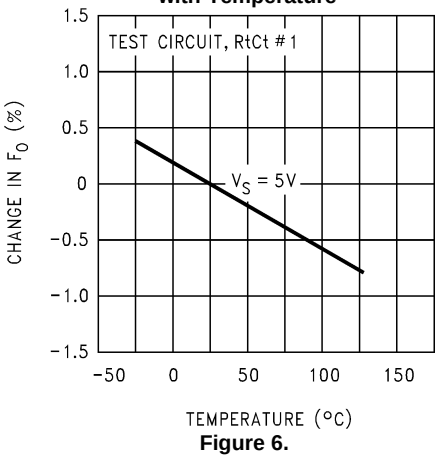



**Figure 6.**

**Frequency Drift with Temperature**

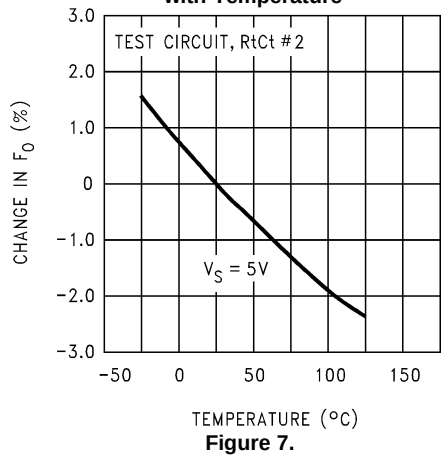



**Figure 7.**

## APPLICATION INFORMATION

(refer to Block Diagram)

### GENERAL

The LMC567 low power tone decoder can be operated at supply voltages of 2V to 9V and at input frequencies ranging from 1 Hz up to 500 kHz.

The LMC567 can be directly substituted in most LM567 applications with the following provisions:

1. Oscillator timing capacitor Ct must be halved to double the oscillator frequency relative to the input frequency (See OSCILLATOR TIMING COMPONENTS).
2. Filter capacitors C1 and C2 must be reduced by a factor of 8 to maintain the same filter time constants.
3. The output current demanded of pin 8 must be limited to the specified capability of the LMC567.

### OSCILLATOR TIMING COMPONENTS

The voltage-controlled oscillator (VCO) on the LMC567 must be set up to run at twice the frequency of the input signal tone to be decoded. The center frequency of the VCO is set by timing resistor Rt and timing capacitor Ct connected to pins 5 and 6 of the IC. The center frequency as a function of Rt and Ct is given by:

$$F_{OSC} \cong \frac{1}{1.4\ RtCt}\ Hz \tag{1}$$

Since this will cause an input tone of half $F_{osc}$ to be decoded,

$$F_{INPUT} \cong \frac{1}{2.8\ RtCt}\ Hz \tag{2}$$

This equation is accurate at low frequencies; however, above 50 kHz ($F_{osc}$ = 100 kHz), internal delays cause the actual frequency to be lower than predicted.

The choice of Rt and Ct will be a tradeoff between supply current and practical capacitor values. An additional supply current component is introduced due to Rt being switched to $V_s$ every half cycle to charge Ct:

$$I_s \text{ due to Rt} = V_s/(4Rt) \tag{3}$$

Thus the supply current can be minimized by keeping Rt as large as possible (see supply current vs. operating frequency curves). However, the desired frequency will dictate an RtCt product such that increasing Rt will require a smaller Ct. Below Ct = 100 pF, circuit board stray capacitances begin to play a role in determining the oscillation frequency which ultimately limits the minimum Ct.

To allow for I.C. and component value tolerances, the oscillator timing components will require a trim. This is generally accomplished by using a variable resistor as part of Rt, although Ct could also be padded. The amount of initial frequency variation due to the LMC567 itself is given in the electrical specifications; the total trim range must also accommodate the tolerances of Rt and Ct.

### SUPPLY DECOUPLING

The decoupling of supply pin 4 becomes more critical at high supply voltages with high operating frequencies, requiring C4 to be placed as close as possible to pin 4.

### INPUT PIN

The input pin 3 is internally ground-referenced with a nominal 40 kΩ resistor. Signals which are already centered on 0V may be directly coupled to pin 3; however, any d.c. potential must be isolated via a coupling capacitor. Inputs of multiple LMC567 devices can be paralleled without individual d.c. isolation.

## LOOP FILTER

Pin 2 is the combined output of the phase detector and control input of the VCO for the phase-locked loop (PLL). Capacitor C2 in conjunction with the nominal 80 kΩ pin 2 internal resistance forms the loop filter.

For small values of C2, the PLL will have a fast acquisition time and the pull-in range will be set by the built in VCO frequency stops, which also determine the largest detection bandwidth (LDBW). Increasing C2 results in improved noise immunity at the expense of acquisition time, and the pull-in range will begin to become narrower than the LDBW (see Bandwidth as a Function of C2 curve). However, the maximum hold-in range will always equal the LDBW.

## OUTPUT FILTER

Pin 1 is the output of a negative-going amplitude detector which has a nominal 0 signal output of 7/9 $V_S$. When the PLL is locked to the input, an increase in signal level causes the detector output to move negative. When pin 1 reaches 2/3 $V_S$ the output is activated (see OUTPUT PIN).

Capacitor C1 in conjunction with the nominal 40 kΩ pin 1 internal resistance forms the output filter. The size of C1 is a tradeoff between slew rate and carrier ripple at the output comparator. Low values of C1 produce the least delay between the input and output for tone burst applications, while larger values of C1 improve noise immunity.

Pin 1 also provides a means for shifting the input threshold higher or lower by connecting an external resistor to supply or ground. However, reducing the threshold using this technique increases sensitivity to pin 1 carrier ripple and also results in more part to part threshold variation.

## OUTPUT PIN

The output at pin 8 is an N-channel FET switch to ground which is activated when the PLL is locked and the input tone is of sufficient amplitude to cause pin 1 to fall below 2/3 $V_S$. Apart from the obvious current component due to the external pin 8 load resistor, no additional supply current is required to activate the switch. The on resistance of the switch is inversely proportional to supply; thus the “sat” voltage for a given output current will increase at lower supplies.

## REVISION HISTORY

| Changes from Revision A (April 2013) to Revision B | Page |
|---|---|
| • Changed layout of National Data Sheet to TI format | 6 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LMC567CM/NOPB | ACTIVE | SOIC | D | 8 | 95 | Green (RoHS & no Sb/Br) | SN \| CU SN | Level-1-260C-UNLIM | -25 to 100 | LMC 567CM | Samples |
| LMC567CMX/NOPB | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | SN \| CU SN | Level-1-260C-UNLIM | -25 to 100 | LMC 567CM | Samples |
| LMC567CN/NOPB | ACTIVE | PDIP | P | 8 | 40 | Green (RoHS & no Sb/Br) | CU SN | Level-1-NA-UNLIM | -25 to 100 | LMC 567CN | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
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**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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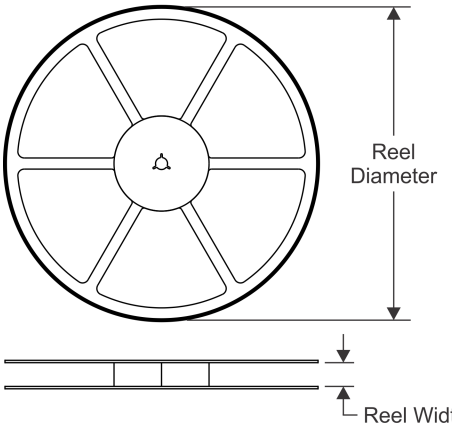
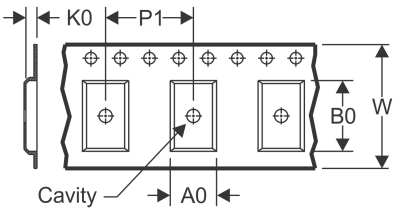
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

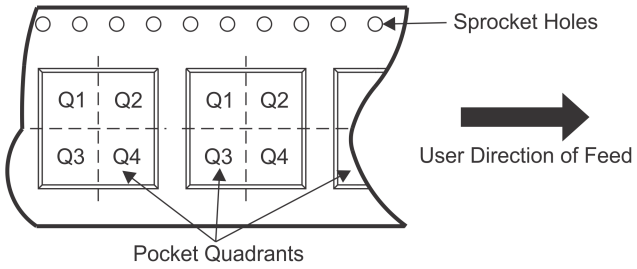



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

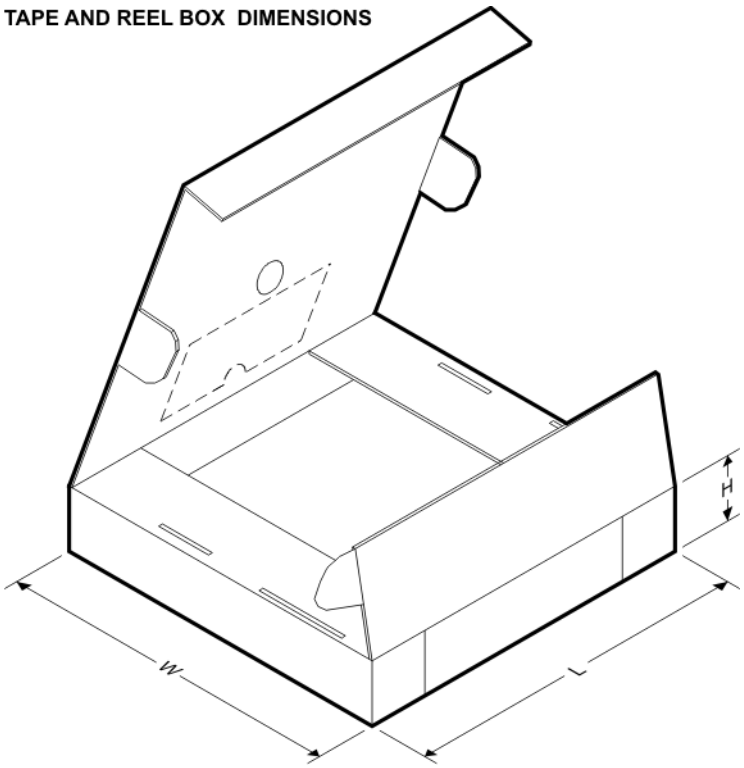
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LMC567CMX/NOPB | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |

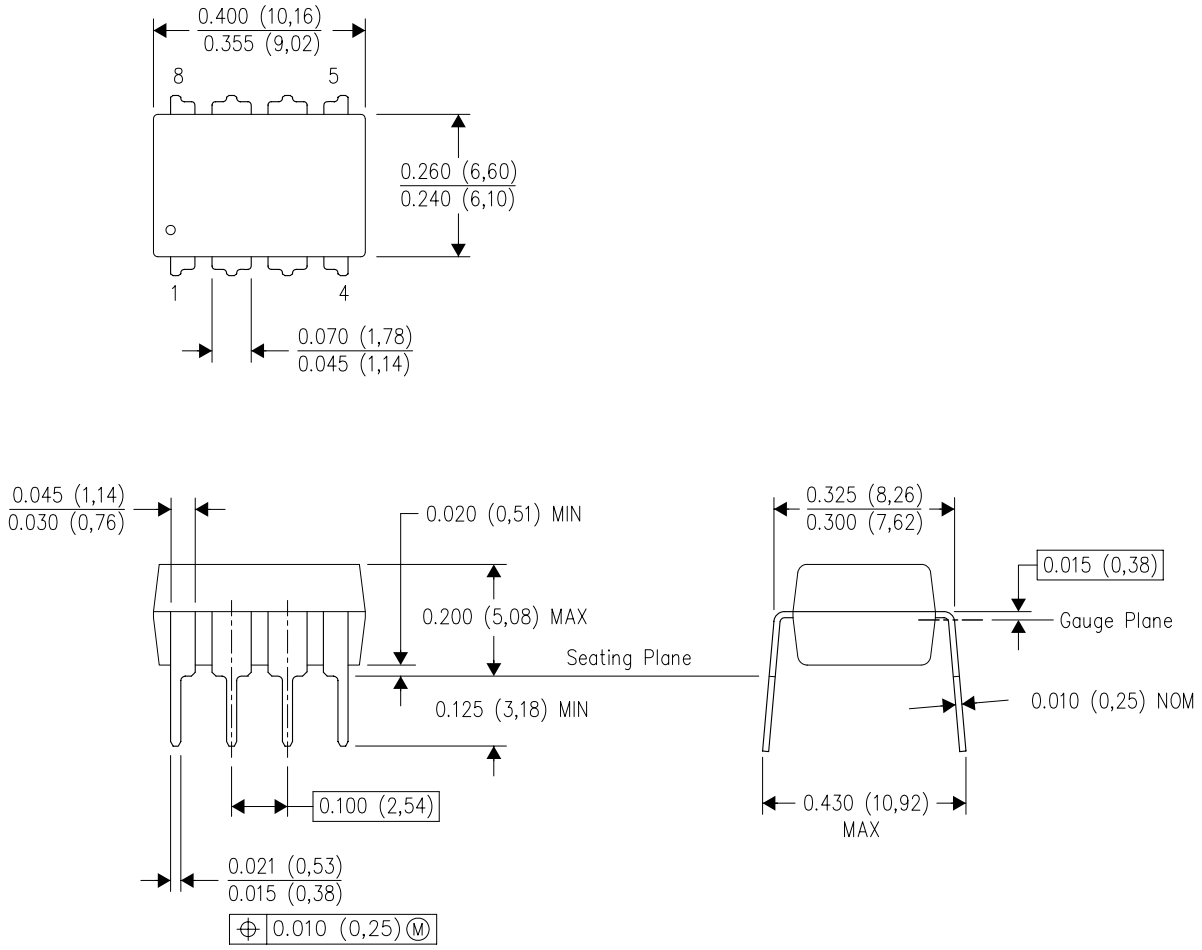
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

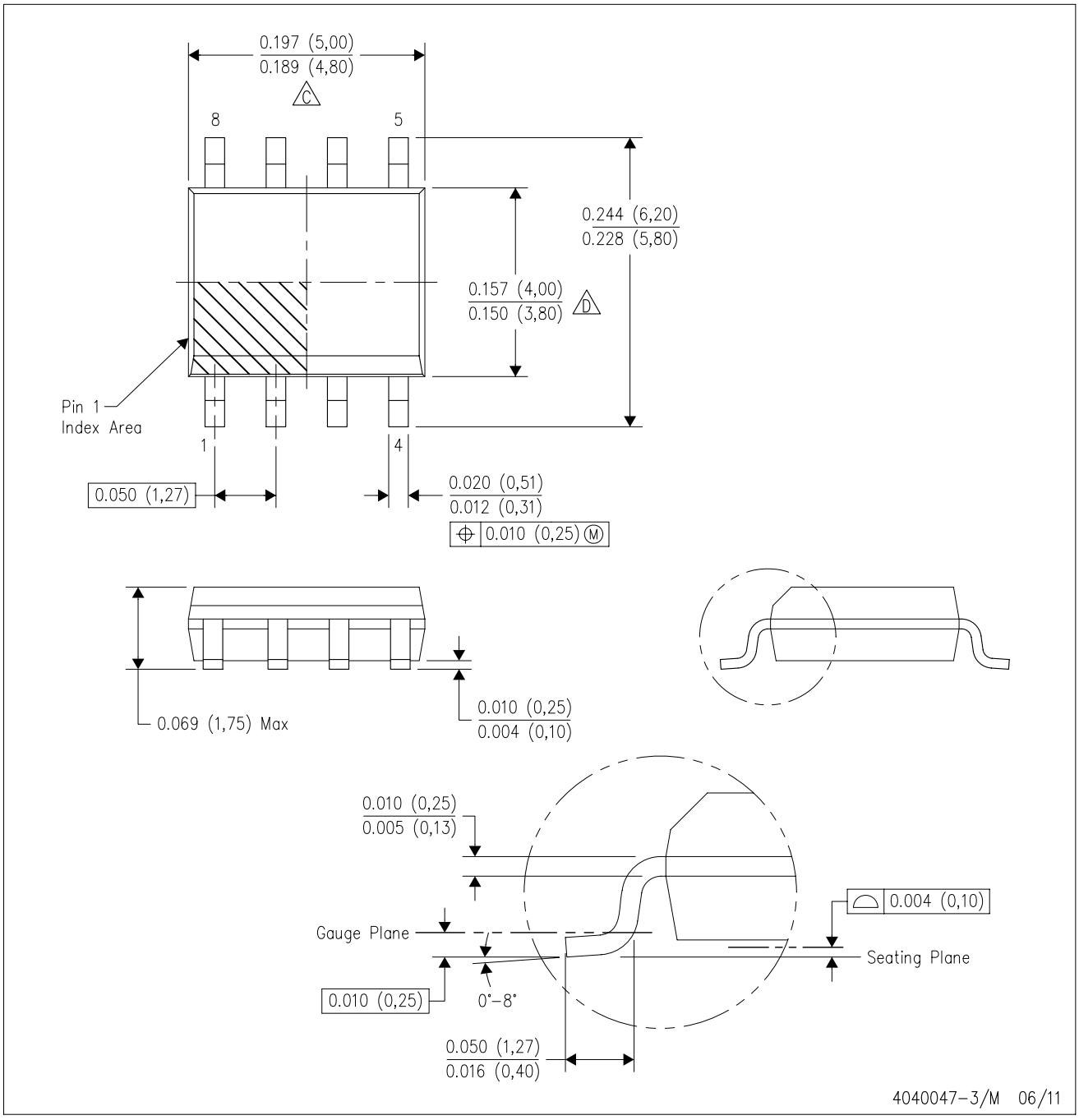
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LMC567CMX/NOPB | SOIC | D | 8 | 2500 | 349.0 | 337.0 | 45.0 |

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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