CDB4384

Evaluation Board for CS4384

Features

- Demonstrates recommended layout and grounding arrangements.
- CS8416 receives S/PDIF, & EIAJ-340 compatible digital audio.
- Headers for external audio input for either PCM or DSD.
- Requires only a digital signal source and power supplies for a complete Digital-to-analog converter system.

Description

The CDB4384 evaluation board is an excellent means for quickly evaluating the CS4384 24-bit, 48-pin, 8-channel, single-ended D/A converter. Evaluation requires an analog signal analyzer, a digital signal source, a PC for controlling the CS4384 (only required for control port mode), and a power supply. Analog line-level outputs are provided via RCA phono jacks.

The CS8416 digital audio receiver IC provides the system timing necessary to operate the digital-to-analog converter and will accept S/PDIF and EIAJ-340-compatible audio data. The evaluation board may also be configured to accept external timing and data signals for operation in a user application during system development.

ORDERING INFORMATION
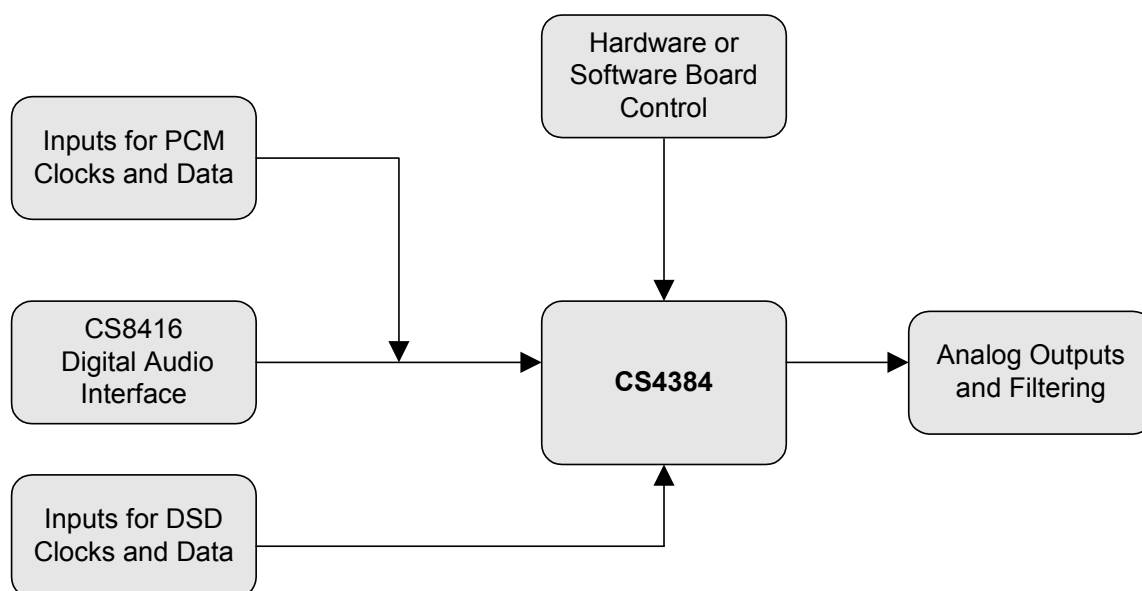CDB4384   Evaluation Board

TABLE OF CONTENTS

LIST OF FIGURES

CDB4384 SYSTEM OVERVIEW

The CDB4384 evaluation board is an excellent means of quickly evaluating the CS4384. The CS8416 digital audio interface receiver provides an easy interface to digital audio signal sources including the majority of digital audio test equipment. The evaluation board also allows the user to supply external PCM or DSD clocks and data through PCB headers for system development.

The CDB4384 uses the CDB4385 as a base PCB board. For this reason, there may be additional circuitry on board which is not populated as it has no function for this device.

The CDB4384 schematic has been partitioned into 9 schematics shown in Figures 2 through 10. Each partitioned schematic is represented in the system diagram shown in Figure 1. Notice that the system diagram also includes the interconnections between the partitioned schematics.

1. CS4384 DIGITAL TO ANALOG CONVERTER

A description of the CS4384 is included in the CS4384 datasheet.

2. CS8416 DIGITAL AUDIO RECEIVER

The system receives and decodes the standard S/PDIF data format using a CS8416 digital audio receiver (Figure 6). The outputs of the CS8416 include a serial bit clock, serial data, left-right clock, and a 128/256 Fs master clock. The CS8416 data format is fixed to I^{2}S. The operation of the CS8416 and a discussion of the digital audio interface is included in the CS8416 datasheet.

The evaluation board has been designed such that the input can be either optical or coaxial, see Figure 6. However, both inputs cannot be driven simultaneously.

Switch position 7 of S1 sets the output MCLK-to-LRCK ratio of the CS8416. This switch should be set to 256 (closed) for inputs Fs ≤ 96 kHz and 128 (open) for Fs ≥ 64 kHz. The CS8416 must be manually reset using 'HW RST' (S2) or through the software when this switch is changed.

3. INPUT FOR CLOCKS AND DATA

The evaluation board has been designed to allow interfacing to external systems via headers J11 and J7. Header J11 allows the evaluation board to accept externally generated PCM clocks and data. The schematic for the clock/data input is shown in Figure 7. Switch position 6 of S1 selects the source as either CS8416 (open) or header J11 (closed).

Header J7 allows the evaluation board to accept externally generated DSD data and clocks. The schematic for the clock/data input is shown in Figure 8. A synchronous MCLK must still be provided via Header J11. Switch position 8 of S1 selects either PCM (open) or DSD (closed).

Please see the CS4384 datasheet for more information.

4. INPUT FOR CONTROL DATA

The evaluation board can be run in either a stand-alone mode or with a PC. Stand-alone mode uses the CS4384 in hardware mode and the mode pins are configured using switch positions 1 through 5 of S1. PC mode uses software to setup the CS4384 through I^{2}C using the PC's serial port. PC mode is automatically selected when the serial port (RS232 or USB) is attached and the CDB4384 software is running. The latest control software may be downloaded from: www.cirrus.com/msasoftware.

Header J15 offers the option for external input of RST and SPI^{TM}/I^{2}C clocks and data. The board is setup from the factory to use the on-board microcontroller in conjunction with the supplied software. To use an external control

source, remove the shunts on J15 and place a ribbon cable so the signal lines are on the center row and the grounds are on the right side. R116 and R119 should be populated with 2 kΩ resistors when using an external I²C source which does not already provide pull-ups.

5. POWER SUPPLY CIRCUITRY

Power is supplied to the evaluation board by four binding posts (GND, +5V, +12V, and -12V), see Figure 10. The '+5V' terminal supplies VA and the rest of the +5 V circuitry on the board. The +3.3 V circuitry is powered from a regulator. The +2.5 V required for VD is also provided from an on-board regulator. The +5 V supply should be set within the recommended values for VA stated in the CS4384 datasheet.

WARNING: Refer to the CS4384 datasheet for maximum allowable voltage levels. Operation outside of this range can cause permanent damage to the device.

6. GROUNDING AND POWER SUPPLY DECOUPLING

As with any high-performance converter, the CS4384 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 2 details the connections to the CS4384 and Figures 11, 12, and 13 show the component placement and top and bottom layout. The decoupling capacitors are located as close to the CS4384 as possible. Extensive use of ground plane fill in the evaluation board yields large reductions in radiated noise.

7. ANALOG OUTPUT FILTERING

The analog output on the CDB4384 has been designed according to the CS4384 datasheet. This output circuit includes a passive 1-pole, 150 kHz filter with an AC coupled output.

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
+5V	Input	+ 5 V power
GND	Input	Ground connection from power supply
+12V	Input	Unused
-12V	Input	Negative supply for the mute circuitry (-5 V to -12 V)
S/PDIF IN - J9	Input	Digital audio interface input via coax
S/PDIF IN - OPT1	Input	Digital audio interface input via optical
PCM INPUT - J11	Input	Input for master, serial, left/right clocks and serial data
DSD INPUT - J7	Input	Input for DSD serial clock and DSD data
OUTA1-B4	Output	RCA line level analog outputs

Table 1. System Connections

JUMPER / SWITCH	PURPOSE	POSITION	FUNCTION SELECTED
J15	Selects source of control data	*shunts on Left shunts removed	*Control from PC and on-board microcontroller External control input using center and right columns
J16	JTAG micro programming	-	Reserved for factory use only
S2	Resets CS8416 and CS4384		The CS8416 must be reset if switch S1 is changed
S1	CS4384 mode settings M0-M4	1-5	Default: M0, M4 open (HI) M1, M2, M3 closed (LO)
	Sets clock source	6	Sets clock source for CS4384 *open = RX(CS8416), closed = $\overline{EXT}$(J11)
	Sets MCLK ratio of CS8416	7	Selects 128x (open) or 256x (*closed) MCLK/LRCK ratio output for CS8416
	Selects PCM or DSD mode	8	For PCM input set to *Open, for DSD set to Closed

Table 2. CDB4384 Jumper Settings

*Default Factory Settings.

8. ERRATA

CDB4384 rev C.

-None at this time.

9. SCHEMATICS

Power
Figure 10 on page 15

Single-Ended Analog Outputs

A1, B1 — Figure 3 on page 8
A2, B2 — Figure 3 on page 8
A3, B3 — Figure 4 on page 9
A4, B4 — Figure 4 on page 9

2 / 2 / 2 / 2

Serial Control Port
Figure 9 on page 14

I²C/SPI Header

CS4384
Figure 2 on page 7

DSD clk_enable

DSD HEADER
Figure 8 on page 13

DSD Clocks/Data

PCM Clocks/Data

PCM mux
Figure 7 on page 12

DSD input enable

M0 - M4 switches
(for stand-alone mode)

PCM source select

CS8416 clock setting

Hardware Control Switches
Figure 9 on page 14

PCM Clocks/Data

PCM Clocks/Data

PCM HEADER
Figure 7 on page 12

CS8416 S/PDIF Input
Figure 6 on page 11

Figure 1. System Block Diagram and Signal Flow
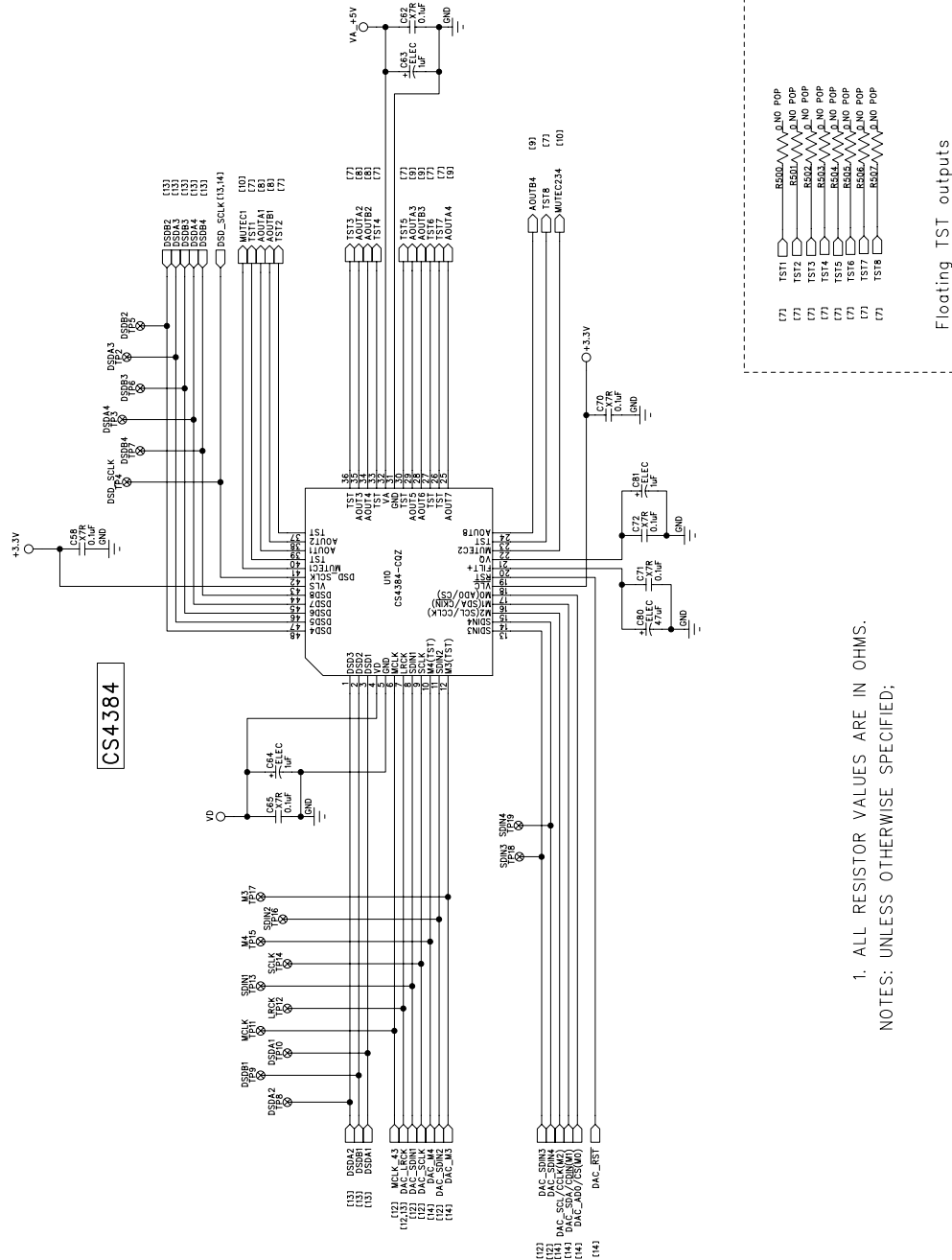
Figure 2. CS4384
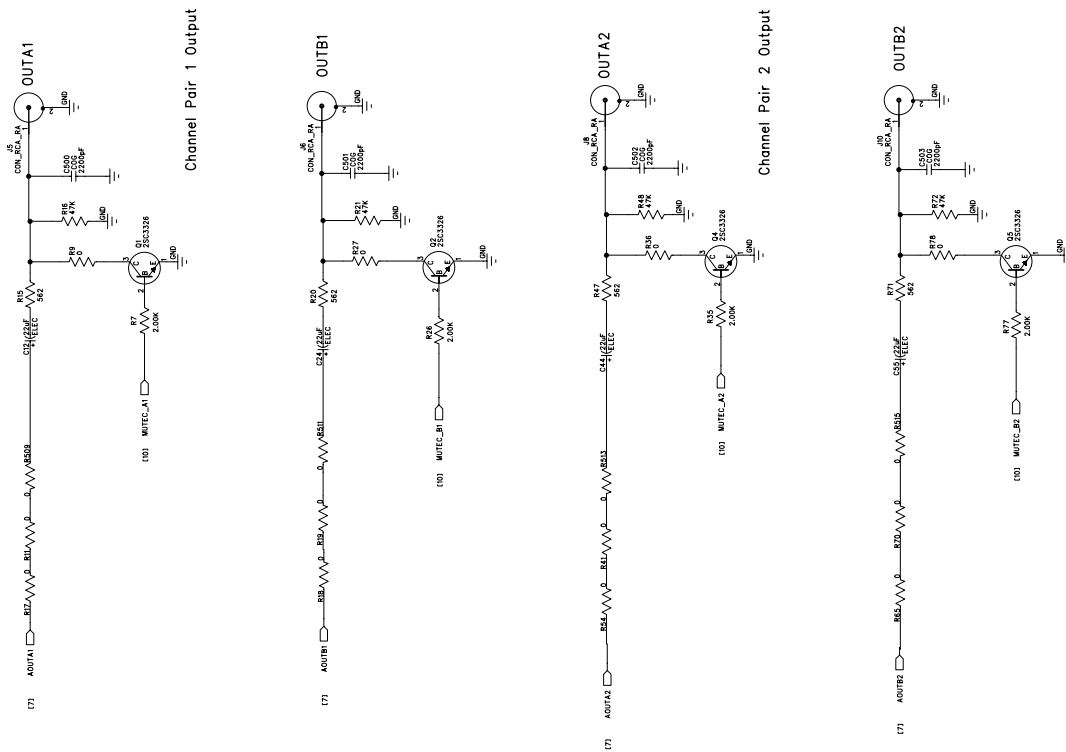
Figure 3. Analog Output Pairs 1 & 2
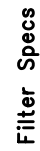
Figure 4. Analog Output Pairs 3 & 4
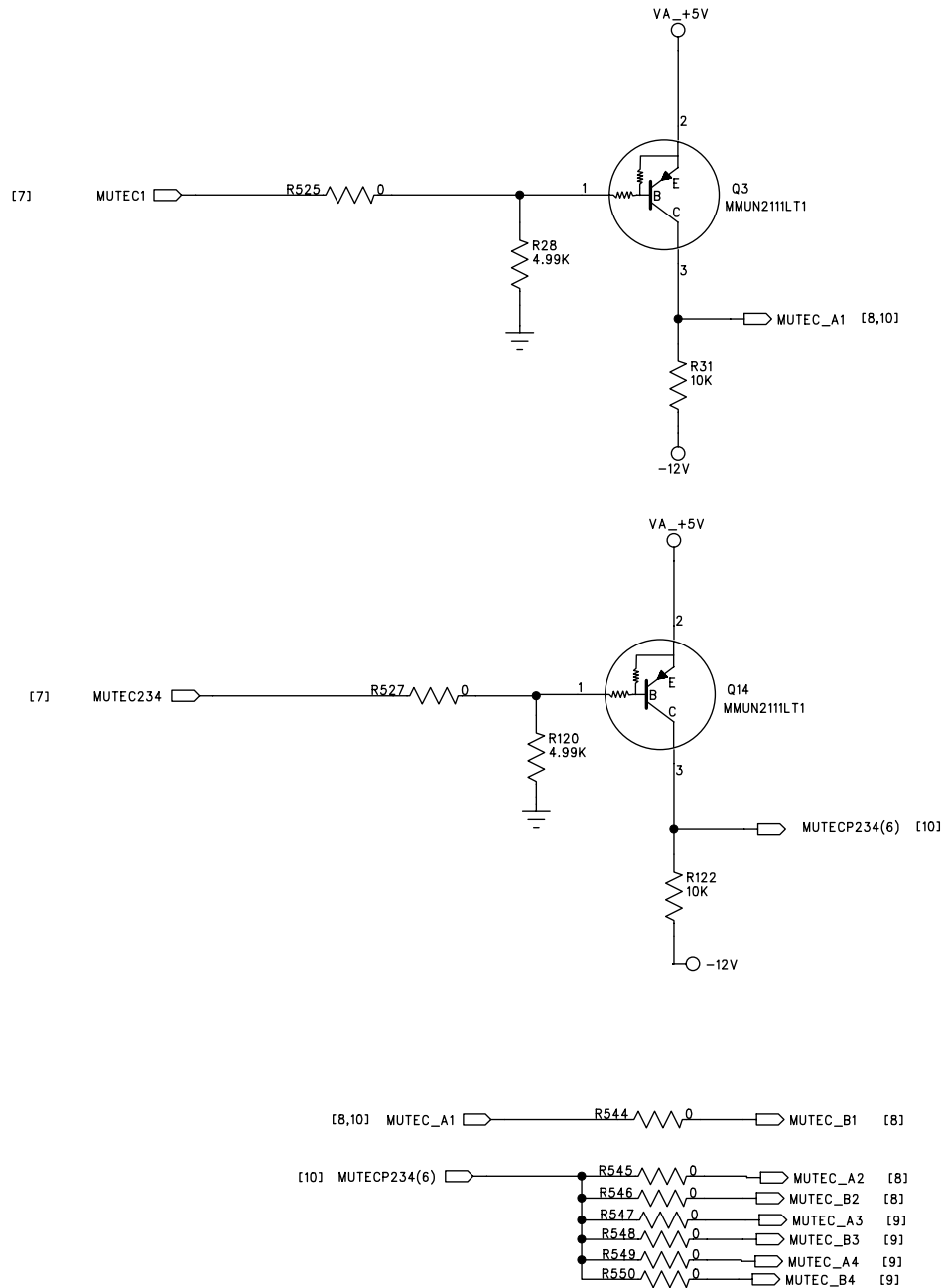
Figure 5. Mute Circuits
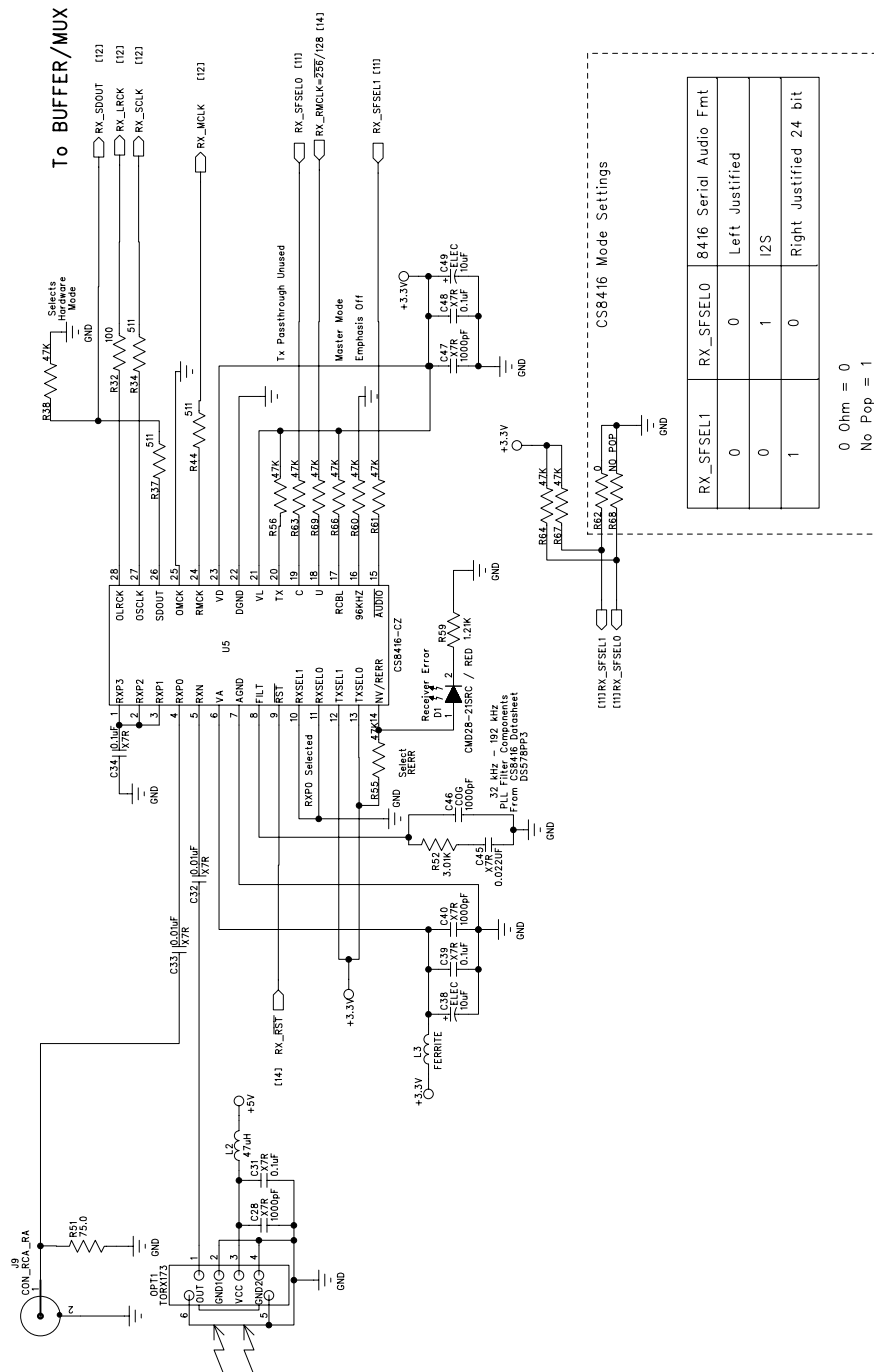
Figure 6. CS8416 S/PDIF Input
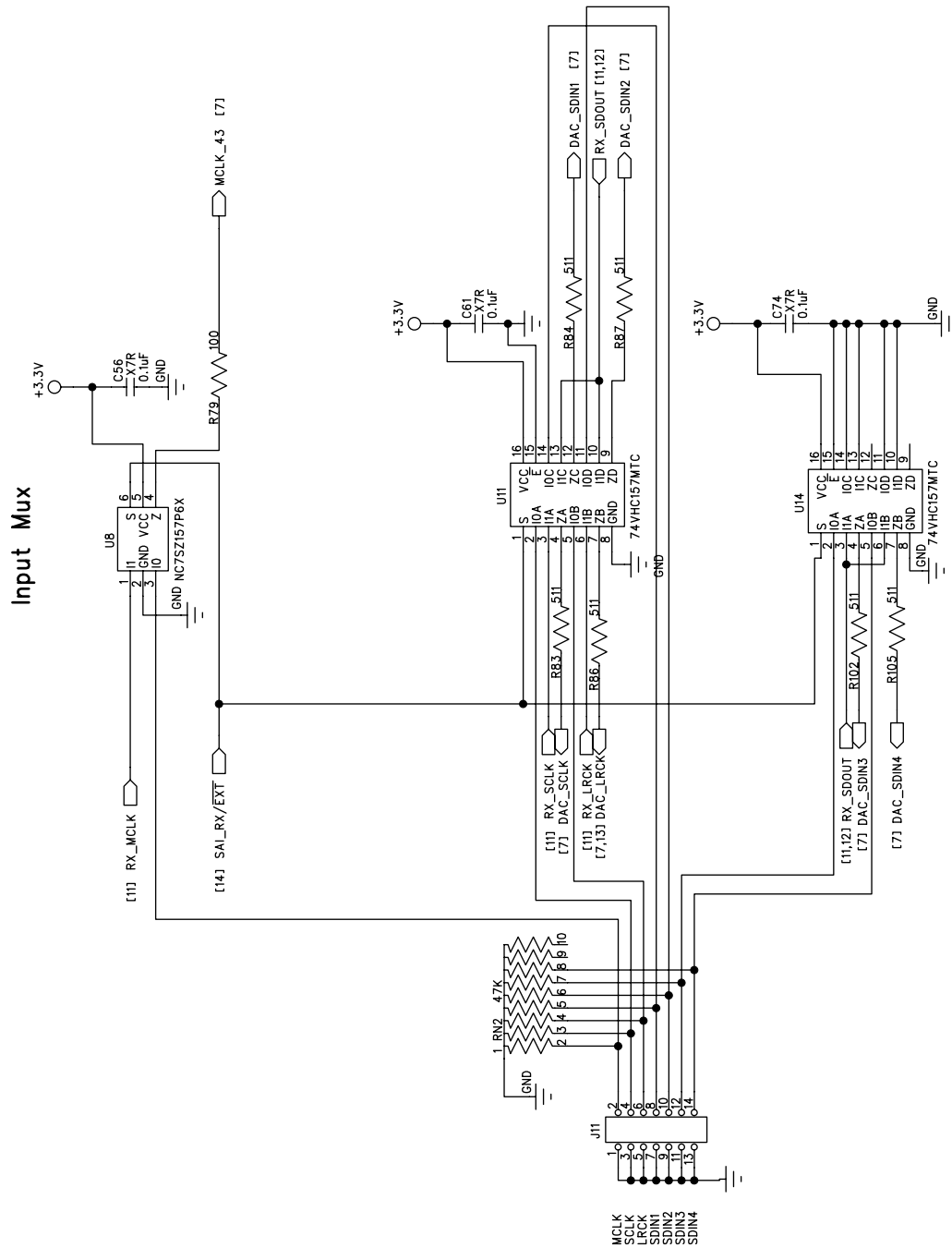
Figure 7. PCM input Header and Muxing
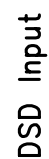
Figure 8. DSD Input Header
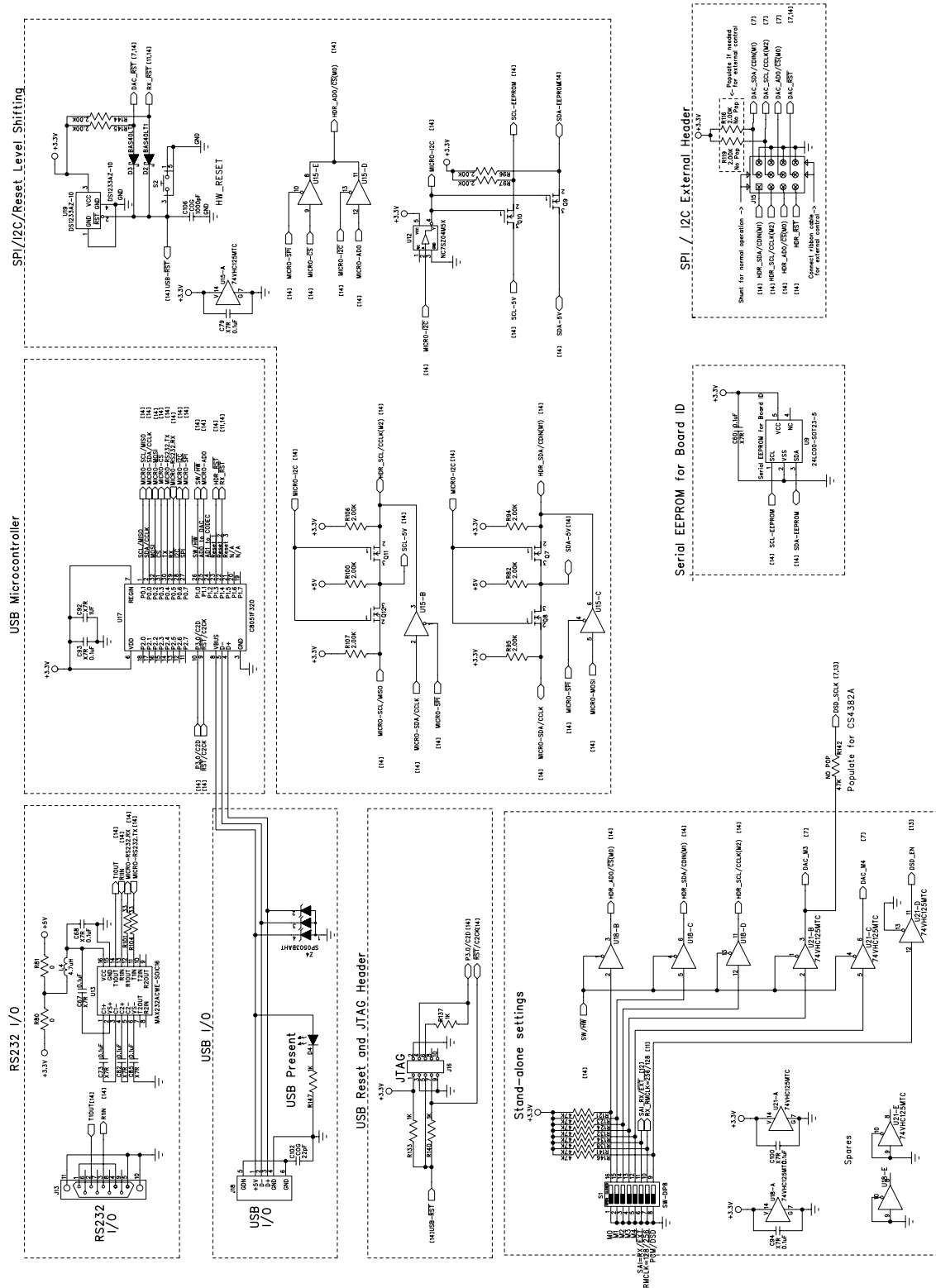
Figure 9. Control Input

Figure 10. Power Inputs

$$Vout = 1.216 * \left[1 + \frac{R2}{R1} \right]$$
$$(R1 = 10k)$$
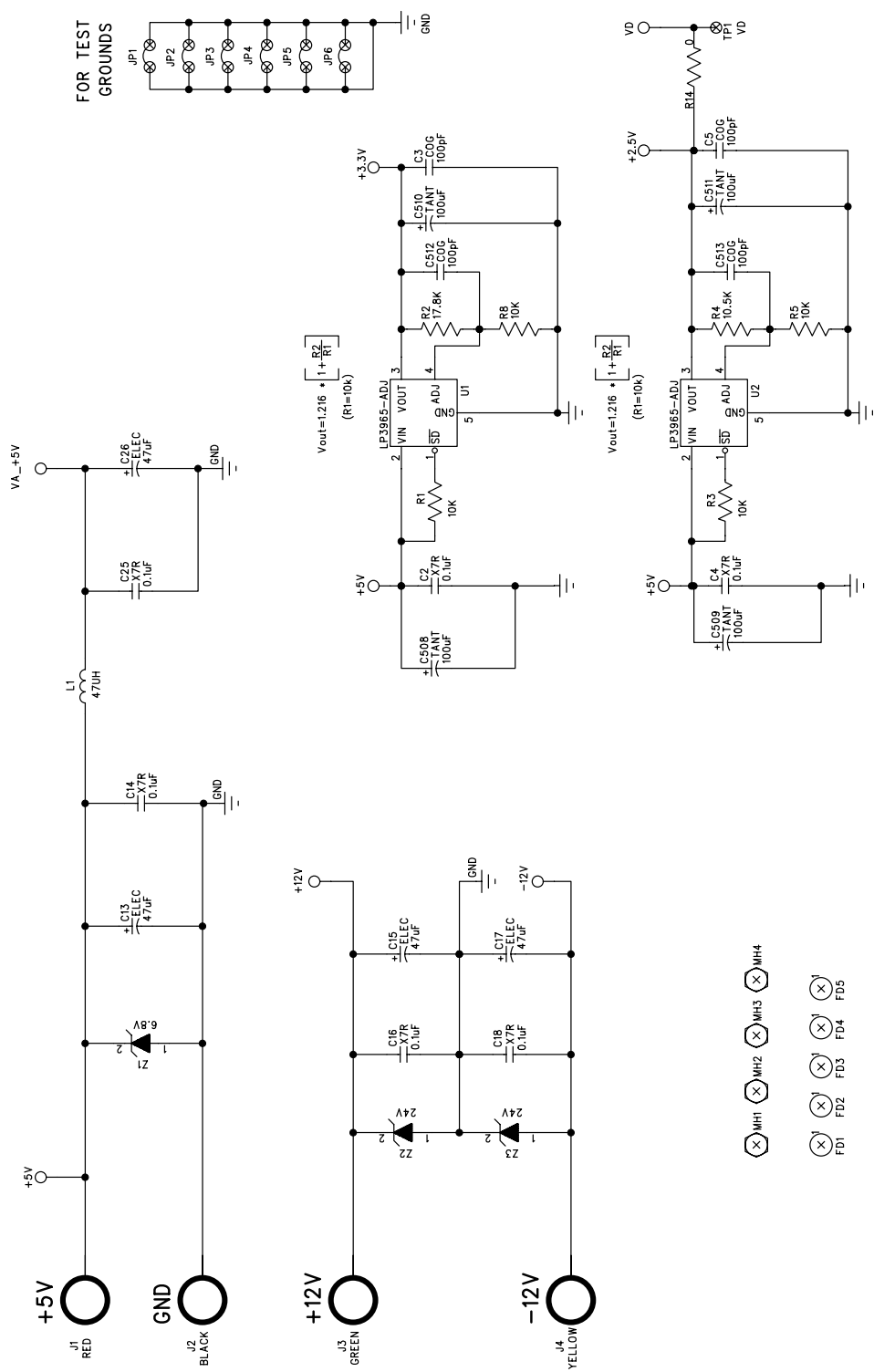
Power Supplies

Figure 11. Silkscreen Top
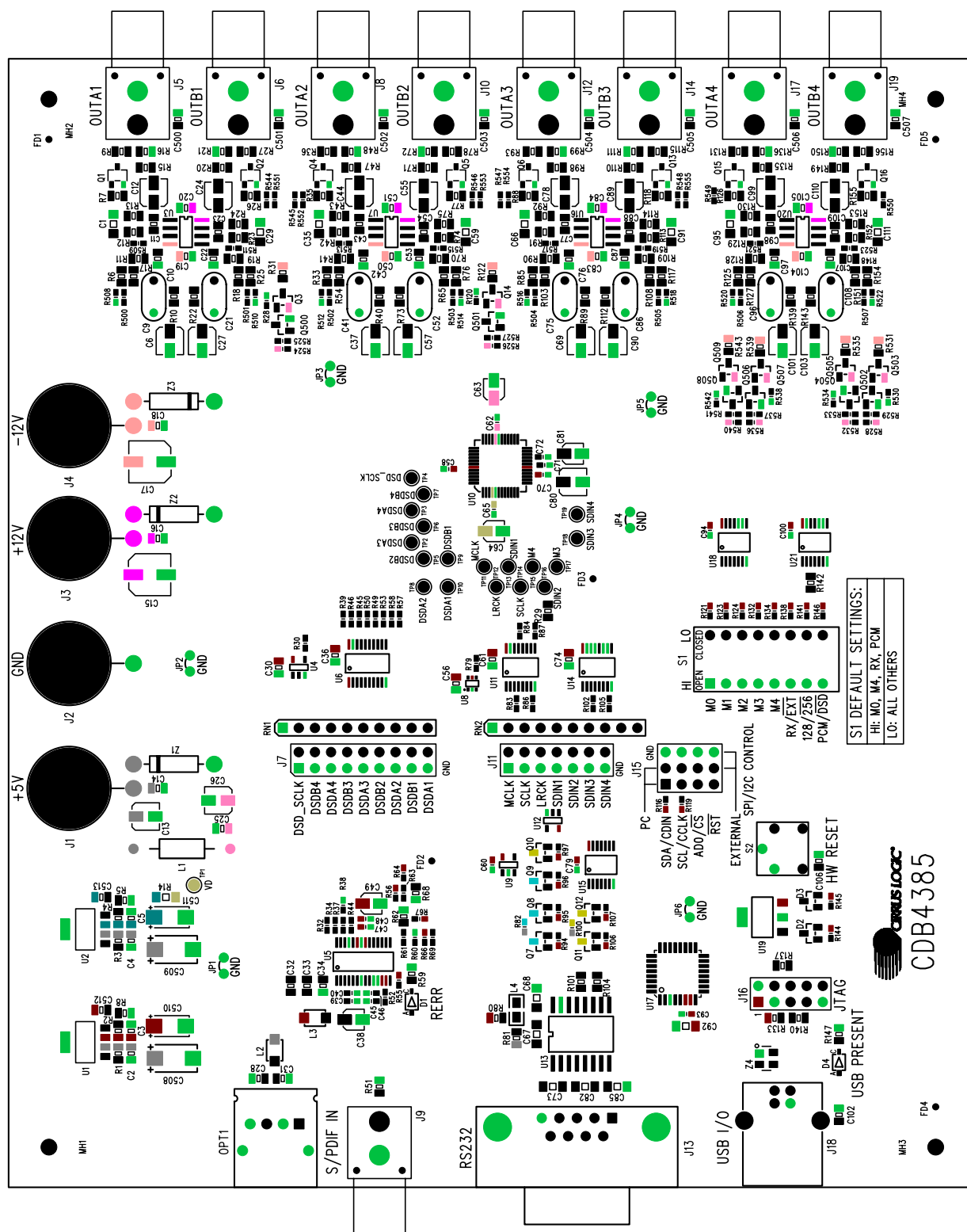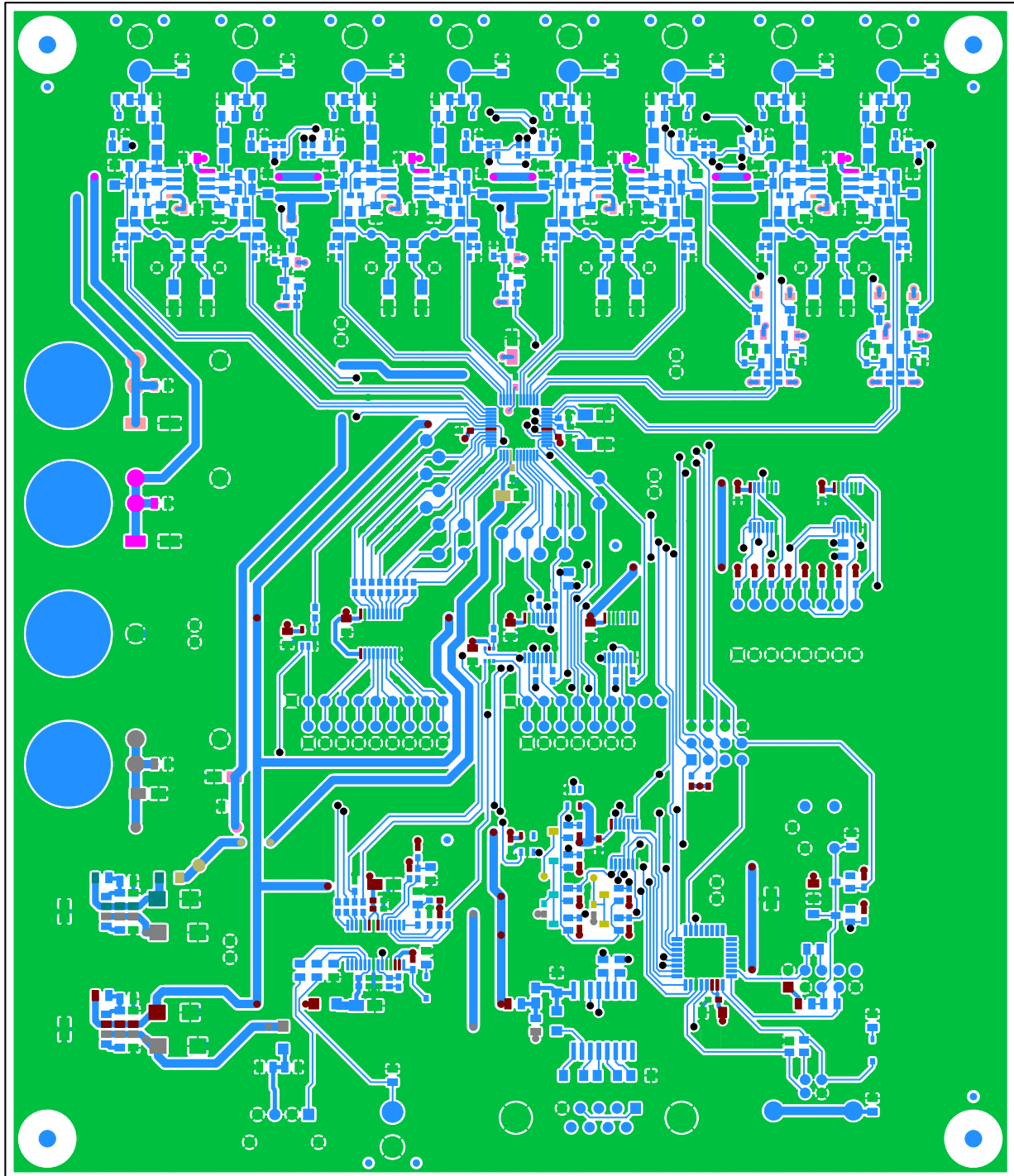
Figure 12. Top Side

CIRRUS LOGIC CDB4385 PCB 240-00123-01 Rev C

PWB 240-00123-01 Rev C
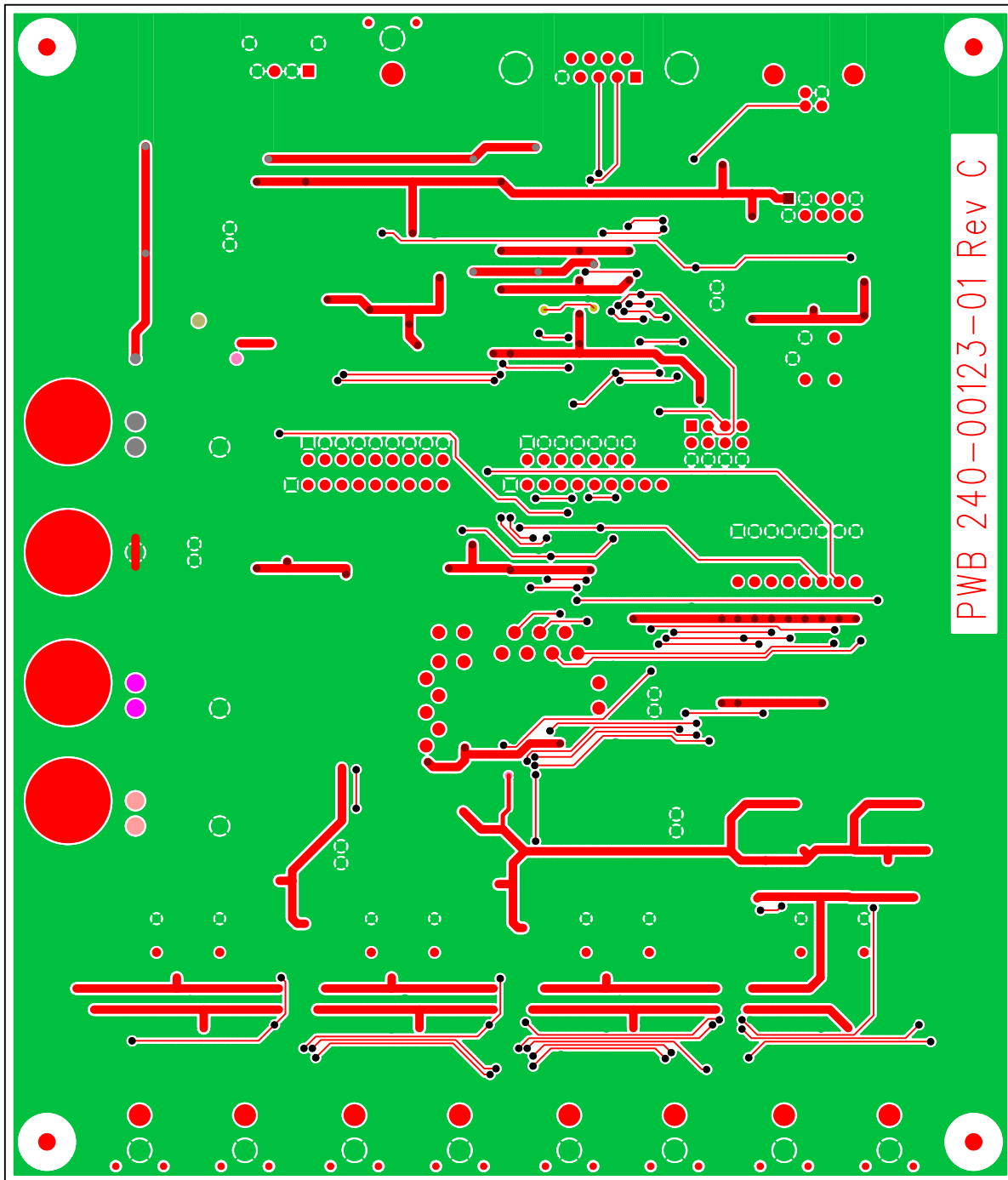
Figure 13. Bottom Side

REVISION HISTORY

Release	Date	Changes
DB1	JULY 2005	Initial Release

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For all product questions and inquiries contact a Cirrus Logic Sales Representative.

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