CY29940

2.5 V or 3.3 V, 200-MHz, 1:18 Clock Distribution Buffer

Features

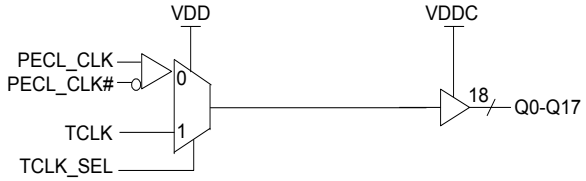
- 200-MHz clock support
- LVPECL or LVCMOS/LVTTL clock input
- LVCMOS/LVTTL compatible inputs
- 18 clock outputs: drive up to 36 clock lines
- 60 ps typical output-to-output skew
- Dual or single supply operation:
  - 3.3 V core and 3.3 V outputs
  - 3.3 V core and 2.5 V outputs
  - 2.5 V core and 2.5 V outputs
- Pin compatible with MPC940L, MPC9109
- Available in Commercial and Industrial temperature
- 32-pin TQFP package

Description

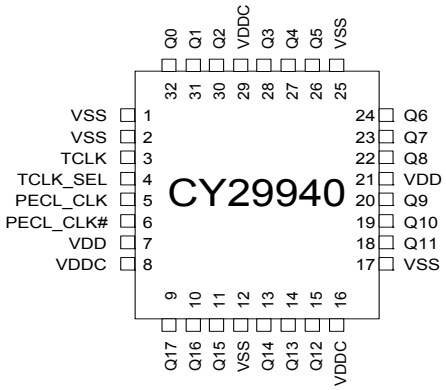
The CY29940 is a low-voltage 200-MHz clock distribution buffer with the capability to select either a differential LVPECL or a LVCMOS/LVTTL compatible input clock. The two clock sources can be used to provide for a test clock as well as the primary system clock. All other control inputs are LVCMOS/LVTTL compatible. The eighteen outputs are 2.5 V or 3.3 V LVCMOS/LVTTL compatible and can drive 50 Ω series or parallel terminated transmission lines. For series terminated transmission lines, each output can drive one or two traces giving the device an effective fanout of 1:36. Low output-to-output skews make the CY29940 an ideal clock distribution buffer for nested clock trees in the most demanding of synchronous systems.

For a complete list of related documentation, click here.

Block Diagram



Pin Configuration



Pin Description[1]

Pin	Name	PWR	I/O	Description
5	PECL_CLK		I, PU	PECL input clock
6	PECL_CLK#		I, PD	PECL input clock
3	TCLK		I, PD	External reference/test clock input
9, 10, 11, 13, 14, 15, 18, 19, 20, 22, 23, 24, 26, 27, 28, 30, 31, 32	Q(17:0)	VDDC	O	Clock outputs
4	TCLK_SEL		I, PD	Clock Select Input. When LOW, PECL clock is selected and when HIGH TCLK is selected.
8, 16, 29	VDDC			3.3 V or 2.5 V power supply for output clock buffers
7, 21	VDD			3.3 V or 2.5 V power supply
1, 2, 12, 17, 25	VSS			Common ground

Note
1. PD = Internal Pull-Down, PU = Internal Pull-up

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. User guidelines are not tested.[2]

Maximum input voltage relative to V_{SS} ..... V_{SS} – 0.3 V

Maximum input voltage relative to V_{DD} ..... V_{DD} + 0.3 V

Storage temperature ..... –65 °C to +150 °C

Operating temperature ..... –40 °C to +85 °C

Maximum ESD protection ..... 2 kV

Maximum power supply ..... 5.5 V

Maximum input current ..... ±20 mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Parameters[2]

V_{DD} = 3.3 V ± 5% or 2.5 V ± 5%, V_{DDC} = 3.3 V ± 5% or 2.5 V ± 5%, T_A = –40 °C to +85 °C

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low voltage		V_{SS}	–	0.8	V
V_{IH}	Input high voltage		2.0	–	V_{DD}	V
I_{IL}	Input low current[3]		–	–	–200	µA
I_{IH}	Input high current[3]		–	–	200	µA
V_{PP}	Peak-to-peak input voltage PECL_CLK		500	–	1000	mV
V_{CMR}	Common mode range[4] PECL_CLK	V_{DD} = 3.3 V	V_{DD} – 1.4	–	V_{DD} – 0.6	V
		V_{DD} = 2.5 V	V_{DD} – 1.0	–	V_{DD} – 0.6	V
V_{OL}	Output low voltage[5, 6, 7]	I_{OL} = 20 mA	–	–	0.5	V
V_{OH}	Output high voltage[5, 6, 7]	I_{OH} = –20 mA, V_{DDC} = 3.3 V	2.4	–	–	V
		I_{OH} = –20 mA, V_{DDC} = 2.5 V	1.8	–	–	V
I_{DDQ}	Quiescent supply current		–	5	7	mA
I_{DD}	Dynamic supply current	V_{DD} = 3.3 V, Outputs at 150 MHz, CL = 15 pF	–	285	–	mA
		V_{DD} = 3.3 V, Outputs at 200 MHz, CL = 15 pF	–	335	–	
		V_{DD} = 2.5 V, Outputs at 150 MHz, CL = 15 pF	–	200	–	
		V_{DD} = 2.5 V, Outputs at 200 MHz, CL = 15 pF	–	240	–	
Z_{out}	Output impedance	V_{DD} = 3.3 V	8	12	16	Ω
		V_{DD} = 2.5 V	10	15	20	
C_{in}	Input capacitance		–	4	–	pF

Notes

2. **Multiple Supplies:** The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is not required.
3. Inputs have pull-up/pull-down resistors that effect input current.
4. The VCMR is the difference from the most positive side of the differential input signal. Normal operation is obtained when the “High” input is within the VCMR range and the input lies within the VPP specification. Driving series or parallel terminated 50 Ω (or 50 Ω to V_{DD}/2) transmission lines
5. Outputs driving 50 Ω transmission lines.
6. See Figure 1 on page 5 and Figure 2 on page 5.
7. 50% input duty cycle.

AC Parameters[8]

V_{DD} = 3.3 V ± 5% or 2.5 V ± 5%, V_{DDC} = 3.3 V ± 5% or 2.5 V ± 5%, T_A = –40 °C to +85 °C

Parameter	Description	Conditions		Min	Typ	Max	Unit
F_{max}	Input frequency		–	–	–	200	MHz
t_{PD}	PECL_CLK to Q Delay[9, 10, 11] ≤ 150 MHz	V_{DD} = 3.3 V, 85 °C	t_{PHL}	2.0	–	3.2	ns
			t_{PLH}	2.1	–	3.4	
		V_{DD} = 3.3 V, 70 °C	t_{PHL}	1.9	–	3.1	
			t_{PLH}	2.0	–	3.2	
		V_{DD} = 2.5 V, 85 °C	t_{PHL}	2.5	–	5.2	
			t_{PLH}	2.6	–	5	
		V_{DD} = 2.5 V, 70 °C	t_{PHL}	2.5	–	5	
			t_{PLH}	2.6	–	5	
t_{PD}	LVCMOS to Q Delay[9, 10, 11] ≤ 150 MHz	V_{DD} = 3.3 V, 85 °C	t_{PHL}	1.9	–	3	ns
			t_{PLH}	2.0	–	3.2	
		V_{DD} = 3.3 V, 70 °C	t_{PHL}	1.8	–	2.9	
			t_{PLH}	1.8	–	3.1	
		V_{DD} = 2.5 V, 85 °C	t_{PHL}	2.5	–	4	
			t_{PLH}	2.5	–	4	
		V_{DD} = 2.5 V, 70 °C	t_{PHL}	2.3	–	3.8	
			t_{PLH}	2.3	–	3.8	
t_J	Total jitter	V_{DD} = 3.3 V @ 150 MHz		–	–	10	ps
FoutDC	Output duty cycle[9, 10, 12]	FCLK < 134 MHz		–	–	55	%
		FCLK > 134 MHz		–	–	60	
T_{skew}	Output-to-output skew[9, 10]	V_{DD} = 3.3 V		–	60	150	ps
		V_{DD} = 2.5 V		–	–	200	
T_{skew}(pp)	Part-to-part skew[13]	PECL, V_{DDC} = 3.3 V		–	–	1.4	ns
		PECL, V_{DDC} = 2.5 V		–	–	2.2	
T_{skew}(pp)	Part-to-part skew[13]	TCLK, V_{DDC} = 3.3 V		–	–	1.2	ns
		TCLK, V_{DDC} = 2.5 V		–	–	1.7	
T_{skew}(pp)	Part-to-part skew[14]	PECL_CLK		–	–	850	ps
		TCLK		–	–	750	
t_R/t_F	Output clocks rise/fall time[9, 10]	0.7 V to 2.0 V, V_{DDC} = 3.3 V		0.3	–	1.1	ns
		0.5 V to 1.8 V, V_{DDC} = 2.5 V		0.3	–	1.2	

Notes
8. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.
9. Outputs driving 50 Ω transmission lines.
10. See Figure 1 on page 5 and Figure 2 on page 5.
11. Parameters tested @ 150 MHz.
12. 50% input duty cycle.
13. Across temperature and voltage ranges, includes output skew.
14. For a specific temperature and voltage, includes output skew.

Figure 1. LVCMOS_CLK CY29940 Test Reference for V_{CC} = 3.3 V and V_{CC} = 2.5 V

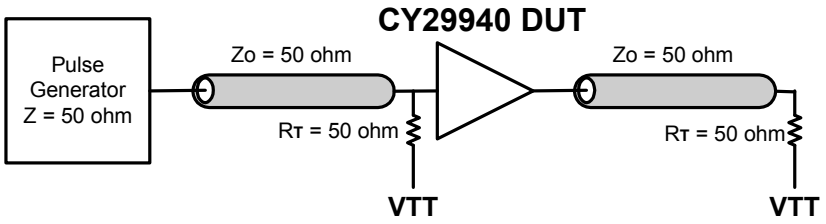


Figure 2. PECL_CLK CY29940 Test Reference for V_{CC} = 3.3 V and V_{CC} = 2.5 V

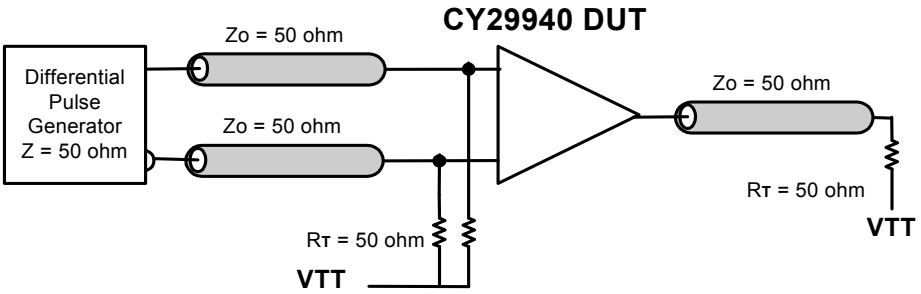


Figure 3. Propagation Delay (TPD) Test Reference

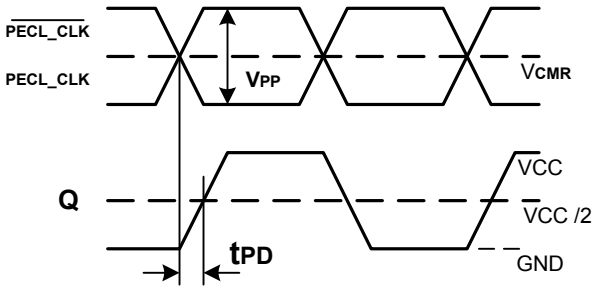


Figure 4. LVCMOS Propagation Delay (TPD) Test Reference

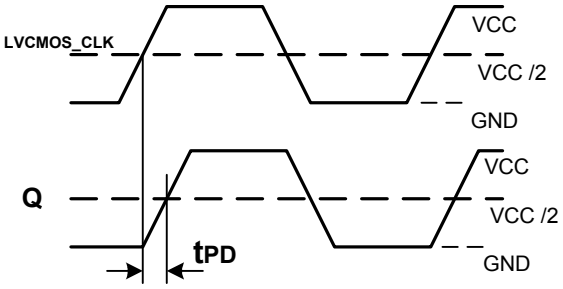


Figure 5. Output Duty Cycle (FoutDC)

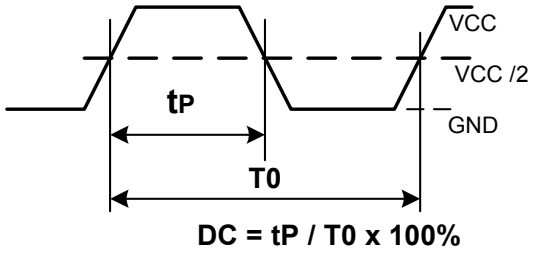
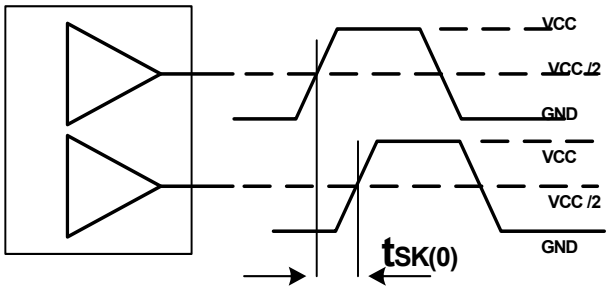


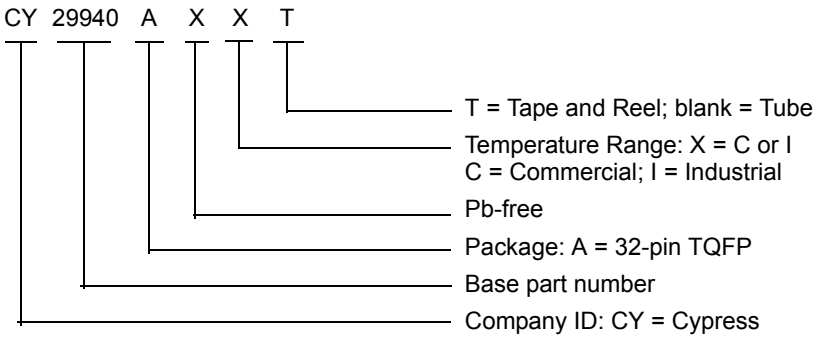
Figure 6. Output-to-Output Skew tsk(0)



Ordering Information

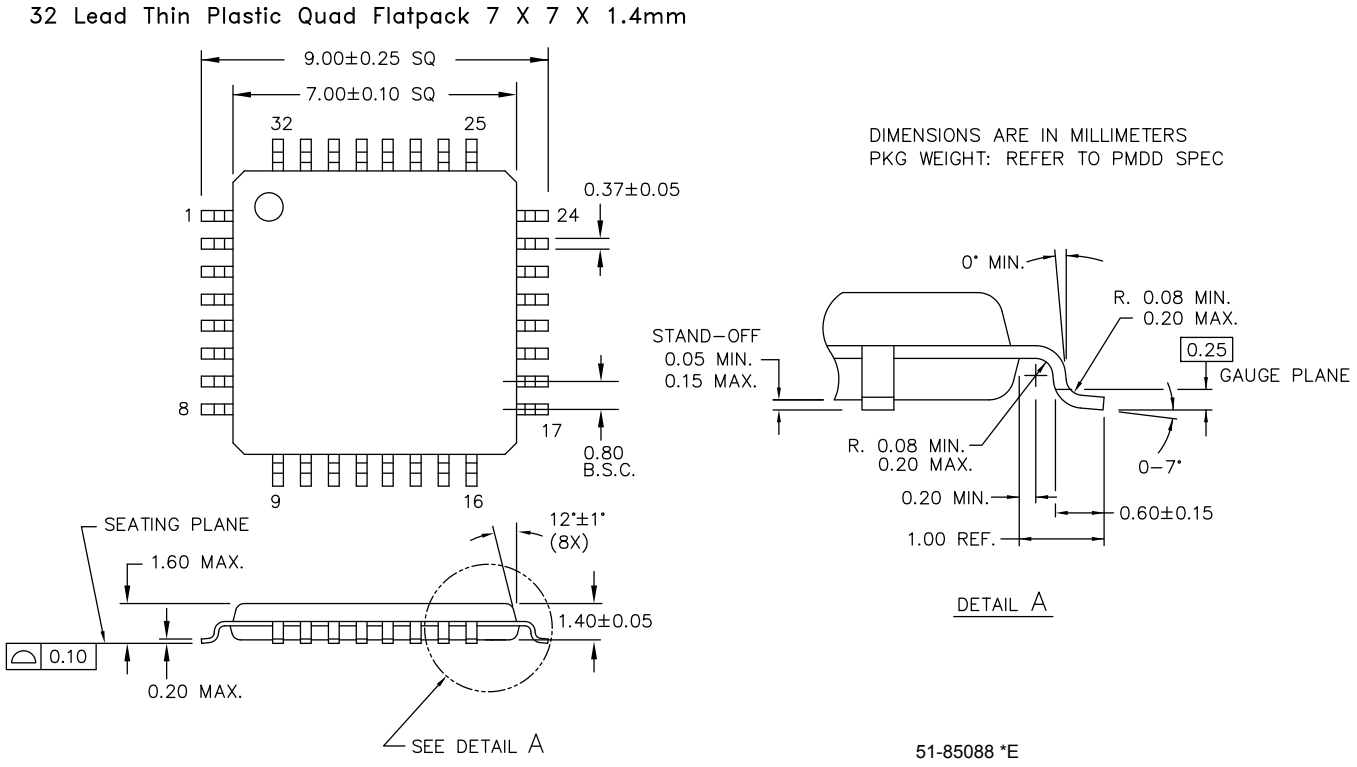
Part Number	Package Type	Production Flow
Pb-free		
CY29940AXI	32-pin TQFP	Industrial, –40 °C to +85 °C
CY29940AXIT	32-pin TQFP – Tape and Reel	Industrial, –40 °C to +85 °C
CY29940AXC	32-pin TQFP	Commercial, 0 °C to 70 °C
CY29940AXCT	32-pin TQFP – Tape and Reel	Commercial, 0 °C to 70 °C

Ordering Code Definitions



Package Drawing and Dimensions

Figure 7. 32-pin TQFP 7 × 7 × 1.4 mm A32.14



Acronyms

Acronym	Description
ESD	electrostatic discharge
I/O	input/output
TQFP	thin quad flat package
LVCMOS	low voltage complementary metal oxide semiconductor
LVPECL	low-voltage positive emitter-coupled logic
LVTTL	low-voltage transistor-transistor logic
TQFP	thin quad flat pack

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kV	kilo Volts
MHz	Mega Hertz
µA	micro Amperes
mA	milli Amperes
mm	milli meter
mV	milli Volts
ns	nano seconds
Ω	ohms
%	percent
pF	pico Farad
ps	pico seconds
V	Volts
W	Watts

Document History Page

Document Title: CY29940, 2.5 V or 3.3 V, 200-MHz, 1:18 Clock Distribution Buffer Document Number: 38-07283				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	111094	02/01/02	BRK	New data sheet
*A	116776	08/15/02	HWT	Incorporate results of final characterization using corporate methods, added output impedance on page 3 and added output duty cycle on page 4. Add commercial temperature range in the ordering information on page 6.
*B	122875	12/21/02	RBI	Add power up requirements to maximum rating information
*C	448379	See ECN	RGL	Add typical value for output-to-output skew Add Lead-free devices
*D	2899304	03/25/10	BASH/KVM	Removed inactive parts from Ordering Information. Updated package diagram.
*E	3254185	05/11/2011	CXQ	Added Ordering Code Definitions. Added Acronyms and Units of Measure. Updated in new template.
*F	3548252	03/12/2012	PURU	Changed LQFP to TQFP throughout document.
*G	4586288	12/03/2014	PURU	Added related documentation hyperlink in page 1. Updated Figure 7 in Package Drawing and Dimensions (spec 51-85088 *D to *E).

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