

## 2.5 V or 3.3 V, 200-MHz, 1:18 Clock Distribution Buffer

### Features

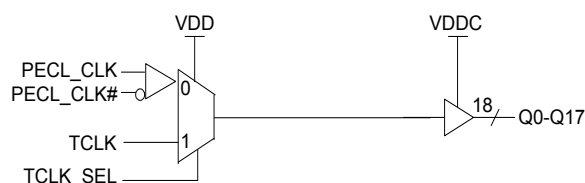
- 200-MHz clock support
- LVPECL or LVCMOS/LVTTL clock input
- LVCMOS/LVTTL compatible inputs
- 18 clock outputs: drive up to 36 clock lines
- 60 ps typical output-to-output skew
- Dual or single supply operation:
  - 3.3 V core and 3.3 V outputs
  - 3.3 V core and 2.5 V outputs
  - 2.5 V core and 2.5 V outputs
- Pin compatible with MPC940L, MPC9109
- Available in Commercial and Industrial temperature
- 32-pin TQFP package

### Description

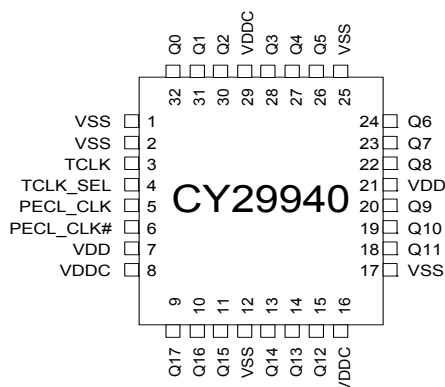
The CY29940 is a low-voltage 200-MHz clock distribution buffer with the capability to select either a differential LVPECL or a LVCMOS/LVTTL compatible input clock. The two clock sources can be used to provide for a test clock as well as the primary system clock. All other control inputs are LVCMOS/LVTTL compatible. The eighteen outputs are 2.5 V or 3.3 V LVCMOS/LVTTL compatible and can drive 50  $\Omega$  series or parallel terminated transmission lines. For series terminated transmission lines, each output can drive one or two traces giving the device an effective fanout of 1:36. Low output-to-output skews make the CY29940 an ideal clock distribution buffer for nested clock trees in the most demanding of synchronous systems.

For a complete list of related documentation, [click here](#).

### Block Diagram



### Pin Configuration



**Pin Description<sup>[1]</sup>**

Pin	Name	PWR	I/O	Description
5	PECL_CLK		I, PU	PECL input clock
6	PECL_CLK#		I, PD	PECL input clock
3	TCLK		I, PD	External reference/test clock input
9, 10, 11, 13, 14, 15, 18, 19, 20, 22, 23, 24, 26, 27, 28, 30, 31, 32	Q(17:0)	VDDC	O	Clock outputs
4	TCLK_SEL		I, PD	Clock Select Input. When LOW, PECL clock is selected and when HIGH TCLK is selected.
8, 16, 29	VDDC			3.3 V or 2.5 V power supply for output clock buffers
7, 21	VDD			3.3 V or 2.5 V power supply
1, 2, 12, 17, 25	VSS			Common ground

**Note**

1. PD = Internal Pull-Down, PU = Internal Pull-up

## Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. User guidelines are not tested.<sup>[2]</sup>

Maximum input voltage relative to  $V_{SS}$  .....  $V_{SS} - 0.3 \text{ V}$

Maximum input voltage relative to  $V_{DD}$  .....  $V_{DD} + 0.3 \text{ V}$

Storage temperature .....  $-65 \text{ }^{\circ}\text{C}$  to  $+150 \text{ }^{\circ}\text{C}$

Operating temperature .....  $-40 \text{ }^{\circ}\text{C}$  to  $+85 \text{ }^{\circ}\text{C}$

Maximum ESD protection ..... 2 kV

Maximum power supply ..... 5.5 V

Maximum input current .....  $\pm 20 \text{ mA}$

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range:

$$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$$

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{SS}$  or  $V_{DD}$ ).

## DC Parameters<sup>[2]</sup>

$V_{DD} = 3.3 \text{ V} \pm 5\%$  or  $2.5 \text{ V} \pm 5\%$ ,  $V_{DDC} = 3.3 \text{ V} \pm 5\%$  or  $2.5 \text{ V} \pm 5\%$ ,  $T_A = -40 \text{ }^{\circ}\text{C}$  to  $+85 \text{ }^{\circ}\text{C}$

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{IL}$	Input low voltage		$V_{SS}$	–	0.8	V
$V_{IH}$	Input high voltage		2.0	–	$V_{DD}$	V
$I_{IL}$	Input low current <sup>[3]</sup>		–	–	–200	$\mu\text{A}$
$I_{IH}$	Input high current <sup>[3]</sup>		–	–	200	$\mu\text{A}$
$V_{PP}$	Peak-to-peak input voltage PECL_CLK		500	–	1000	mV
$V_{CMR}$	Common mode range <sup>[4]</sup> PECL_CLK	$V_{DD} = 3.3 \text{ V}$	$V_{DD} - 1.4$	–	$V_{DD} - 0.6$	V
		$V_{DD} = 2.5 \text{ V}$	$V_{DD} - 1.0$	–	$V_{DD} - 0.6$	V
$V_{OL}$	Output low voltage <sup>[5, 6, 7]</sup>	$I_{OL} = 20 \text{ mA}$	–	–	0.5	V
$V_{OH}$	Output high voltage <sup>[5, 6, 7]</sup>	$I_{OH} = -20 \text{ mA}$ , $V_{DDC} = 3.3 \text{ V}$	2.4	–	–	V
		$I_{OH} = -20 \text{ mA}$ , $V_{DDC} = 2.5 \text{ V}$	1.8	–	–	V
$I_{DDQ}$	Quiescent supply current		–	5	7	mA
$I_{DD}$	Dynamic supply current	$V_{DD} = 3.3 \text{ V}$ , Outputs at 150 MHz, CL = 15 pF	–	285	–	mA
		$V_{DD} = 3.3 \text{ V}$ , Outputs at 200 MHz, CL = 15 pF	–	335	–	
		$V_{DD} = 2.5 \text{ V}$ , Outputs at 150 MHz, CL = 15 pF	–	200	–	
		$V_{DD} = 2.5 \text{ V}$ , Outputs at 200 MHz, CL = 15 pF	–	240	–	
$Z_{out}$	Output impedance	$V_{DD} = 3.3 \text{ V}$	8	12	16	$\Omega$
		$V_{DD} = 2.5 \text{ V}$	10	15	20	
$C_{in}$	Input capacitance		–	4	–	pF

### Notes

- Multiple Supplies:** The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is not required.
- Inputs have pull-up/pull-down resistors that effect input current.
- The VCMR is the difference from the most positive side of the differential input signal. Normal operation is obtained when the "High" input is within the VCMR range and the input lies within the VPP specification. Driving series or parallel terminated 50  $\Omega$  (or 50  $\Omega$  to  $V_{DD}/2$ ) transmission lines
- Outputs driving 50  $\Omega$  transmission lines.
- See Figure 1 on page 5 and Figure 2 on page 5.
- 50% input duty cycle.

## AC Parameters<sup>[8]</sup>

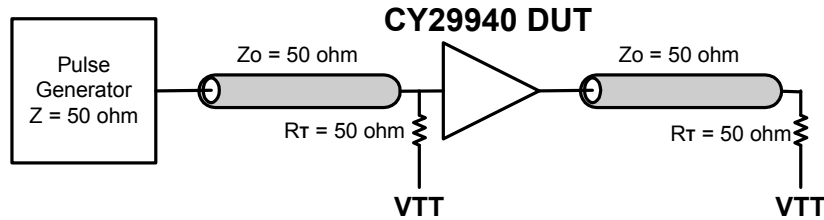
$V_{DD} = 3.3 \text{ V} \pm 5\%$  or  $2.5 \text{ V} \pm 5\%$ ,  $V_{DDC} = 3.3 \text{ V} \pm 5\%$  or  $2.5 \text{ V} \pm 5\%$ ,  $T_A = -40 \text{ }^{\circ}\text{C}$  to  $+85 \text{ }^{\circ}\text{C}$

Parameter	Description	Conditions		Min	Typ	Max	Unit
F <sub>max</sub>	Input frequency		–	–	–	200	MHz
t <sub>PD</sub>	PECL_CLK to Q Delay <sup>[9, 10, 11]</sup> ≤ 150 MHz	V <sub>DD</sub> = 3.3 V, 85 °C	t <sub>PHL</sub>	2.0	–	3.2	ns
			t <sub>PLH</sub>	2.1	–	3.4	
		V <sub>DD</sub> = 3.3 V, 70 °C	t <sub>PHL</sub>	1.9	–	3.1	
			t <sub>PLH</sub>	2.0	–	3.2	
		V <sub>DD</sub> = 2.5 V, 85 °C	t <sub>PHL</sub>	2.5	–	5.2	
			t <sub>PLH</sub>	2.6	–	5	
		V <sub>DD</sub> = 2.5 V, 70 °C	t <sub>PHL</sub>	2.5	–	5	
			t <sub>PLH</sub>	2.6	–	5	
t <sub>PD</sub>	LVCMOS to Q Delay <sup>[9, 10, 11]</sup> ≤ 150 MHz	V <sub>DD</sub> = 3.3 V, 85 °C	t <sub>PHL</sub>	1.9	–	3	ns
			t <sub>PLH</sub>	2.0	–	3.2	
		V <sub>DD</sub> = 3.3 V, 70 °C	t <sub>PHL</sub>	1.8	–	2.9	
			t <sub>PLH</sub>	1.8	–	3.1	
		V <sub>DD</sub> = 2.5 V, 85 °C	t <sub>PHL</sub>	2.5	–	4	
			t <sub>PLH</sub>	2.5	–	4	
		V <sub>DD</sub> = 2.5 V, 70 °C	t <sub>PHL</sub>	2.3	–	3.8	
			t <sub>PLH</sub>	2.3	–	3.8	
t <sub>J</sub>	Total jitter	V <sub>DD</sub> = 3.3 V @ 150 MHz		–	–	10	ps
F <sub>outDC</sub>	Output duty cycle <sup>[9, 10, 12]</sup>	FCLK < 134 MHz		–	–	55	%
		FCLK > 134 MHz		–	–	60	
T <sub>skew</sub>	Output-to-output skew <sup>[9, 10]</sup>	V <sub>DD</sub> = 3.3 V		–	60	150	ps
		V <sub>DD</sub> = 2.5 V		–	–	200	
T <sub>skew</sub> (pp)	Part-to-part skew <sup>[13]</sup>	PECL, V <sub>D</sub> DC = 3.3 V		–	–	1.4	ns
		PECL, V <sub>D</sub> DC = 2.5 V		–	–	2.2	
T <sub>skew</sub> (pp)	Part-to-part skew <sup>[13]</sup>	TCLK, V <sub>D</sub> DC = 3.3 V		–	–	1.2	ns
		TCLK, V <sub>D</sub> DC = 2.5 V		–	–	1.7	
T <sub>skew</sub> (pp)	Part-to-part skew <sup>[14]</sup>	PECL_CLK		–	–	850	ps
		TCLK		–	–	750	
t <sub>R</sub> /t <sub>F</sub>	Output clocks rise/fall time <sup>[9, 10]</sup>	0.7 V to 2.0 V, V <sub>D</sub> DC = 3.3 V		0.3	–	1.1	ns
		0.5 V to 1.8 V, V <sub>D</sub> DC = 2.5 V		0.3	–	1.2	

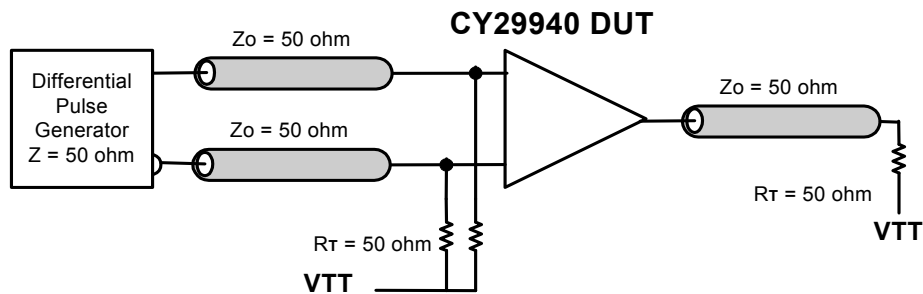
### Notes

8. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.
9. Outputs driving  $50 \Omega$  transmission lines.
10. See [Figure 1 on page 5](#) and [Figure 2 on page 5](#).
11. Parameters tested @ 150 MHz.
12. 50% input duty cycle.
13. Across temperature and voltage ranges, includes output skew.
14. For a specific temperature and voltage, includes output skew.

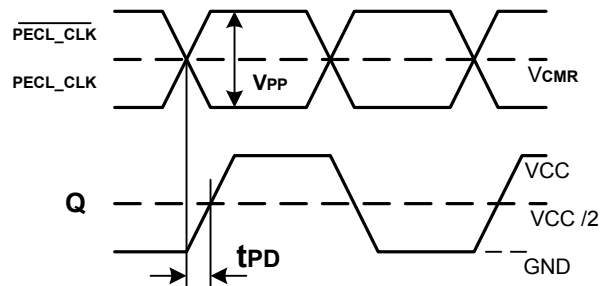
**Figure 1. LVCMOS\_CLK CY29940 Test Reference for  $V_{CC} = 3.3\text{ V}$  and  $V_{CC} = 2.5\text{ V}$**



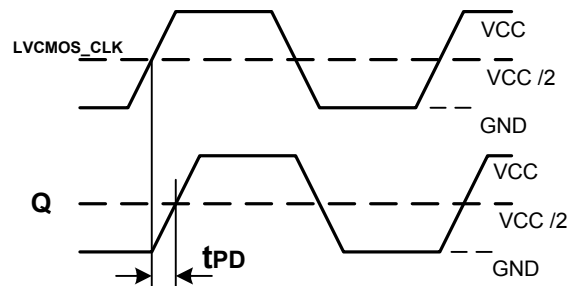
**Figure 2. PECL\_CLK CY29940 Test Reference for  $V_{CC} = 3.3\text{ V}$  and  $V_{CC} = 2.5\text{ V}$**



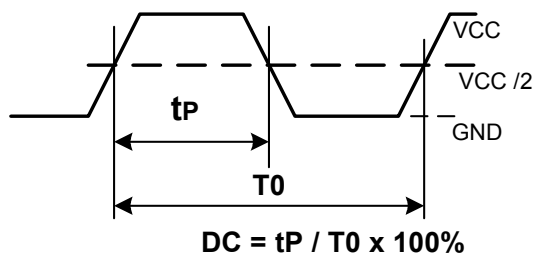
**Figure 3. Propagation Delay (TPD) Test Reference**



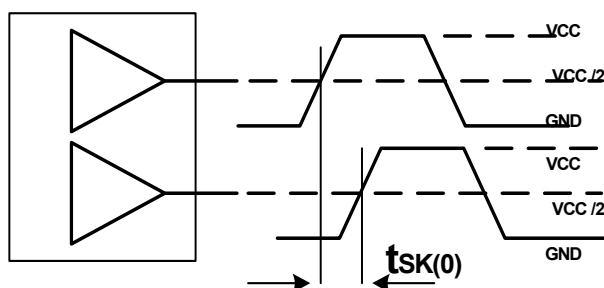
**Figure 4. LVCMOS Propagation Delay (TPD) Test Reference**



**Figure 5. Output Duty Cycle (FoutDC)**



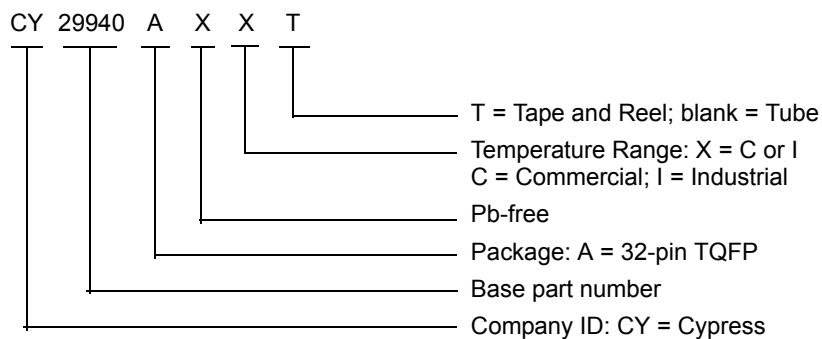
**Figure 6. Output-to-Output Skew tsk(0)**



## Ordering Information

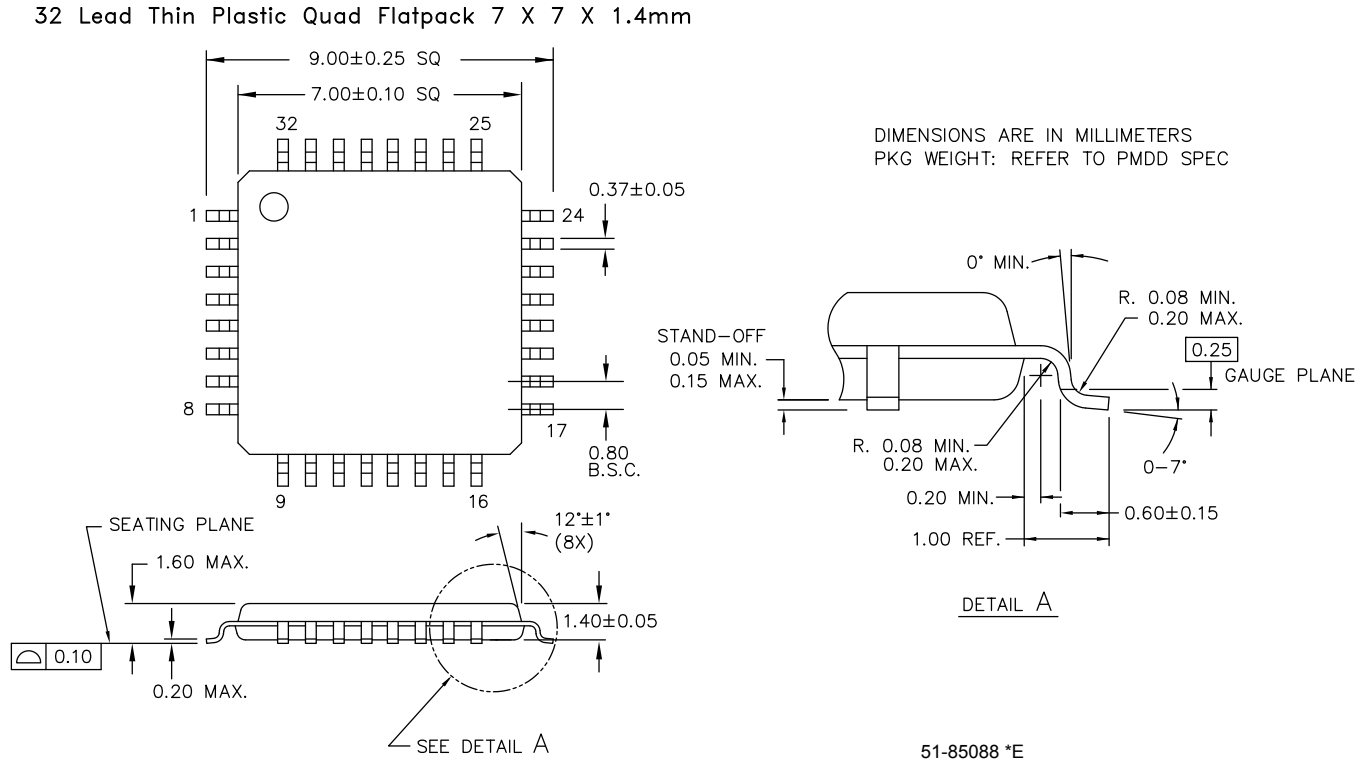
Part Number	Package Type	Production Flow
<b>Pb-free</b>		
CY29940AXI	32-pin TQFP	Industrial, -40 °C to +85 °C
CY29940AXIT	32-pin TQFP – Tape and Reel	Industrial, -40 °C to +85 °C
CY29940AXC	32-pin TQFP	Commercial, 0 °C to 70 °C
CY29940AXCT	32-pin TQFP – Tape and Reel	Commercial, 0 °C to 70 °C

## Ordering Code Definitions



## Package Drawing and Dimensions

**Figure 7. 32-pin TQFP 7 × 7 × 1.4 mm A32.14**



## Acronyms

Acronym	Description
ESD	electrostatic discharge
I/O	input/output
TQFP	thin quad flat package
LVC MOS	low voltage complementary metal oxide semiconductor
LVPECL	low-voltage positive emitter-coupled logic
LVTTTL	low-voltage transistor-transistor logic
TQFP	thin quad flat pack

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kV	kilo Volts
MHz	Mega Hertz
μA	micro Amperes
mA	milli Amperes
mm	milli meter
mV	milli Volts
ns	nano seconds
Ω	ohms
%	percent
pF	pico Farad
ps	pico seconds
V	Volts
W	Watts



## Document History Page

Document Title: CY29940, 2.5 V or 3.3 V, 200-MHz, 1:18 Clock Distribution Buffer Document Number: 38-07283				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	111094	02/01/02	BRK	New data sheet
*A	116776	08/15/02	HWT	Incorporate results of final characterization using corporate methods, added output impedance on page 3 and added output duty cycle on page 4. Add commercial temperature range in the ordering information on page 6.
*B	122875	12/21/02	RBI	Add power up requirements to maximum rating information
*C	448379	See ECN	RGL	Add typical value for output-to-output skew Add Lead-free devices
*D	2899304	03/25/10	BASH/KVM	Removed inactive parts from Ordering Information. Updated package diagram.
*E	3254185	05/11/2011	CXQ	Added <a href="#">Ordering Code Definitions</a> . Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> . Updated in new template.
*F	3548252	03/12/2012	PURU	Changed LQFP to TQFP throughout document.
*G	4586288	12/03/2014	PURU	Added related documentation hyperlink in page 1. Updated <a href="#">Figure 7</a> in <a href="#">Package Drawing and Dimensions</a> (spec 51-85088 *D to *E).

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

### Products

Automotive	<a href="http://cypress.com/go/automotive">cypress.com/go/automotive</a>
Clocks & Buffers	<a href="http://cypress.com/go/clocks">cypress.com/go/clocks</a>
Interface	<a href="http://cypress.com/go/interface">cypress.com/go/interface</a>
Lighting & Power Control	<a href="http://cypress.com/go/powerpsoc">cypress.com/go/powerpsoc</a> <a href="http://cypress.com/go/plc">cypress.com/go/plc</a>
Memory	<a href="http://cypress.com/go/memory">cypress.com/go/memory</a>
Optical & Image Sensing	<a href="http://cypress.com/go/image">cypress.com/go/image</a>
PSoC	<a href="http://cypress.com/go/psoc">cypress.com/go/psoc</a>
Touch Sensing	<a href="http://cypress.com/go/touch">cypress.com/go/touch</a>
USB Controllers	<a href="http://cypress.com/go/USB">cypress.com/go/USB</a>
Wireless/RF	<a href="http://cypress.com/go/wireless">cypress.com/go/wireless</a>

### PSoC Solutions

[psoc.cypress.com/solutions](http://psoc.cypress.com/solutions)

PSoC 1 | PSoC 3 | PSoC 5

© Cypress Semiconductor Corporation, 2002-2014. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.

# AMEYA360

Components Supply Platform

Authorized Distribution Brand :



Website :

Welcome to visit [www.ameya360.com](http://www.ameya360.com)

Contact Us :

➤ Address :

401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd  
Minhang District, Shanghai , China

➤ Sales :

Direct     +86 (21) 6401-6692  
  
Email       amall@ameya360.com  
  
QQ          800077892  
  
Skype       ameyasales1 ameyasales2

➤ Customer Service :

Email       service@ameya360.com

➤ Partnership :

Tel          +86 (21) 64016692-8333  
  
Email       mkt@ameya360.com