

# MC14067B

## Analog Multiplexers / Demultiplexers

The MC14067 multiplexer/demultiplexer is a digitally controlled analog switch featuring low ON resistance and very low leakage current. This device can be used in either digital or analog applications.

The MC14067 is a 16-channel multiplexer/demultiplexer with an inhibit and four binary control inputs A, B, C, and D. These control inputs select 1-of-16 channels by turning ON the appropriate analog switch (see MC14067 truth table.)

### Features

- Low OFF Leakage Current
- Matched Channel Resistance
- Low Quiescent Power Consumption
- Low Crosstalk Between Channels
- Wide Operating Voltage Range: 3 to 18 V
- Low Noise
- Pin for Pin Replacement for CD4067B
- These Devices are Pb-Free and are RoHS Compliant
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ )

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	- 0.5 to + 18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	- 0.5 to $V_{DD} + 0.5$	V
$I_{in}$	Input Current (DC or Transient), per Control Pin	$\pm 10$	mA
$I_{sw}$	Switch Through Current	$\pm 25$	mA
$P_D$	Power Dissipation, per Package (Note 1)	500	mW
$T_A$	Ambient Temperature Range	- 55 to + 125	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	- 65 to + 150	$^{\circ}C$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}C$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

#### 1. Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}C$  From 65 $^{\circ}C$  To 125 $^{\circ}C$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



ON Semiconductor®

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SOIC-24  
DW SUFFIX  
CASE 751E

### MARKING DIAGRAM



A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

### ORDERING INFORMATION

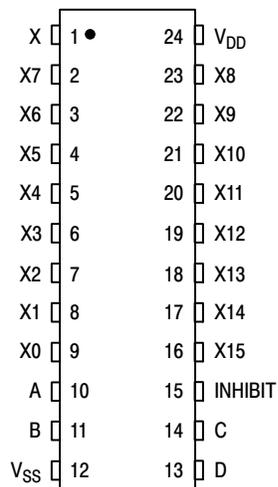
See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

# MC14067B

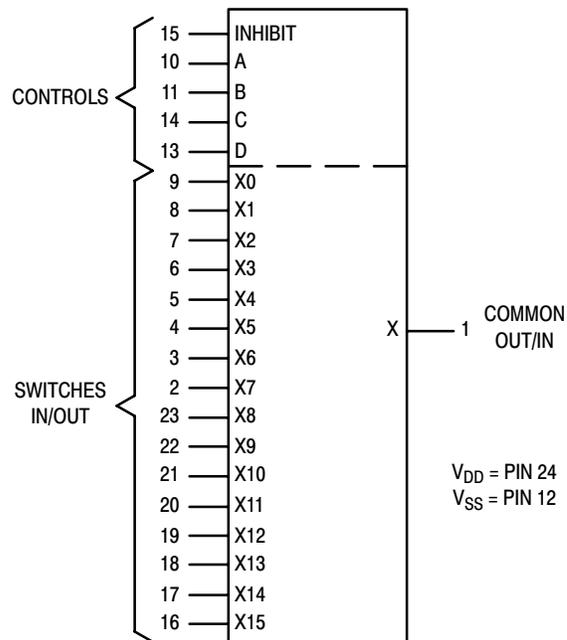
## TRUTH TABLE

Control Inputs					Selected Channel
A	B	C	D	Inh	
X	X	X	X	1	None
0	0	0	0	0	X0
1	0	0	0	0	X1
0	1	0	0	0	X2
1	1	0	0	0	X3
0	0	1	0	0	X4
1	0	1	0	0	X5
0	1	1	0	0	X6
1	1	1	0	0	X7
0	0	0	1	0	X8
1	0	0	1	0	X9
0	1	0	1	0	X10
1	1	0	1	0	X11
0	0	1	1	0	X12
1	0	1	1	0	X13
0	1	1	1	0	X14
1	1	1	1	0	X15

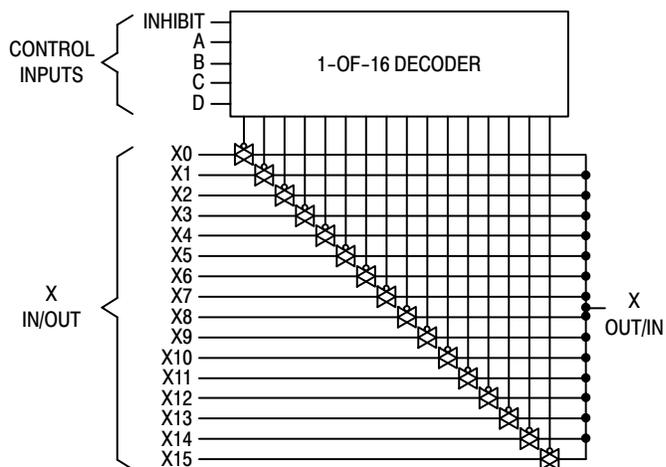
## PIN ASSIGNMENT



## 16-Channel Analog Multiplexer/Demultiplexer



## FUNCTIONAL DIAGRAM



# MC14067B

## ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V <sub>DD</sub>	Test Conditions	- 55°C		25°C			125°C		Unit
				Min	Max	Min	Typ <sup>(2)</sup>	Max	Min	Max	

### SUPPLY REQUIREMENTS (Voltages Referenced to V<sub>SS</sub>)

Power Supply Voltage Range	V <sub>DD</sub>	-		3.0	18	3.0	-	18	3.0	18	V
Quiescent Current Per Package	I <sub>DD</sub>	5.0	Control Inputs: V <sub>in</sub> = V <sub>SS</sub> or V <sub>DD</sub> , Switch I/O: V <sub>SS</sub> ≤ V <sub>I/O</sub> ≤ V <sub>DD</sub> , and ΔV <sub>switch</sub> ≤ 500 mV <sup>(3)</sup>	-	5.0	-	0.005	5.0	-	150	μA
		10		-	10	-	0.010	10	-	300	
		15		-	20	-	0.015	20	-	600	
Total Supply Current (Dynamic Plus Quiescent, Per Package)	I <sub>D(AV)</sub>	5.0 10 15	T <sub>A</sub> = 25°C only (The channel component, (V <sub>in</sub> - V <sub>out</sub> )/R <sub>on</sub> , is not included.)	Typical (0.07 μA/kHz) f + I <sub>DD</sub> (0.20 μA/kHz) f + I <sub>DD</sub> (0.36 μA/kHz) f + I <sub>DD</sub>						μA	

### CONTROL INPUTS — INHIBIT, A, B, C, D (Voltages Referenced to V<sub>SS</sub>)

Low-Level Input Voltage	V <sub>IL</sub>	5.0	R <sub>on</sub> = per spec, I <sub>off</sub> = per spec	-	1.5	-	2.25	1.5	-	1.5	V
		10		-	3.0	-	4.50	3.0	-	3.0	
		15		-	4.0	-	6.75	4.0	-	4.0	
High-Level Input Voltage	V <sub>IH</sub>	5.0	R <sub>on</sub> = per spec, I <sub>off</sub> = per spec	3.5	-	3.5	2.75	-	3.5	-	V
		10		7.0	-	7.0	5.50	-	7.0	-	
		15		11	-	11	8.25	-	11	-	
Input Leakage Current	I <sub>in</sub>	15	V <sub>in</sub> = 0 or V <sub>DD</sub>	-	±0.1	-	±0.00001	±0.1	-	1.0	μA
Input Capacitance	C <sub>in</sub>	—		-	-	-	5.0	7.5	-	-	pF

### SWITCHES IN/OUT AND COMMONS OUT/IN — X, Y (Voltages Referenced to V<sub>SS</sub>)

Recommended Peak-to-Peak Voltage Into or Out of the Switch	V <sub>I/O</sub>	-	Channel On or Off	0	V <sub>DD</sub>	0	-	V <sub>DD</sub>	0	V <sub>DD</sub>	V <sub>p-p</sub>
Recommended Static or Dynamic Voltage Across the Switch <sup>(3)</sup> (Figure 1)	ΔV <sub>switch</sub>	-	Channel On	0	600	0	-	600	0	300	mV
Output Offset Voltage	V <sub>OO</sub>	-	V <sub>in</sub> = 0 V, No Load	-	-	-	10	-	-	-	μV
ON Resistance	R <sub>on</sub>	5.0	ΔV <sub>switch</sub> ≤ 500 mV <sup>(3)</sup> , V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> (Control), and V <sub>in</sub> 0 to V <sub>DD</sub> (Switch)	-	800	-	250	1050	-	1300	Ω
		10		-	400	-	120	500	-	550	
		15		-	220	-	80	280	-	320	
ΔON Resistance Between Any Two Channels in the Same Package	ΔR <sub>on</sub>	5.0		-	70	-	25	70	-	135	Ω
		10		-	50	-	10	50	-	95	
		15		-	45	-	10	45	-	65	
Off-Channel Leakage Current (Figure 2)	I <sub>off</sub>	15	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> (Control) Channel to Channel or Any One Channel	-	±100	-	±0.05	±100	-	±1000	nA
Capacitance, Switch I/O	C <sub>I/O</sub>	-	Inhibit = V <sub>DD</sub>	-	—	—	10	-	-	-	pF
Capacitance, Common O/I	C <sub>O/I</sub>	-	Inhibit = V <sub>DD</sub> (MC14067B) (MC14097B)	-	-	-	100	-	-	-	pF
				-	-	-	60	-	-	-	
Capacitance, Feedthrough (Channel Off)	C <sub>I/O</sub>	-	Pins Not Adjacent	-	-	-	0.47	-	-	-	pF
		-	Pins Adjacent	-	-	-		-	-	-	

2. Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

3. For voltage drops across the switch (ΔV<sub>switch</sub>) > 600 mV (> 300 mV at high temperature), excessive V<sub>DD</sub> current may be drawn; i.e. the current out of the switch may contain both V<sub>DD</sub> and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

# MC14067B

## ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C)

Characteristic	Symbol	V <sub>DD</sub> - V <sub>SS</sub> V <sub>dc</sub>	Typ (4)	Max	Unit
Propagation Delay Times Channel Input-to-Channel Output (R <sub>L</sub> = 200 kΩ) MC14067B	t <sub>PLH</sub> , t <sub>PHL</sub> (Figure 3)	5.0 10 15	35 15 12	90 40 30	ns
Propagation Delay Times Channel Input-to-Channel Output (R <sub>L</sub> = 1.0 kΩ) MC14067B	t <sub>PLH</sub> , t <sub>PHL</sub> (Figure 3)	5.0 10 15		50 30 20	ns
Control Input-to-Channel Output Channel Turn-On Time (R <sub>L</sub> = 10 kΩ) MC14067B	t <sub>PZH</sub> , t <sub>PZL</sub>	5.0 10 15	240 115 75	600 290 190	ns
Channel Turn-Off Time (R <sub>L</sub> = 300 kΩ) MC14067B	(Figure 4) t <sub>PHZ</sub> , t <sub>PLZ</sub>	5.0 10 15	250 120 75	625 300 190	ns
Channel Turn-Off Time (R <sub>L</sub> = 10 kΩ) MC14067B	(Figure 4)	5.0 10 15		625 450 350	ns
Any Pair of Address Inputs to Output MC14067B	t <sub>PLH</sub> , t <sub>PHL</sub>	5.0 10 15	280 115 85	700 290 215	ns
Second Harmonic Distortion (R <sub>L</sub> = 10 kΩ, f = 1 kHz, V <sub>in</sub> = 5 V <sub>p-p</sub> )	-	10	0.3	-	%
ON Channel Bandwidth [R <sub>L</sub> = 50 Ω, V <sub>in</sub> = 1/2 (V <sub>DD</sub> - V <sub>SS</sub> ) p-p (sine-wave)] 20 Log <sub>10</sub> (V <sub>out</sub> /V <sub>in</sub> ) = - 3 dB MC14067B	BW (Figure 5)	10	15	-	MHz
Off Channel Feedthrough Attenuation [R <sub>L</sub> = 50 Ω, V <sub>in</sub> = 1/2 (V <sub>DD</sub> - V <sub>SS</sub> ) p-p (sine-wave)] f <sub>in</sub> = 20 MHz - MC14067B	- (Figure 5)	10	- 40	-	dB
Channel Separation [R <sub>L</sub> = 1 kΩ, V <sub>in</sub> = 1/2 (V <sub>DD</sub> - V <sub>SS</sub> ) p-p (sine-wave)] f <sub>in</sub> = 20 MHz	- (Figure 6)	10	- 40	-	dB
Crosstalk, Control Inputs-to-Common O/I (R <sub>1</sub> = 1 kΩ, R <sub>L</sub> = 10 kΩ, Control t <sub>r</sub> = t <sub>f</sub> = 20 ns, Inhibit = V <sub>SS</sub> )	- (Figure 7)	10	30	-	mV

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# MC14067B

## ORDERING INFORMATION

Device	Package	Shipping†
MC14067BDWG	SOIC-24 (Pb-Free)	30 Units / Rail
NLV14067BDWG*		
MC14067BDWR2G	SOIC-24 (Pb-Free)	1000 Units / Tape & Reel
NLV14067BDWR2G*		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

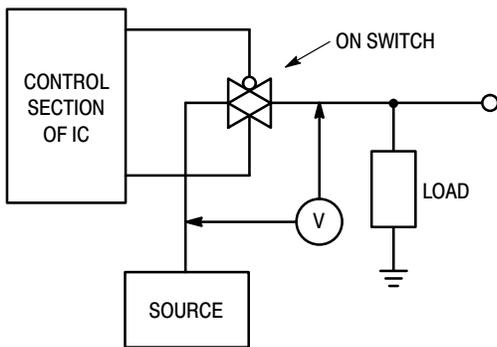


Figure 1.  $\Delta V$  Across Switch

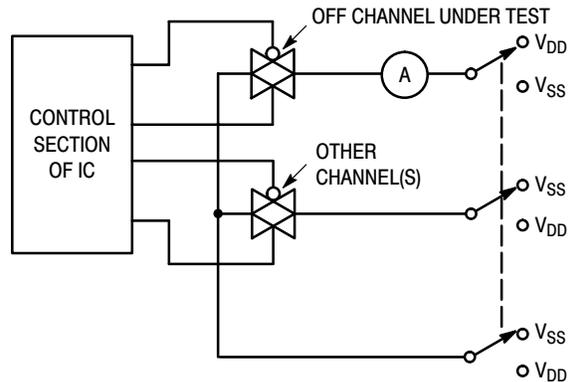


Figure 2. Off Channel Leakage

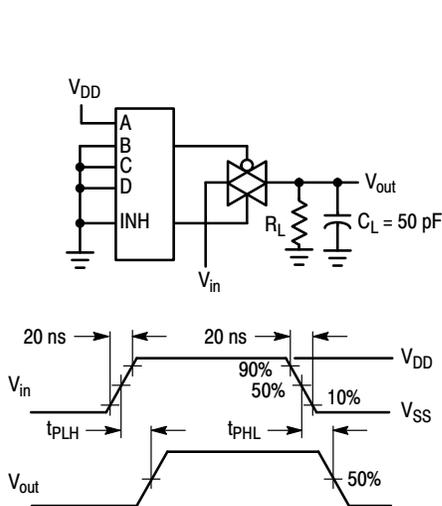


Figure 3. Propagation Delay Test Circuit and Waveforms  $V_{in}$  to  $V_{out}$

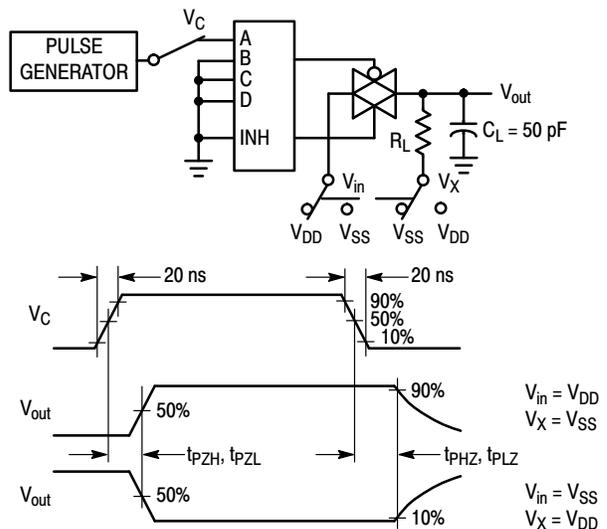
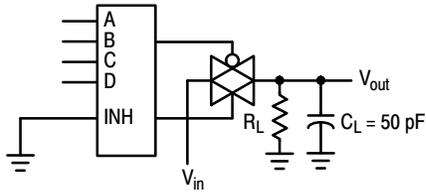


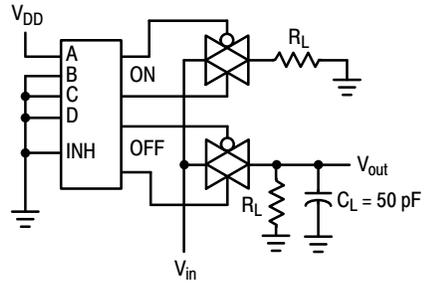
Figure 4. Turn-On and Delay Turn-Off Test Circuit and Waveforms

# MC14067B

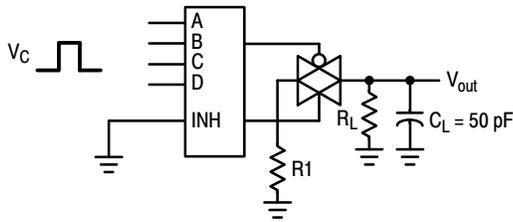
A, B, and C inputs used to turn ON or OFF the switch under test.



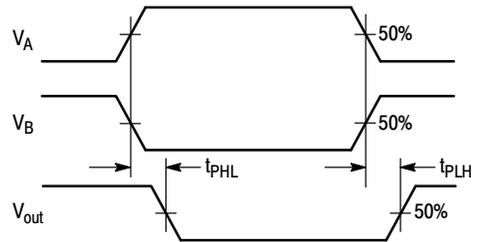
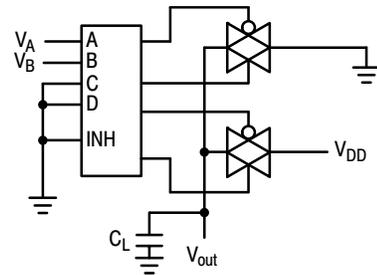
**Figure 5. Bandwidth and Off-Channel Feedthrough Attenuation**



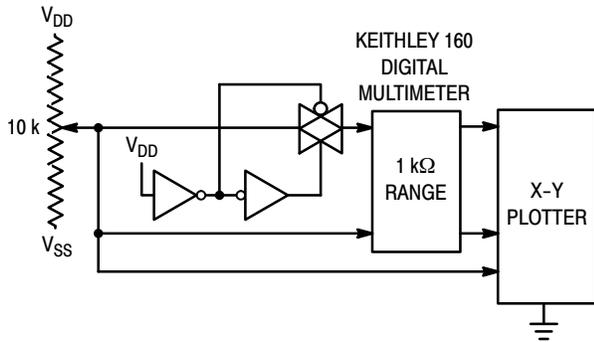
**Figure 6. Channel Separation (Adjacent Channels Used for Setup)**



**Figure 7. Crosstalk, Control to Common O/I**



**Figure 9. Propagation Delay, Any Pair of Address Inputs to Output**



**Figure 8. Channel Resistance ( $R_{ON}$ ) Test Circuit**

TYPICAL RESISTANCE CHARACTERISTICS

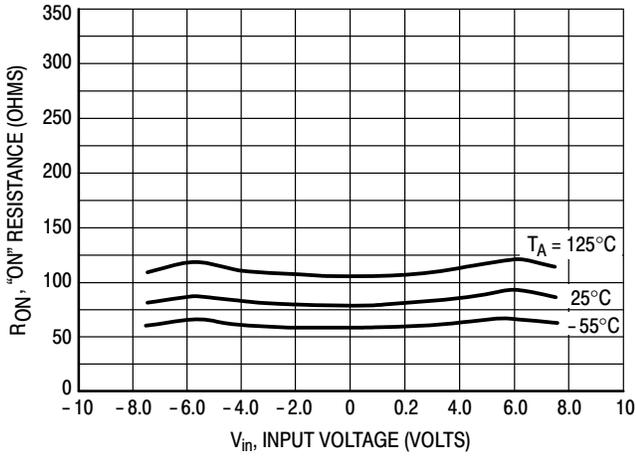


Figure 10.  $V_{DD} = 7.5\text{ V}$ ,  $V_{SS} = -7.5\text{ V}$

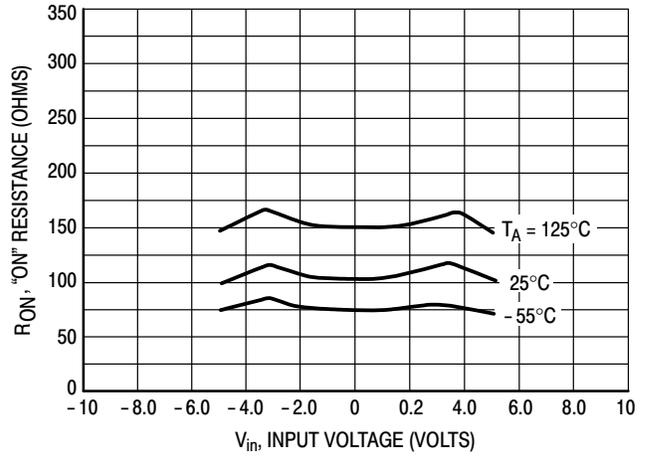


Figure 11.  $V_{DD} = 5.0\text{ V}$ ,  $V_{SS} = -5.0\text{ V}$

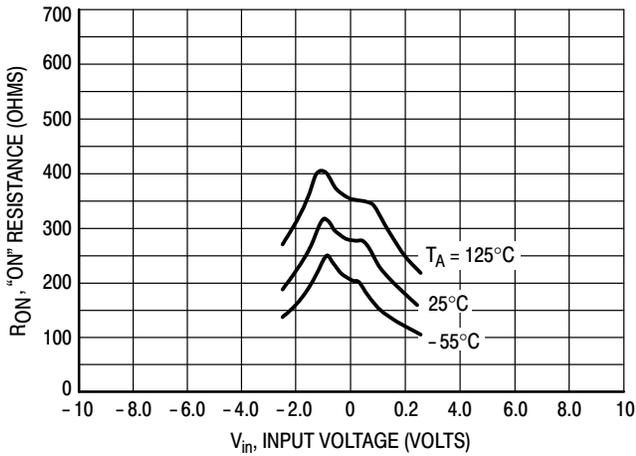


Figure 12.  $V_{DD} = 2.5\text{ V}$ ,  $V_{SS} = -2.5\text{ V}$

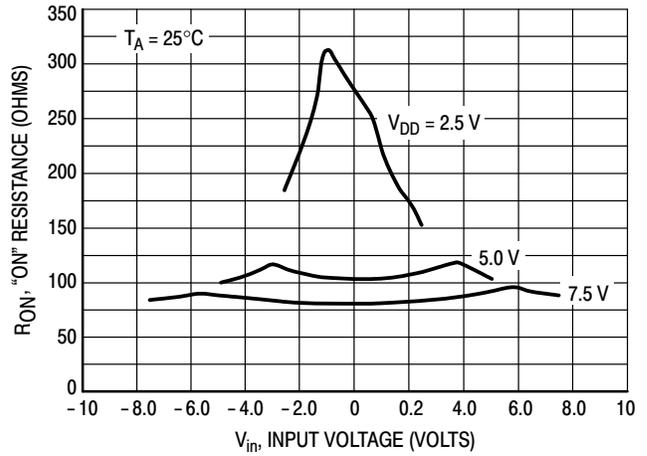


Figure 13. Comparison at 25°C,  $V_{DD} = -V_{SS}$

APPLICATIONS INFORMATION

Figure A illustrates use of the Analog Multiplexer / Demultiplexer. The 0-to-5 V Digital Control signal is used to directly control a 5 V<sub>p-p</sub> analog signal.

The digital control logic levels are determined by V<sub>DD</sub> and V<sub>SS</sub>. The V<sub>DD</sub> voltage is the logic high voltage; the V<sub>SS</sub> voltage is logic low. For the example, V<sub>DD</sub> = +5 V = logic high at the control inputs; V<sub>SS</sub> = GND = 0 V = logic low.

The maximum analog signal level is determined by V<sub>DD</sub> and V<sub>SS</sub>. The analog voltage must swing neither higher than V<sub>DD</sub> nor lower than V<sub>SS</sub>. The example shows a 5 V<sub>p-p</sub>

signal which allows no margin at either peak. If voltage transients above V<sub>DD</sub> and/or below V<sub>SS</sub> are anticipated on the analog channels, external diodes (D<sub>x</sub>) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The absolute maximum potential difference between V<sub>DD</sub> and V<sub>SS</sub> is 18.0 volts. Most parameters are specified up to 15 V which is the recommended maximum difference between V<sub>DD</sub> and V<sub>SS</sub>.

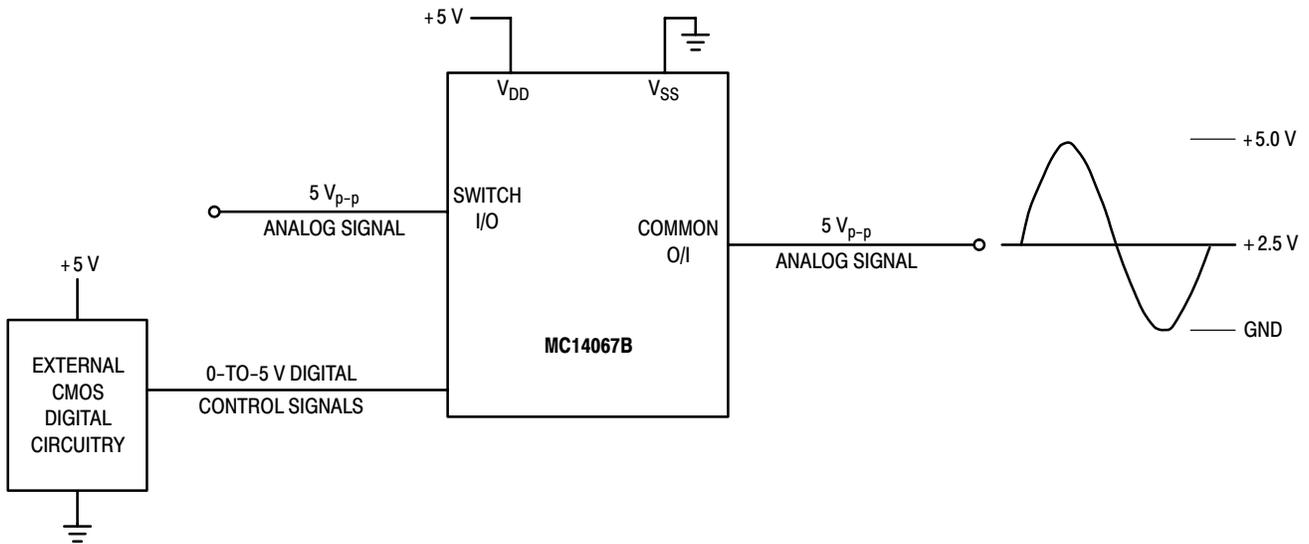


Figure A. Application Example

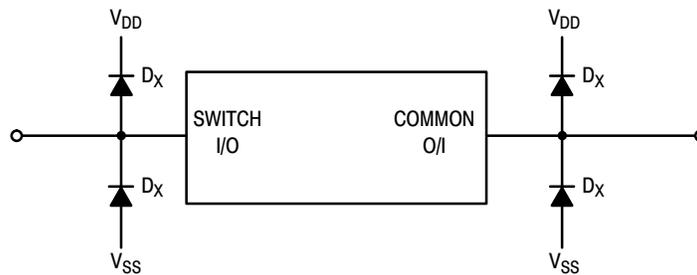
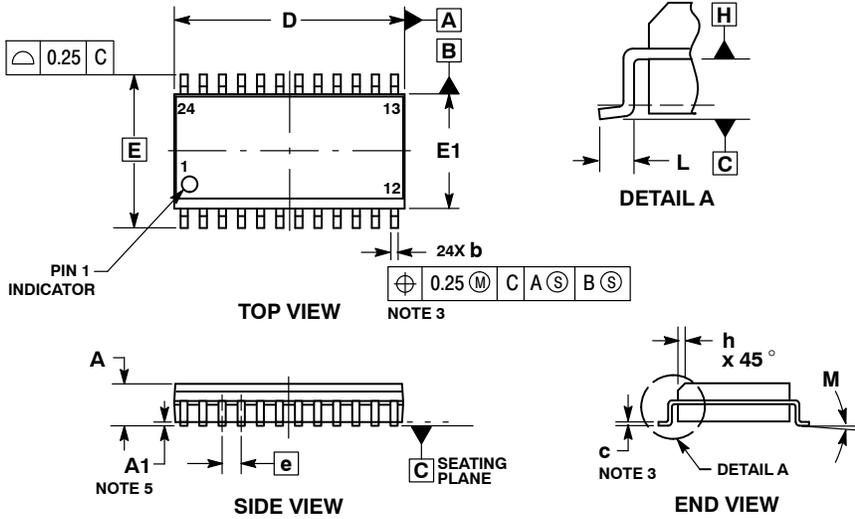


Figure B. External Germanium or Schottky Clipping Diodes

# MC14067B

## PACKAGE DIMENSIONS

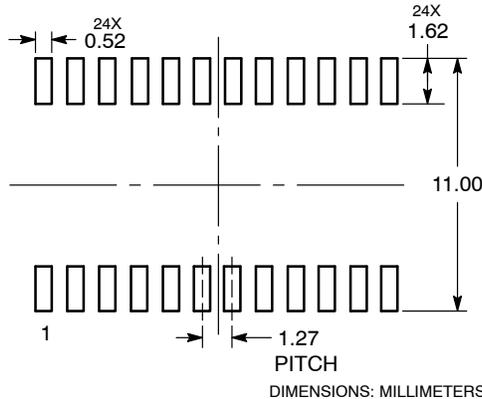
SOIC-24 WB  
CASE 751E-04  
ISSUE F



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD AND ARE MEASURED BETWEEN 0.10 AND 0.25 FROM THE LEAD TIP.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

### RECOMMENDED SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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