



## SNx4HC05 Hex Inverters With Open-Drain Outputs

### 1 Features

- Wide Operating Voltage Range of 2 V to 6 V
- Outputs can Drive up to 10 LSTTL Loads
- Low-Power Consumption, 20- $\mu$ A Maximum ICC
- Typical  $t_{pd} = 8$  ns
- $\pm 4$ -mA Output Drive at 5 V
- Low Input Current of 1- $\mu$ A Maximum

### 2 Applications

- Mice
- Printers
- AC Inverter Drives
- UPS
- AC Servo Drives
- Other Motor Drives

### 3 Description

The SNx4HC05 devices contain six independent inverters. They perform the Boolean function  $Y = \bar{A}$  in positive logic. The open-drain outputs require pullup resistors to perform correctly. They may be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74HC05	PDIP (14)	19.30 mm $\times$ 6.40 mm
	SOIC (14)	8.65 mm $\times$ 3.91 mm
	SOP (14)	10.30 mm $\times$ 5.30 mm
	TSSOP (14)	5.00 mm $\times$ 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Logic Diagram (Positive Logic)



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	8.2 Functional Block Diagram .....	<b>7</b>
<b>2 Applications</b> .....	<b>1</b>	8.3 Feature Description .....	<b>7</b>
<b>3 Description</b> .....	<b>1</b>	8.4 Device Functional Modes .....	<b>7</b>
<b>4 Revision History</b> .....	<b>2</b>	<b>9 Application and Implementation</b> .....	<b>8</b>
<b>5 Pin Configuration and Functions</b> .....	<b>3</b>	9.1 Application Information .....	<b>8</b>
<b>6 Specifications</b> .....	<b>4</b>	9.2 Typical Application .....	<b>8</b>
6.1 Absolute Maximum Ratings .....	<b>4</b>	<b>10 Power Supply Recommendations</b> .....	<b>9</b>
6.2 ESD Ratings .....	<b>4</b>	<b>11 Layout</b> .....	<b>9</b>
6.3 Recommended Operating Conditions .....	<b>4</b>	11.1 Layout Guidelines .....	<b>9</b>
6.4 Thermal Information .....	<b>5</b>	11.2 Layout Example .....	<b>9</b>
6.5 Electrical Characteristics .....	<b>5</b>	<b>12 Device and Documentation Support</b> .....	<b>10</b>
6.6 Switching Characteristics .....	<b>5</b>	12.1 Documentation Support .....	<b>10</b>
6.7 Operating Characteristics .....	<b>5</b>	12.2 Related Links .....	<b>10</b>
6.8 Typical Characteristics .....	<b>6</b>	12.3 Trademarks .....	<b>10</b>
<b>7 Parameter Measurement Information</b> .....	<b>6</b>	12.4 Electrostatic Discharge Caution .....	<b>10</b>
<b>8 Detailed Description</b> .....	<b>7</b>	12.5 Glossary .....	<b>10</b>
8.1 Overview .....	<b>7</b>	<b>13 Mechanical, Packaging, and Orderable Information</b> .....	<b>10</b>

## 4 Revision History

### Changes from Revision D (August 2003) to Revision E

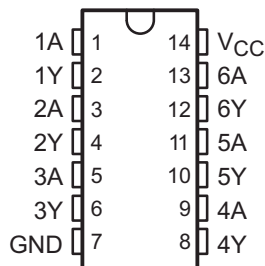
Page

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ..... **1**

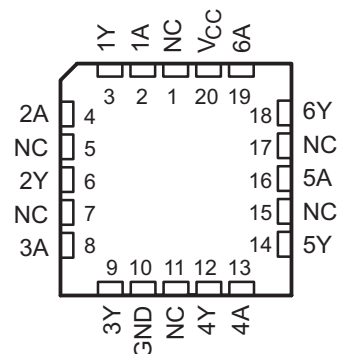
## 5 Pin Configuration and Functions

**SN74HC05: D, N, NS, or PW Package, 14-Pin SOIC, PDIP, SOP, or TSSOP**

**SN54HC05: J or W Package, 19-Pin CDIP or CFP (Top View)**



**SN54HC05: FK Package 20-Pin LCCC (Top View)**



NC – No internal connection

### Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.	LCCC NO.		
1A	1	2	I	Input 1
1Y	2	3	O	Output 1
2A	3	4	I	Input 2
2Y	4	6	O	Output 2
3A	5	8	I	Input 3
3Y	6	9	O	Output 3
GND	7	10	–	Ground pin
4A	9	13	I	Input 4
4Y	8	12	O	Output 4
5A	11	16	I	Input 5
5Y	10	14	O	Output 5
6A	13	19	I	Input 6
6Y	12	18	O	Output 6
NC	–	1, 5, 7, 11, 15, 17	–	No connect
V <sub>CC</sub>	14	20	–	Power pin

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	−0.5	7	V
$I_{IK}$	Input clamp current, $V_I < 0$ or $V_I > V_{CC}$ <sup>(2)</sup>	−20	20	mA
$I_{OK}$	Output clamp current, $V_O < 0$ or $V_O > V_{CC}$ <sup>(2)</sup>	−20	20	mA
$I_O$	Continuous output current, $V_O = 0$ to $V_{CC}$	−25	25	mA
	Continuous current through $V_{CC}$ or GND	−50	50	mA
$T_{stg}$	Storage temperature	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±1000	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

See <sup>(1)</sup>

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	2	5	6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5		V
		$V_{CC} = 4.5\text{ V}$	3.15		
		$V_{CC} = 6\text{ V}$	4.2		
$V_{IL}$	Low-level input voltage	$V_{CC} = 2\text{ V}$		0.5	V
		$V_{CC} = 4.5\text{ V}$		1.35	
		$V_{CC} = 6\text{ V}$		1.8	
$V_I$	Input voltage	0		$V_{CC}$	V
$V_O$	Output voltage	0		$V_{CC}$	V
$\Delta t/\Delta v$	Input transition rise or fall time	$V_{CC} = 2\text{ V}$		1000	ns
		$V_{CC} = 4.5\text{ V}$		500	
		$V_{CC} = 6\text{ V}$		400	
$T_A$	Operating free-air temperature	SN54HC05	−55	125	°C
		SN74HC05	−40	125	

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74HC05				UNIT
		D (SOIC)	N (PDIP)	NS (SOP)	PW (TSSOP)	
		14 PINS	14 PINS	14 PINS	14 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	89.1	85.9	86.4	117.1	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	50.6	43.8	42.4	46.1	
R <sub>θJB</sub>	Junction-to-board thermal resistance	43.3	44.6	45.1	58.7	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	16.3	12	11.8	4.8	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	43	44.2	44.7	58.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC05		SN74HC05 –40°C to 85°C		SN74HC05 –40°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
I <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>O</sub> = V <sub>CC</sub>	6 V		0.01	0.5		10		5		5	μA
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	2 V	0.002	0.1		0.1		0.1		0.1	V
			4.5 V	0.001	0.1		0.1		0.1		0.1	
			6 V	0.001	0.1		0.1		0.1		0.1	
		I <sub>OL</sub> = 4 mA	4.5 V	0.17	0.26		0.4		0.33		0.33	
		I <sub>OL</sub> = 5.2 mA	6 V	0.15	0.26		0.4		0.33		0.33	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0	6 V		±0.1	±100		±1000		±1000		±1000	nA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0	6 V			2		40		20		20	μA
C <sub>i</sub>		2 to 6 V		3	10		10		10		10	pF

## 6.6 Switching Characteristics

over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see [Figure 3](#))

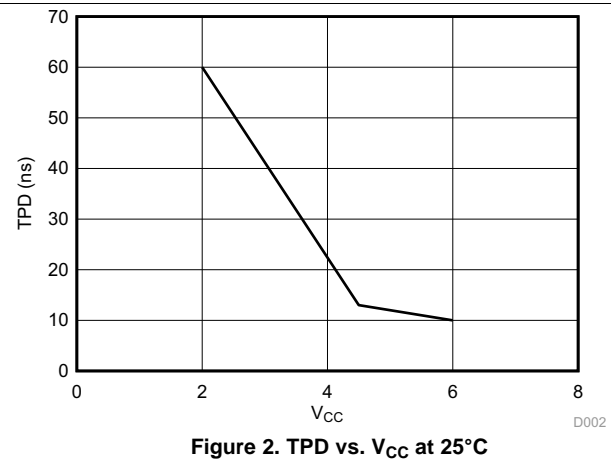
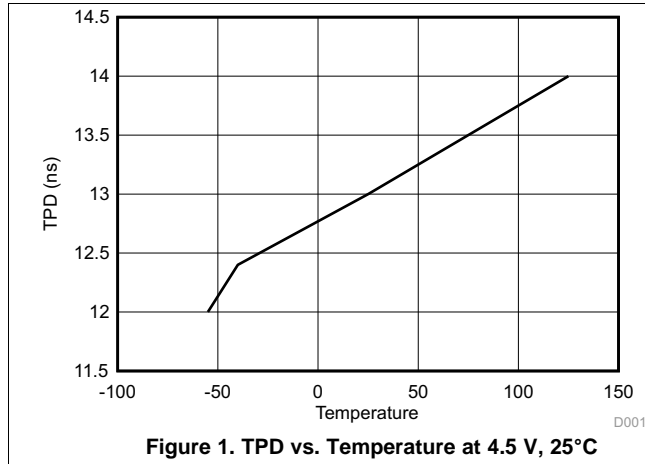
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC05		SN74HC05 –40°C to 85°C		SN74HC05 –40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A	Y	2 V		60	115		175		145		160	ns
			4.5 V		13	23		35		29		31	
			6 V		10	20		30		25		28	
t <sub>PHL</sub>	A	Y	2 V		45	85		130		105		120	
			4.5 V		9	17		26		21		23	
			6 V		8	14		22		18		21	
t <sub>f</sub>		Y	2 V		38	75		110		95		110	
			4.5 V		8	15		22		19		22	
			6 V		6	13		19		16		19	

## 6.7 Operating Characteristics

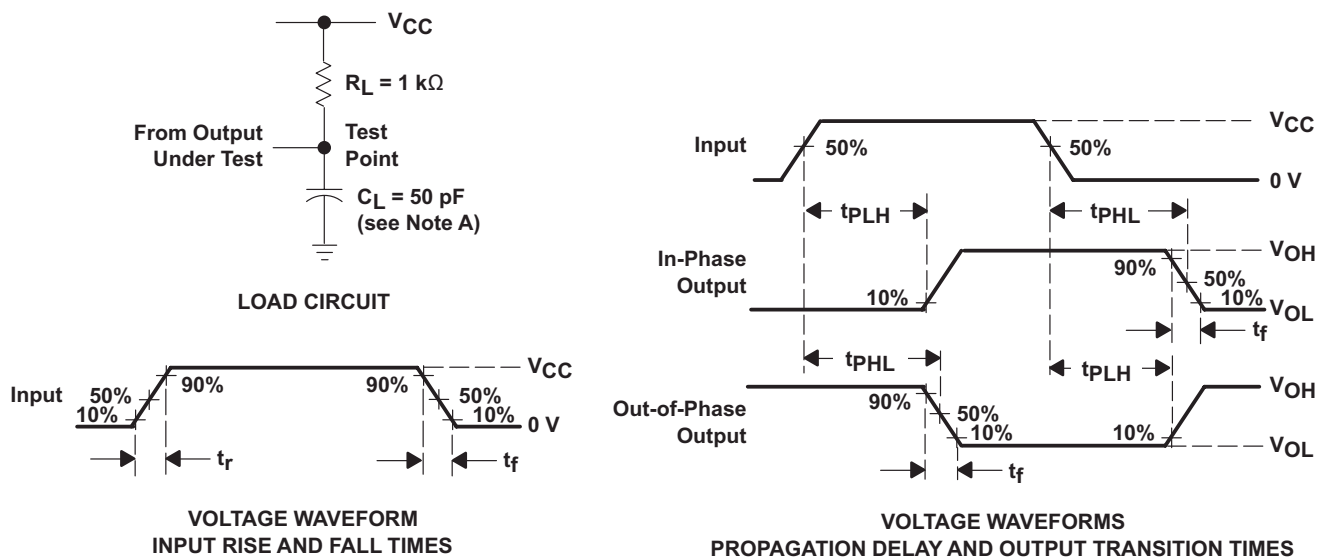
T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance per inverter	No load	20	pF

## 6.8 Typical Characteristics



## 7 Parameter Measurement Information



- $C_L$  includes probe and test-fixture capacitance.
- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.
- The outputs are measured one at a time with one input transition per measurement.

**Figure 3. Load Circuit and Voltage Waveforms**

## 8 Detailed Description

### 8.1 Overview

The SNx4HC05 devices contain six independent inverters. They perform the Boolean function  $Y = \bar{A}$  in positive logic. The open-drain outputs require pullup resistors to perform correctly. They may be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

### 8.2 Functional Block Diagram



**Figure 4. Logic Diagram (Positive Logic)**

### 8.3 Feature Description

The device's wide operating range allows it to be used in a variety of systems that use different logic levels. The strong current-sinking outputs allow the device to drive medium loads without significant increases in output voltage. In addition, the low power consumption makes this device a good choice for portable and battery power-sensitive applications.

### 8.4 Device Functional Modes

**Table 1. Function Table  
(Each Inverter)**

INPUT A	OUTPUT Y
H	L
L	H

## 9 Application and Implementation

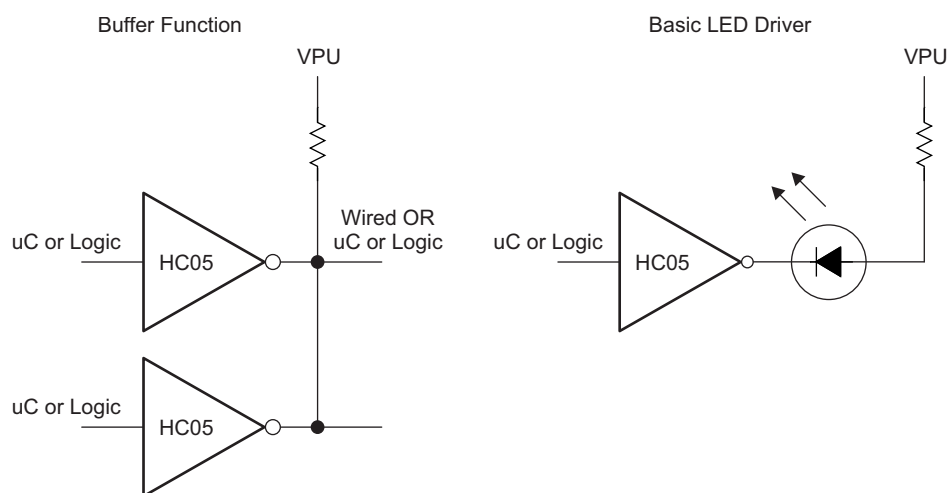
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The SN74HC05 device is a low drive open-drain CMOS device that can be used for a multitude of buffer type functions. The open-drain output can be pulled to any voltage between GND and  $V_{CC}$  making them ideal for down translation.

### 9.2 Typical Application



**Figure 5. Simplified Application Schematic**

#### 9.2.1 Design Requirements

This device uses CMOS technology and is open-drain so it has low-output drive only. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. Parallel output drive can create fast edges into light loads so consider routing and load conditions to prevent ringing.

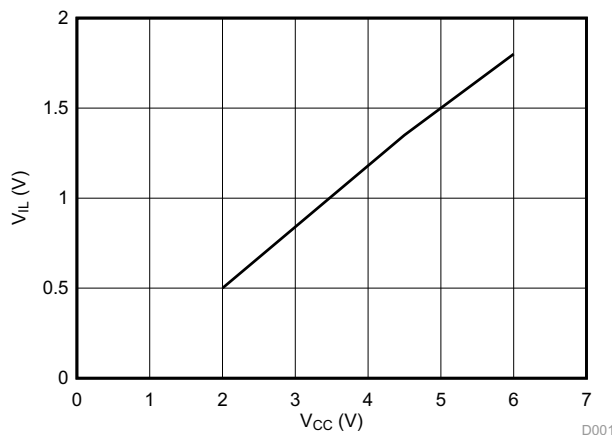
#### 9.2.2 Detailed Design Procedure

- Recommended input conditions:
  - Rise time and fall time specs see  $(\Delta t/\Delta V)$  in [Recommended Operating Conditions](#).
  - Specified high and low levels. See  $(V_{IH}$  and  $V_{IL})$  in [Recommended Operating Conditions](#).
- Recommended output conditions:
  - Load currents should not exceed 25 mA per output and 50 mA total for the part.



## Typical Application (continued)

### 9.2.3 Application Curve



**Figure 6. Max  $V_{IL}$  vs.  $V_{CC}$  Level**

## 10 Power Supply Recommendations

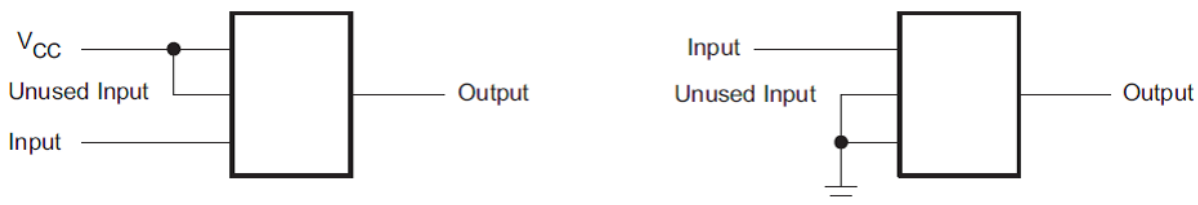
The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#). Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1- $\mu$ F capacitor. If there are multiple  $V_{CC}$  terminals, then TI recommends a 0.01- $\mu$ F or 0.022- $\mu$ F capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1  $\mu$ F and 1  $\mu$ F are commonly used in parallel. The bypass capacitor should be installed as close as possible to the power terminal for best results.

## 11 Layout

### 11.1 Layout Guidelines

When using multiple bit logic devices, inputs should never float. In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$  whichever makes more sense or is more convenient. Floating outputs is generally acceptable, unless the part is a transceiver.

### 11.2 Layout Example



**Figure 7. Layout Recommendation**

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

*Implications of Slow or Floating CMOS Inputs*, [SCBA004](#)

### 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54HC05	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
SN74HC05	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 12.3 Trademarks

All trademarks are the property of their respective owners.

### 12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-88718012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 88718012A SNJ54HC 05FK	<a href="#">Samples</a>
5962-8871801CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8871801CA SNJ54HC05J	<a href="#">Samples</a>
SN54HC05J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54HC05J	<a href="#">Samples</a>
SN74HC05D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC05	<a href="#">Samples</a>
SN74HC05DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC05	<a href="#">Samples</a>
SN74HC05DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC05	<a href="#">Samples</a>
SN74HC05DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 125	HC05	<a href="#">Samples</a>
SN74HC05DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC05	<a href="#">Samples</a>
SN74HC05DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC05	<a href="#">Samples</a>
SN74HC05DT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC05	<a href="#">Samples</a>
SN74HC05DTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC05	<a href="#">Samples</a>
SN74HC05N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	SN74HC05N	<a href="#">Samples</a>
SN74HC05N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	-40 to 85		
SN74HC05NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	SN74HC05N	<a href="#">Samples</a>
SN74HC05NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC05	<a href="#">Samples</a>
SN74HC05NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC05	<a href="#">Samples</a>
SN74HC05NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC05	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HC05PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 125	HC05	<a href="#">Samples</a>
SN74HC05PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC05	<a href="#">Samples</a>
SN74HC05PWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC05	<a href="#">Samples</a>
SN74HC05PWTG4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC05	<a href="#">Samples</a>
SNJ54HC05FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 88718012A SNJ54HC 05FK	<a href="#">Samples</a>
SNJ54HC05J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8871801CA SNJ54HC05J	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54HC05, SN74HC05 :**

- Catalog: [SN74HC05](#)
- Military: [SN54HC05](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC05DR	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.3	8.0	16.0	Q1
SN74HC05DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC05DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC05DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC05DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC05DT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC05NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74HC05PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC05PWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC05DR	SOIC	D	14	2500	364.0	364.0	27.0
SN74HC05DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74HC05DR	SOIC	D	14	2500	333.2	345.9	28.6
SN74HC05DRG4	SOIC	D	14	2500	367.0	367.0	38.0
SN74HC05DRG4	SOIC	D	14	2500	333.2	345.9	28.6
SN74HC05DT	SOIC	D	14	250	367.0	367.0	38.0
SN74HC05NSR	SO	NS	14	2000	367.0	367.0	38.0
SN74HC05PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74HC05PWT	TSSOP	PW	14	250	367.0	367.0	35.0

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

Automotive and Transportation	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)



# AMEYA360

Components Supply Platform

Authorized Distribution Brand :



Website :

Welcome to visit [www.ameya360.com](http://www.ameya360.com)

Contact Us :

➤ Address :

401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd  
Minhang District, Shanghai , China

➤ Sales :

Direct     +86 (21) 6401-6692  
  
Email       amall@ameya360.com  
  
QQ         800077892  
  
Skype       ameyasales1 ameyasales2

➤ Customer Service :

Email       service@ameya360.com

➤ Partnership :

Tel         +86 (21) 64016692-8333  
  
Email       mkt@ameya360.com