P-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

$V_{(BR)DSS}$	$R_{DS(on)\ max}$	I_D $T_A = +25°C$
-50V	10Ω @ V_{GS} = -5V	-130mA

Description

This MOSFET has been designed to minimize the on-state resistance ($R_{DS(on)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

- General Purpose Interfacing Switch
- Power Management Functions
- Analog Switch

Features and Benefits

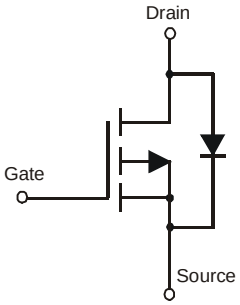
- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

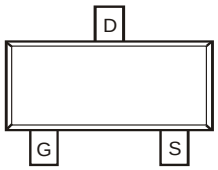
- Case: SOT23
- Case Material: UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Matte Tin Finish (Lead Free Plating) Solderable per MIL-STD-202, Method 208 e3
- Terminal Connections: See Diagram
- Weight: 0.008 grams (approximate)

SOT23

Top View



Equivalent Circuit



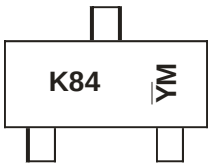
Top View

Ordering Information (Note 4)

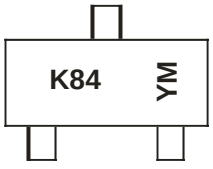
Part Number	Qualification	Case	Packaging
BSS84-7-F	Commercial	SOT23	3000/Tape & Reel
BSS84Q-7-F	Automotive	SOT23	3000/Tape & Reel
BSS84-13-F	Commercial	SOT23	10000/Tape & Reel
BSS84Q-13-F	Automotive	SOT23	10000/Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at http://www.diodes.com/products/packages.html

Marking Information



Chengdu A/T Site



Shanghai A/T Site

K84 = Product Type Marking Code
YM = Date Code Marking for SAT (Shanghai Assembly/ Test site)
YM = Date Code Marking for CAT (Chengdu Assembly/ Test site)
Y or Y = Year (ex: A = 2013)
M = Month (ex: 9 = September)

Date Code Key

Year	1998	1999	2000	2001	2002	2003	2004	…	2011	2012	2013	2014	2015	2016	2017
Code	J	K	L	M	N	P	R	…	Y	Z	A	B	C	D	E

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

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Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Units
Drain-Source Voltage		V_{DSS}	-50	V
Drain-Gate Voltage $R_{GS} \leq 20K\Omega$		V_{DGR}	-50	V
Gate-Source Voltage	Continuous	V_{GSS}	±20	V
Drain Current (Note 5)	Continuous	I_D	-130	mA
Pulsed Drain Current		I_{DM}	-1.2	A

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Units
Total Power Dissipation (Note 5)	P_D	300	mW
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	417	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 6)						
Drain-Source Breakdown Voltage	BV_{DSS}	-50	—	—	V	V_{GS} = 0V, I_D = -250µA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1	µA	V_{DS} = -50V, V_{GS} = 0V, T_J = +25°C
		—	—	-2	µA	V_{DS} = -50V, V_{GS} = 0V, T_J = +125°C
		—	—	-100	nA	V_{DS} = -25V, V_{GS} = 0V, T_J = +25°C
Gate-Body Leakage	I_{GSS}	—	—	±10	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 6)						
Gate Threshold Voltage	$V_{GS(th)}$	-0.8	—	-2.0	V	V_{DS} = V_{GS}, I_D = -1mA
Static Drain-Source On-Resistance	$R_{DS\ (ON)}$	—	—	10	Ω	V_{GS} = -5V, I_D = -0.100A
Forward Transconductance	g_{FS}	0.05	—	—	S	V_{DS} = -25V, I_D = -0.1A
DYNAMIC CHARACTERISTICS (Note 7)						
Input Capacitance	C_{iss}	—	—	45	pF	V_{DS} = -25V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	—	25	pF	
Reverse Transfer Capacitance	C_{rss}	—	—	12	pF	
SWITCHING CHARACTERISTICS (Note 7)						
Turn-On Delay Time	$t_{D(ON)}$	—	10	—	ns	V_{DD} = -30V, I_D = -0.27A,
Turn-Off Delay Time	$t_{D(OFF)}$	—	18	—	ns	R_{GEN} = 50Ω, V_{GS} = -10V

Notes:
5. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch; pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at http://www.diodes.com.
6. Short duration pulse test used to minimize self-heating effect.
7. Guaranteed by design. Not subject to production testing

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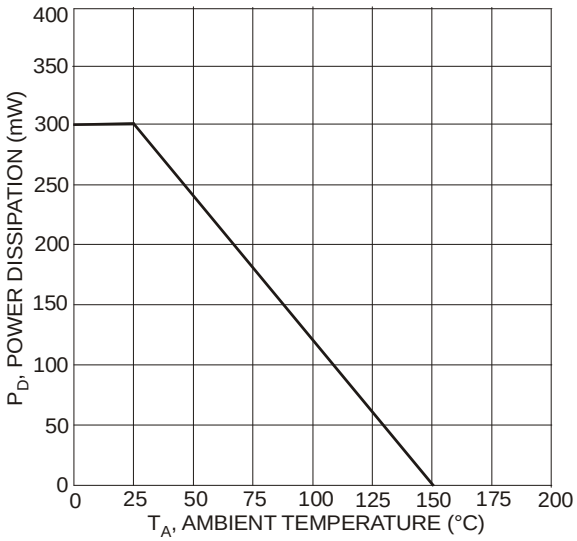

Fig. 1 Max Power Dissipation vs. Ambient Temperature

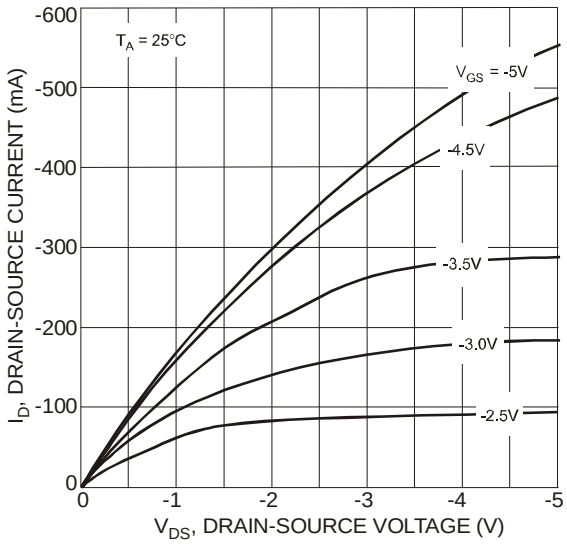

Fig. 2 Drain-Source Current vs. Drain-Source Voltage

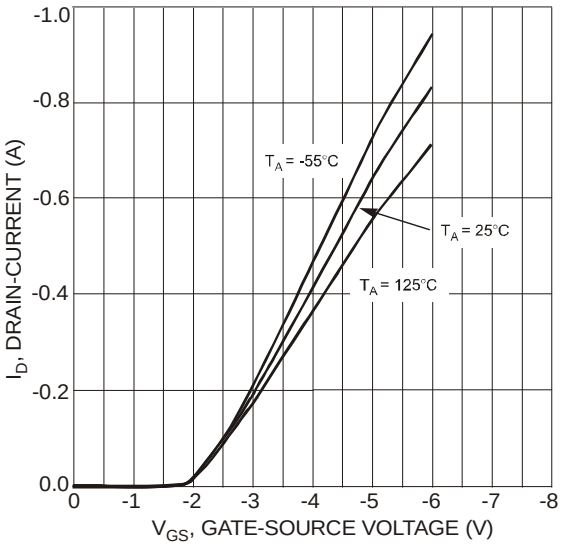

Fig. 3 Drain-Current vs. Gate-Source Voltage

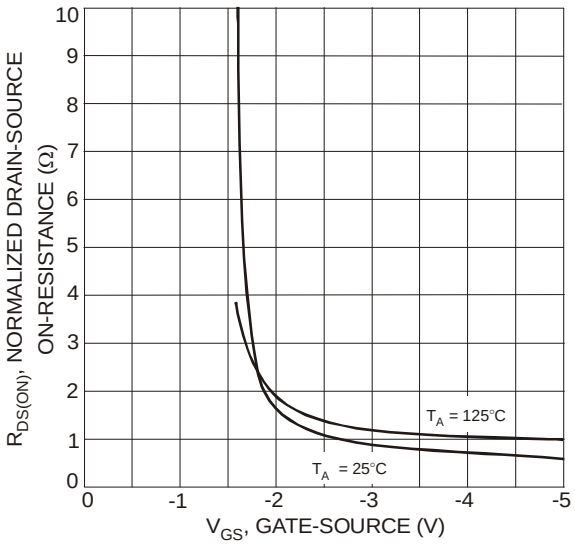

Fig. 4 On-Resistance vs. Gate-Source Voltage

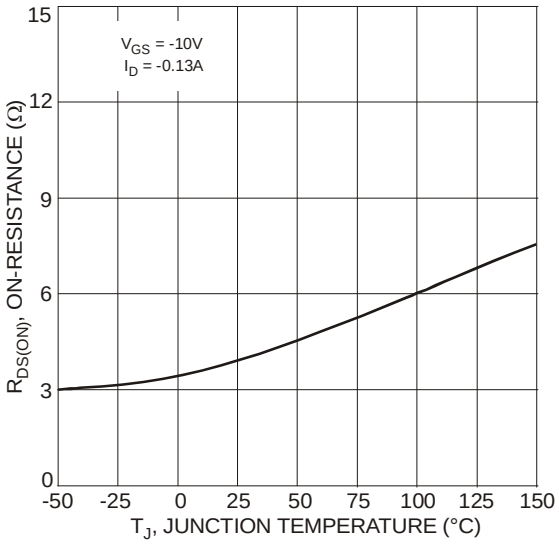

Fig. 5 On-Resistance vs. Junction Temperature

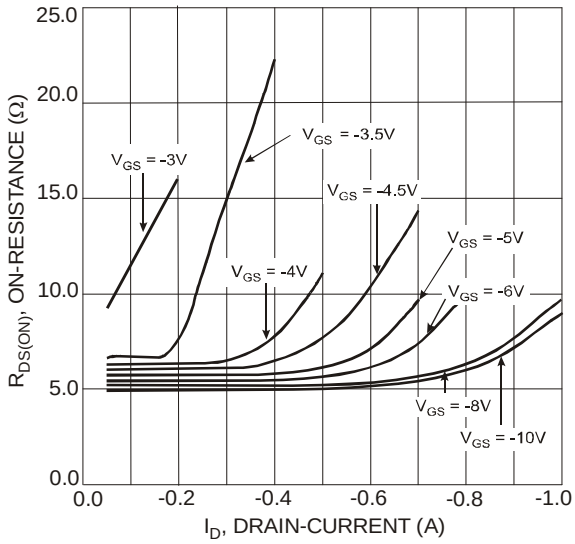

Fig. 6 On-Resistance vs. Drain-Current

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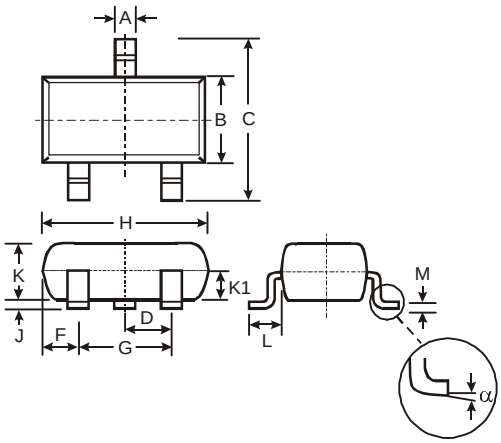
Package Outline Dimensions

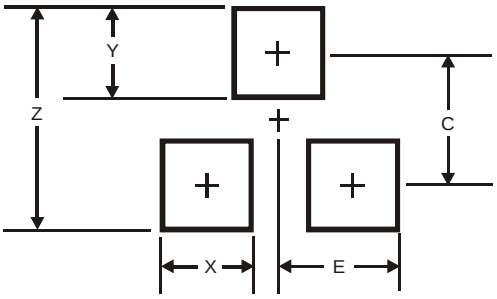
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for latest version.



SOT23			
Dim	**Min**	**Max**	**Typ**
A	0.37	0.51	0.40
B	1.20	1.40	1.30
C	2.30	2.50	2.40
D	0.89	1.03	0.915
F	0.45	0.60	0.535
G	1.78	2.05	1.83
H	2.80	3.00	2.90
J	0.013	0.10	0.05
K	0.903	1.10	1.00
K1	-	-	0.400
L	0.45	0.61	0.55
M	0.085	0.18	0.11
α	0°	8°	-
All Dimensions in mm			

Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.



Dimensions	Value (in mm)
Z	2.9
X	0.8
Y	0.9
C	2.0
E	1.35

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