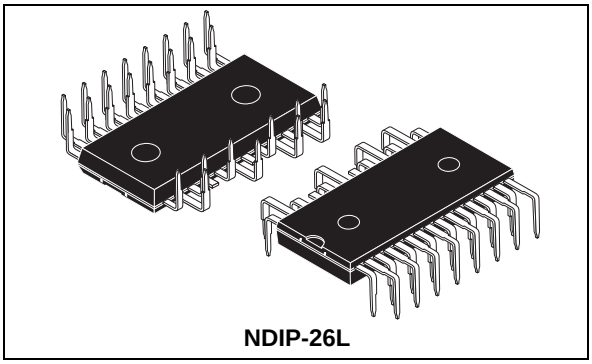
STGIPN3H60T-H

SLLIMM™-nano (small low-loss intelligent molded module) IPM, 3 A - 600 V 3-phase IGBT inverter bridge

Datasheet - production data



NDIP-26L

Features

- IPM 3 A, 600 V, 3-phase IGBT inverter bridge including control ICs for gate driving and freewheeling diodes
- Optimized for low electromagnetic interference
- $V_{CE(sat)}$ negative temperature coefficient
- 3.3 V, 5 V, 15 V CMOS/TTL inputs comparators with hysteresis and pull down/pull up resistors
- Undervoltage lockout
- Internal bootstrap diode
- Interlocking function
- Smart shutdown function
- Comparator for fault protection against overtemperature and overcurrent
- Op amp for advanced current sensing
- Optimized pin out for easy board layout
- NTC for temperature control (UL 1434 CA 2 and 4)

Applications

- 3-phase inverters for motor drives
- Dish washers, refrigerator compressors, heating systems, air-conditioning fans, draining and recirculation pumps

Description

This intelligent power module implements a compact, high performance AC motor drive in a simple, rugged design. It is composed of six IGBTs with freewheeling diodes and three half-bridge HVICs for gate driving, providing low electromagnetic interference (EMI) characteristics with optimized switching speed. The package is optimized for thermal performance and compactness in built-in motor applications, or other low power applications where assembly space is limited. This IPM includes an operational amplifier, completely uncommitted, and a comparator that can be used to design a fast and efficient protection circuit. SLLIMM™ is a trademark of STMicroelectronics.

Table 1. Device summary

Order code	Marking	Package	Packaging
STGIPN3H60T-H	GIPN3H60T-H	NDIP-26L	Tube

Contents

1 Internal schematic diagram and pin configuration

Figure 1. Internal schematic diagram

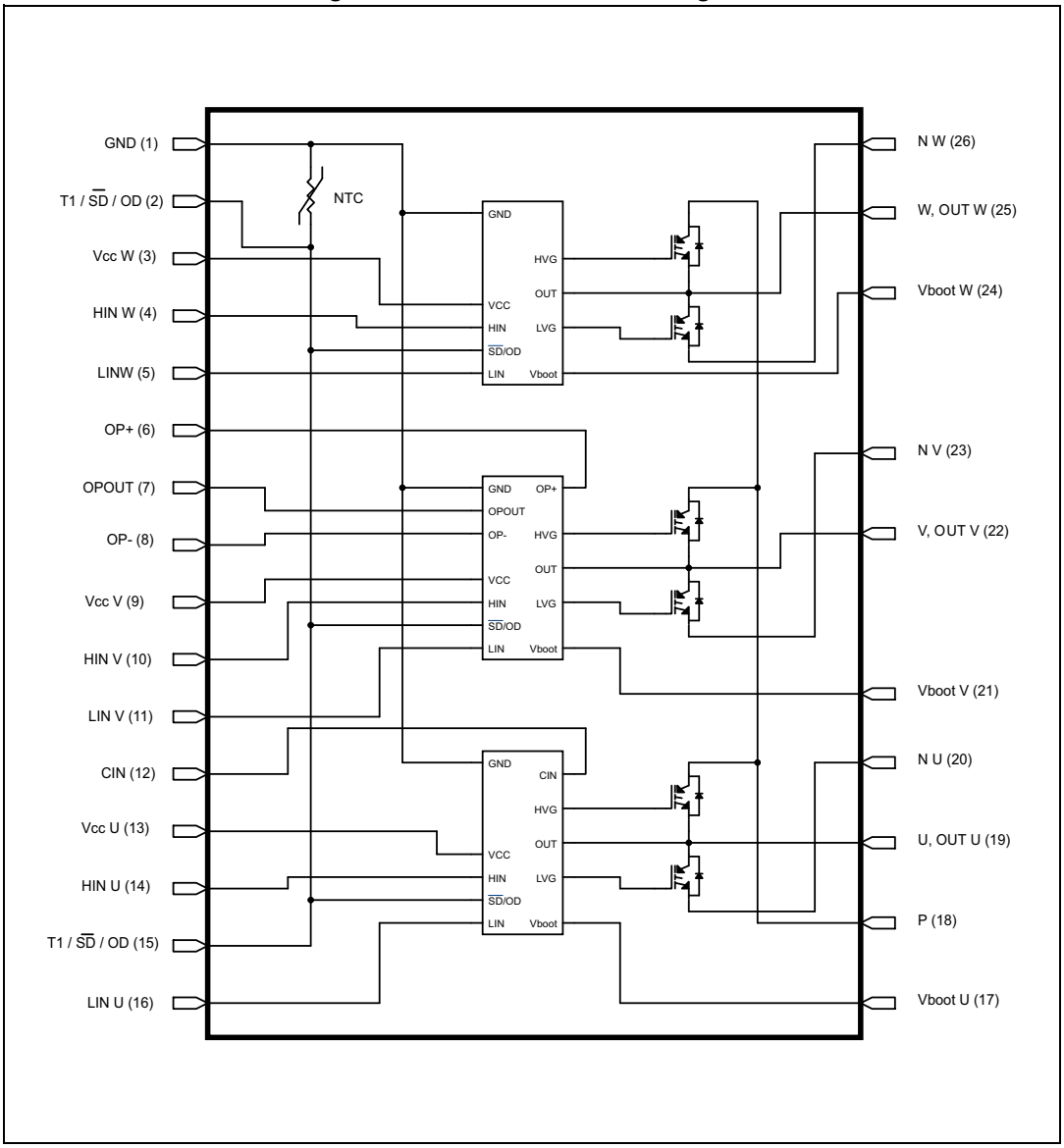
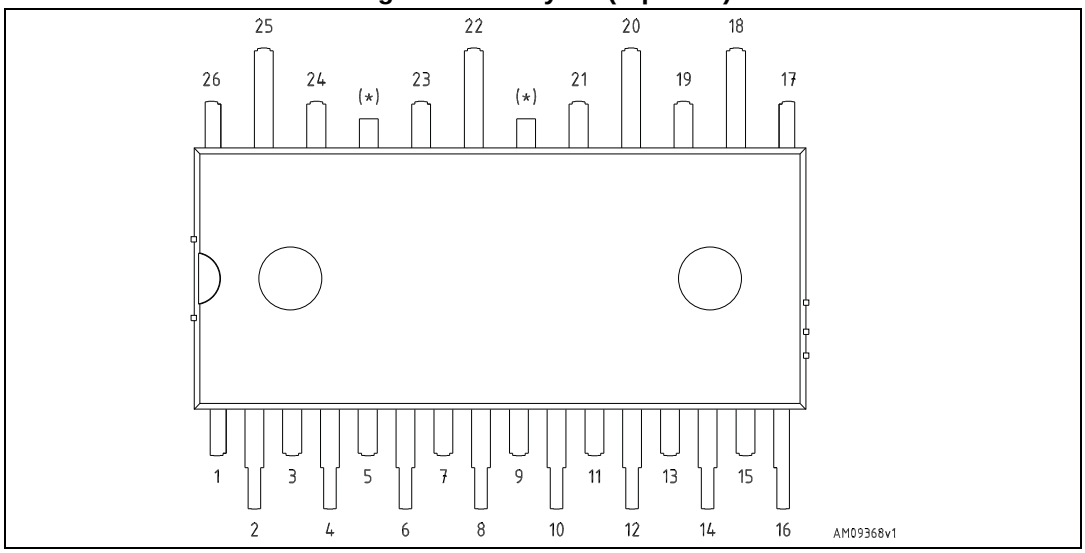


Table 2. Pin description

Pin	Symbol	Description
1	GND	Ground
2	T/$\overline{SD}$/OD	NTC thermistor terminal / shut down logic input (active low) / open drain (comparator output)
3	V_{CC} W	Low voltage power supply W phase
4	HIN W	High side logic input for W phase
5	LIN W	Low side logic input for W phase
6	OP+	Op amp non inverting input
7	OP_{OUT}	Op amp output
8	OP-	Op amp inverting input
9	V_{CC} V	Low voltage power supply V phase
10	HIN V	High side logic input for V phase
11	LIN V	Low side logic input for V phase
12	CIN	Comparator input
13	V_{CC} U	Low voltage power supply for U phase
14	HIN U	High side logic input for U phase
15	T/$\overline{SD}$/OD	NTC thermistor terminal / shut down logic input (active low) / open drain (comparator output)
16	LIN U	Low side logic input for U phase
17	V_{BOOT} U	Bootstrap voltage for U phase
18	P	Positive DC input
19	U, OUT_U	U phase output
20	N_U	Negative DC input for U phase
21	V_{BOOT} V	Bootstrap voltage for V phase
22	V, OUT_V	V phase output
23	N_V	Negative DC input for V phase
24	V_{BOOT} W	Bootstrap voltage for W phase
25	W, OUT_W	W phase output
26	N_W	Negative DC input for W phase

Figure 2. Pin layout (top view)



(*) Dummy pin internally connected to P (positive DC input).

2 Electrical ratings

2.1 Absolute maximum ratings

Table 3. Inverter part

Symbol	Parameter	Value	Unit
V_{CES}	Each IGBT collector emitter voltage (V_{IN}(1) = 0)	600	V
± I_C (2)	Each IGBT continuous collector current at T_C = 25°C	3	A
± I_{CP} (3)	Each IGBT pulsed collector current	18	A
P_{TOT}	Each IGBT total dissipation at T_C = 25°C	8	W

1. Applied between HIN_i, LIN_i and GND for i = U, V, W
2. Calculated according to the iterative formula:

$$I_C(T_C) = \frac{T_{j(max)} - T_C}{R_{thj-c} \times V_{CE(sat)(max)}(T_{j(max)}, I_C(T_C))}$$

3. Pulse width limited by max junction temperature

Table 4. Control part

Symbol	Parameter	Min.	Max.	Unit
V_{OUT}	Output voltage applied between OUT_U, OUT_V, OUT_W - GND	V_{boot} - 21	V_{boot} + 0.3	V
V_{CC}	Low voltage power supply	- 0.3	21	V
V_{CIN}	Comparator input voltage	- 0.3	V_{CC} +0.3	V
V_{op+}	OPAMP non-inverting input	- 0.3	V_{CC} +0.3	V
V_{op-}	OPAMP inverting input	- 0.3	V_{CC} +0.3	V
V_{boot}	Bootstrap voltage	- 0.3	620	V
V_{IN}	Logic input voltage applied between HIN, LIN and GND	- 0.3	15	V
$V_{T/\overline{SD}/OD}$	Open drain voltage	- 0.3	15	V
$\Delta V_{OUT/dT}$	Allowed output slew rate		50	V/ns

Table 5. Total system

Symbol	Parameter	Value	Unit
V_{ISO}	Isolation withstand voltage applied between each pin and heatsink plate (AC voltage, t = 60 sec.)	1000	V
T_j	Power chips operating junction temperature	-40 to 150	°C
T_C	Module case operation temperature	-40 to 125	°C

2.2 Thermal data

Table 6. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	50	°C/W

3 Electrical characteristics

T_J = 25 °C unless otherwise specified.

Table 7. Inverter part

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector-cut off current (V_{IN}(1)= 0 “logic state”)	V_{CE} = 550 V, V_{CC} = 15 V; V_{BS} = 15 V	-		250	µA
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{CC} = V_{boot} = 15 V, V_{IN}(1)= 0 - 5 V, I_C = 1 A	-	2.15	2.6	V
		V_{CC} = V_{boot} = 15 V, V_{IN}(1)= 0 - 5 V, I_C = 1 A, T_J = 125 °C	-	1.65		
V_F	Diode forward voltage	V_{IN}(1) = 0 “logic state”, I_C = 1 A	-		1.7	V
Inductive load switching time and energy(2)						
t_{on}	Turn-on time	V_{DD} = 300 V, V_{CC} = V_{boot} = 15 V, V_{IN}(1) = 0 - 5 V, I_C = 1 A (see *Figure 4*)	-	275		ns
$t_{c(on)}$	Crossover time (on)		-	90		
t_{off}	Turn-off time		-	890		
$t_{c(off)}$	Crossover time (off)		-	125		
t_{rr}	Reverse recovery time		-	50		
E_{on}	Turn-on switching losses		-	18		µJ
E_{off}	Turn-off switching losses		-	13		

1. Applied between HIN_i, LIN_i and GND for i = U, V, W.
2. t_{on} and t_{off} include the propagation delay time of the internal drive. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the internally given gate driving condition.

Figure 3. Switching time test circuit

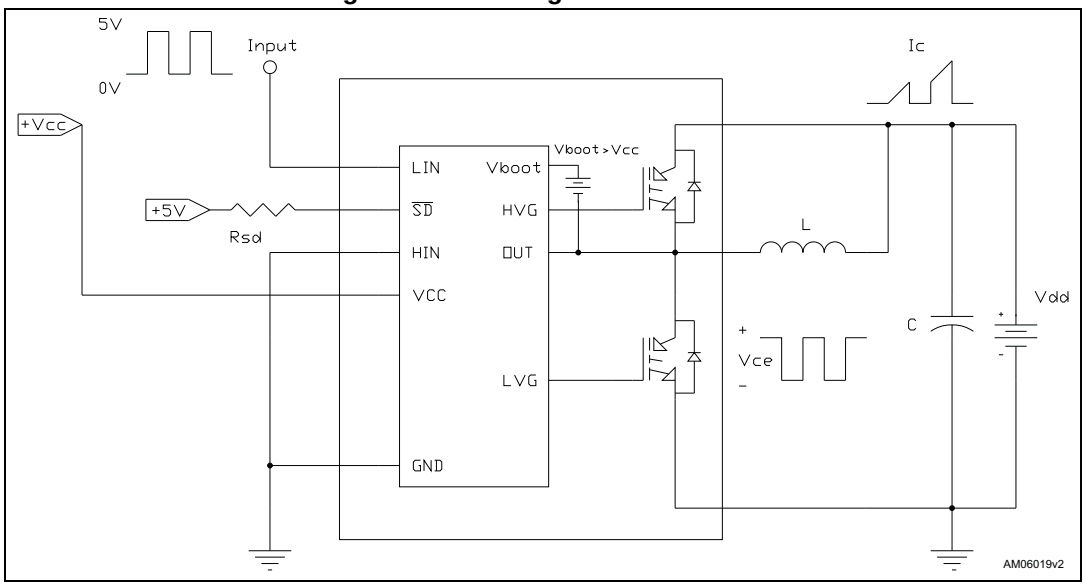
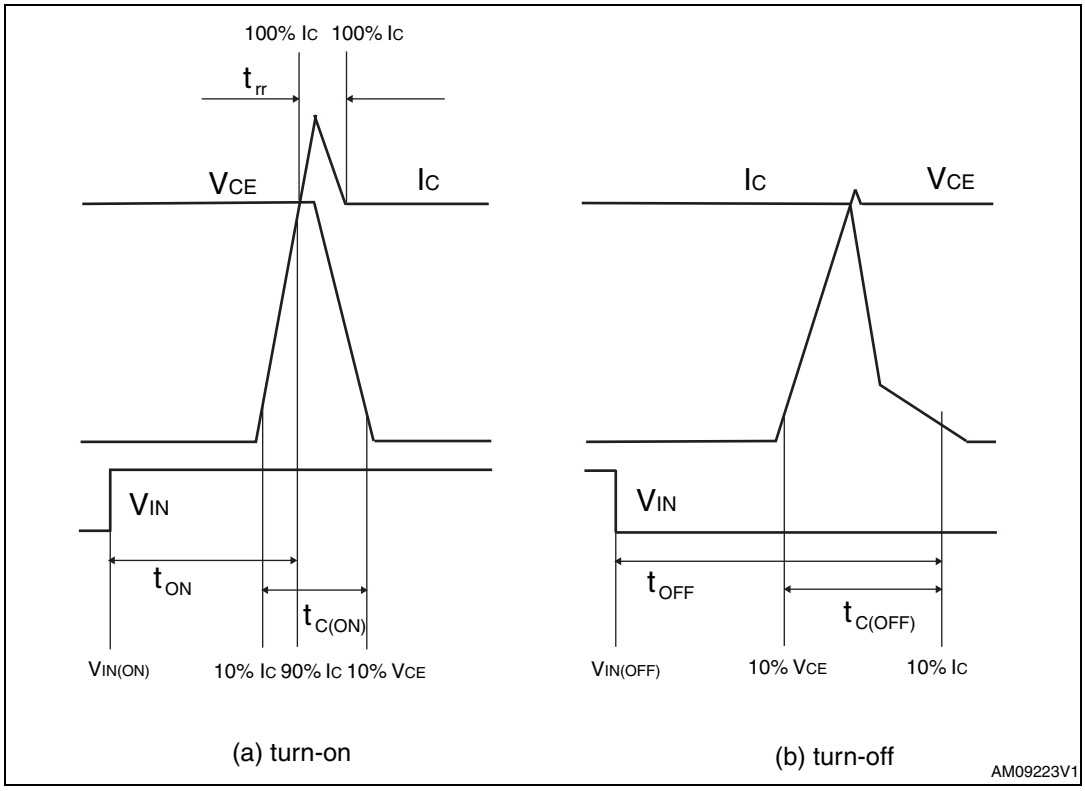


Figure 4. Switching time definition



Note: Figure 4 "Switching time definition" refers to HIN, LIN inputs (active high).

3.1 Control part

Table 8. Low voltage power supply (V_{CC} = 15 V unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC_hys}	V_{CC} UV hysteresis		1.2	1.5	1.8	V
V_{CC_thON}	V_{CC} UV turn ON threshold		11.5	12	12.5	V
V_{CC_thOFF}	V_{CC} UV turn OFF threshold		10	10.5	11	V
I_{qccu}	Undervoltage quiescent supply current	V_{CC} = 10 V T/$\overline{SD}$/OD = 5 V; LIN = 0; H_{IN} = 0, C_{IN} = 0			150	µA
I_{qcc}	Quiescent current	V_{cc} = 15 V T/$\overline{SD}$/OD = 5 V; LIN = 0; H_{IN} = 0, C_{IN} = 0			1	mA
V_{ref}	Internal comparator (CIN) reference voltage		0.5	0.54	0.58	V

Table 9. Bootstrapped voltage (V_{CC} = 15 V unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{BS_hys}	V_{BS} UV hysteresis		1.2	1.5	1.8	V
V_{BS_thON}	V_{BS} UV turn ON threshold		11.1	11.5	12.1	V
V_{BS_thOFF}	V_{BS} UV turn OFF threshold		9.8	10	10.6	V
I_{QBSU}	Undervoltage V_{BS} quiescent current	V_{BS} < 9 V T/$\overline{SD}$/OD = 5 V; LIN = 0; and HIN = 5 V; C_{IN} = 0		70	110	µA
I_{QBS}	V_{BS} quiescent current	V_{BS} = 15 V T/$\overline{SD}$/OD = 5 V; LIN = 0; and HIN = 5 V; C_{IN} = 0		200	300	µA
$R_{DS(on)}$	Bootstrap driver on resistance	LVG ON		120		Ω

Table 10. Logic inputs (V_{CC} = 15 V unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{il}	Low logic level voltage		0.8		1.1	V
V_{ih}	High logic level voltage		1.9		2.25	V
I_{HINh}	HIN logic “1” input bias current	HIN = 15 V	20	40	100	µA
I_{HINl}	HIN logic “0” input bias current	HIN = 0 V			1	µA
I_{LINh}	LIN logic “1” input bias current	LIN = 15 V	20	40	100	µA
I_{LINl}	LIN logic “0” input bias current	LIN = 0 V			1	µA
I_{SDh}	$\overline{SD}$ logic “0” input bias current	$\overline{SD}$ = 15 V	220	295	370	µA
I_{SDl}	$\overline{SD}$ logic “1” input bias current	$\overline{SD}$ = 0 V			3	µA
Dt	Dead time	see *Figure 9*		180		ns

Table 11. OP AMP characteristics (V_{CC} = 15 V unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage	V_{ic} = 0 V, V_o = 7.5 V			6	mV
I_{io}	Input offset current	V_{ic} = 0 V, V_o = 7.5 V		4	40	nA
I_{ib}	Input bias current (1)			100	200	nA
V_{icm}	Input common mode voltage range		0			V
V_{OL}	Low level output voltage	R_L = 10 kΩ to V_{CC}		75	150	mV
V_{OH}	High level output voltage	R_L = 10 kΩ to GND	14	14.7		V
I_o	Output short-circuit current	Source, V_{id} = +1; V_o = 0 V	16	30		mA
		Sink, V_{id} = -1; V_o = V_{CC}	50	80		mA
SR	Slew rate	V_i = 1 - 4 V; C_L = 100 pF; unity gain	2.5	3.8		V/µs
GBWP	Gain bandwidth product	V_o = 7.5 V	8	12		MHz
A_{vd}	Large signal voltage gain	R_L = 2 kΩ	70	85		dB
SVR	Supply voltage rejection ratio	vs. V_{CC}	60	75		dB
CMRR	Common mode rejection ratio		55	70		dB

1. The direction of input current is out of the IC.

Table 12. Sense comparator characteristics (V_{CC} = 15 V unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{ib}	Input bias current	V_{CIN} = 1 V			3	µA
V_{od}	Open drain low level output voltage	I_{od} = 3 mA			0.5	V
R_{ON_OD}	Open drain low level output resistance	I_{od} = 3 mA		166		Ω
R_{PD_SD}	$\overline{SD}$ pull down resistor(1)			125		kΩ
t_{d_comp}	Comparator delay	T/$\overline{SD}$/OD pulled to 5 V through 100 kΩ resistor		90	130	ns
SR	Slew rate	C_L = 180 pF; R_{pu} = 5 kΩ		60		V/µsec

Table 12. Sense comparator characteristics (V_{CC} = 15 V unless otherwise specified) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{sd}	Shutdown to high / low side driver propagation delay	V_{OUT} = 0, V_{boot} = V_{CC}, V_{IN} = 0 to 3.3 V	50	125	200	ns
t_{isd}	Comparator triggering to high / low side driver turn-off propagation delay	Measured applying a voltage step from 0 V to 3.3 V to pin CIN	50	200	250	

1. equivalent value derived from the resistances of three drivers in parallel

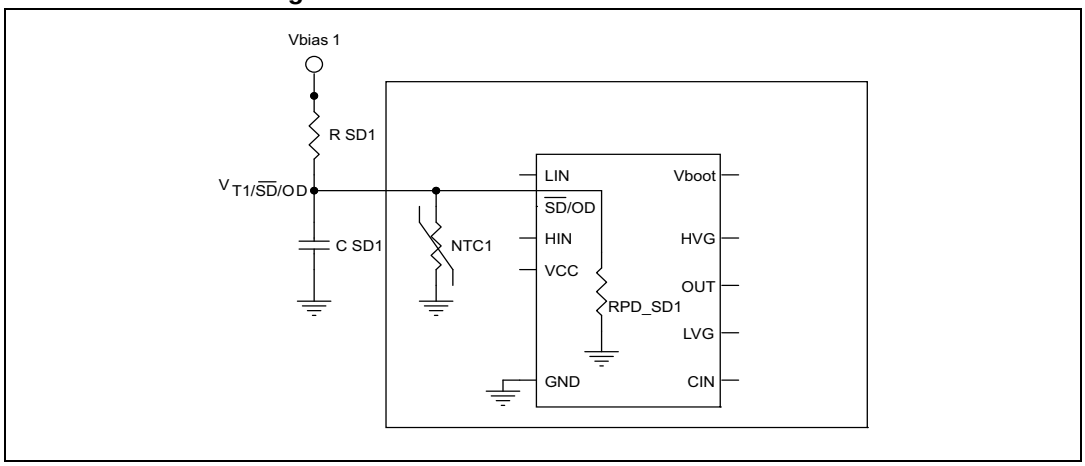
Table 13. Truth table

Condition	Logic input (V_I)			Output	
	T/$\overline{SD}$/OD	LIN	HIN	LVG	HVG
Shutdown enable half-bridge tri-state	L	X(1)	X(1)	L	L
Interlocking half-bridge tri-state	H	H	H	L	L
0 “logic state” half-bridge tri-state	H	L	L	L	L
1 “logic state” low side direct driving	H	H	L	H	L
1 “logic state” high side direct driving	H	L	H	L	H

1. X = don’t care

3.1.1 NTC thermistor

Figure 5. Internal structure of SD and NTC(a)



a. RPD_SD: equivalent value as result of resistances of three drivers in parallel.

Figure 6. Equivalent resistance (NTC//R_{PD_SD})

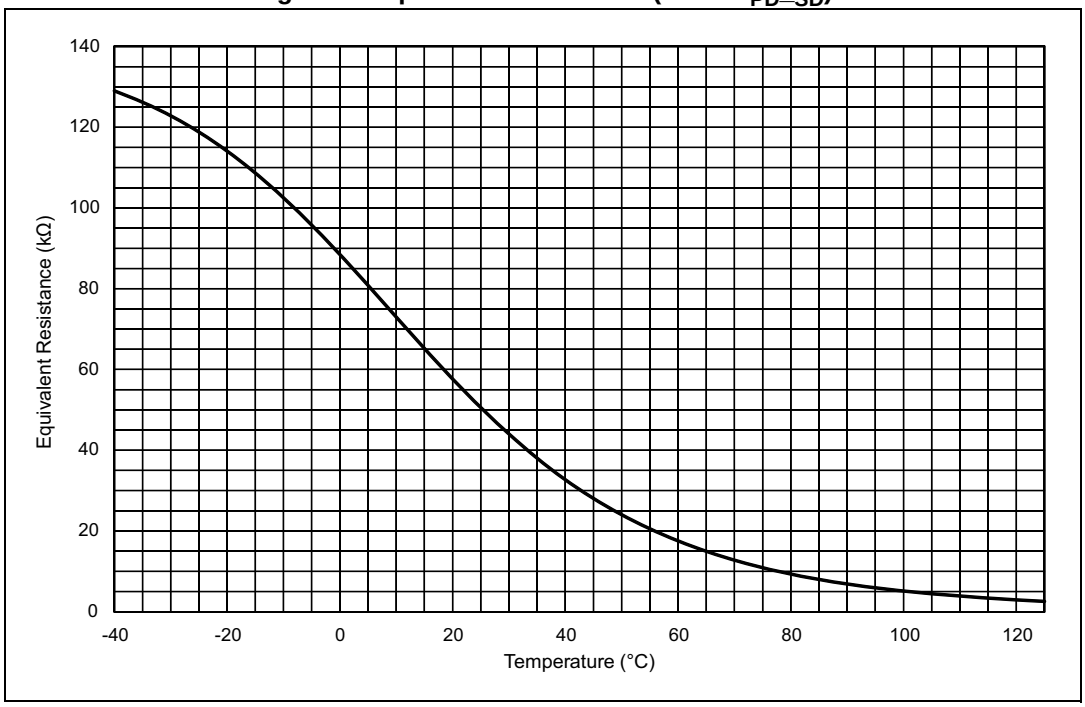


Figure 7. Equivalent resistance (NTC//R_{PD_SD}) zoom

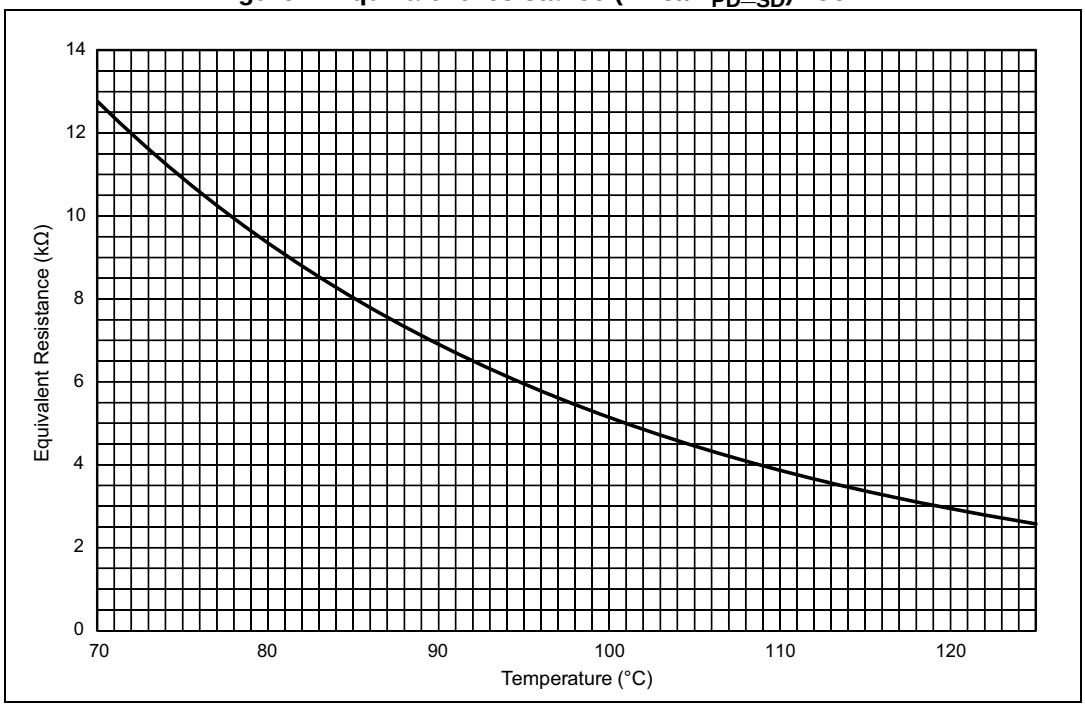
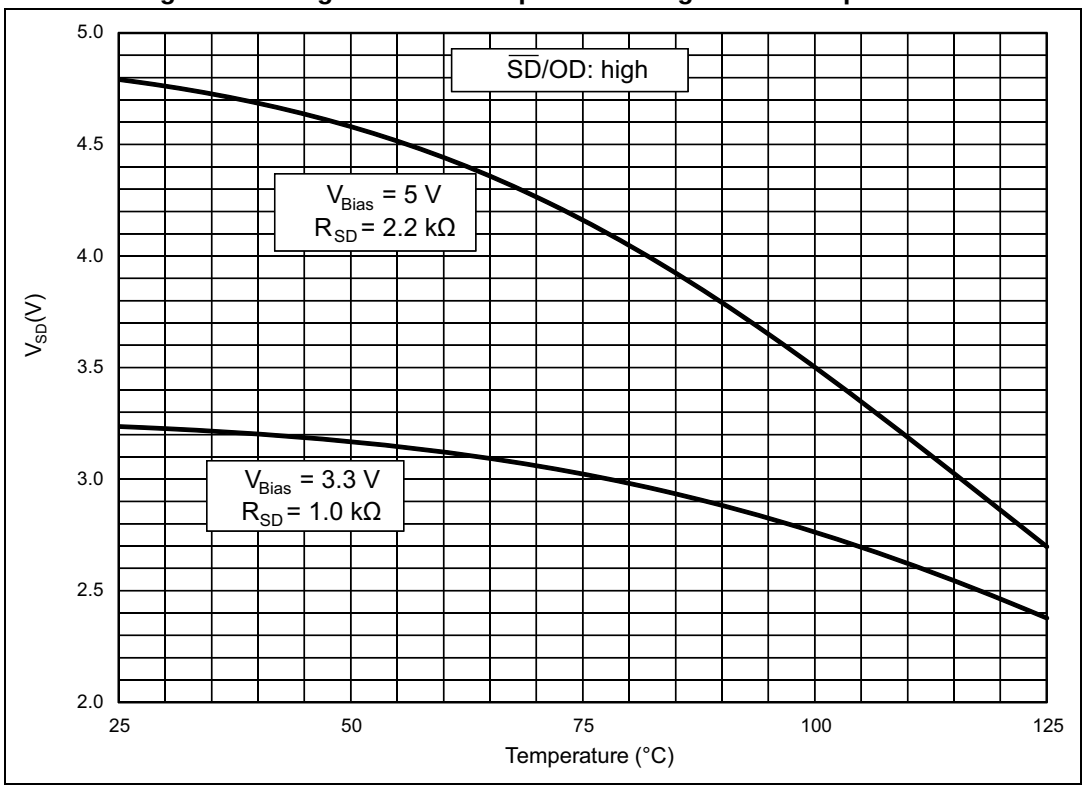
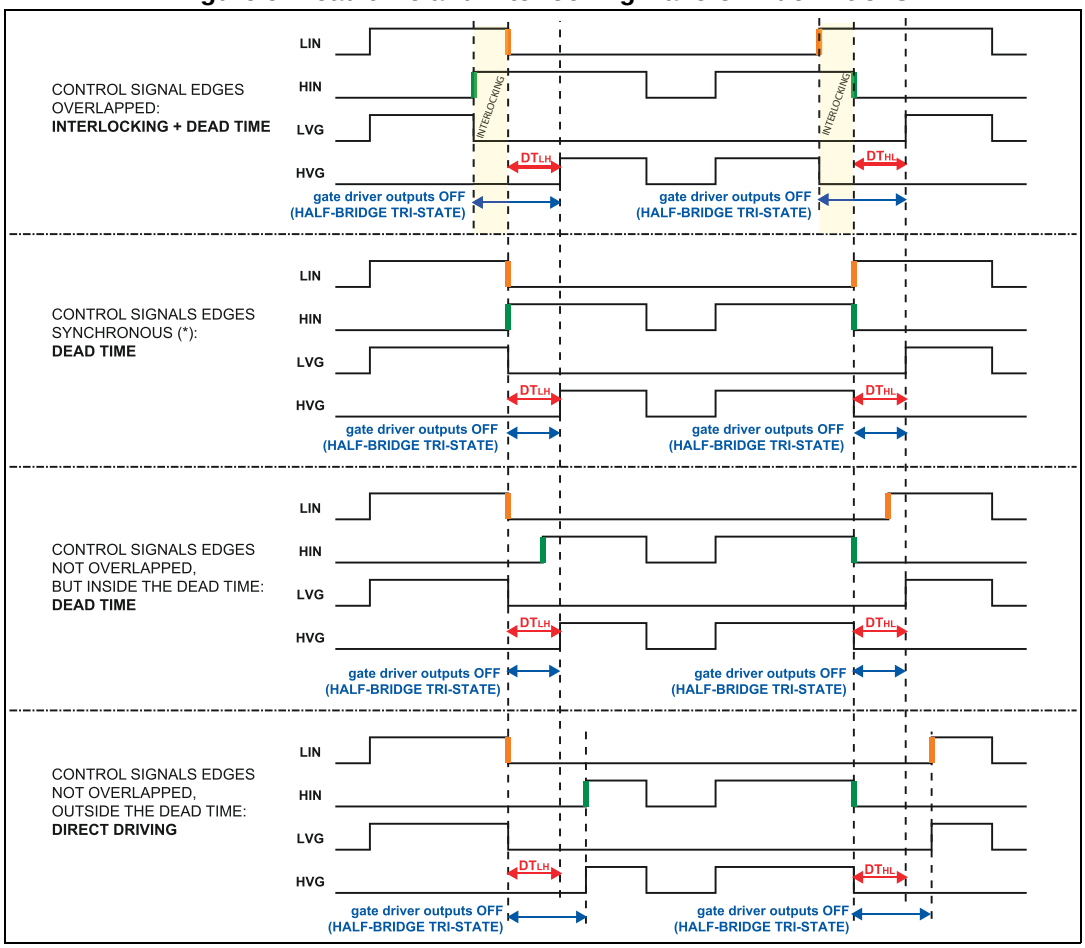


Figure 8. Voltage of T1/$\overline{SD}$/OD pin according to NTC temperature



3.2 Waveform definitions

Figure 9. Dead time and interlocking waveform definitions



4 Smart shutdown function

The device integrates a comparator for fault sensing purposes. The comparator has an internal voltage reference V_{REF} connected to the inverting input, while the non-inverting input on pin (CIN) can be connected to an external shunt resistor for simple overcurrent protection.

When the comparator triggers, the device is set to the Shutdown state and both its outputs are switched to the low-level setting, causing the half bridge to enter a tri-state.

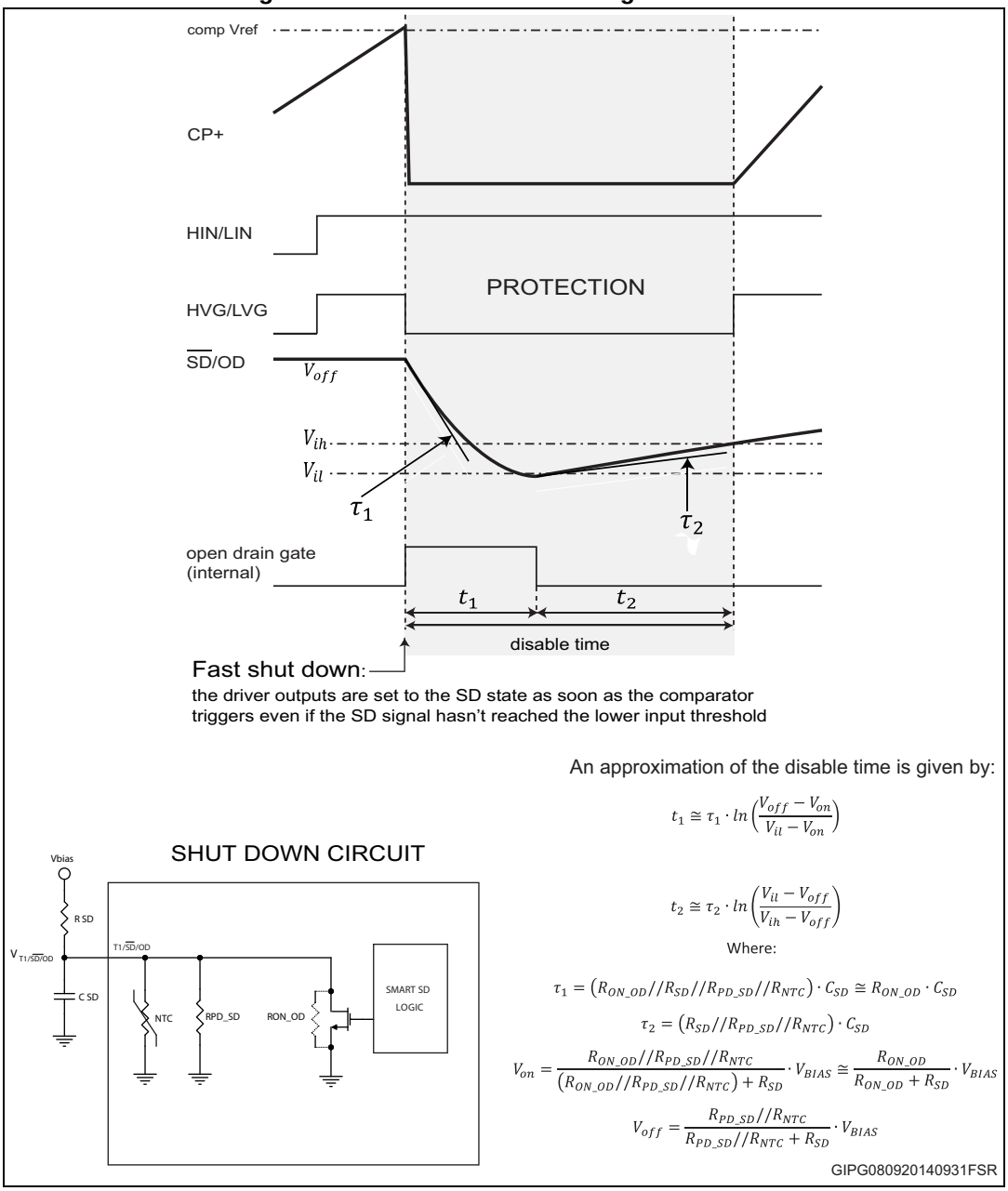
In common overcurrent protection architectures, the comparator output is usually connected to the Shutdown input through an RC network that provides a mono-stable circuit which implements a protection time following a fault condition.

Our smart shutdown architecture immediately turns off the output gate driver in case of overcurrent along a preferential path for the fault signal which directly switches off the outputs. The time delay between the fault and output shutdown no longer depends on the RC values of the external network connected to the shutdown pin. At the same time, the DMOS connected to the open-drain output (pin T1/$\overline{SD}$/OD) is turned on by the internal logic, which holds it on until the shutdown voltage is lower than the logic input lower threshold (Vil).

Also, the smart shutdown function allows increasing the real disable time without increasing the constant time of the external RC network.

An NTC thermistor for temperature monitoring is internally connected in parallel to the $\overline{SD}$ pin. To avoid undesired shutdown, keep the voltage $V_{T1/\overline{SD}/OD}$ higher than the high-level logic threshold by setting the pull-up resistor $R_{\overline{SD}}$ to 1 kΩ or 2.2 kΩ for the 3.3 V or 5 V MCU power supplies, respectively.

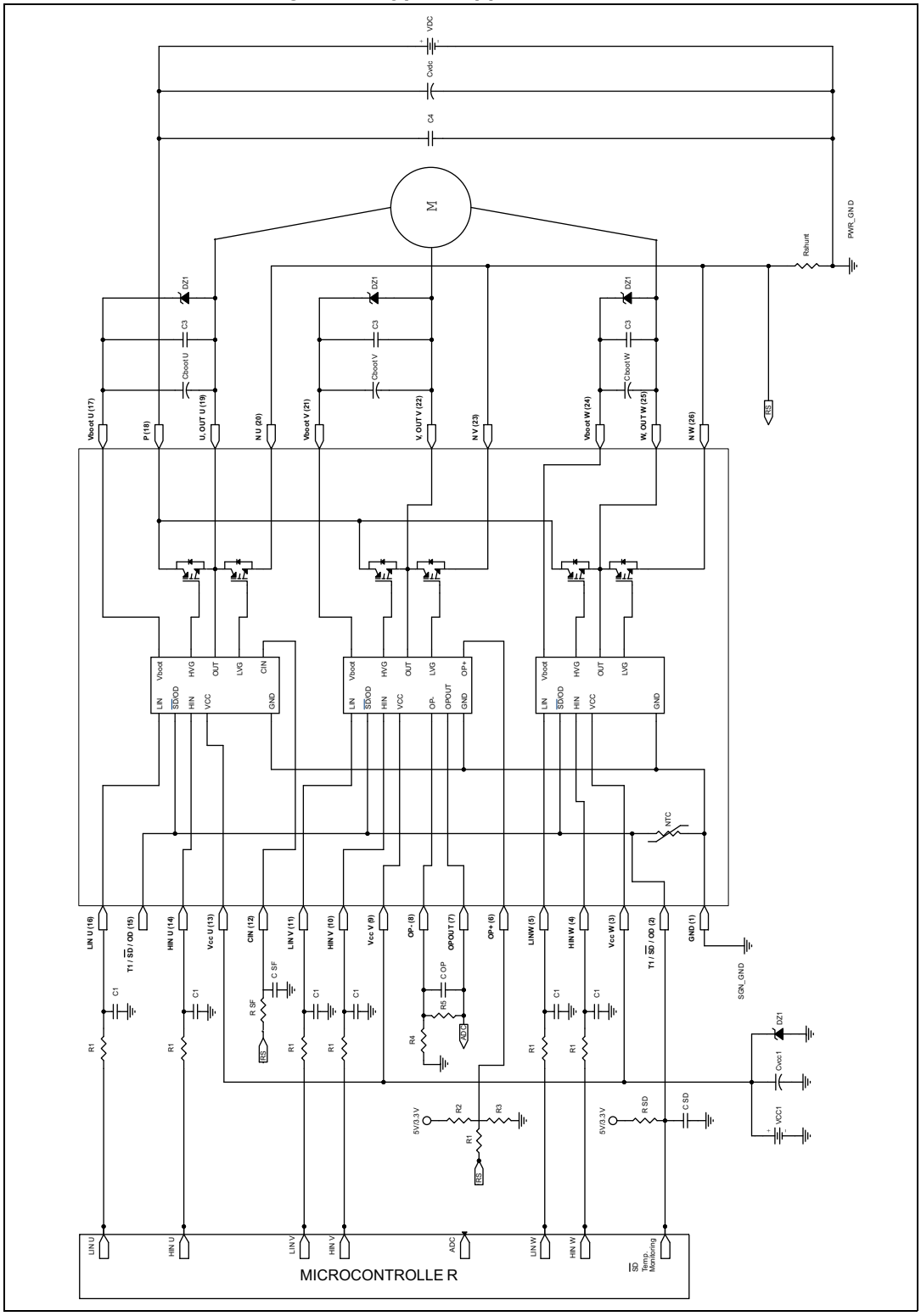
Figure 10. Smart shutdown timing waveforms



Please refer to *Table 12* for internal propagation delay time details.

5 Application information

Figure 11. Typical application circuit



5.1 Recommendations

- HIN and LIN are active-high logic input signals, each having an integrated 500 kΩ (typ.) pull-down resistor. Wire each input as short as possible and use RC filters (R1, C1) on each to prevent input signal oscillation. The filters should have a time constant of approximately 100 ns and must be placed as close as possible to the IPM input pins.
- Use a bypass capacitor Cvcc (aluminum or tantalum) to reduce the transient circuit demand on the power supply and a decoupling capacitor C2 (from 100 to 220 nF, ceramic with low ESR), placed as close as possible to each Vcc pin and in parallel to the bypass capacitor, to reduce high frequency switching noise distributed on the power supply lines.
- To prevent circuit malfunction, place an RC filter (RSF, CSF) with a time constant (RSF x CSF) of 1µs as close as possible to the CIN pin.
- The $\overline{SD}$ is an input/output pin (open drain type if used as output). An integrated NTC thermistor is connected internally between the $\overline{SD}$ pin and GND. The pull-up resistor RSD causes the voltage VSD-GND to decrease as the temperature increases. To always maintain the voltage above the high-level logic threshold, use a 1 kΩ or 2.2 kΩ pull-up resistor for a 3.3 V or 5 V MCU power supply, respectively. Size the filter on $\overline{SD}$ appropriately to obtain the desired re-start time after a fault event, and locate it as close as possible to the $\overline{SD}$ pin.
- Filter high-frequency disturbances by placing the decoupling capacitor C3 (from 100 to 220 nF, ceramic with low ESR) in parallel with each Cboot.
- Prevent overvoltage with Zener diodes DZ1 between the V_{CC} pins and GND and in parallel with each Cboot.
- Locate the decoupling capacitor C4 (from 100 to 220 nF, ceramic with low ESR) in parallel with the electrolytic capacitor Cvdc to prevent surge destruction. Place capacitors C4 (especially) and Cvdc as close as possible to the IPM.
- By integrating an application-specific type HVIC inside the module, direct coupling to the MCU terminals without an opto-coupler is possible.
- Use low inductance shunt resistors for phase leg current sensing.
- The wiring between N pins, the shunt resistor and PWR_GND should be as short as possible.
- Connect SGN_GND to PWR_GND at only one point (near the shunt resistor terminal), to avoid any malfunction due to power ground fluctuation.

Table 14. Recommended operating conditions

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{PN}	Supply voltage	Applied between P-Nu, Nv, Nw		300	500	V
V_{CC}	Control supply voltage	Applied between V_{CC}-GND	13.5	15	18	V
V_{BS}	High side bias voltage	Applied between V_{BOOTi}-OUT_i for i = U, V, W	13		18	V
t_{dead}	Blanking time to prevent Arm-short	For each input signal	1.5			µs

Table 14. Recommended operating conditions (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
f_{PWM}	PWM input signal	-40°C < T_c < 100°C -40°C < T_j < 125°C			25	kHz
T_C	Case operation temperature				100	°C

6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 12. NDIP-26L drawing

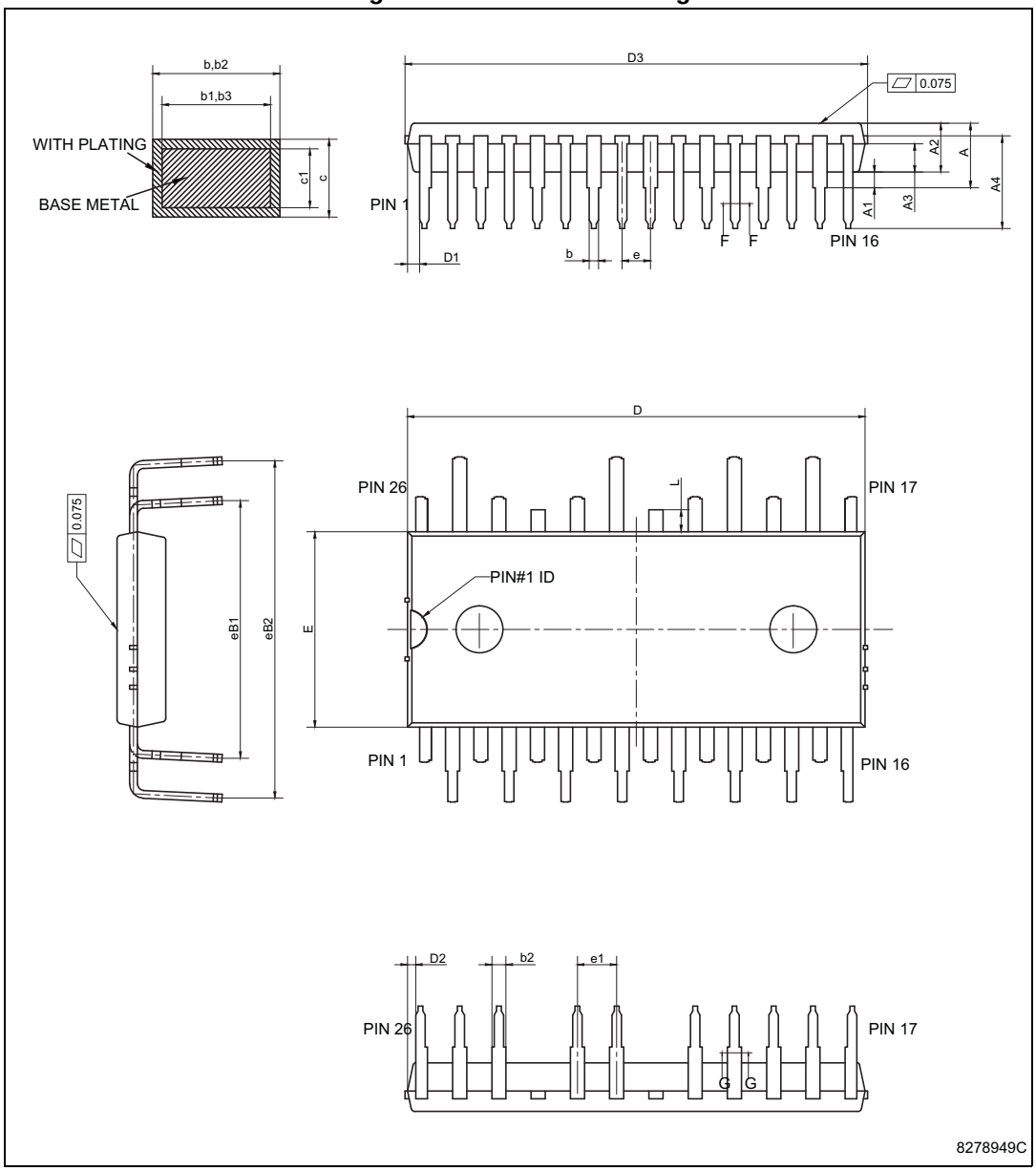
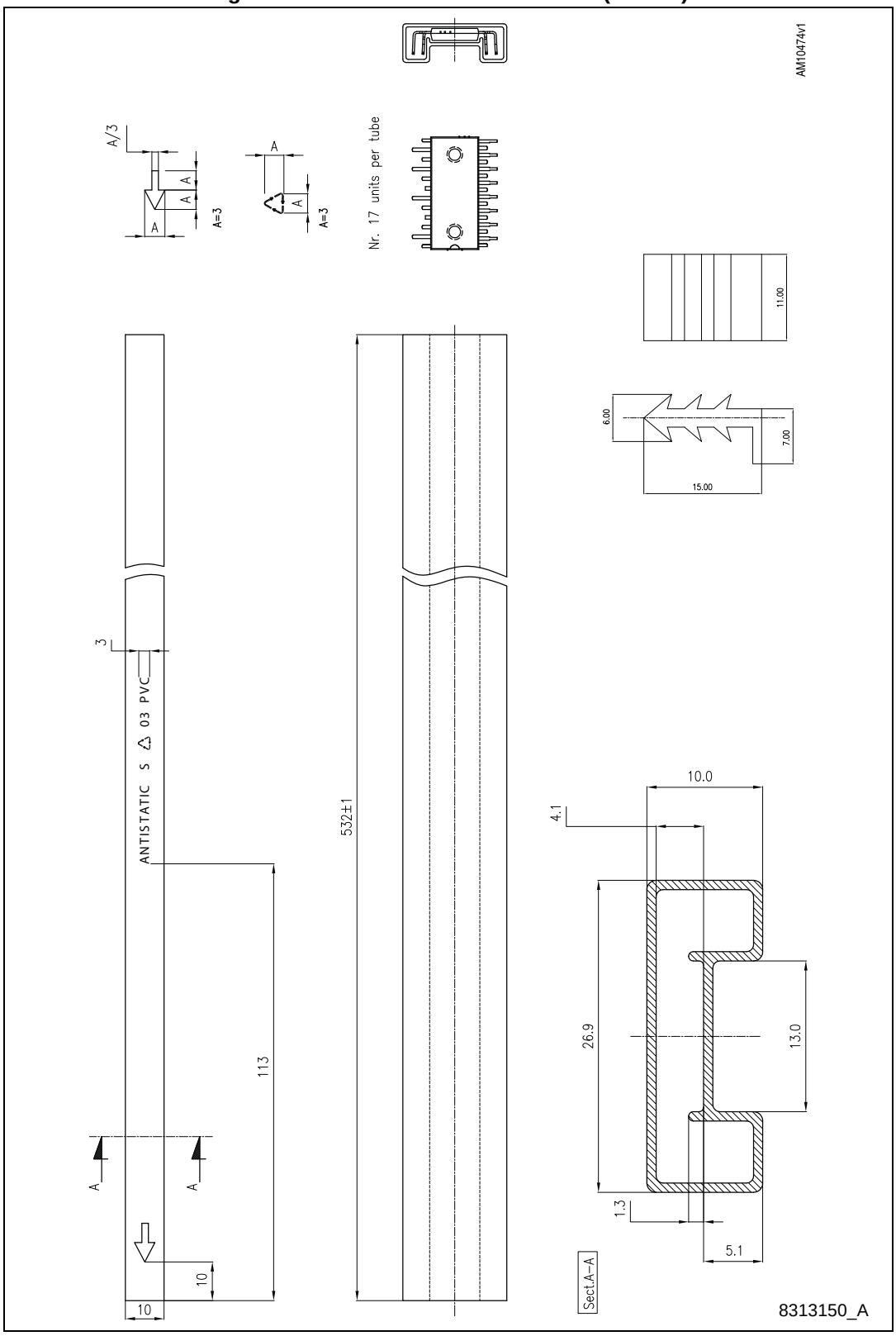


Table 15.NDIP-26L mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A			4.40
A1	0.80	1.00	1.20
A2	3.00	3.10	3.20
A3	1.70	1.80	1.90
A4	5.70	5.90	6.10
b	0.53		0.72
b1	0.52	0.60	0.68
b2	0.83		1.02
b3	0.82	0.90	0.98
c	0.46		0.59
c1	0.45	0.50	0.55
D	29.05	29.15	29.25
D1	0.50	0.77	1.00
D2	0.35	0.53	0.70
D3			29.55
E	12.35	12.45	12.55
e	1.70	1.80	1.90
e1	2.40	2.50	2.60
eB1	16.10	16.40	16.70
eB2	21.18	21.48	21.78
L	1.24	1.39	1.54

Figure 13. NDIP-26L tube dimensions (in mm.)



Note: Base quantity 17 pcs, bulk quantity 476 pcs.

7 Revision history

Table 16. Document revision history

Date	Revision	Changes
19-Dec-2013	1	Initial release.
23-Apr-2014	2	Updated *Figure 1: Internal schematic diagram* and *Section 3: Electrical characteristics*. Minor text changes.
05-May-2014	3	Updated features in cover page.
04-Nov-2014	4	Updated: – *Figure 1: Internal schematic diagram* – *Table 10: Logic inputs (VCC = 15 V unless otherwise specified)* – *Table 12: Sense comparator characteristics (VCC = 15 V unless otherwise specified)* – *Section 3.1.1: NTC thermistor* – *Section 4: Smart shutdown function* description – *Figure 10: Smart shutdown timing waveforms* – *Figure 11: Typical application circuit* – *Section 5.1: Recommendations* – minor text changes
07-Nov-2014	5	Minor text and formatting edits throughout document.

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