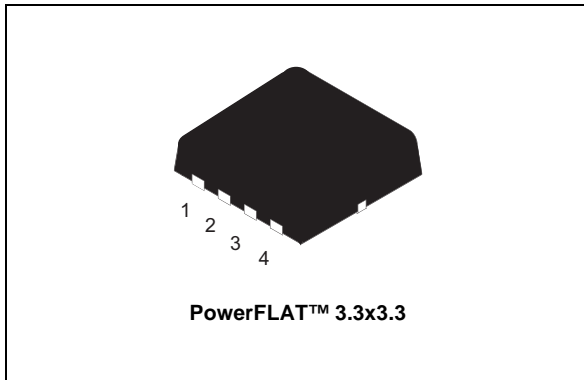


## N-channel 100 V, 0.062 $\Omega$ typ., 4.5 A STripFET™ VII DeepGATE™ Power MOSFET in a PowerFLAT™ 3.3x3.3 package

Datasheet - production data



### Features

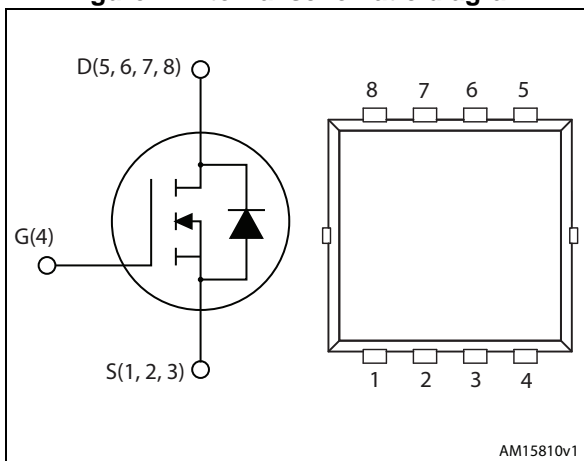
Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STL4N10F7	100 V	0.07 $\Omega$	4.5 A

- N-channel enhancement mode
- Lower R<sub>DS(on)</sub> x area vs previous generation
- 100% avalanche rated

### Applications

- Switching applications

Figure 1. Internal schematic diagram



### Description

This device utilizes the 7<sup>th</sup> generation of design rules of ST's proprietary STripFET™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest R<sub>DS(on)</sub> in all packages.

Table 1. Device summary

Order code	Marking	Package	Packaging
STL4N10F7	4N1F7	PowerFLAT™ 3.3x3.3	Tape and reel

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	100	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_{amb} = 25\text{ }^\circ\text{C}$	4.5	A
$I_D^{(1)}$	Drain current (continuous) at $T_{amb}=100\text{ }^\circ\text{C}$	3.2	A
$I_{DM}^{(1)(2)}$	Drain current (pulsed)	18	A
$I_D^{(3)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	18	A
$I_D^{(3)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	11.25	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	72	A
$P_{TOT}^{(3)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	50	W
$P_{TOT}^{(1)}$	Total dissipation at $T_{amb} = 25\text{ }^\circ\text{C}$	2.9	W
$T_J$	Operating junction temperature	-55 to 150	$^\circ\text{C}$
$T_{stg}$	Storage temperature		$^\circ\text{C}$

1. The value is rated according  $R_{thj-amb}$
2. Pulse width limited by safe operating area.
3. This value is rated according to  $R_{thj-case}$

**Table 3. Thermal resistance**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.50	$^\circ\text{C}/\text{W}$
$R_{thj-amb}^{(1)}$	Thermal resistance junction-amb	42.8	$^\circ\text{C}/\text{W}$
$R_{thj-amb}^{(2)}$	Thermal resistance junction-amb	63.5	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1inch<sup>2</sup>, 2oz Cu,  $t < 10\text{sec}$
2. When mounted on FR-4 board of 1inch<sup>2</sup>, 2oz Cu, steady state

## 2 Electrical characteristics

( $T_{CASE}=25\text{ °C}$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu A, V_{GS} = 0$	100			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 100\text{ V}$			1	$\mu A$
		$V_{DS} = 100\text{ V}, T_C = 125\text{ °C}$			100	$\mu A$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = +20\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu A$	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 2.25\text{ A}$		0.062	0.07	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 50\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$	-	408	-	pF
$C_{oss}$	Output capacitance		-	112	-	pF
$C_{rss}$	Reverse transfer capacitance		-	10	-	pF
$Q_g$	Total gate charge	$V_{DD} = 50\text{ V}, I_D = 4.5\text{ A}$ $V_{GS} = 10\text{ V}$ (see Figure 14)	-	7.8	-	nC
$Q_{gs}$	Gate-source charge		-	3	-	nC
$Q_{gd}$	Gate-drain charge		-	1.7	-	nC

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 50\text{ V}, I_D = 2.25\text{ A}, R_G = 4.7\ \Omega, V_{GS} = 10\text{ V}$ (see Figure 13)	-	6.3	-	ns
$t_r$	Rise time		-	3	-	ns
$t_{d(off)}$	Turn-off delay time		-	11	-	ns
$t_f$	Fall time		-	4	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		4.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		18	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}= 2.25\text{ A}$ , $V_{GS}=0$	-		1.1	V
$t_{rr}$	Reverse recovery time	$I_{SD}= 2.25\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD}= 80\text{ V}$ , $T_J=150\text{ }^\circ\text{C}$ <i>(see Figure 18)</i>	-	30		ns
$Q_{rr}$	Reverse recovery charge		-	24		nC
$I_{RRM}$	Reverse recovery current		-	1.6		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

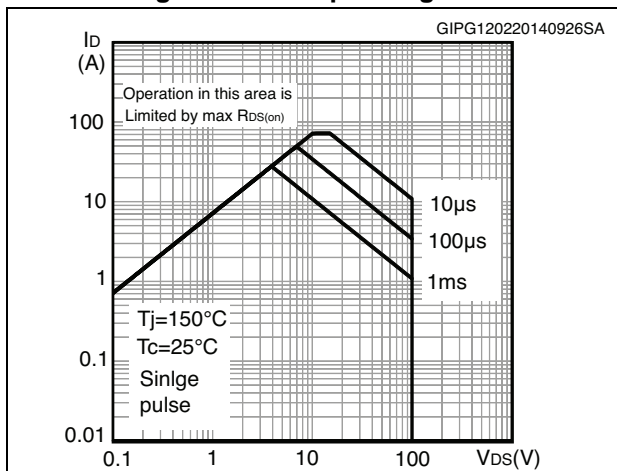


Figure 3. Thermal impedance

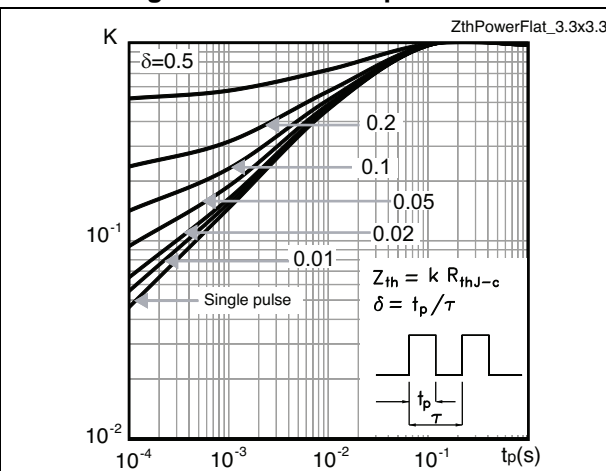


Figure 4. Output characteristics

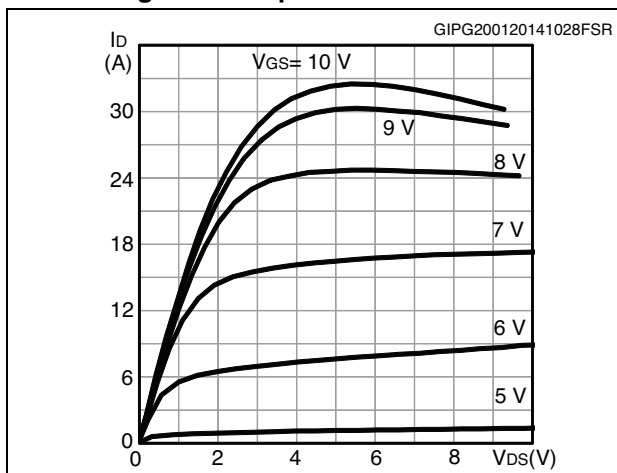


Figure 5. Transfer characteristics

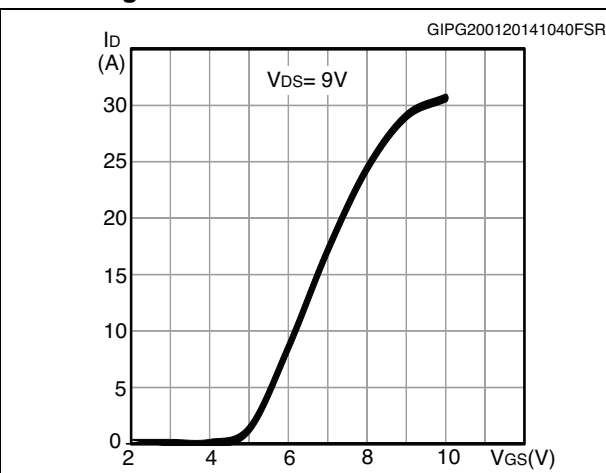


Figure 6. Gate charge vs gate-source voltage

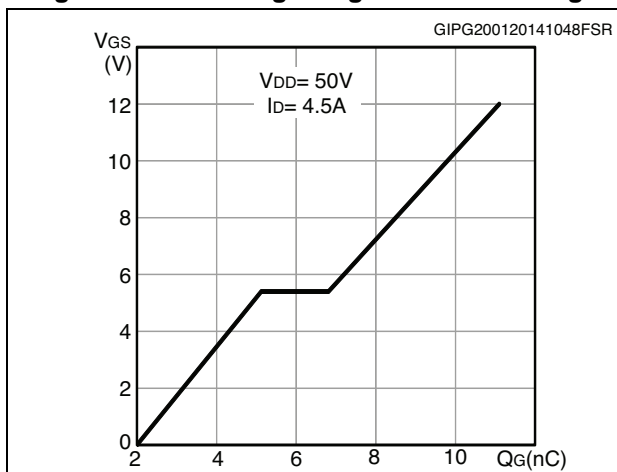


Figure 7. Static drain-source on-resistance

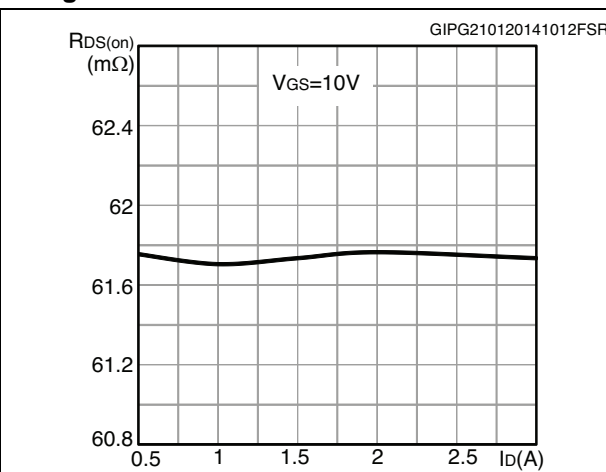


Figure 8. Capacitance variations

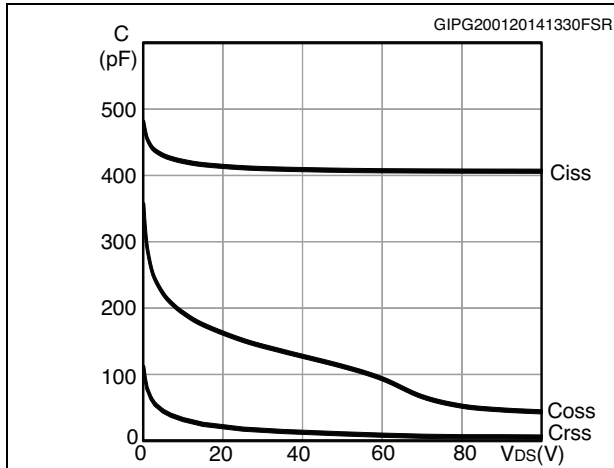


Figure 9. Normalized  $V_{(BR)DSS}$  vs temperature

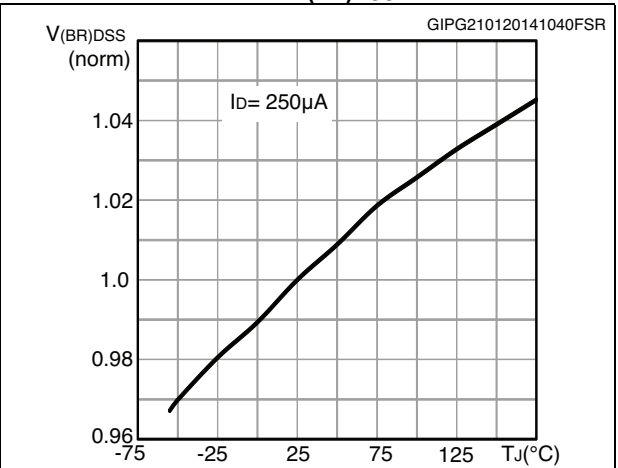


Figure 10. Normalized gate threshold voltage vs temperature

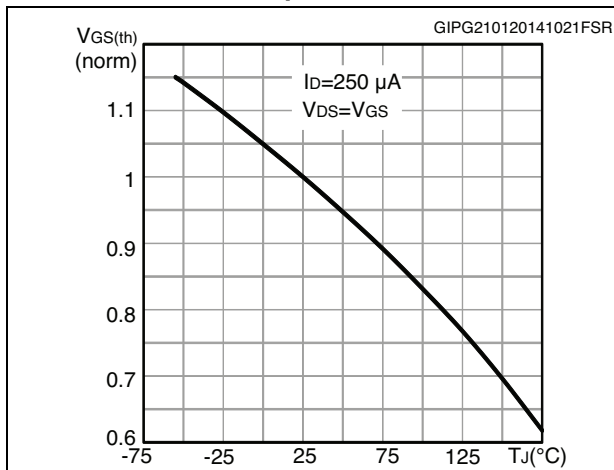


Figure 11. Normalized on-resistance vs temperature

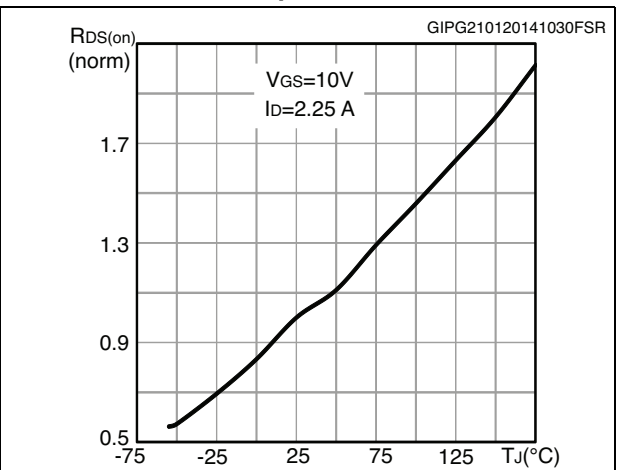
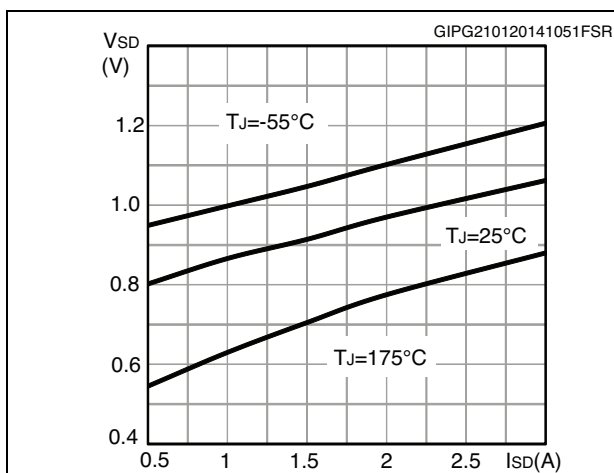


Figure 12. Source-drain diode forward characteristics



### 3 Test circuits

Figure 13. Switching times test circuit for resistive load

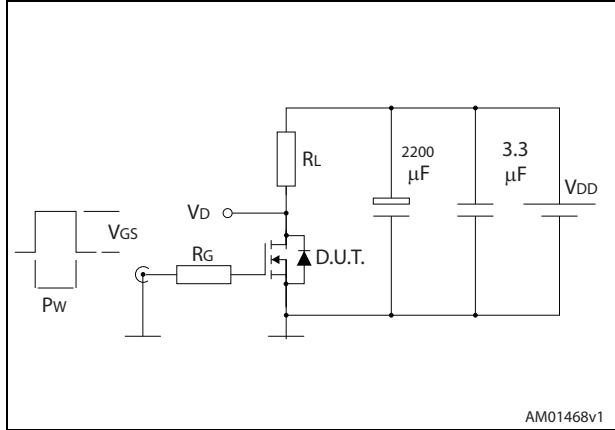


Figure 14. Gate charge test circuit

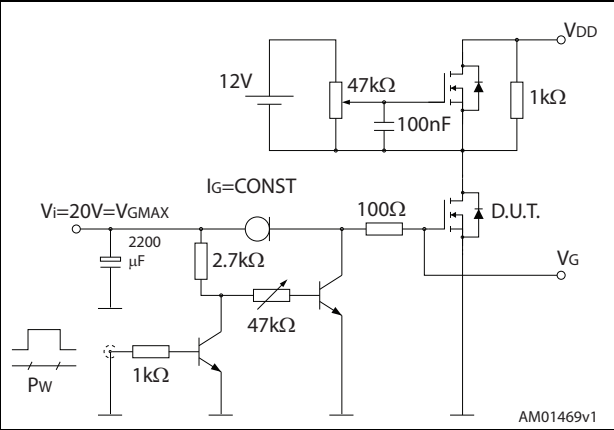


Figure 15. Test circuit for inductive load switching and diode recovery times

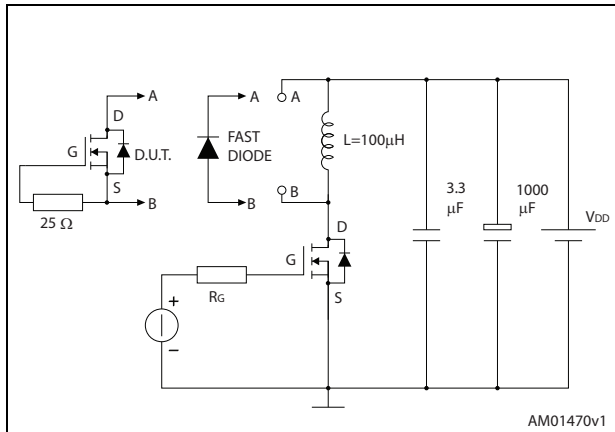


Figure 16. Unclamped inductive load test circuit

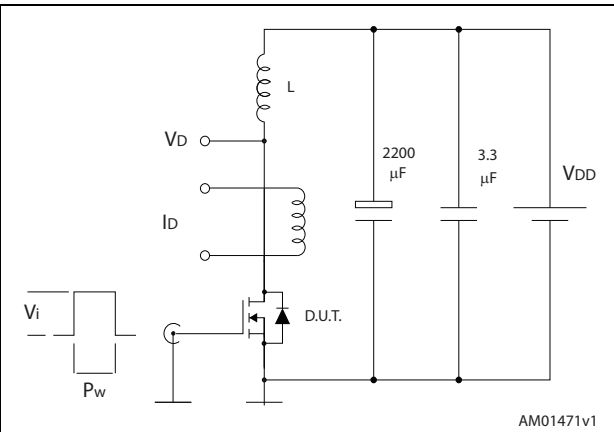


Figure 17. Unclamped inductive waveform

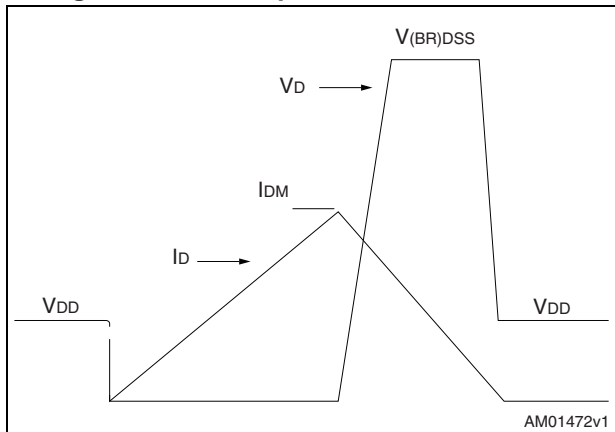
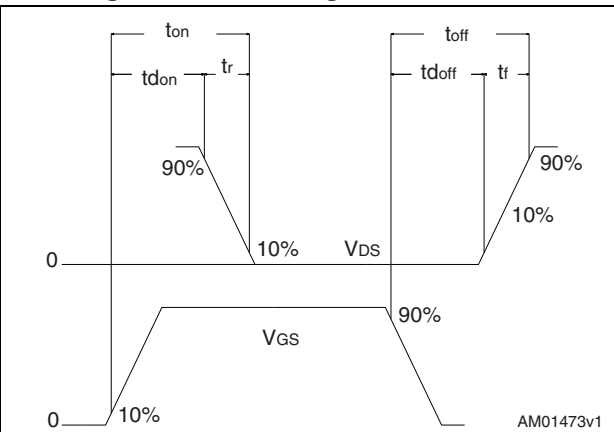


Figure 18. Switching time waveform



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Figure 19. PowerFLAT™ 3.3 x 3.3 drawing

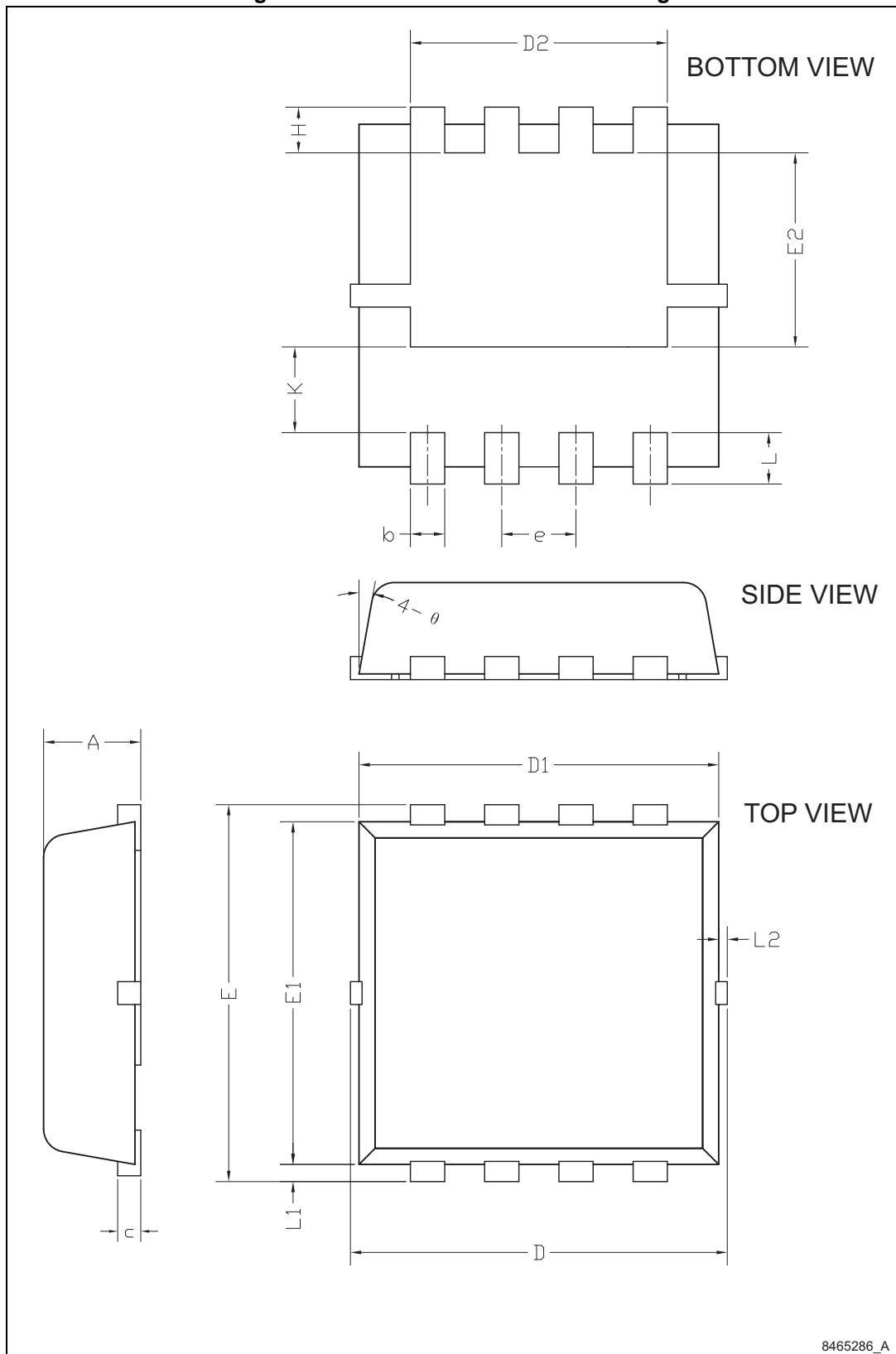
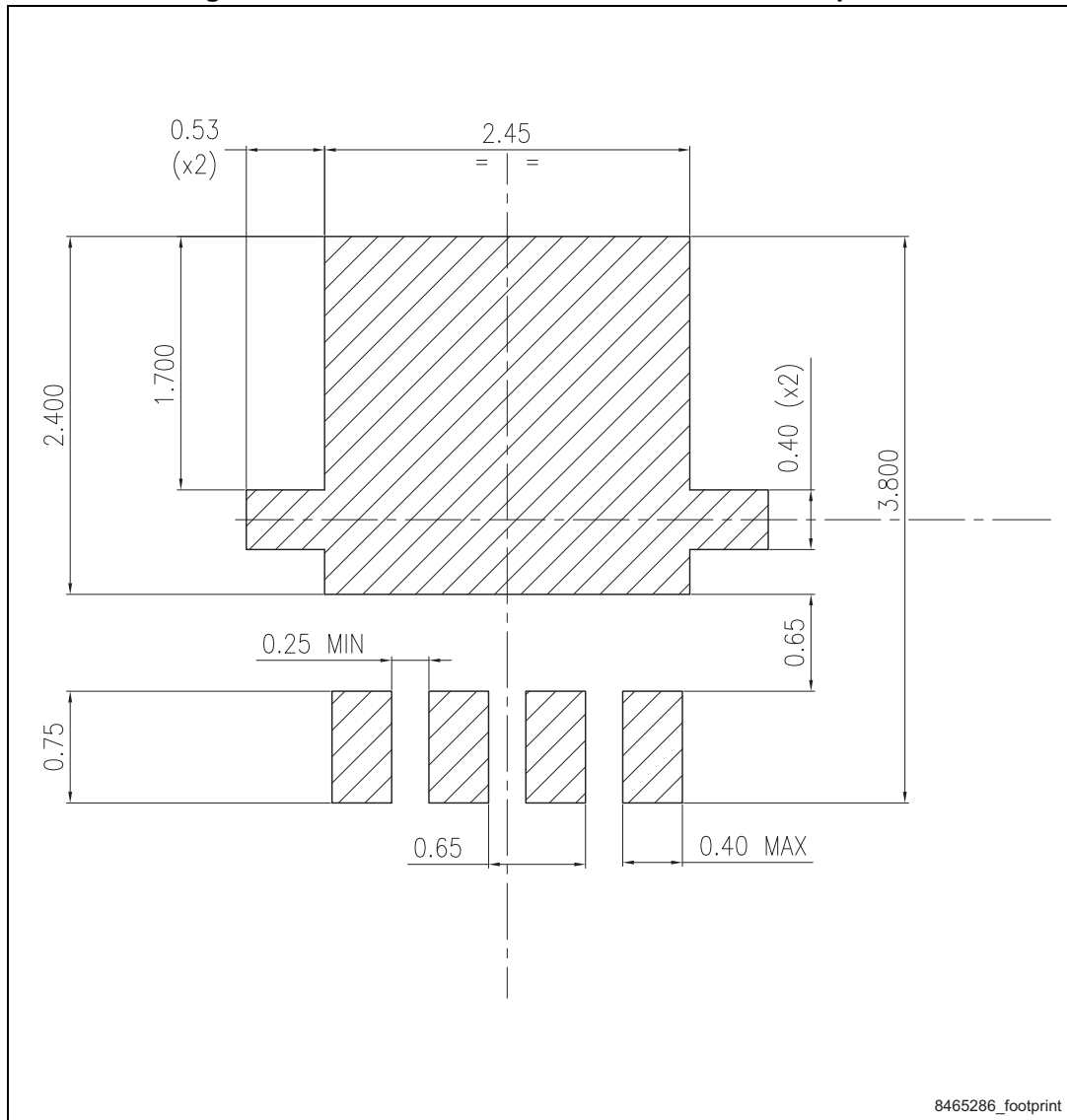


Table 8. PowerFLAT™ 3.3 x 3.3 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.70	0.80	0.90
b	0.25	0.30	0.39
c	0.14	0.15	0.20
D	3.10	3.30	3.50
D1	3.05	3.15	3.25
D2	2.15	2.25	2.35
e	0.55	0.65	0.75
E	3.10	3.30	3.50
E1	2.90	3.00	3.10
E2	1.60	1.70	1.80
H	0.25	0.40	0.55
K	0.65	0.75	0.85
L	0.30	0.45	0.60
L1	0.05	0.15	0.25
L2			0.15
∠	8°	10°	12°

Figure 20. PowerFLAT™ 3.3 x 3.3 recommended footprint



## 5 Revision history

Table 9. Document revision history

Date	Revision	Changes
10-Jul-2013	1	First release.
21-Jan-2014	2	– Inserted <a href="#">Section 2.1: Electrical characteristics (curves)</a> . – Document status promoted from preliminary to production data.
19-Feb-2014	3	– Added: $I_D$ (at $T_C=25\text{ °C}$ and $125\text{ °C}$ ), $I_{DM}$ and $P_{TOT}$ in <a href="#">Table 2</a> – Modified: <a href="#">Figure 2</a> and <a href="#">3</a> – Minor text changes
10-Mar-2014	4	– Modified: marking in <a href="#">Table 1</a> – Minor text changes

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