



N0118GA

SCR

22 July 2014

Product data sheet

1. General description

Planar passivated Silicon Controlled Rectifier with ultra-sensitive gate in a SOT54 (TO-92) plastic package.

2. Features and benefits

- High voltage capability
- Planar passivated for voltage ruggedness and reliability
- Ultra sensitive gate

3. Applications

- Electronic ballasts
- Safety shut down and protection circuits
- Sensing circuits
- Smoke detectors
- Switched Mode Power Supplies

4. Quick reference data

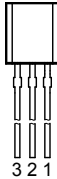

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	600	V
V_{RRM}	repetitive peak reverse voltage		-	-	600	V
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{\text{j(init)}} = 25\text{ }^{\circ}\text{C}$; $t_{\text{p}} = 10\text{ ms}$; Fig. 4 ; Fig. 5	-	-	8	A
$I_{\text{T(AV)}}$	average on-state current	half sine wave; $T_{\text{lead}} \leq 67\text{ }^{\circ}\text{C}$; Fig. 1	-	-	0.51	A
$I_{\text{T(RMS)}}$	RMS on-state current	half sine wave; $T_{\text{lead}} \leq 67\text{ }^{\circ}\text{C}$; Fig. 2 ; Fig. 3	-	-	0.8	A
Static characteristics						
I_{GT}	gate trigger current	$V_{\text{D}} = 12\text{ V}$; $I_{\text{T}} = 10\text{ mA}$; $T_{\text{j}} = 25\text{ }^{\circ}\text{C}$; Fig. 7	0.5	-	7	μA



5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	A	anode	 TO-92 (SOT54)	 sym037
2	G	gate		
3	K	cathode		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
N0118GA	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	600	V
V_{RRM}	repetitive peak reverse voltage		-	600	V
$I_{\text{T(AV)}}$	average on-state current	half sine wave; $T_{\text{lead}} \leq 67^\circ\text{C}$; Fig. 1	-	0.51	A
$I_{\text{T(RMS)}}$	RMS on-state current	half sine wave; $T_{\text{lead}} \leq 67^\circ\text{C}$; Fig. 2 ; Fig. 3	-	0.8	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{\text{j(init)}} = 25^\circ\text{C}$; $t_{\text{p}} = 10\text{ ms}$; Fig. 4 ; Fig. 5	-	8	A
		half sine wave; $T_{\text{j(init)}} = 25^\circ\text{C}$; $t_{\text{p}} = 8.3\text{ ms}$	-	9	A
I^2t	I^2t for fusing	$t_{\text{p}} = 10\text{ ms}$; SIN	-	0.32	A^2s
di_{T}/dt	rate of rise of on-state current	$I_{\text{T}} = 0.8\text{ A}$; $I_{\text{G}} = 10\text{ mA}$; $di_{\text{G}}/dt = 0.1\text{ A}/\mu\text{s}$	-	50	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current		-	1	A
V_{RGM}	peak reverse gate voltage		-	5	V
P_{GM}	peak gate power		-	2	W
$P_{\text{G(AV)}}$	average gate power	over any 20 ms period	-	0.1	W
T_{stg}	storage temperature		-40	150	$^\circ\text{C}$
T_{j}	junction temperature		-	125	$^\circ\text{C}$

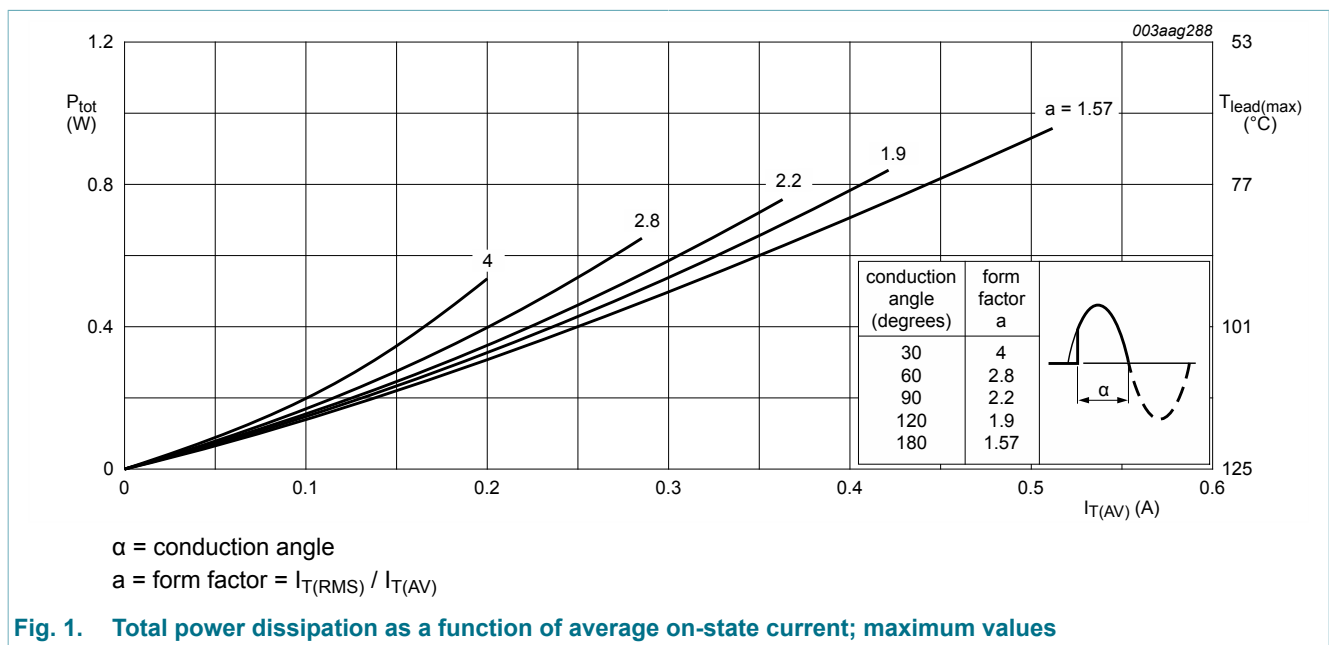


Fig. 1. Total power dissipation as a function of average on-state current; maximum values

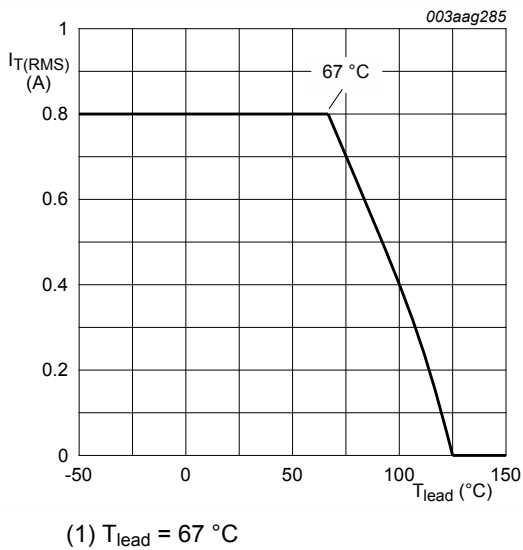


Fig. 2. RMS on-state current as a function of lead temperature; maximum values

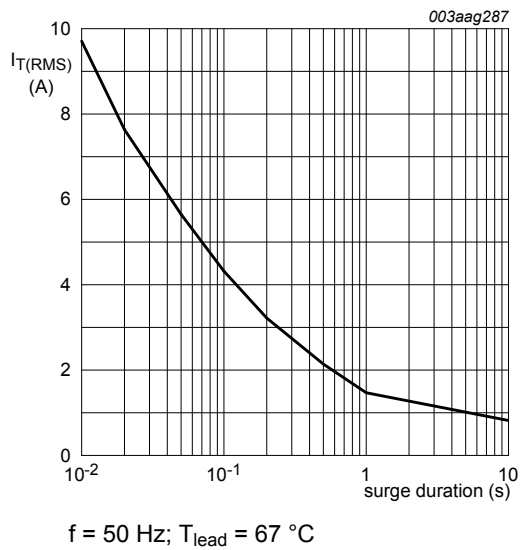


Fig. 3. RMS on-state current as a function of surge duration; maximum values

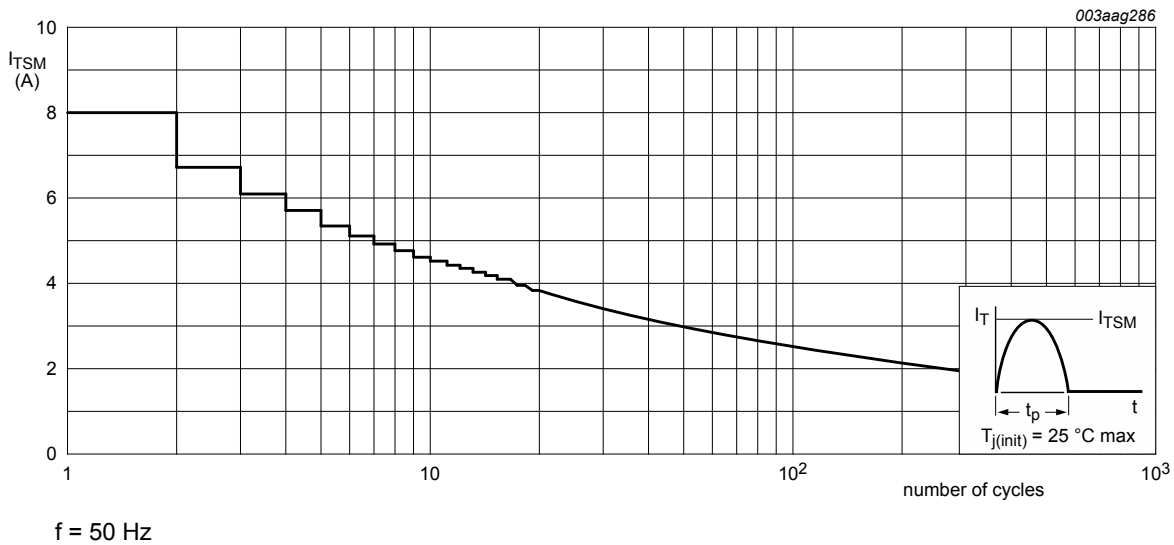
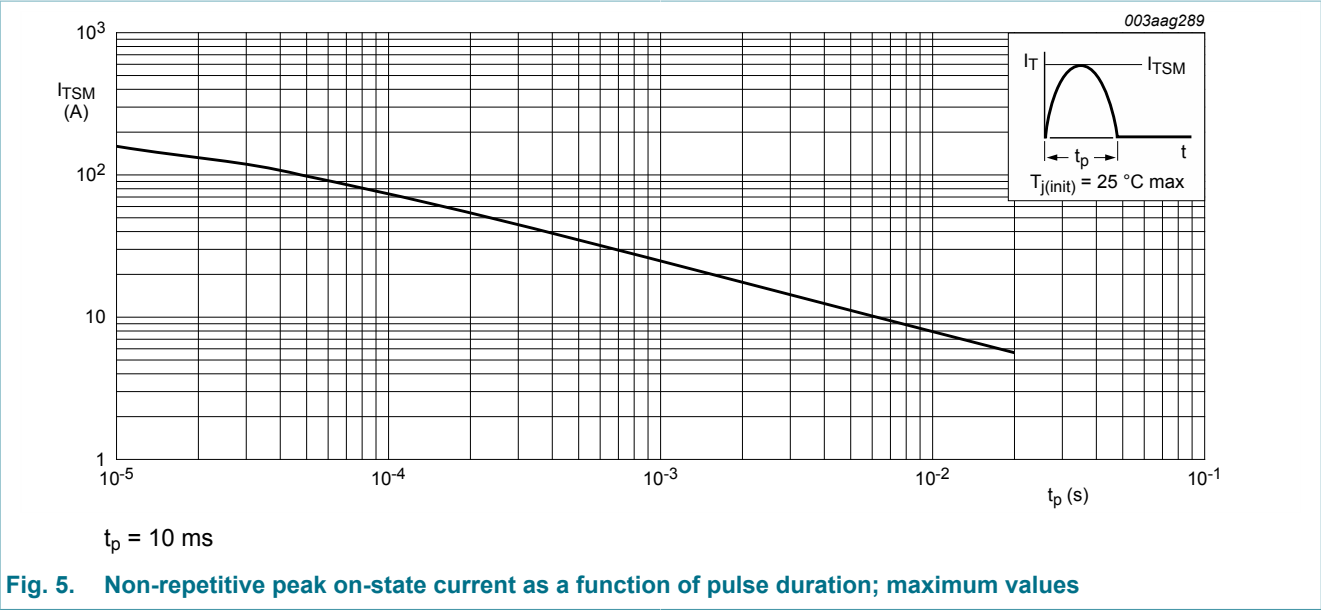


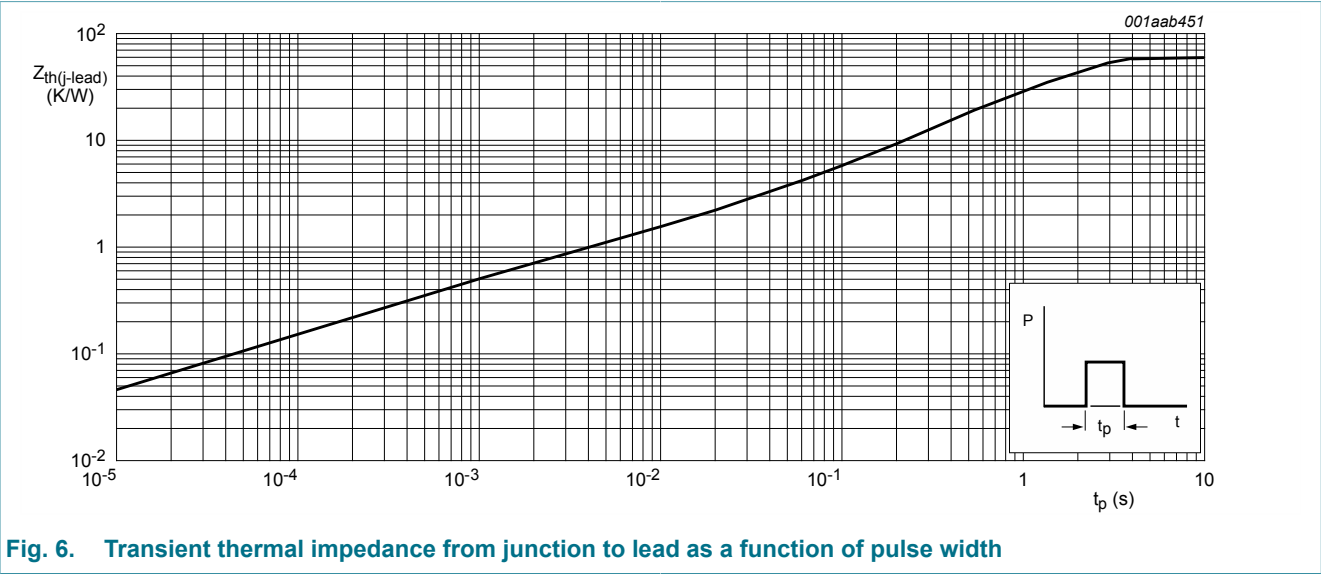
Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-lead)}$	thermal resistance from junction to lead	Fig. 6	-	-	60	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	printed circuit board mounted: lead length = 4 mm	-	150	-	K/W



9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I _{GT}	gate trigger current	V _D = 12 V; I _T = 10 mA; T _j = 25 °C; Fig. 7		0.5	-	7	μA
I _L	latching current	V _D = 12 V; I _G = 0.1 A; T _j = 25 °C; Fig. 8		-	-	6	mA
I _H	holding current	V _D = 12 V; T _j = 25 °C; Fig. 9 ; Fig. 10		-	-	5	mA
V _T	on-state voltage	I _T = 1.6 A; T _j = 25 °C; Fig. 11		-	1.4	1.95	V
V _{GT}	gate trigger voltage	V _D = 12 V; I _T = 0.1 A; T _j = 25 °C; Fig. 12		-	-	0.8	V
I _D	off-state current	V _D = 400 V; T _j = 25 °C		-	-	10	μA
		V _D = 600 V; T _j = 125 °C; R _{GK} = 1 kΩ		-	-	100	μA
I _R	reverse current	V _R = 600 V; T _j = 25 °C; R _{GK} = 1 kΩ		-	-	10	μA
		V _R = 600 V; T _j = 125 °C; R _{GK} = 1 kΩ		-	-	100	μA
Dynamic characteristics							
dV _D /dt	rate of rise of off-state voltage	V _{DM} = 402 V; T _j = 125 °C; R _{GK} = 1 kΩ; (V _{DM} = 67% of V _{DRM}); exponential waveform; Fig. 13 ; Fig. 14		75	-	-	V/μs

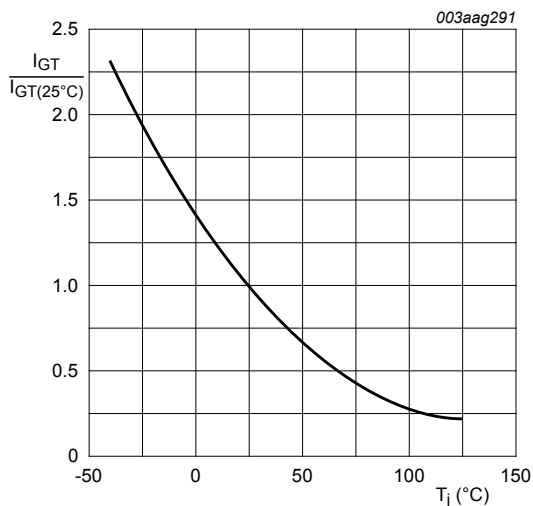
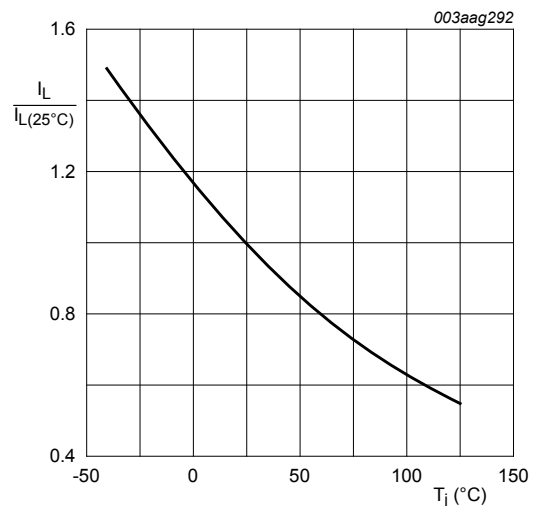


Fig. 7. Normalized gate trigger current as a function of junction temperature



$R_{GK} = 1\text{ k}\Omega$

Fig. 8. Normalized latching current as a function of junction temperature

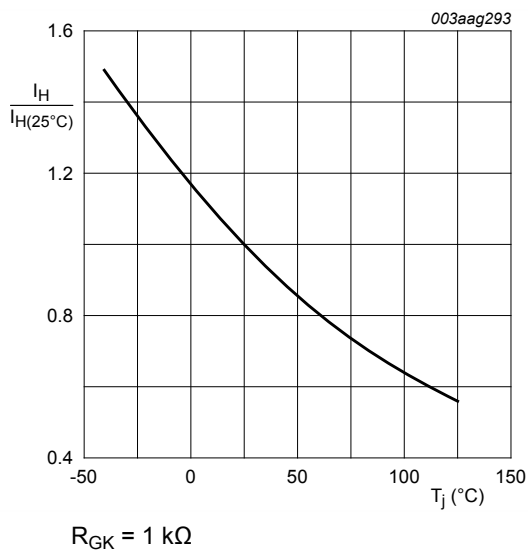


Fig. 9. Normalized holding current as a function of junction temperature

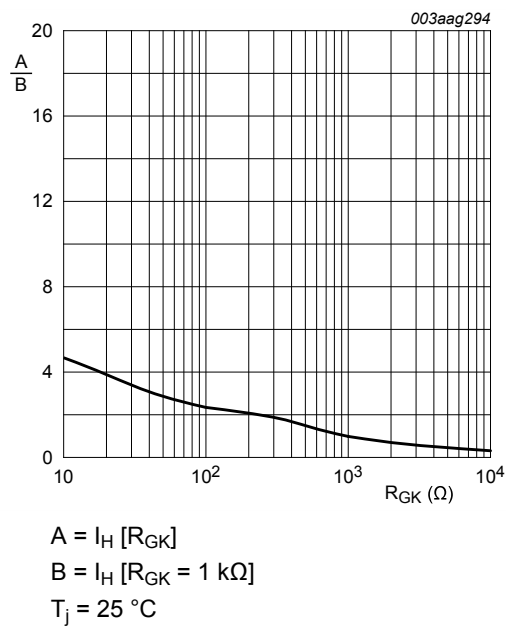


Fig. 10. Normalized holding current as a function of gate-cathode resistance (typical values)

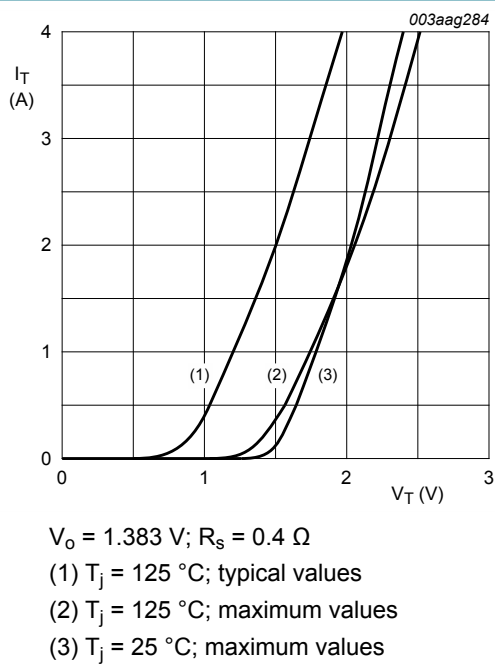


Fig. 11. On-state current as a function of on-state voltage

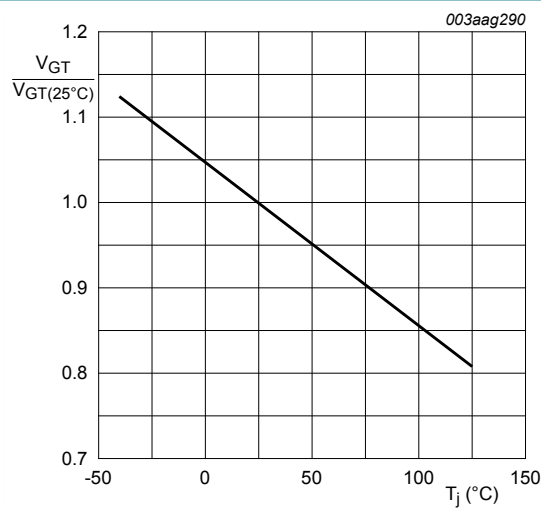
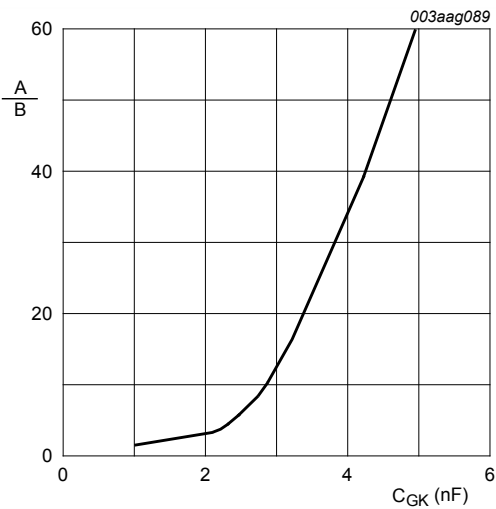
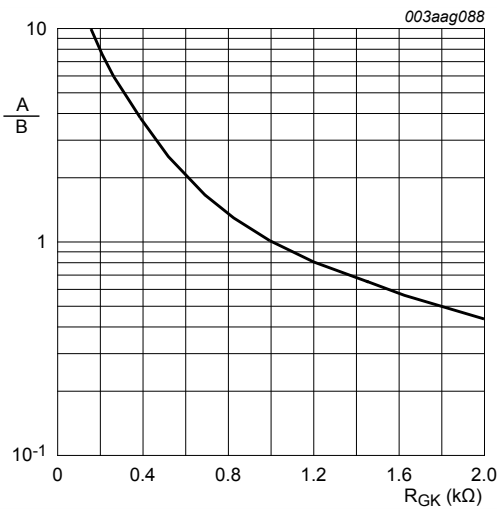


Fig. 12. Normalized gate trigger voltage as a function of junction temperature



$A = dV / dt [C_{GK}]$
 $B = dV / dt [R_{GK} = 1\text{ k}\Omega]$
 $T_j = 125\text{ }^{\circ}\text{C};$
 $R_{GK} = 1\text{ k}\Omega; V_{DM} = 402\text{ V}$

Fig. 13. Normalized dVd/dt immunity as a function of gate-cathode capacitance (typical values)



$A = dV / dt [C_{GK}]$
 $B = dV / dt [R_{GK} = 1\text{ k}\Omega]$
 $T_j = 125\text{ }^{\circ}\text{C};$
 $R_{GK} = 1\text{ k}\Omega; V_{DM} = 402\text{ V}$

Fig. 14. Normalized dVd/dt immunity as a function of gate-cathode resistance (typical values)

10. Package outline

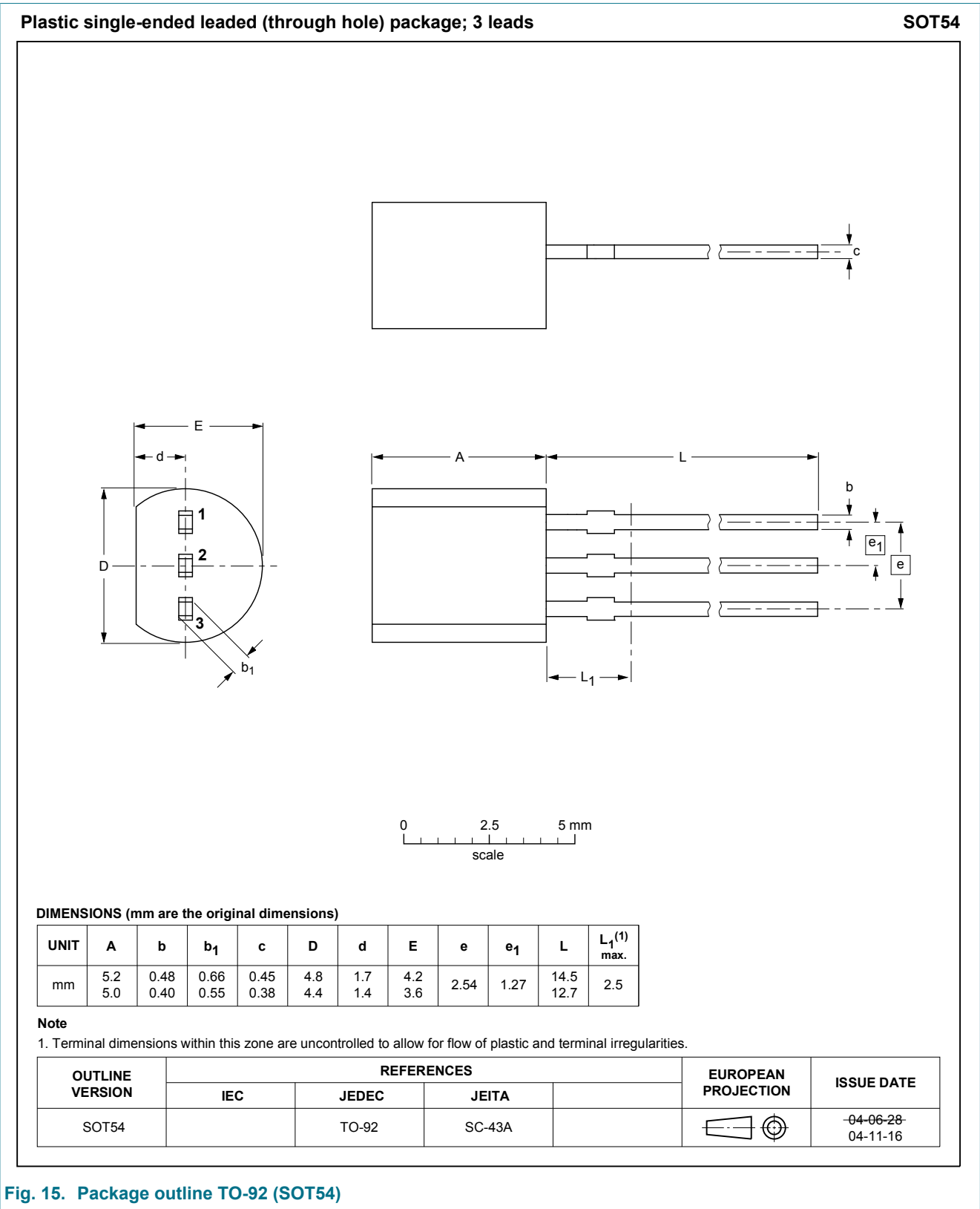


Fig. 15. Package outline TO-92 (SOT54)

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Contact Us :

➤ Address :

401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd
Minhang District, Shanghai , China

➤ Sales :

Direct +86 (21) 6401-6692
Email amall@ameya360.com
QQ 800077892
Skype ameyasales1 ameyasales2

➤ Customer Service :

Email service@ameya360.com

➤ Partnership :

Tel +86 (21) 64016692-8333
Email mkt@ameya360.com