

## 1.5A SWITCH STEP DOWN SWITCHING REGULATOR

### 1 General Features

- 1.5A INTERNAL SWITCH
- OPERATING INPUT VOLTAGE FROM 4.4V TO 36V
- 3.3V / ( $\pm 2\%$ ) REFERENCE VOLTAGE
- OUTPUT VOLTAGE ADJUSTABLE FROM 1.235V TO 35V
- LOW DROPOUT OPERATION: 100% DUTY CYCLE
- 500KHz INTERNALLY FIXED FREQUENCY
- VOLTAGE FEEDFORWARD
- ZERO LOAD CURRENT OPERATION
- INTERNAL CURRENT LIMITING
- INHIBIT FOR ZERO CURRENT CONSUMPTION
- SYNCHRONIZATION
- PROTECTION AGAINST FEEDBACK DISCONNECTION
- THERMAL SHUTDOWN

#### 1.1 APPLICATIONS:

- CONSUMER: STB, DVD, TV, VCR, CAR RADIO, LCD MONITORS
- NETWORKING: XDSL, MODEMS, DC-DC MODULES
- COMPUTER: PRINTERS, AUDIO/GRAPHIC CARDS, OPTICAL STORAGE, HARD DISK DRIVE
- INDUSTRIAL: CHARGERS, CAR BATTERY DC-DC CONVERTERS

Figure 1. Package

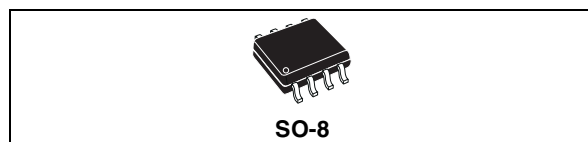


Table 1. Order Codes

Part Number	Package
L5970AD	SO-8
L5970ADTR	SO-8 in Tape & Reel

### 2 Description

The L5970AD is a step down monolithic power switching regulator with a switch current limit of 1.5A so it is able to deliver more than 1A DC current to the load depending on the application conditions.

The output voltage can be set from 1.235V to 35V.

The device uses an internal P-Channel D-MOS transistor (with a typical  $R_{DS(ON)}$  of 200m $\Omega$ ) as switching element to avoid the use of bootstrap capacitor and guarantee high efficiency.

An internal oscillator fixes the switching frequency at 500KHz to minimize the size of external components. Having a minimum input voltage of 4.4V only, it is particularly suitable for 5V bus, available in all computer related applications.

Pulse by pulse current limit with the internal frequency modulation offers an effective constant current short circuit protection.

Figure 2. Test and Application Circuit

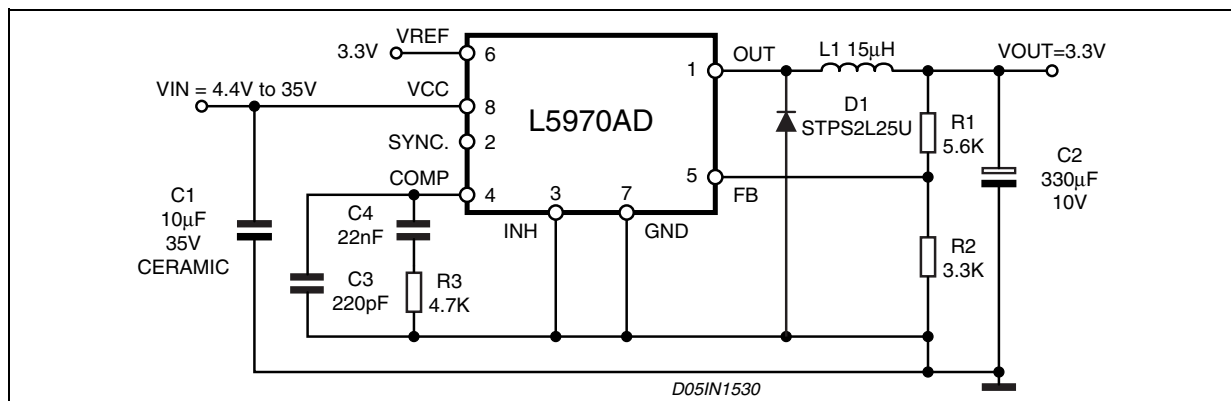


Table 2. Thermal Data

Symbol	Parameter	Value	Unit
$R_{th(j-amb)}$	Thermal Resistance Junction to ambient Max.	120 (*)	°C/W

(\*) Package mounted on board

Figure 3. Pin Connection (top view)

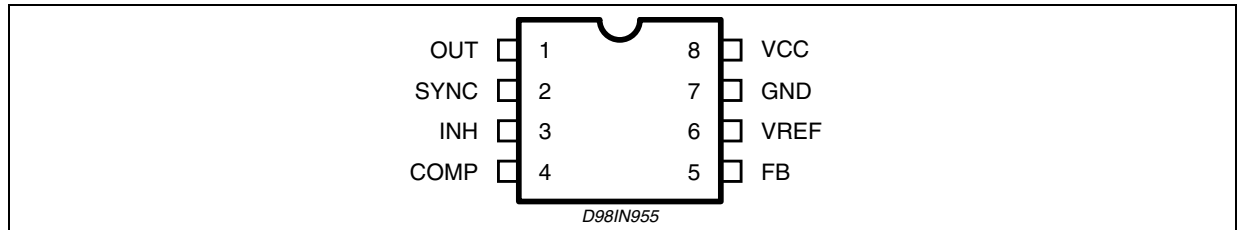


Table 3. Pin Description

N.	Name	Description
1	OUT	Regulator Output.
2	SYNC	Master/Slave Synchronization. When it is open, a signal synchronous with the turn-off of the internal power is present at the pin. When connected to an external signal at a frequency higher than the internal one, then the device is synchronized by the external signal. Connecting together the SYNC pin of two devices, the one with the higher frequency works as master and the other one, works as slave.
3	INH	A logical signal (active high) disables the device. With INH higher than 2.2V the device is OFF and with INH lower than 0.8V, the device is ON. If INH is not used the pin must be grounded. When it is open, an internal pull-up disables the device.
4	COMP	E/A output to be used for frequency compensation.
5	FB	Stepdown feedback input. Connecting the output voltage directly to this pin results in an output voltage of 1.235V. An external resistor divider is required for higher output voltages (the typical value for the resistor connected between this pin and ground is 4.7K).
6	$V_{REF}$	Reference voltage of 3.3V. No filter capacitor is needed to stability.
7	GND	Ground.
8	$V_{CC}$	Unregulated DC input voltage.

Table 4. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
$V_8$	Input Voltage	40	V
$V_1$	Output DC voltage Output peak voltage at $t = 0.1\mu s$	-1 to 40 -5 to 40	V V
$I_1$	Maximum output current	int. limit.	
$V_4, V_5$	Analog pins	4	V
$V_3$	INH	-0.3V to $V_{CC}$	
$V_2$	SYNC	-0.3 to 4	V
$P_{tot}$	Power dissipation at $T_{amb} \leq 60^\circ C$	0.75	W
$T_j$	Operating junction temperature range	-40 to 150	°C
$T_{stg}$	Storage temperature range	-55 to 150	°C

**Table 5. Electrical Characteristics** ( $T_j = 25^\circ\text{C}$ ,  $V_{CC} = 12\text{V}$ , unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_{CC}$	Operating input voltage range		4.4		36	V
$R_{DS(on)}$	Mosfet on Resistance			0.250	0.5	$\Omega$
$I_l$	Maximum limiting current	$V_{CC} = 4.4\text{V to }36\text{V}$		1.8		A
$f_s$	Switching frequency			500		KHz
	Duty cycle		0		100	%
<b>DYNAMIC CHARACTERISTICS</b>						
$V_5$	Voltage feedback	$4.4\text{V} < V_{CC} < 36\text{V}$	1.220	1.235	1.25	V
$\eta$	Efficiency	$V_O = 5\text{V}, V_{CC} = 12\text{V}$		90		%
<b>DC CHARACTERISTICS</b>						
$I_{qop}$	Total Operating Quiescent Current			5	7	mA
$I_q$	Quiescent current	Duty Cycle = 0; $V_{FB} = 1.5\text{V}$			2.7	mA
$I_{qst-by}$	Total stand-by quiescent current	$V_{inH} > 2.2\text{V}$		50	100	$\mu\text{A}$
<b>INHIBIT</b>						
	INH Threshold Voltage	Device ON			0.8	V
		Device OFF	2.2			V
<b>ERROR AMPLIFIER</b>						
$V_{OH}$	High level output voltage	$V_{FB} = 1\text{V}$	3.5			V
$V_{OL}$	Low level output voltage	$V_{FB} = 1.5\text{V}$			0.4	V
$I_{o\ source}$	Source output current	$V_{COMP} = 1.9\text{V}; V_{FB} = 1\text{V}$	200	300		$\mu\text{A}$
$I_{o\ sink}$	Sink output current	$V_{COMP} = 1.9\text{V}; V_{FB} = 1.5\text{V}$	1	1.5		mA
$I_b$	Source bias current			2.5	4	$\mu\text{A}$
	DC open loop gain	$R_L = \infty$	50	57		dB
$g_m$	Transconductance	$I_{comp} = -0.1\text{mA to }0.1\text{mA}$ $V_{COMP} = 1.9\text{V}$		2.3		mS
<b>SYNC FUNCTION</b>						
	High Input Voltage	$V_{CC} = 4.4\text{V to }36\text{V}$	2.5		$V_{REF}$	V
	Low Input Voltage	$V_{CC} = 4.4\text{V to }36\text{V}$			0.74	V
	Slave Sink Current	$V_{sync} = 0.74\text{V}^{(1)}$ $V_{sync} = 2.33\text{V}$	0.11		0.25	mA
			0.21		0.45	mA
	Master Output Amplitude	$I_{source} = 3\text{mA}$	2.75	3		V
	Output Pulse Width	no load, $V_{sync} = 1.65\text{V}$	0.20	0.35		$\mu\text{s}$
<b>REFERENCE SECTION</b>						
	Reference Voltage		3.234	3.3	3.366	V
		$I_{REF} = 0\text{ to }5\text{mA}$ $V_{CC} = 4.4\text{V to }36\text{V}$	3.2	3.3	3.399	V
	Line Regulation	$I_{REF} = 0\text{mA}$ $V_{CC} = 4.4\text{V to }36\text{V}$		5	10	mV
	Load Regulation	$I_{REF} = 0\text{ to }5\text{mA}$		8	15	mV
	Short Circuit Current		10	18	30	mA

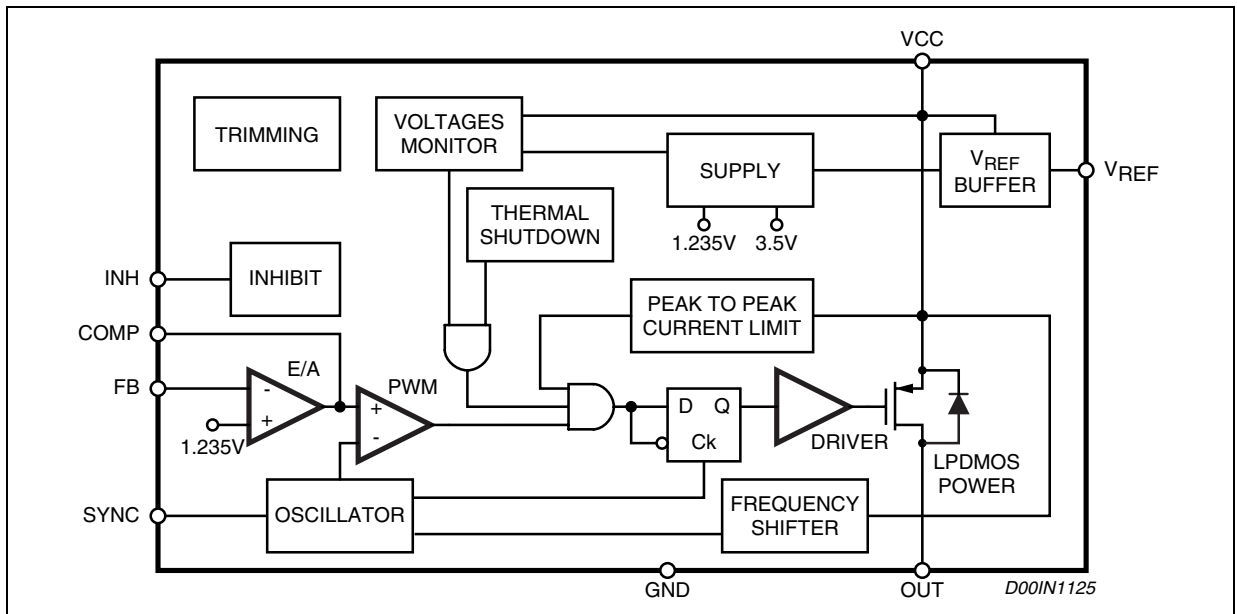
Note: 1. Guaranteed by design

### 3 Functional Description

The main internal blocks are shown in Fig. 4, where is reported the device block diagram. They are:

- A voltage regulator that supplies the internal circuitry. From this regulator, a 3.3V reference voltage is externally available.
- A voltage monitor circuit that checks the input and internal voltages.
- A fully integrated sawtooth oscillator whose frequency is 500KHz
- Two embedded current limitations circuitries which control the current that flows through the power switch. The Pulse by Pulse Current Limit forces the power switch OFF cycle by cycle if the current reaches an internal threshold, while the Frequency Shifter reduces the switching frequency in order to strongly reduce the duty cycle.
- A transconductance error amplifier.
- A pulse width modulator (PWM) comparator and the relative logic circuitry necessary to drive the internal power.
- An high side driver for the internal P-MOS switch.
- An inhibit block for stand-by operation.
- A circuit to realize the thermal protection function.

Figure 4. Block Diagram



#### 3.1 POWER SUPPLY & VOLTAGE REFERENCE

The internal regulator circuit (shown in Figure 2) consists of a start-up circuit, an internal voltage Preregulator, the Bandgap voltage reference and the Bias block that provides current to all the blocks.

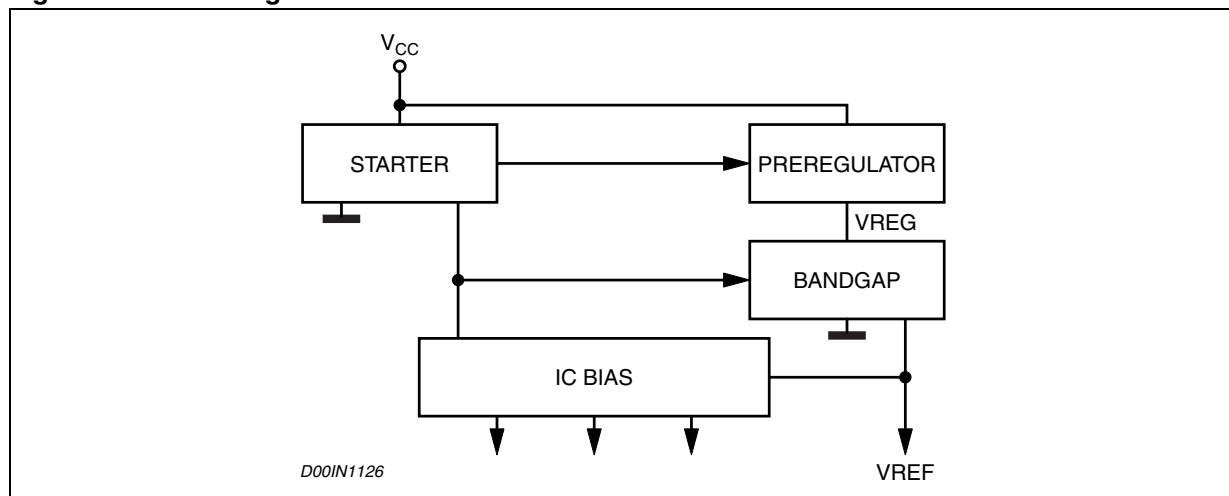
The Starter gives the start-up currents to the whole device when the input voltage goes high and the device is enabled (inhibit pin connected to ground).

The Preregulator block supplies the Bandgap cell with a preregulated voltage  $V_{REG}$  that has a very low supply voltage noise sensitivity.

#### 3.2 VOLTAGES MONITOR

An internal block senses continuously the  $V_{CC}$ ,  $V_{ref}$  and  $V_{bg}$ . If the voltages go higher than their thresholds, the regulator starts to work. There is also an hysteresis on the  $V_{CC}$  (UVLO).

Figure 5. Internal Regulator Circuit



### 3.3 OSCILLATOR & SYNCHRONIZATOR

Figure 6 shows the block diagram of the oscillator circuit.

The Clock Generator provides the switching frequency of the device that is internally fixed at 500KHz. The frequency shifter block acts reducing the switching frequency in case of strong overcurrent or short circuit. The clock signal is then used in the internal logic circuitry and is the input of the Ramp Generator and Synchronizator blocks.

The Ramp Generator circuit provides the sawtooth signal, used to realize the PWM control and the internal voltage feed forward, while the Synchronizator circuit generates the synchronization signal. Infact the device has a synchronization pin that can works both as Master and Slave.

As Master to synchronize external devices to the internal switching frequency.

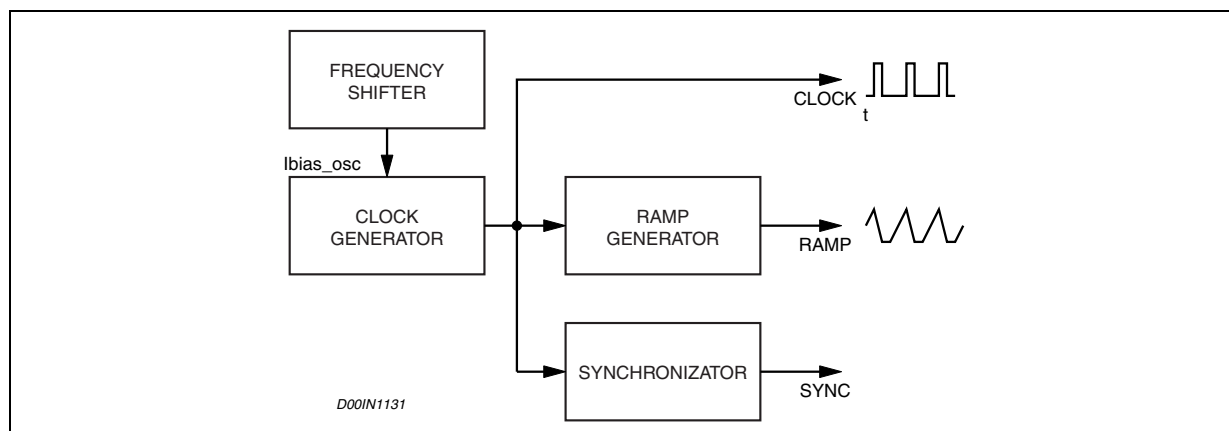
As Slave to synchronize itself by external signal.

In particular, connecting together two devices, the one with the lower switching frequency works as Slave and the other one works as Master.

To synchronize the device, the SYNC pin has to pass from a low level to a level higher than the synchronization threshold with a duty cycle that can vary approximately from 10% to 90%, depending also on the signal frequency and amplitude.

The frequency of the synchronization signal must be at least higher than the internal switching frequency of the device (500KHz).

Figure 6. Oscillator Circuit





The turn on of the power element, or better, the rise time of the current at turn on, is a very critical parameter to compromise.

At a first approach, it looks like the faster it is the rise time, the lower are the turn on losses.

But there is a limit introduced by the recovery time of the recirculation diode.

In fact when the current of the power element equals the inductor current, the diode turns off and the drain of the power is free to go high. But during its recovery time, the diode can be considered as an high value capacitor and this produces a very high peak current, responsible of many problems:

Spikes on the device supply voltage that cause oscillations (and thus noise) due to the board parasitics.

Turn on overcurrent causing a decrease of the efficiency and system reliability.

Big EMI problems.

Shorter freewheeling diode life.

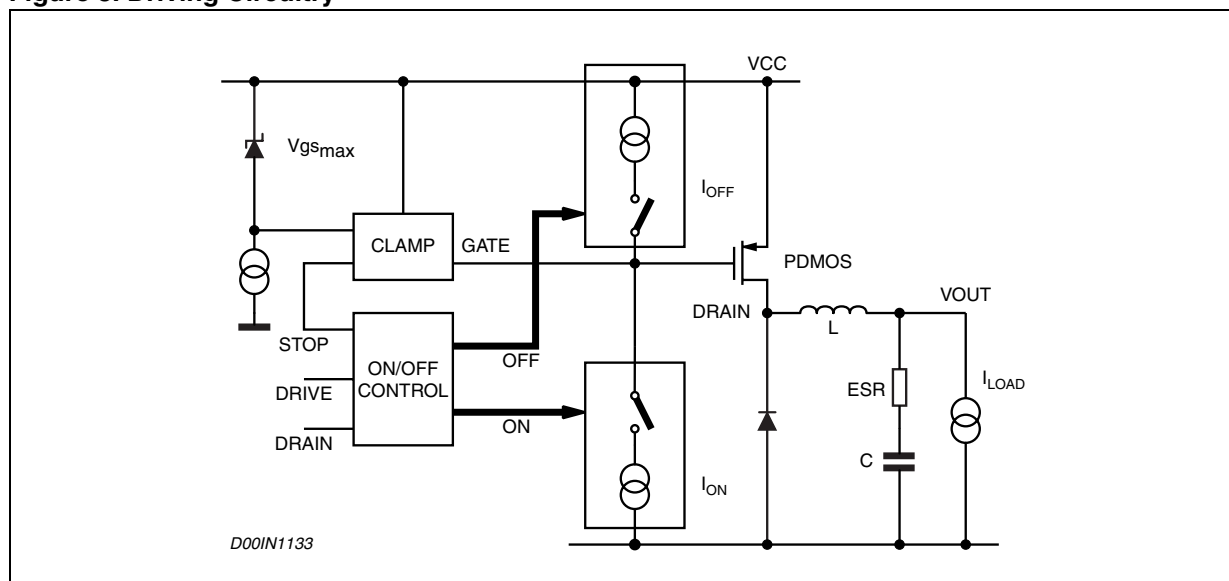
The fall time of the current during the turn off is also critical. In fact it produces voltage spikes (due to the parasitics elements of the board) that increase the voltage drop across the PDMOS.

In order to minimize all these problems, a new topology of driving circuit has been used and its block diagram is shown in fig. 8.

The basic idea is to change the current levels used to turn on and off the power switch, according with the PDMOS status and with the gate clamp status.

This circuitry allow to turn off and on quickly the power switch and to manage the above question related to the freewheeling diode recovery time problem. The gate clamp is necessary to avoid that  $V_{gs}$  of the internal switch goes higher than  $V_{gsmax}$ . The ON/OFF Control block avoids any cross conduction between the supply line and ground.

**Figure 8. Driving Circuitry**



### 3.7 INHIBIT FUNCTION

The inhibit feature allows to put in stand-by mode the device. With INH pin higher than 2.2V the device is disabled and the power consumption is reduced to less than 100 $\mu$ A. With INH pin lower than 0.8V, the device is enabled. If the INH pin is left floating, an internal pull up ensures that the voltage at the pin reaches the inhibit threshold and the device is disabled. The pin is also Vcc compatible.

### **3.8 THERMAL SHUTDOWN**

The shutdown block generates a signal that turns off the power stage if the temperature of the chip goes higher than a fixed internal threshold (150°C). The sensing element of the chip is very close to the PDMOS area, so ensuring an accurate and fast temperature detection. An hysteresis of approximately 20°C avoids that the devices turns on and off continuously

## **4 Additional Features and Protections**

### **4.1 FEEDBACK DISCONNECTION**

In case of feedback disconnection, the duty cycle increases versus the maximum allowed value, bringing the output voltage close to the input supply. This condition could destroy the load.

To avoid this dangerous condition, the device is turned off if the feedback pin remains floating.

### **4.2 OUTPUT OVERVOLTAGE PROTECTION**

The overvoltage protection, OVP, is realized by using an internal comparator, which input is connected to the feedback, that turns off the power stage when the OVP threshold is reached. This threshold is typically 30% higher than the feedback voltage.

When a voltage divider is requested for adjusting the output voltage (see test application circuit), the OVP intervention will be set at:

$$V_{OVP} = 1.3 \cdot \frac{R_1 + R_2}{R_2} \cdot V_{FB}$$

Where  $R_1$  is the resistor connected between the output voltage and the feedback pin, while  $R_2$  is between the feedback pin and ground.

### **4.3 ZERO LOAD**

Due to the fact that the internal power is a PDMOS, no bootstrap capacitor is required and so, the device works properly also with no load at the output. In this condition it works in burst mode, with random repetition rate of the burst.

## **5 Application Ideas**

L5970AD belongs to L597x family.

Related part numbers are:

- L5970D: 1.5A ( $I_{SW}$ ), 250KHz Step Down DC-DC Converter in SO8
- L5972D: 2A ( $I_{SW}$ ), 250KHz Step Down DC-DC Converter in SO8
- L5973AD: 2A ( $I_{SW}$ ), 500KHz Step Down DC-DC Converter in HSOP8
- L5973D: 2.5A ( $I_{SW}$ ), 250KHz Step Down DC-DC Converter in HSOP8

In case higher current is needed, the nearest DC-DC Converter family is L497x.

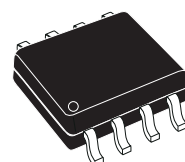
## 6 Package Information

Figure 9. SO-8 Mechanical Data & Package Dimensions

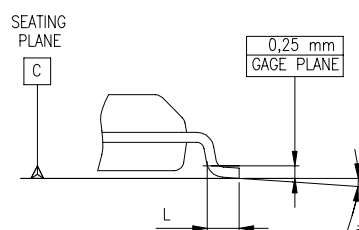
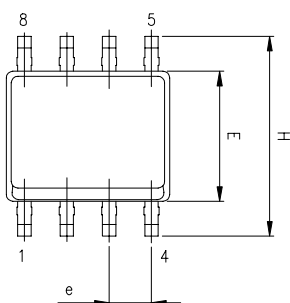
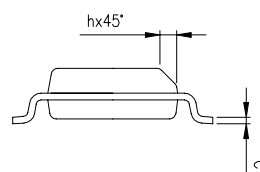
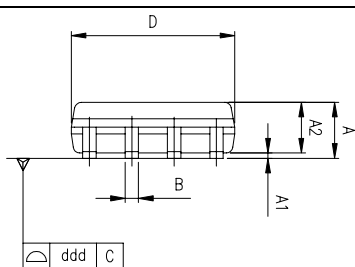
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D <sup>(1)</sup>	4.80		5.00	0.189		0.197
E	3.80		4.00	0.15		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

Note: (1) Dimensions D does not include mold flash, protrusions or gate burrs.  
Mold flash, protrusions or gate burrs shall not exceed 0.15mm (.006inch) in total (both side).

### OUTLINE AND MECHANICAL DATA



SO-8



0016023 C

## 7 REVISION HISTORY

**Table 6. Revision History**

Date	Revision	Description of Changes
March 2005	1	Initial load.

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