FAIRCHILD
SEMICONDUCTOR®

December 2013

# 74VCX08
# Low Voltage Quad 2-Input AND Gate with 3.6V Tolerant Inputs and Outputs

## Features

- 1.2V to 3.6V $V_{CC}$ supply operation
- 3.6V tolerant inputs and outputs
- $t_{PD}$:
  - 2.8ns max. for 3.0V to 3.6V $V_{CC}$
- Power-off high impedance inputs and outputs
- Static Drive ($I_{OH}$/$I_{OL}$)
  - ±24mA @ 3.0V $V_{CC}$
- Uses proprietary Quiet Series™ noise/EMI reduction circuitry
- Latchup performance exceeds 300mA
- ESD performance:
  - Human body model > 2000V
  - Machine model > 250V
- Leadless DQFN package

## General Description

The VCX08 contains four 2-input AND gates. This product is designed for low voltage (1.2V to 3.6V) $V_{CC}$ applications with I/O compatibility up to 3.6V.

The VCX08 is fabricated with an advanced CMOS technology to achieve high-speed operation while maintaining low CMOS power dissipation.

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## Ordering Information

| Order Number | Package Number | Package Description |
|---|---|---|
| 74VCX08M | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| 74VCX08BQX(1) | MLP14A | 14-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 3.0mm |
| 74VCX08MTC | MTC14 | 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |

**Note:**

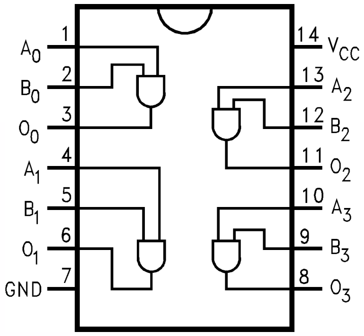
1. DQFN package available in Tape and Reel only.

Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering number.

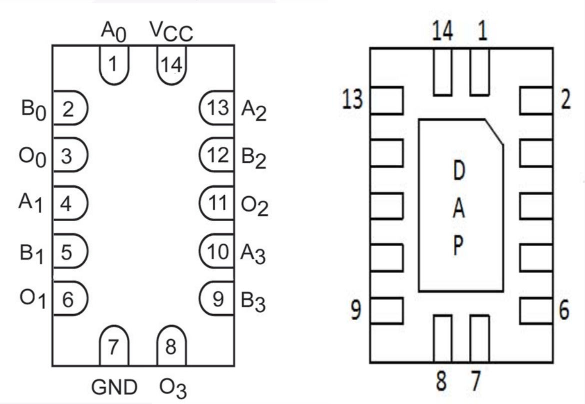
All packages are lead free per JEDEC: J-STD-020B standard.

## Connection Diagrams

### Pin Assignments for SOIC and TSSOP



### Pad Assignments for DQFN

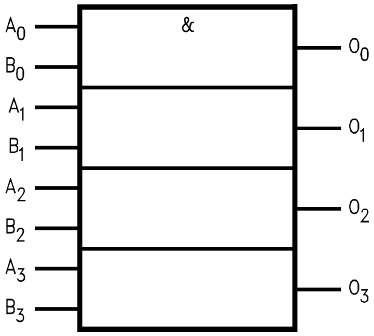


(Top View)

(Bottom View)

## Logic Symbol

### IEEE/IEC



## Pin Description

| Pin Names | Description |
|---|---|
| $A_n$, $B_n$ | Inputs |
| $O_n$ | Outputs |
| DAP | No Connect |

Note: DAP (Die Attach Pad)

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Rating |
|---|---|---|
| $V_{CC}$ | Supply Voltage | –0.5V to +4.6V |
| $V_I$ | DC Input Voltage | –0.5V to 4.6V |
| $V_O$ | DC Output Voltage<br>HIGH or LOW State[2] | –0.5V to $V_{CC}$+0.5V |
| | $V_{CC}$ = 0V | –0.5V to +4.6V |
| $I_{IK}$ | DC Input Diode Current, $V_I < 0V$ | –50mA |
| $I_{OK}$ | DC Output Diode Current<br>$V_O < 0V$ | –50mA |
| | $V_O > V_{CC}$ | +50mA |
| $I_{OH} / I_{OL}$ | DC Output Source/Sink Current | +50mA |
| $I_{CC}$ or GND | DC $V_{CC}$ or Gound Current per Supply Pin | ±100mA |
| $T_{STG}$ | Storage Temperature Range | –65°C to +150°C |

**Note:**

2. $I_O$ Absolute Maximum Rating must be observed.

## Recommended Operating Conditions[3]

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol | Parameter | Rating |
|---|---|---|
| $V_{CC}$ | Power Supply Operating | 1.2V to 3.6V |
| $V_I$ | Input Voltage | –0.3V to 3.6V |
| $V_O$ | Output Voltage, HIGH or LOW State | 0V to $V_{CC}$ |
| $I_{OH} / I_{OL}$ | Output Current<br>$V_{CC}$ = 3.0V to 3.6V | ±24mA |
| | $V_{CC}$ = 2.3V to 2.7V | ±18mA |
| | $V_{CC}$ = 1.65V to 2.3V | ±6mA |
| | $V_{CC}$ = 1.4V to 1.6V | ±2mA |
| | $V_{CC}$ = 1.2V | ±100µA |
| $T_A$ | Free Air Operating Temperature | –40°C to +85°C |
| $\Delta t / \Delta V$ | Minimum Input Edge Rate, $V_{IN}$ = 0.8V to 2.0V, $V_{CC}$ = 3.0V | 10ns/V |

**Note:**

3. Floating or unused inputs must be held HIGH or LOW

## DC Electrical Characteristics

| Symbol | Parameter | $V_{CC}$ (V) | Conditions | Min | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | HIGH Level Input Voltage | 2.7–3.6 | | 2.0 | | V |
| | | 2.3–2.7 | | 1.6 | | |
| | | 1.65–2.3 | | $0.65 \times V_{CC}$ | | |
| | | 1.4–1.6 | | $0.65 \times V_{CC}$ | | |
| | | 1.2 | | $0.65 \times V_{CC}$ | | |
| $V_{IL}$ | LOW Level Input Voltage | 2.7–3.6 | | | 0.8 | V |
| | | 2.3–2.7 | | | 0.7 | |
| | | 1.65–2.3 | | | $0.35 \times V_{CC}$ | |
| | | 1.4–1.6 | | | $0.35 \times V_{CC}$ | |
| | | 1.2 | | | $0.05 \text{ x } V_{CC}$ | |
| $V_{OH}$ | HIGH Level Output Voltage | 2.7–3.6 | $I_{OH} = -100\mu A$ | $V_{CC} - 0.2$ | | V |
| | | 2.7 | $I_{OH} = -12mA$ | 2.2 | | |
| | | 3.0 | $I_{OH} = -18mA$ | 2.4 | | |
| | | 3.0 | $I_{OH} = -24mA$ | 2.2 | | |
| | | 2.3–2.7 | $I_{OH} = -100\mu A$ | $V_{CC} - 0.2$ | | |
| | | 2.3 | $I_{OH} = -6mA$ | 2.0 | | |
| | | 2.3 | $I_{OH} = -12mA$ | 1.8 | | |
| | | 2.3 | $I_{OH} = -18mA$ | 1.7 | | |
| | | 1.65–2.3 | $I_{OH} = -100\mu A$ | $V_{CC} - 0.2$ | | |
| | | 1.65 | $I_{OH} = -6mA$ | 1.25 | | |
| | | 1.4–1.6 | $I_{OH} = -100\mu A$ | $V_{CC} - 0.2$ | | |
| | | 1.4 | $I_{OH} = -2mA$ | 1.05 | | |
| | | 1.2 | $I_{OH} = -100\mu A$ | $V_{CC} - 0.2$ | | |
| $V_{OL}$ | LOW Level Output Voltage | 2.7–3.6 | $I_{OL} = 100\mu A$ | | 0.2 | V |
| | | 2.7 | $I_{OL} = 12mA$ | | 0.4 | |
| | | 3.0 | $I_{OL} = 18mA$ | | 0.4 | |
| | | 3.0 | $I_{OL} = 24mA$ | | 0.55 | |
| | | 2.3–2.7 | $I_{OL} = 100\mu A$ | | 0.2 | |
| | | 2.3 | $I_{OL} = 12mA$ | | 0.4 | |
| | | 2.3 | $I_{OL} = 18mA$ | | 0.6 | |
| | | 1.65–2.3 | $I_{OL} = 100\mu A$ | | 0.2 | |
| | | 1.65 | $I_{OL} = 6mA$ | | 0.2 | |
| | | 1.4–1.6 | $I_{OL} = 100\mu A$ | | 0.2 | |
| | | 1.4 | $I_{OL} = 2mA$ | | 0.35 | |
| | | 1.2 | $I_{OL} = 100\mu A$ | | 0.05 | |
| $I_I$ | Input Leakage Current | 1.2–3.6 | $0 \leq V_I \leq 3.6V$ | | ±5.0 | µA |
| $I_{OFF}$ | Power-OFF Leakage Current | 0 | $0 \leq (V_I, V_O) \leq 3.6V$ | | 10 | µA |
| $I_{CC}$ | Quiescent Supply Current | 1.2–3.6 | $V_I = V_{CC}$ or GND | | 20 | µA |
| | | | $V_{CC} \leq V_I \leq 3.6V$ | | ±20 | |
| $\Delta I_{CC}$ | Increase in $I_{CC}$ per Input | 2.7–3.6 | $V_{IH} = V_{CC} -0.6V$ | | 750 | µA |

## AC Electrical Characteristics(4)

| Symbol | Parameter | $V_{CC}$ (V) | Conditions | $T_A$ = –40°C to +85°C | | Units | Figure Number |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | | |
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay | 3.3 ± 0.3 | $C_L$ = 30pF, $R_L$ = 500Ω | 0.6 | 2.8 | ns | Fig. 1<br>Fig. 2 |
| | | 2.5 ± 0.2 | | 0.8 | 3.7 | | |
| | | 1.8 ± 0.15 | | 1.0 | 7.4 | | |
| | | 1.5 ± 0.1 | $C_L$ = 15pF, $R_L$ = 2kΩ | 1.0 | 14.8 | | Fig. 3<br>Fig. 4 |
| | | 1.2 | | 1.5 | 37.0 | | |
| $t_{OSHL}$, $t_{OSLH}$ | Output to Output Skew(5) | 3.3 ± 0.3 | $C_L$ = 30pF, $R_L$ = 500Ω | | 0.5 | ns | |
| | | 2.5 ± 0.2 | | | 0.5 | | |
| | | 1.8 ± 0.15 | | | 0.75 | | |
| | | 1.5 ± 0.1 | $C_L$ = 15pF, $R_L$ = 2kΩ | | 1.5 | | |
| | | 1.2 | | | 1.5 | | |

**Note:**

4. For $C_L$ = 50pF, add approximately 300ps to the AC Maximum specification.

5. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ($t_{OSHL}$) or LOW-to-HIGH ($t_{OSLH}$).

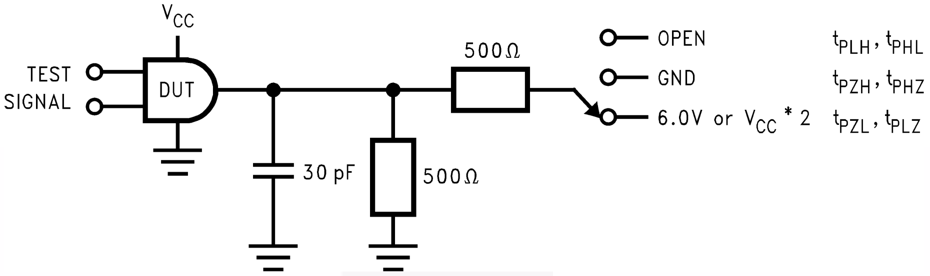
## Dynamic Switching Characteristics

| Symbol | Parameter | $V_{CC}$ (V) | Conditions | $T_A$ = 25°C | Unit |
|---|---|---|---|---|---|
| | | | | Typical | |
| $V_{OLP}$ | Quiet Output Dynamic Peak $V_{OL}$ | 1.8 | $C_L$ = 30pF, $V_{IH}$ = $V_{CC}$, $V_{IL}$ = 0V | 0.25 | V |
| | | 2.5 | | 0.6 | |
| | | 3.3 | | 0.8 | |
| $V_{OLV}$ | Quiet Output Dynamic Valley $V_{OL}$ | 1.8 | $C_L$ = 30pF, $V_{IH}$ = $V_{CC}$, $V_{IL}$ = 0V | –0.25 | V |
| | | 2.5 | | –0.6 | |
| | | 3.3 | | –0.8 | |
| $V_{OHV}$ | Quiet Output Dynamic Valley $V_{OH}$ | 1.8 | $C_L$ = 30pF, $V_{IH}$ = $V_{CC}$, $V_{IL}$ = 0V | 1.5 | V |
| | | 2.5 | | 1.9 | |
| | | 3.3 | | 2.2 | |

## Capacitance

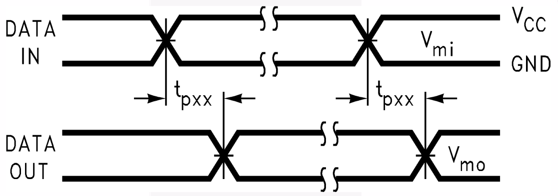
| Symbol | Parameter | Conditions | $T_A$ = +25°C | Units |
|---|---|---|---|---|
| | | | Typical | |
| $C_{IN}$ | Input Capacitance | $V_I$ = 0V or $V_{CC}$, $V_{CC}$ = 1.8V, 2.5V or 3.3V | 6.0 | pF |
| $C_{OUT}$ | Output Capacitance | $V_I$ = 0V or $V_{CC}$, $V_{CC}$ = 1.8V, 2.5V or 3.3V | 7.0 | pF |
| $C_{PD}$ | Power Dissipation Capacitance | $V_I$ = 0V or $V_{CC}$, f = 10MHz, $V_{CC}$ = 1.8V, 2.5V or 3.3V | 20.0 | pF |

## AC Loading and Waveforms ($V_{CC}$ 3.3V ± 0.3V to 1.8V ± 0.15V)



| Test | Switch |
|---|---|
| $t_{PLH}$, $t_{PHL}$ | Open |

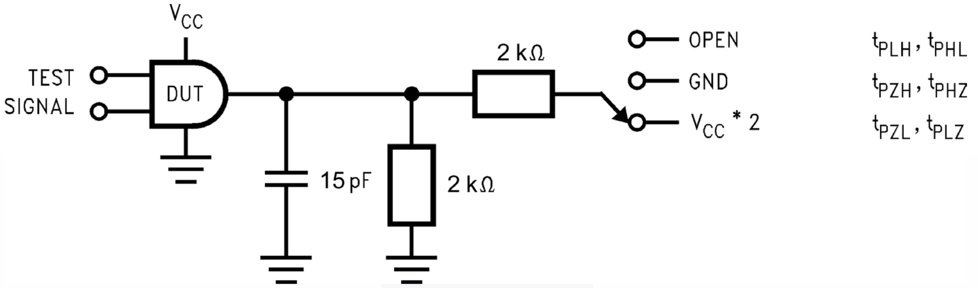
Figure 1. AC Test Circuit



| Symbol | $V_{CC}$ | | |
|---|---|---|---|
| | 3.3V ± 0.3V | 2.5V ± 0.2V | 1.8V ± 0.15V |
| $V_{mi}$ | 1.5V | $V_{CC}$ / 2 | $V_{CC}$ / 2 |
| $V_{mo}$ | 1.5V | $V_{CC}$ / 2 | $V_{CC}$ / 2 |

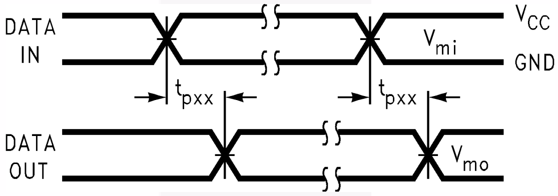
Figure 2. Waveform for Inverting and Non-inverting Functions

## AC Loading and Waveforms ($V_{CC}$ 1.5 ± 0.1V to 1.2V)



| Test | Switch |
|---|---|
| $t_{PLH}$, $t_{PHL}$ | Open |
| $t_{PZL}$, $t_{PLZ}$ | $V_{CC}$ x 2 at $V_{CC}$ = 1.5V ± 0.1V |
| $t_{PZH}$, $t_{PHZ}$ | GND |

**Figure 3. AC Test Circuit**



| Symbol | $V_{CC}$ |
|---|---|
| | **1.5V ± 0.1V** |
| $V_{mi}$ | $V_{CC}$ / 2 |
| $V_{mo}$ | $V_{CC}$ / 2 |

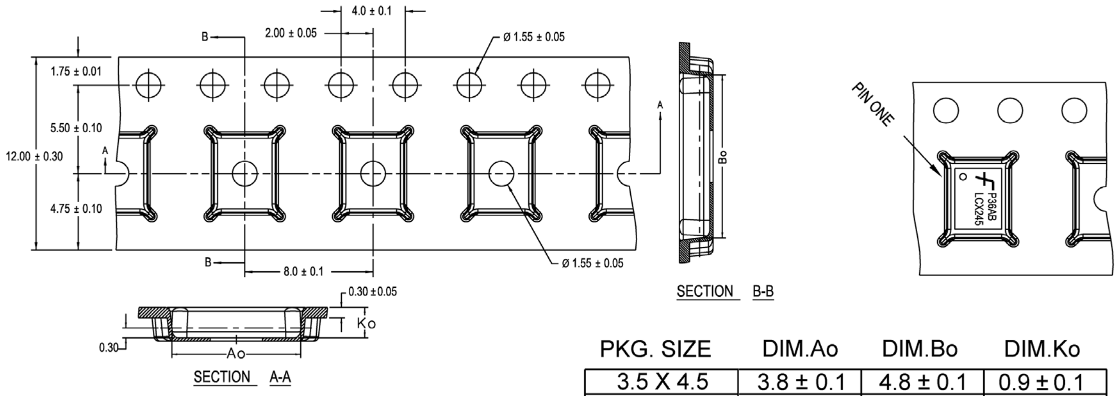
**Figure 4. Waveform for Inverting and Non-Inverting Functions**

## Tape and Reel Specification

### Tape Format for DQFN

| Package Designator | Tape Section | Number of Cavities | Cavity Status | Cover Tape Status |
|---|---|---|---|---|
| BQX | Leader (Start End) | 125 (Typ.) | Empty | Sealed |
| | Carrier | 3000 | Filled | Sealed |
| | Trailer (Hub End) | 75 (Typ.) | Empty | Sealed |

### **Tape Dimensions** inches (millimeters)



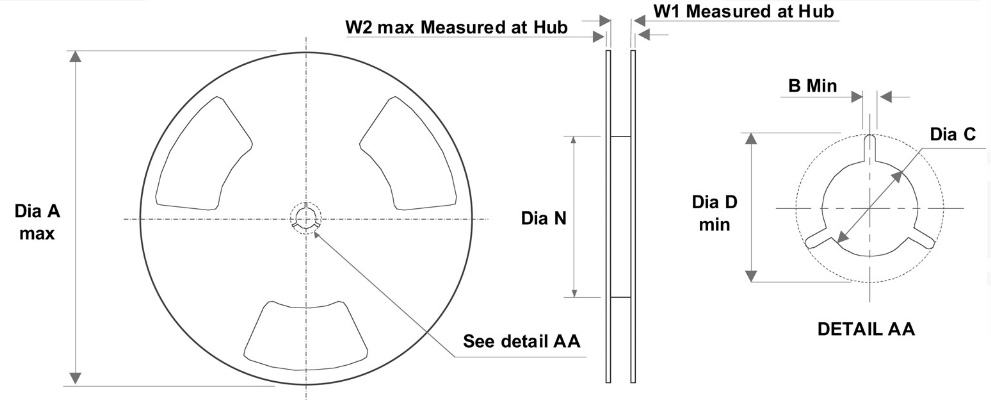
| PKG. SIZE | DIM.Ao | DIM.Bo | DIM.Ko |
|---|---|---|---|
| 3.5 X 4.5 | 3.8 ± 0.1 | 4.8 ± 0.1 | 0.9 ± 0.1 |
| 3.0 X 3.0 | 3.3 ± 0.1 | 3.3 ± 0.1 | 0.9 ± 0.1 |
| 2.5 X 4.5 | 2.8 ± 0.1 | 4.8 ± 0.1 | 0.9 ± 0.1 |
| 2.5 X 3.5 | 2.8 ± 0.1 | 3.8 ± 0.1 | 0.9 ± 0.1 |
| 2.5 X 3.0 | 2.8 ± 0.1 | 3.3 ± 0.1 | 0.9 ± 0.1 |
| 2.5 X 2.5 | 2.8 ± 0.1 | 2.8 ± 0.1 | 0.9 ± 0.1 |

DIMENSIONS ARE IN MILLIMETERS

NOTES: unless otherwise specified

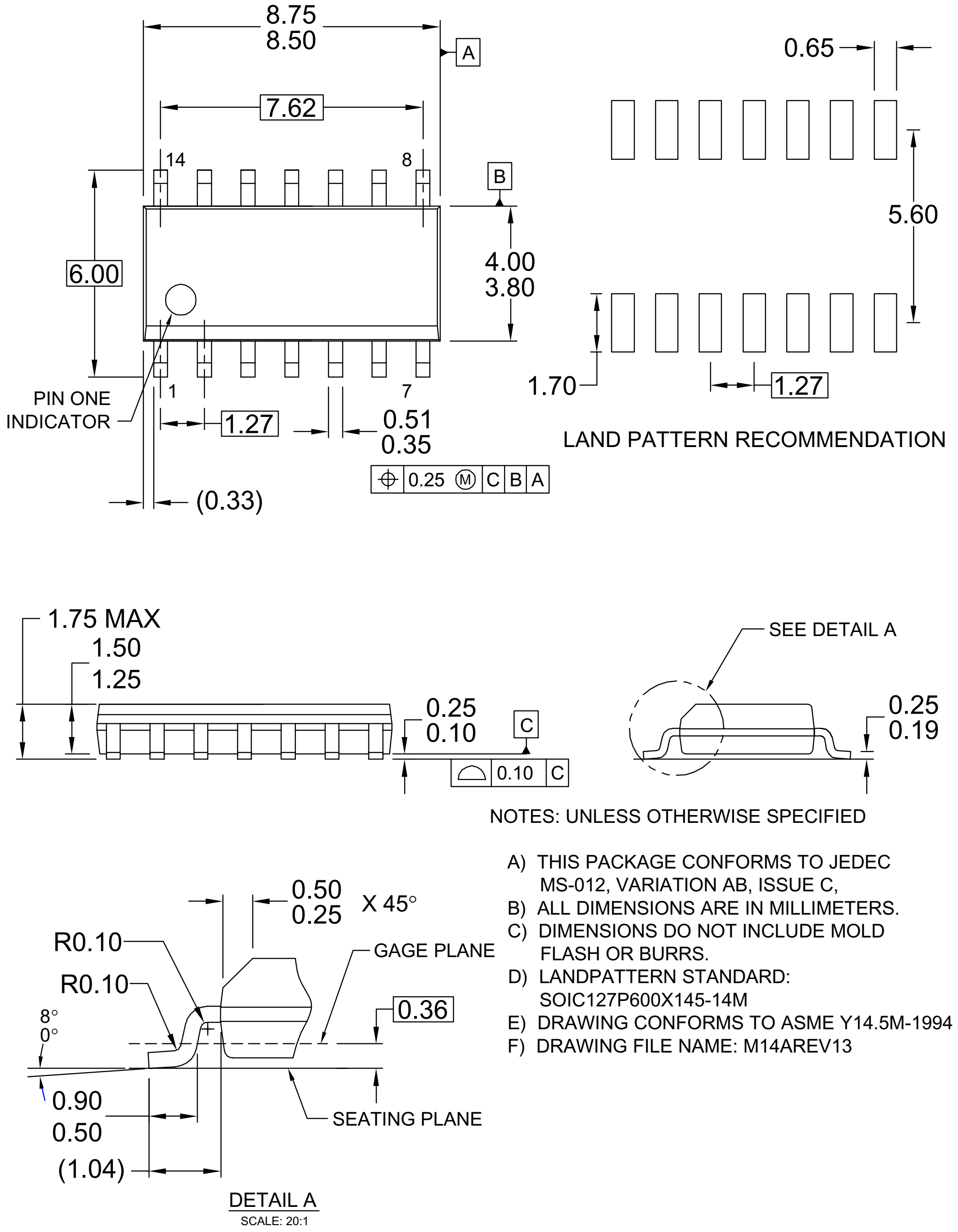
1. Cummulative pitch for feeding holes and cavities (chip pockets) not to exceed 0.008[0.20] over 10 pitch span.
2. Smallest allowable bending radius.
3. Thru hole inside cavity is centered within cavity.
4. Tolerance is ±0.002[0.05] for these dimensions on all 12mm tapes.
5. Ao and Bo measured on a plane 0.120[0.30] above the bottom of the pocket.
6. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
7. Pocket position relative to sprocket hole measured as true position of pocket. Not pocket hole.
8. Controlling dimension is millimeter. Diemension in inches rounded.

### **Reel Dimensions** inches (millimeters)



| Tape Size | A | B | C | D | N | W1 | W2 |
|---|---|---|---|---|---|---|---|
| 12mm | 13.0 (330.0) | 0.059 (1.50) | 0.512 (13.00) | 0.795 (20.20) | 2.165 (55.00) | 0.488 (12.4) | 0.724 (18.4) |

## Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C,
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X145-14M
E) DRAWING CONFORMS TO ASME Y14.5M-1994
F) DRAWING FILE NAME: M14AREV13

**Figure 5. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow**

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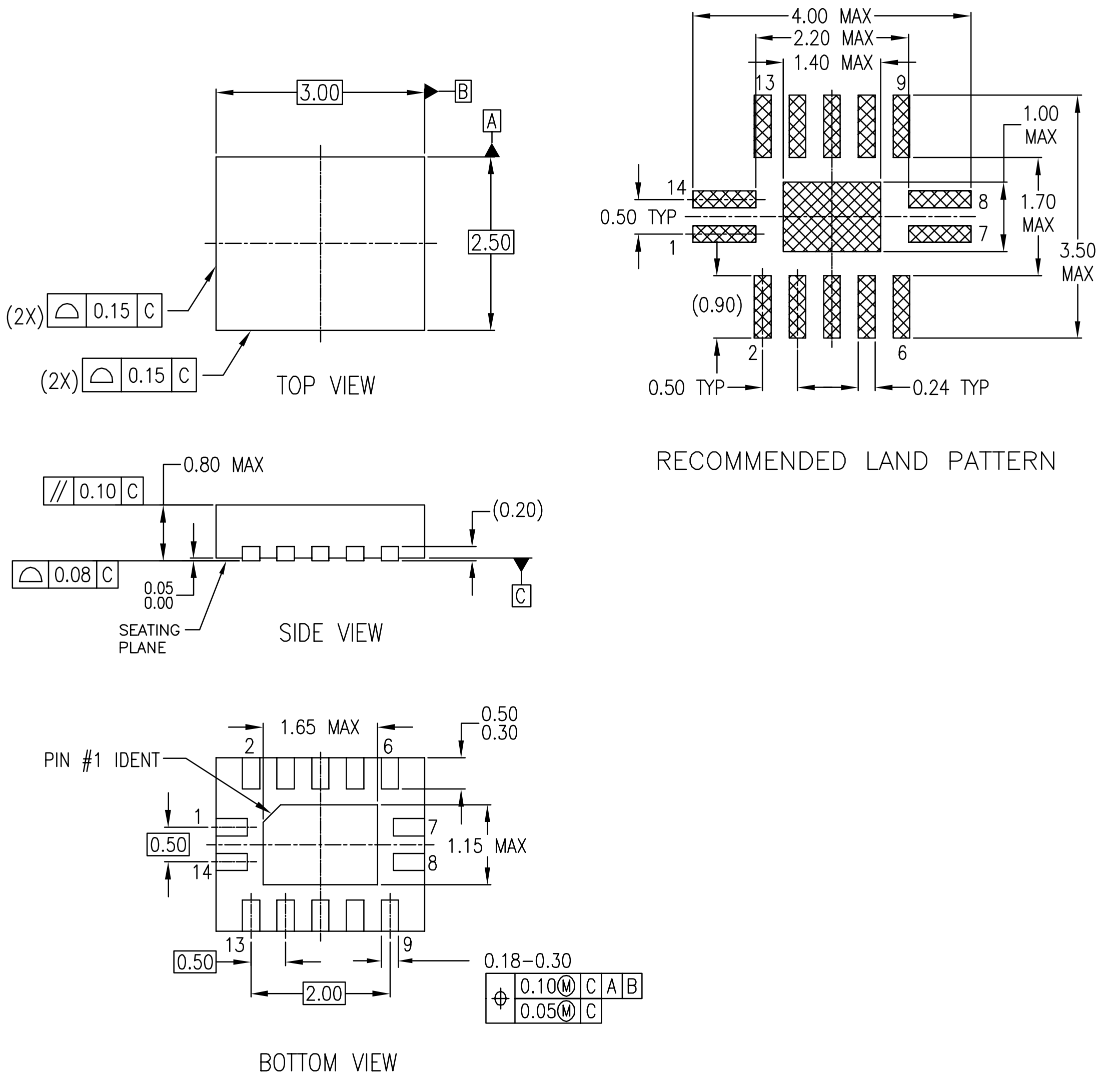
## Physical Dimensions (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO–241, VARIATION AA

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP14ArevA

**Figure 6. 14-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 3.0mm**

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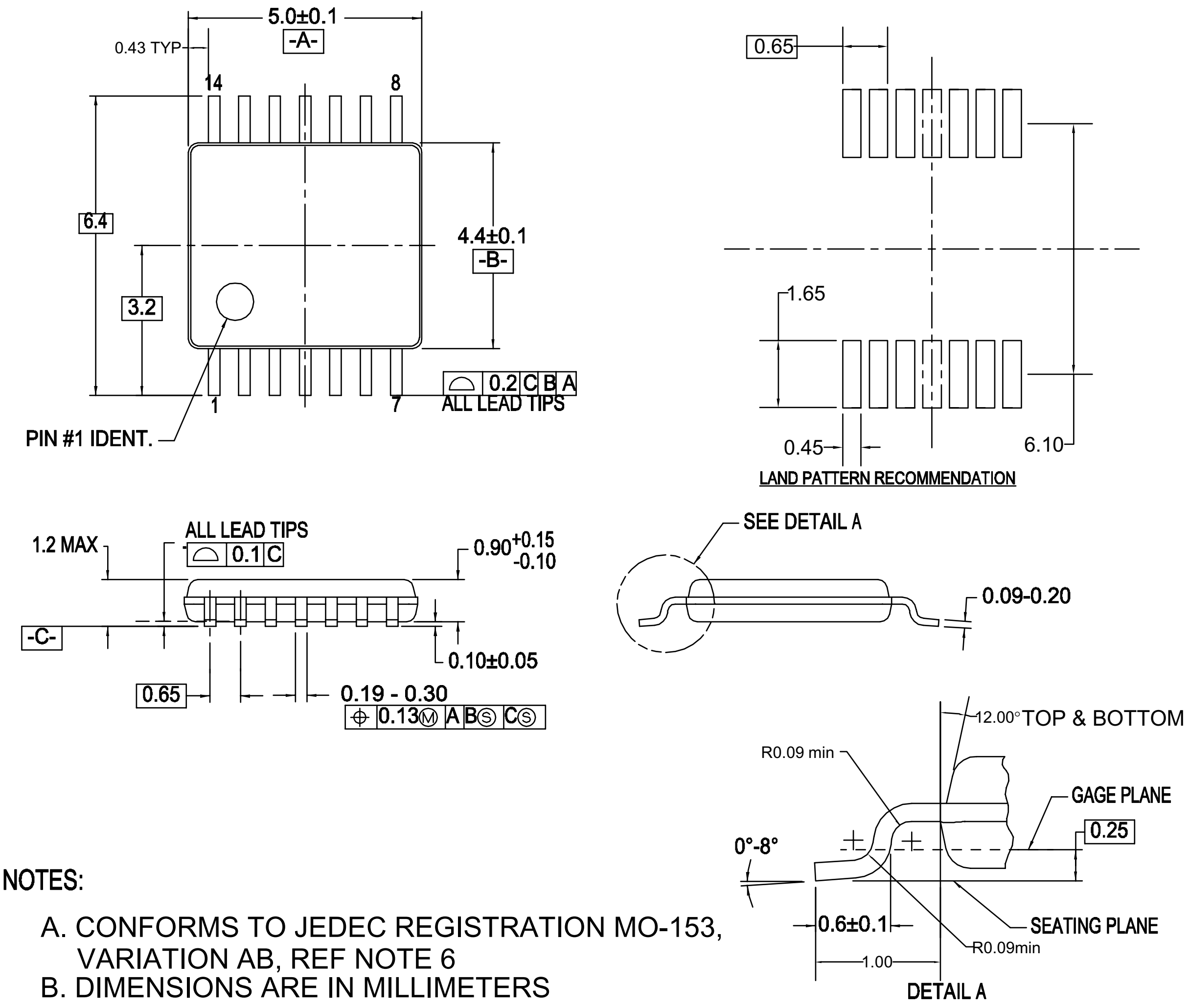
## Physical Dimensions (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6
B. DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982
E. LANDPATTERN STANDARD: SOP65P640X110-14M
F. DRAWING FILE NAME: MTC14REV6

**Figure 7. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide**

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FETBench™
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Green FPS™
Green FPS™ e-Series™
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SuperFET®
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SuperSOT™-6
SuperSOT™-8
SupreMOS®
SyncFET™
Sync-Lock™
SYSTEM GENERAL®*
TinyBoost®
TinyBuck®
TinyCalc™
TinyLogic®
TINYOPTO™
TinyPower™
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## ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

| Datasheet Identification | Product Status | Definition |
|---|---|---|
| Advance Information | Formative / In Design | Datasheet contains the design specifications for product development. Specifications may change in any manner without notice. |
| Preliminary | First Production | Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design. |
| No Identification Needed | Full Production | Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design. |
| Obsolete | Not In Production | Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only. |

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