Polyphase Multifunction Energy Metering IC

Preliminary Technical Data

ADE7854

FEATURES

Highly accurate; supports EN 50470-1, EN 50470-3, IEC 62053-21, IEC 62053-22, and IEC 62053-23
Compatible with 3-phase, 3- or 4-wire (delta or wye), and other 3-phase services
Supplies total active/apparent energy on each phase and on the overall system
<0.1% error in active energy over a dynamic range of 1000:1 at 25°C
<0.2% error in active energy over a dynamic range of 3000:1 at 25°C
Supports current transformer and di/dt current sensors
<0.1% error in voltage and current rms over a dynamic range of 1000:1 at 25°C
Supply-sampled waveform data on all 3 phases
Selectable no-load threshold level for total active powers and for apparent powers
Phase angle measurements in both current and voltage channels with maximum 0.3° error
Reference 1.2 V (drift 10 ppm/°C typical) with external overdrive capability
Single 3.3 V supply
40-lead frame chip scale (LFCSP) RoHS-compliant package
Operating temperature: –40° to +85°C
Flexible I²C, SPI, HSDC serial interfaces

GENERAL DESCRIPTION

The ADE7854[1] is a high accuracy, 3-phase electrical energy measurement IC with serial interfaces and three flexible pulse outputs. The ADE7854 incorporates second-order, sigma-delta (Σ-Δ) analog-to-digital converters (ADCs), a digital integrator, reference circuitry, and all the signal processing required to perform total active and apparent energy measurement and rms calculations. A fixed function digital signal processor (DSP) executes this signal processing.

The ADE7854 is suitable for measuring active and apparent energy in various 3-phase configurations, such as wye or delta services, with both three and four wires. The ADE7854 provides system calibration features for each phase, that is, rms offset correction, phase calibration, and gain calibration. The CF1, CF2, and CF3 logic outputs provide a wide choice of power information: total active power, total apparent power, or the sum of the current rms values.

The ADE7854 includes waveform sample registers that allow access to all ADC outputs. The device also incorporates power quality measurements, such as short duration low or high voltage detections, short duration high current variations, line voltage period measurement, and angles between phase voltages and currents. The SPI and I²C serial interfaces can be used to communicate with the ADE7854. A dedicated high speed interface, the high speed data capture (HSDC) port, can be used in conjunction with I²C to provide access to the ADC outputs and real-time power information. The ADE7854 has also two interrupt request pins, $\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$, to indicate that an enabled interrupt event has occurred.

The ADE7854 is available in a 40-lead LFCSP RoHS-compliant package.

[1] U.S. patents pending.

Rev. PrD

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FUNCTIONAL BLOCK DIAGRAM

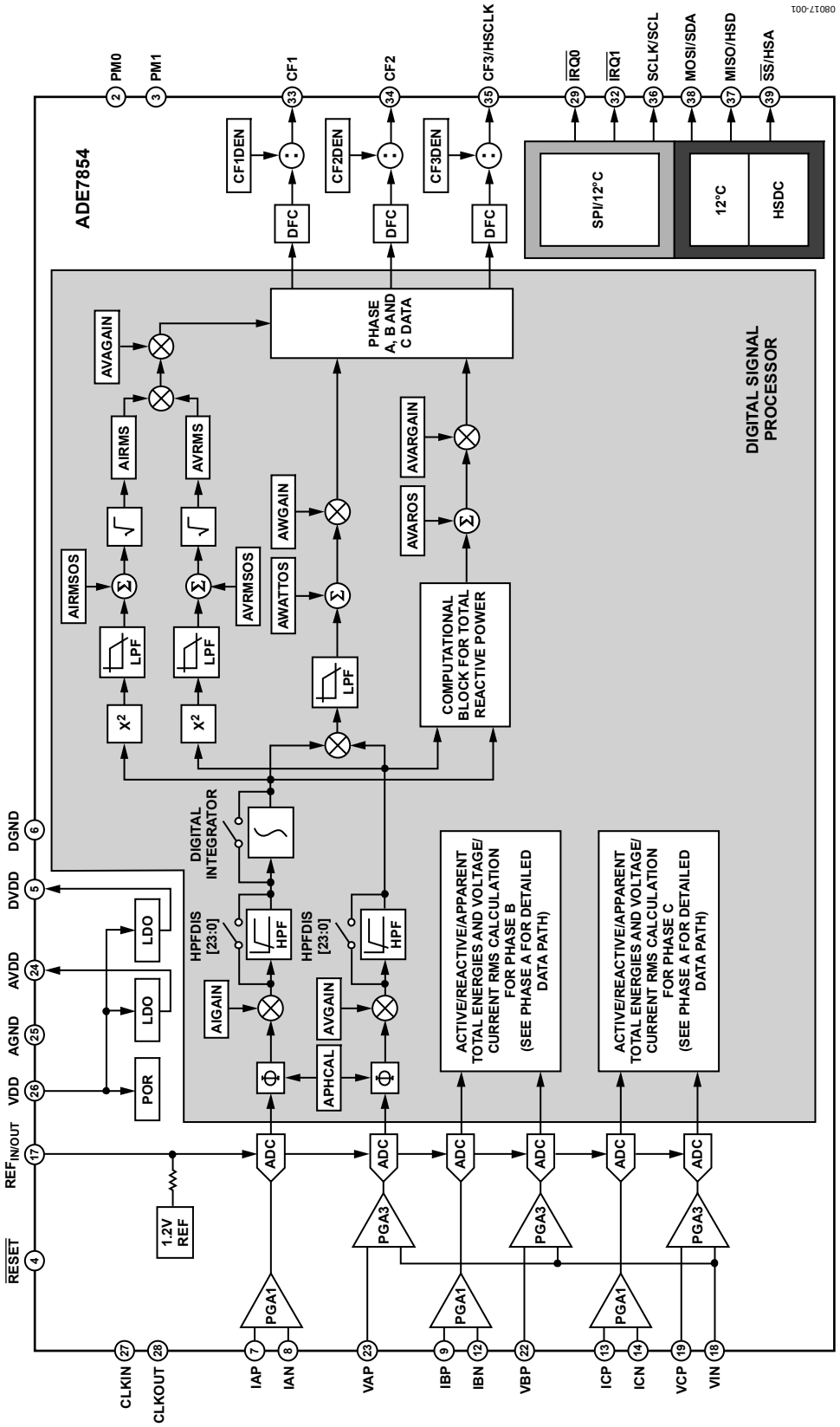


Figure 1.

SPECIFICATIONS

VDD = 3.3 V ± 10%, AGND = DGND = 0 V, on-chip reference, CLKIN = 16.384 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C, unless otherwise noted.

Table 1.

Parameter[1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments
ACTIVE ENERGY MEASUREMENT					
Total Active Energy Measurement Error (Per Phase)		0.1		%	Over a dynamic range of 1000 to 1, PGA = 1, 2, 4; integrator off
		0.2		%	Over a dynamic range of 3000 to 1, PGA = 1, 2, 4; integrator off
		0.1		%	Over a dynamic range of 500 to 1, PGA = 8, 16; integrator on
Phase Error Between Channels					Line frequency = 45 Hz to 65 Hz, HPF on
PF = 0.8 Capacitive			±0.05	Degrees	Phase lead: 37°
PF = 0.5 Inductive			±0.05	Degrees	Phase lag: 60°
AC Power Supply Rejection					
Output Frequency Variation		0.01		%	TBD conditions
DC Power Supply Rejection					
Output Frequency Variation		0.01		%	VDD ± 10%
Total Active Energy Measurement Bandwidth		2		kHz	
RMS MEASUREMENTS					
IRMS and VRMS Measurement Bandwidth		2		kHz	
IRMS and VRMS Measurement Error (PSM0 Mode[3])		0.1		%	Over a dynamic range of 1000:1, PGA = 1, 2, 4; integrator off
		0.1		%	Over a dynamic range of 500:1, PGA = 8, 16; integrator on
ANALOG INPUTS					
Maximum Signal Levels			±500	mV	Differential inputs: IAP − IAN, IBP − IBN, ICP − ICN, and INP − INN; single-ended inputs: VAP − VN, VBP − VN, and VCP − VN
Input Impedance (DC)	400			kΩ	
ADC Offset Error			±25	mV	Uncalibrated error; see the Terminology section
Gain Error		±4		%	External 1.2 V reference
WAVEFORM SAMPLING					Sampling CLKIN/2048, 16.384 MHz/2048 = 8 kSPS
Current and Voltage Channels					See the Waveform Sampling Mode section
Signal-to-Noise Ratio		55		dB	
Signal-to-Noise Plus Distortion		62		dB	
Bandwidth (−3 dB)		2		kHz	
TIME INTERVAL BETWEEN PHASES					
Measurement Error		0.3		Degrees	Line frequency = 45 Hz to 65 Hz, HPF on
CF1, CF2, CF3 PULSE OUTPUTS					
Maximum Output Frequency		8		kHz	
Duty Cycle		50		%	If CF1, CF2, or CF3 frequency > 6.25 Hz
Active Low Pulse Width		80		ms	If CF1, CF2, or CF3 frequency < 6.25 Hz
Jitter		0.04		%	For CF1, CF2, or CF3 frequency = 1 Hz
REFERENCE INPUT					
$REF_{IN/OUT}$ Input Voltage Range			1.3	V	1.2 V + 8%
	1.1			V	1.2 V − 8%
Input Capacitance			10	pF	
ON-CHIP REFERENCE (PSM0 MODE)					Nominal 1.2 V at $REF_{IN/OUT}$ pin
Reference Error			±0.9	mV	
Output Impedance	4			kΩ	
Temperature Coefficient		10		ppm/°C	
			50	ppm/°C	

Parameter[1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments
CLKIN					All specifications for CLKIN frequency = 16.384 MHz
Input Clock Frequency			16.384	MHz	
Crystal Equivalent Series Resistance	30		50	kΩ	
CLKIN Input Capacitance		12		pF	
CLKOUT Output Capacitance		12		pF	
LOGIC INPUTS—MOSI/SDA, SCLK/SCL, CLKIN, and $\overline{SS}$					
Input High Voltage, V_{INH}	2.4			V	VDD = 3.3 V ± 10%
Input Low Voltage, V_{INL}			0.8	V	VDD = 3.3 V ± 10%
Input Current, I_{IN}			±3	µA	Typical 10 nA, V_{IN} = 0 V to VDD
Input Capacitance, C_{IN}			10	pF	
LOGIC OUTPUTS					
$\overline{IRQ0}$, $\overline{IRQ1}$, MISO/HSDATA, HSCLKand CLKOUT					DVDD = 3.3 V ± 10%
Output High Voltage, V_{OH}	3.0			V	I_{SOURCE} = 800 µA
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 2 mA
CF1, CF2, and CF3					
Output High Voltage, V_{OH}	2.4			V	I_{SOURCE} = 500 µA
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 2 mA
POWER SUPPLY IN PSM0 MODE					For specified performance
VDD	3.0			V	3.3 V − 10%
			3.6	V	3.3 V + 10%
I_{DD}		TBD		mA	
POWER SUPPLY IN PSM3 MODE					For specified performance
VDD	2.4			V	
			3.7	V	
I_{DD} in PSM3 Mode		1		µA	

[1] See the Typical Performance Characteristics section.
[2] See the Terminology section for a definition of the parameters.
[3] See the Power Management section for details on the various power modes.

TIMING CHARACTERISTICS

I²C-Compatible Interface Timing

VDD = 3.3 V ± 10%, AGND = DGND = 0 V, on-chip reference, CLKIN = 16.384 MHz , T_{MIN} to T_{MAX} = −40°C to +85°C, unless otherwise noted.

Table 2.

		Standard mode		Fast Mode		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold Time (Repeated) Start Condition	$t_{HD;STA}$	4.0		0.6		µs
Low Period of SCL Clock	t_{LOW}	4.7		1.3		µs
High Period of SCL Clock	t_{HIGH}	4.0		0.6		µs
Setup Time for a Repeated Start Condition	$t_{SU;STA}$	4.7		0.6		µs
Data Hold Time	$t_{HD;DAT}$	0	3.45	0	0.9	µs
Data Setup Time	$t_{SU;DAT}$	250		100		ns
Rise Time of Both SDA and SCL Signals	t_R		1000	20	300	ns
Fall Time of Both SDA and SCL Signals	t_F		300	20	300	ns
Setup Time for Stop Condition	$t_{SU;STO}$	4.0		0.6		µs
Bus Free Time Between a Stop and Start Condition	t_{BUF}	4.7		1.3		µs
Pulse Width of Suppressed Spikes	t_{SP}	N/A			50	ns

I²C-Compatible Interface Timing Diagram

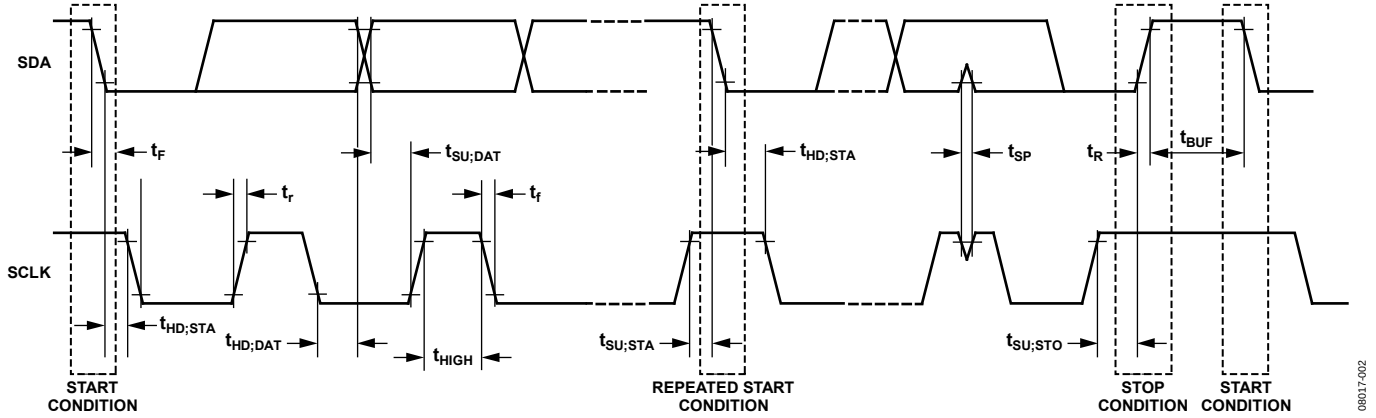


Figure 2. I²C-Compatible Interface Timing

SPI Interface Timing

Table 3.

Parameter	Symbol	Min	Max	Unit
$\overline{SS}$ to SCLK Edge	t_{SS}	50		ns
SCLK Period		400		ns
SCLK Low Pulse Width	t_{SL}	175		ns
SCLK High Pulse Width	t_{SH}	175		ns
Data Output Valid After SCLK Edge	t_{DAV}	5	40	ns
Data Input Setup Time Before SCLK Edge	t_{DSU}	20		ns
Data Input Hold Time After SCLK Edge	t_{DHD}	5		ns
Data Output Fall Time	t_{DF}		20	ns
Data Output Rise Time	t_{DR}		20	ns
SCLK Rise Time	t_{SR}		20	ns
SCLK Fall Time	t_{SF}		20	ns
MISO Disable After $\overline{SS}$ Rising Edge	t_{DIS}	5	40	ns
$\overline{SS}$ High After SCLK Edge	t_{SFS}	0		ns

SPI Interface Timing Diagram

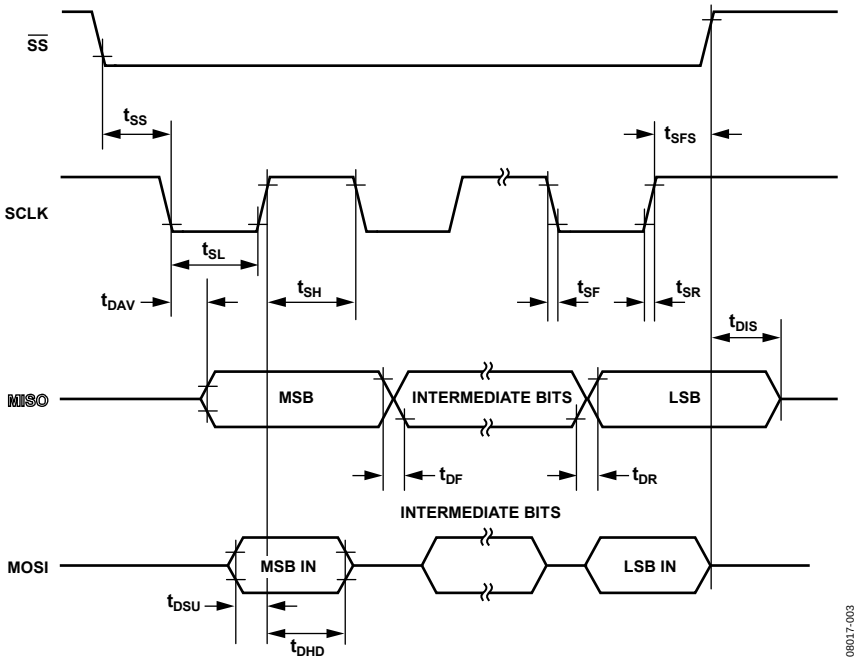


Figure 3. SPI Interface Timing

HSDC Interface Timing

Table 4.

Parameter	Symbol	Min	Max	Unit
HSA to SCLK Edge	t_{SS}	0		ns
HSCLK Period		125		
HSCLK Low Pulse Width	t_{SL}	50		ns
HSCLK High Pulse Width	t_{SH}	50		ns
Data Output Valid After HSCLK Edge	t_{DAV}	5	40	ns
Data Output Fall Time	t_{DF}		20	ns
Data Output Rise Time	t_{DR}		20	ns
HSCLK Rise Time	t_{SR}		10	ns
HSCLK Fall Time	t_{SF}		10	ns
HSD Disable After HAS Rising Edge	t_{DIS}	40		ns
HSA High After HSCLK Edge	t_{SFS}	0		ns

HSDC Interface Timing Diagram and Circuit Drawing

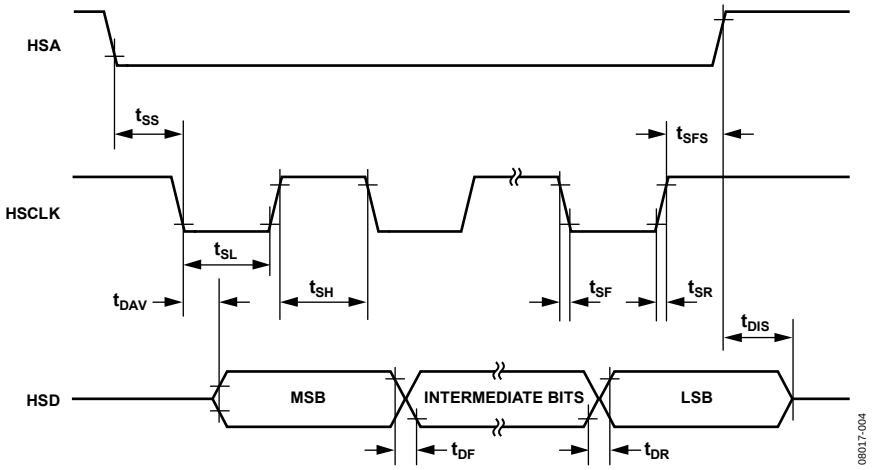


Figure 4. HSDC Interface Timing

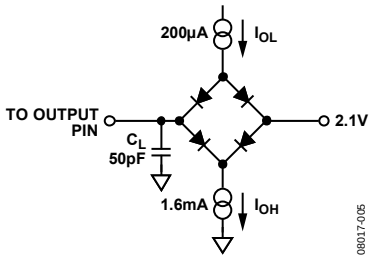


Figure 5. Load Circuit for Timing Specifications

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
VDD to AGND	–0.3 V to +3.7 V
VDD to DGND	–0.3 V to +3.7 V
Analog Input Voltage to AGND, IAP, IAN, IBP, IBN, ICP, ICN, VAP, VBP, VCP, VN	–2 V to +2 V
Reference Input Voltage to AGND	–0.3 V to VDD + 0.3 V
Digital Input Voltage to DGND	–0.3 V to VDD + 0.3 V
Digital Output Voltage to DGND	–0.3 V to VDD + 0.3 V
Operating Temperature	
Industrial Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
40-Lead LFCSP, Power Dissipation	TBD mW
θ_{JA} Thermal Impedance	29.3°C/W
θ_{JC} Thermal Impedance	1.8°C/W

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

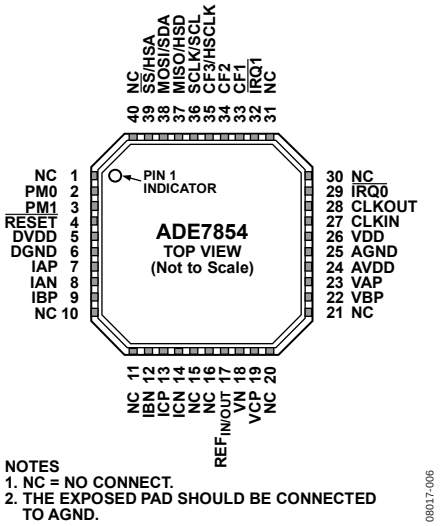


Figure 6. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 10, 11, 20, 21, 30, 31, 40	NC	These pins are not connected internally.
2	PM0	Power Mode Pin 0. For proper operation, this pin should be set to VDD via a 10 kΩ pull-up resistor.
3	PM1	Power Mode Pin 1. This pin defines the power mode of the ADE7854, as described in Table 7.
4	$\overline{\text{RESET}}$	Reset Input, Active Low. In PSM0 mode, this pin should stay low for at least 10 µs to trigger a hardware reset.
5	DVDD	This pin provides access to the on-chip 2.5 V digital LDO. No external active circuitry should be connected to this pin. This pin should be decoupled with a 4.7 µF capacitor in parallel with a ceramic 100 nF capacitor.
6	DGND	Ground Reference for Digital Circuitry.
7, 8, 9, 12, 13, 14	IAP, IAN, IBP, IBN, ICP, ICN	Analog Inputs for Current Channel. This channel is used with the current transducers and is referenced in this document as the current channel. These inputs are fully differential voltage inputs with a maximum differential level of ±0.5 V. This channel has an internal PGA for IAx, IBx, and ICx.
15, 16	NC	Connect to AGND.
17	$REF_{IN/OUT}$	This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 1.2 V ± 0.075% and a maximum temperature coefficient of 50 ppm/°C. An external reference source with 1.2 V ± 8% can also be connected at this pin. In either case, this pin should be decoupled to AGND with a 4.7 µF capacitor in parallel with a ceramic 100 nF capacitor. After reset, the on-chip reference is enabled.
18, 19, 22, 23	VN, VCP, VBP, VAP	Analog Inputs for the Voltage Channel. This channel is used with the voltage transducer and is referenced as the voltage channel in this document. These inputs are single-ended voltage inputs with the maximum signal level of ±0.5 V with respect to VN for specified operation. This channel has also an internal PGA.
24	AVDD	This pin provides access to the on-chip 2.5 V analog LDO. No external active circuitry should be connected to this pin. This pin should be decoupled with a 4.7 µF capacitor in parallel with a ceramic 220 nF capacitor.
25	AGND	This pin provides the ground reference for the analog circuitry in the ADE7854. This pin should be tied to the analog ground plane or the quietest ground reference in the system. This quiet ground reference should be used for all analog circuitry, for example, antialiasing filters, current, and voltage transducers.
26	VDD	This pin provides the supply voltage for the ADE7854. In PSM0 (normal power mode) the supply voltage should be maintained at 3.3 V ± 10% for specified operation. In PSM3 (sleep mode), when the ADE7854 is supplied from a battery, the supply voltage should be maintained between 2.4 V and 3.7 V. This pin should be decoupled to DGND with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.
27	CLKIN	Master Clock. An external clock can be provided at this logic input. Alternatively, a parallel resonant AT crystal can be connected across CLKIN and CLKOUT to provide a clock source for the ADE7854. The clock frequency for specified operation is 16.384 MHz. Ceramic load capacitors of a few tens of picofarads should be used with the gate oscillator circuit. Refer to the crystal manufacturer's data sheet for the load capacitance requirements.

Pin No.	Mnemonic	Description
28	CLKOUT	A crystal can be connected across this pin and CLKIN as previously described to provide a clock source for the ADE7854. The CLKOUT pin can drive one CMOS load when either an external clock is supplied at CLKIN or a crystal is being used.
29, 32	$\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$	Interrupt Request Outputs. These are active low logic outputs. See the Interrupts section for a detailed presentation of the events that can trigger interrupts.
33, 34, 35	CF1, CF2, CF3/HSCLK	Calibration Frequency Logic Outputs (CFx). These outputs provide power information based on the CF1SEL, the CF2SEL, and the CF3SEL bits in the CFMODE register and are used for operational and calibration purposes. The full-scale output frequency can be scaled by writing to the CF1DEN, CF2DEN, CF3DEN registers, respectively (see the Energy-to-Frequency Conversion section). Serial Clock Output of the HSDC Port (HSCLK). CF3 is multiplexed with this output.
36	SCLK/SCL	Serial Clock Input for the SPI Port (SCLK)/Serial Clock Input for the I^2C Port (SCL). All serial data transfers are synchronized to this clock (see the Serial Interfaces section). This pin has a Schmitt trigger input for use with a clock source that has a slow edge transition time, for example, when using opto-isolator outputs.
37	MISO/HSD	Data Output for the SPI Port (MISO). Data Output for the HSDC Port (HSD).
38	MOSI/SDA	Data Input for the SPI Port (MOSI). Data Output for the I^2C Port (SDA).
39	$\overline{\text{SS}}$/HSA	Slave Select for the SPI Port ($\overline{\text{SS}}$). HSDC Port Active (HSA).
EPAD	Exposed Pad	The exposed pad should be connected to AGND.

TYPICAL PERFORMANCE CHARACTERISTICS

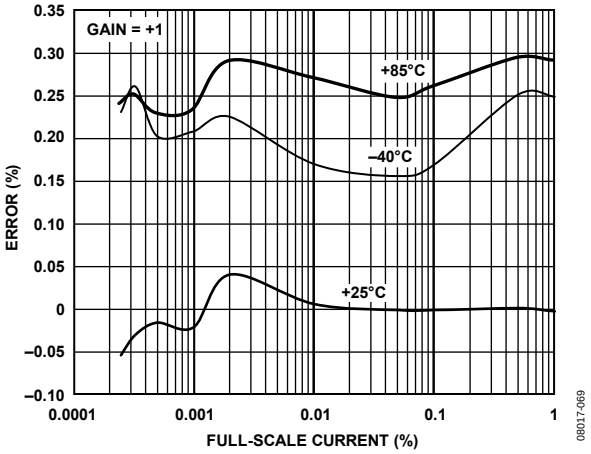


Figure 7. Total Active Energy Error as a Percentage of Reading (Gain = +1) over Temperature with Internal Reference and Integrator Off

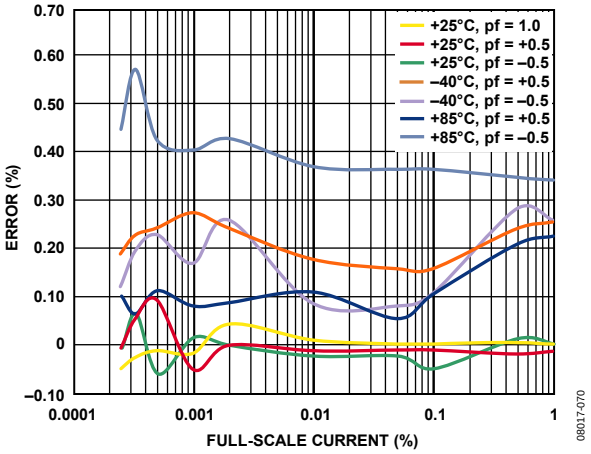


Figure 8. Total Active Energy Error as a Percentage of Reading (Gain = +1) over Power Factor with Internal Reference and Integrator Off

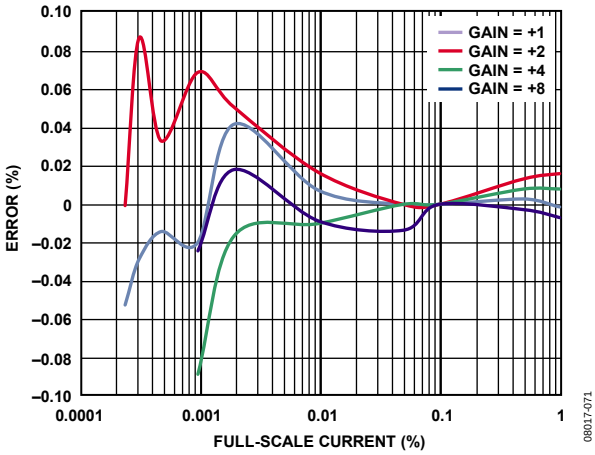


Figure 9. Total Active Energy Error as a Percentage of Reading over Gain with Internal Reference and Integrator Off

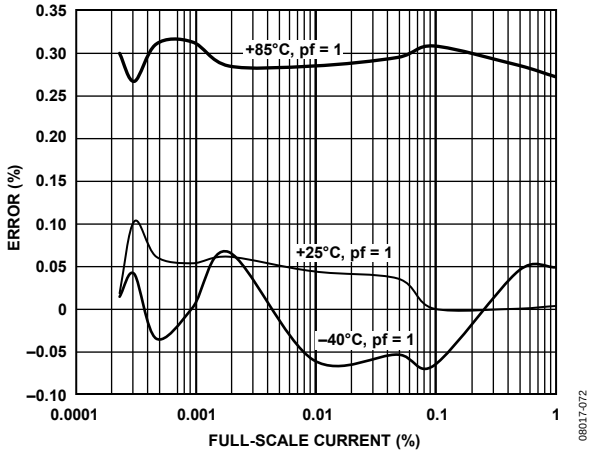


Figure 10. Total Active Energy Error as a Percentage of Reading (Gain = +1) over Temperature with External Reference and Integrator Off

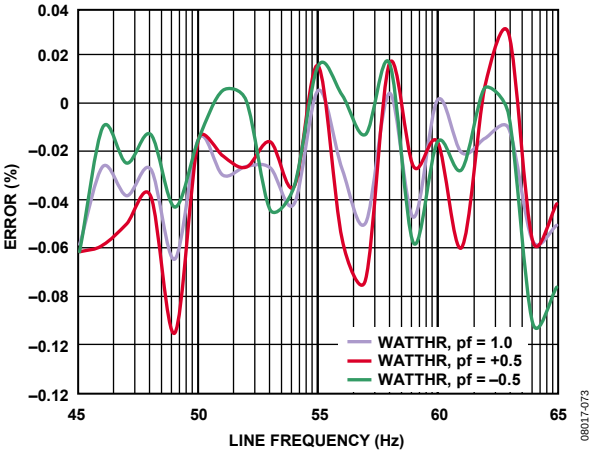


Figure 11. Total Active Energy Error as a Percentage of Reading (Gain = +1) over Frequency with Internal Reference and Integrator Off

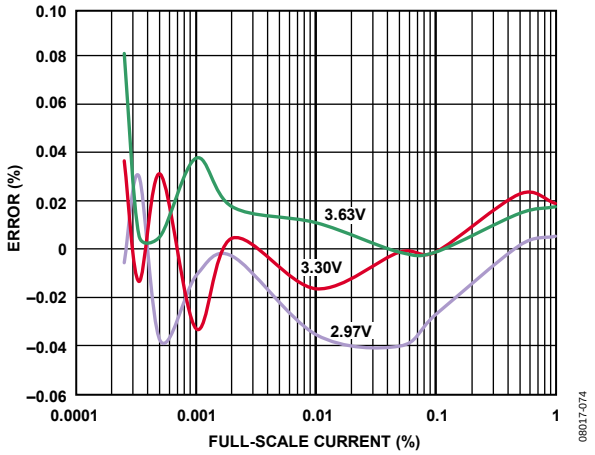


Figure 12. Total Active Energy Error as a Percentage of Reading (Gain = +1) over Power Supply with Internal Reference and Integrator Off

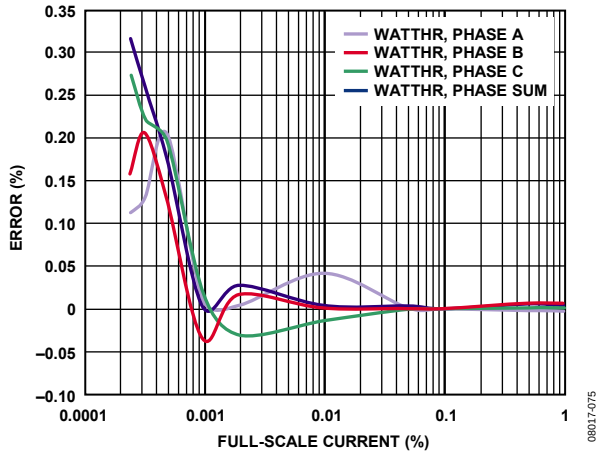


Figure 13. CF Total Active Energy Error as a Percentage of Reading (Gain = +1) with Internal Reference and Integrator Off

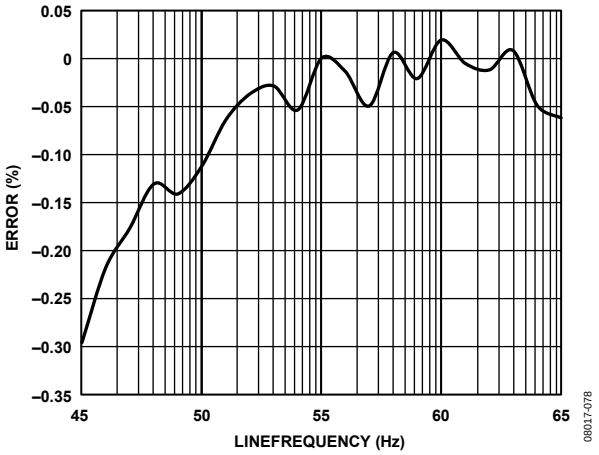


Figure 16. Total Active Energy Error as a Percentage of Reading (Gain = +16) over Frequency with Internal Reference and Integrator On

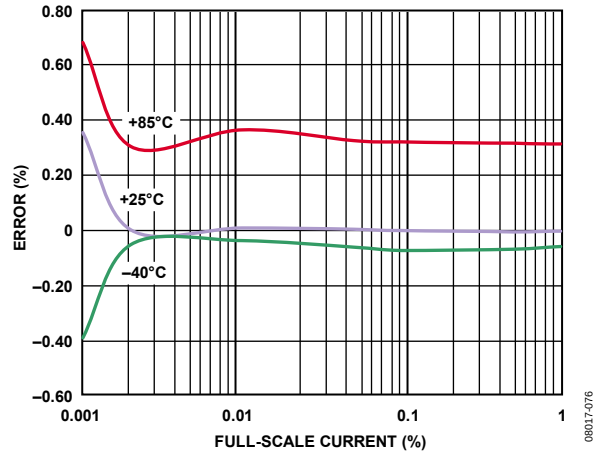


Figure 14. Total Active Energy Error as a Percentage of Reading (Gain = +16) over Temperature with Internal Reference and Integrator On

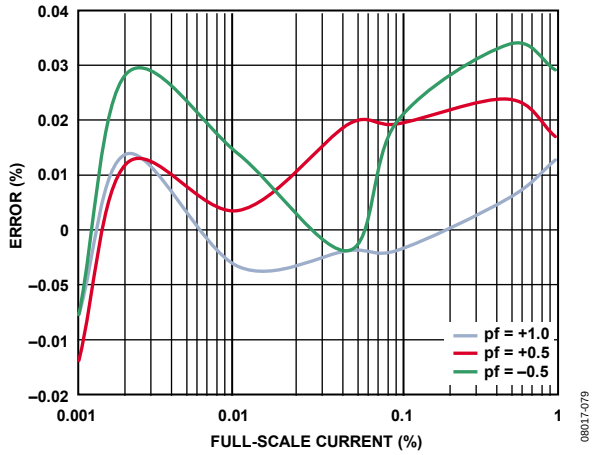


Figure 17. Apparent Energy Error as a Percentage of Reading (Gain = +1) over Temperature with Internal Reference and Integrator Off

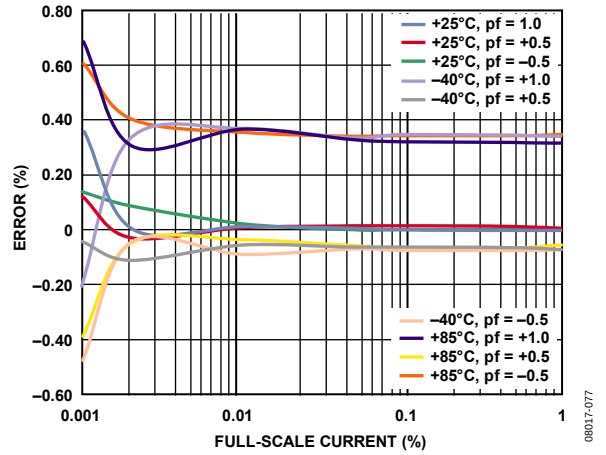


Figure 15. Total Active Energy Error as a Percentage of Reading (Gain = +16) over Power Factor with Internal Reference and Integrator On

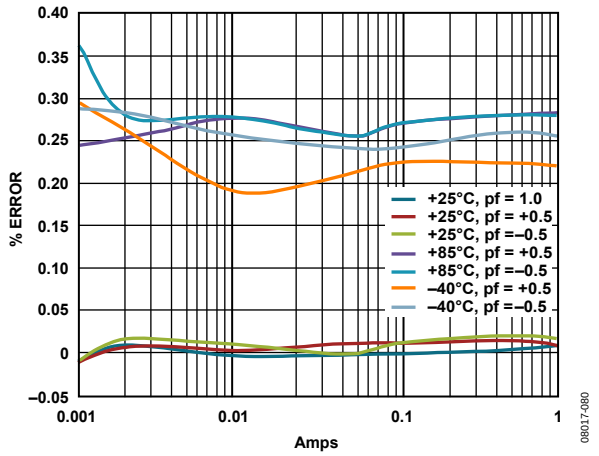


Figure 18. Apparent Energy Error as a Percentage of Reading (Gain = +1) over Power Factor with Internal Reference and Integrator Off

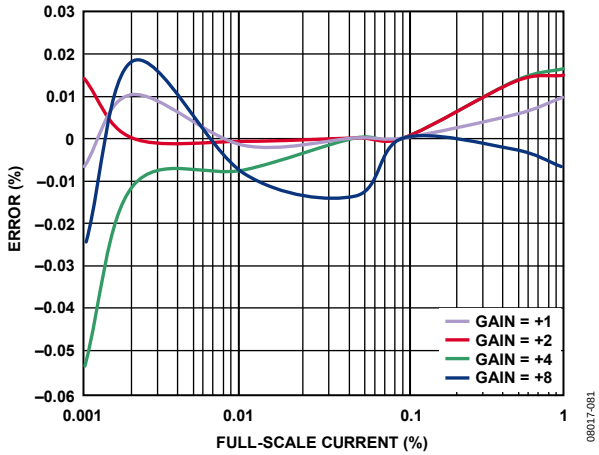


Figure 19. Apparent Energy Error as a Percentage of Reading over Gain with Internal Reference and Integrator Off

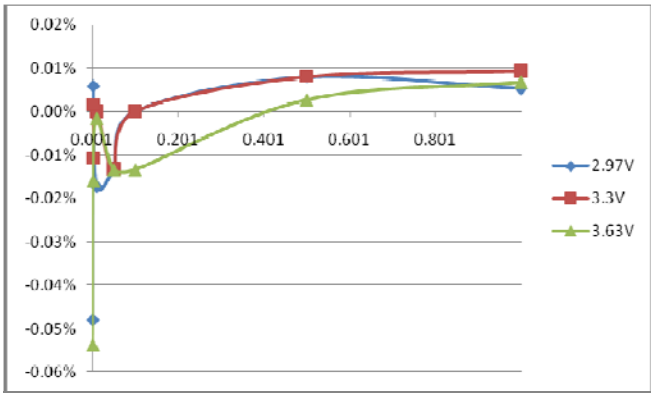


Figure 22. Total Active Energy Error as a Percentage of Reading (Gain = +1) over Power Factor with Internal Reference and Integrator Off

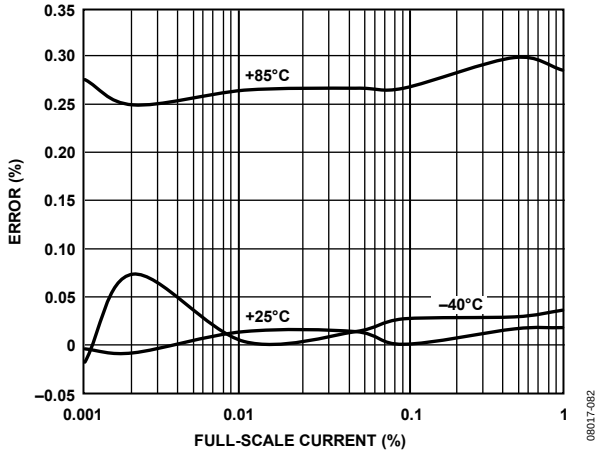


Figure 20. Apparent Energy Error as a Percentage of Reading (Gain = +1) over Temperature with External Reference and Integrator Off

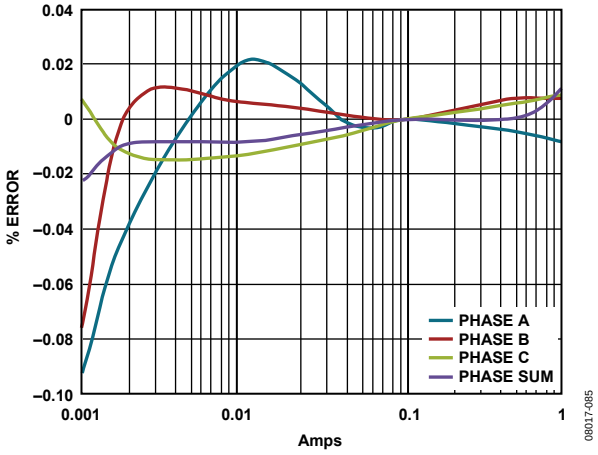


Figure 23. CF Apparent Energy Error as a Percentage of Reading (Gain = +1) with Internal Reference and Integrator Off

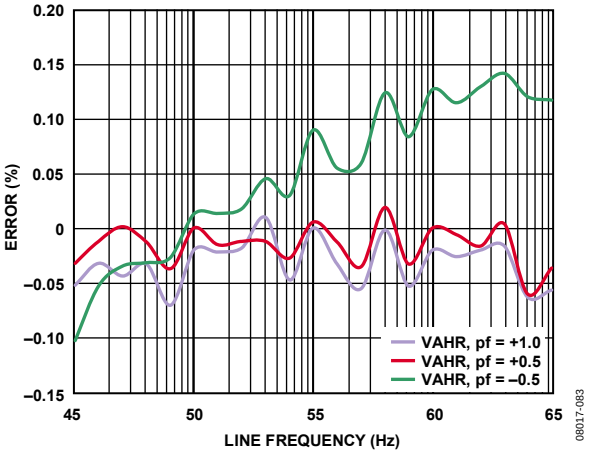


Figure 21. Apparent Energy Error as a Percentage of Reading (Gain = +1) over Frequency with Internal Reference and Integrator Off

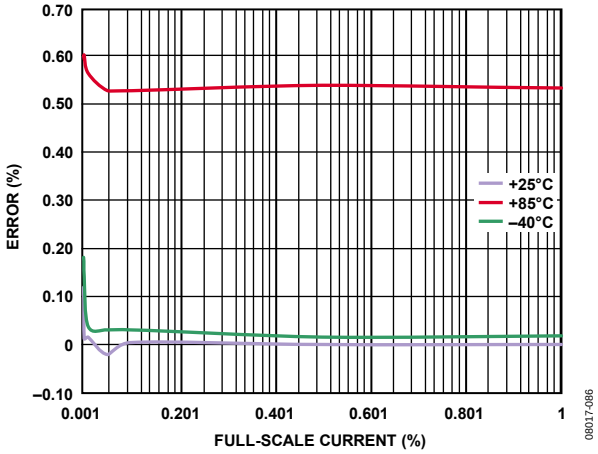


Figure 24. Apparent Energy Error as a Percentage of Reading (Gain = +16) over Temperature with Internal Reference and Integrator On

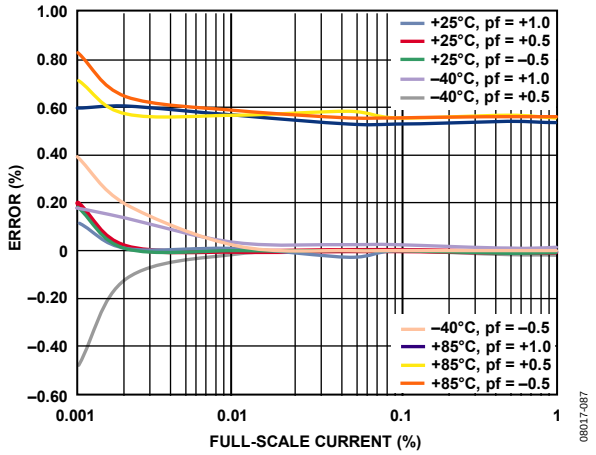


Figure 25. Apparent Energy Error as a Percentage of Reading (Gain = +16) over Power Factor with Internal Reference and Integrator On

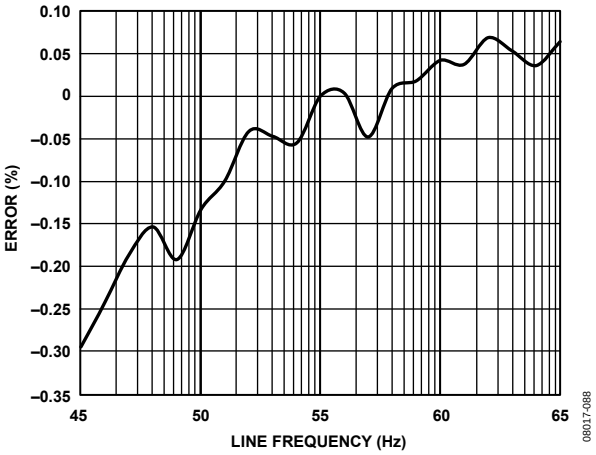


Figure 26. Apparent Energy Error as a Percentage of Reading (Gain = +16) over Frequency with Internal Reference and Integrator On

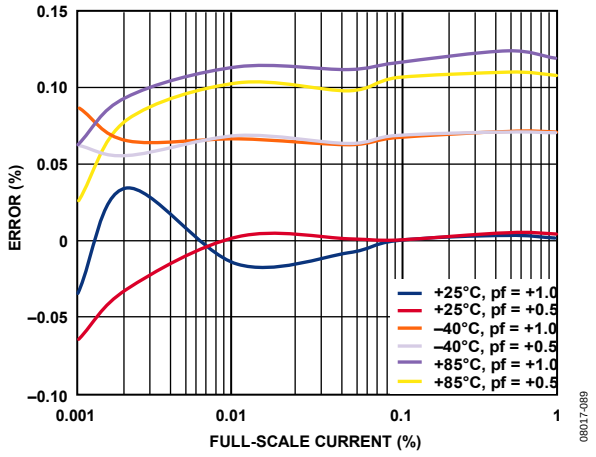


Figure 27. IRMS Error as a Percentage of Reading (Gain = +1) over Temperature with Internal Reference and Integrator Off

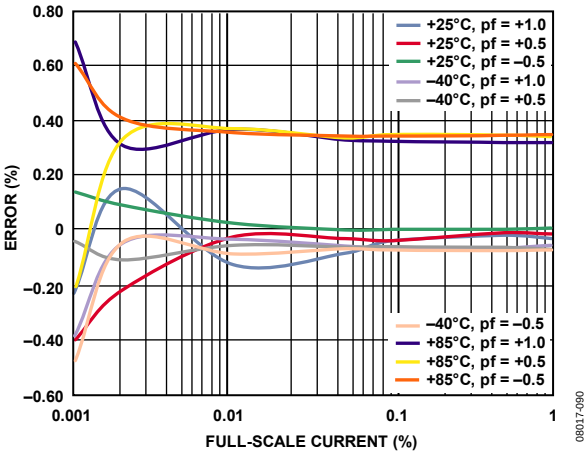


Figure 28. IRMS Error as a Percentage of Reading (Gain = +16) over Temperature with Internal Reference and Integrator On

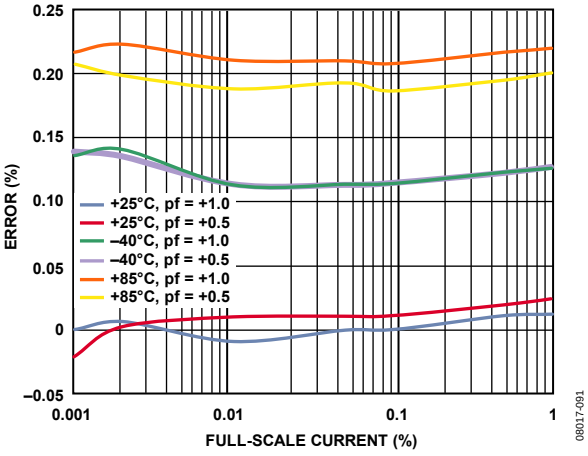


Figure 29. VRMS Error as a Percentage of Reading (Gain = +1) over Temperature with Internal Reference and Integrator Off

TBD

Figure 30. Phase A Current Channel Offset Distribution

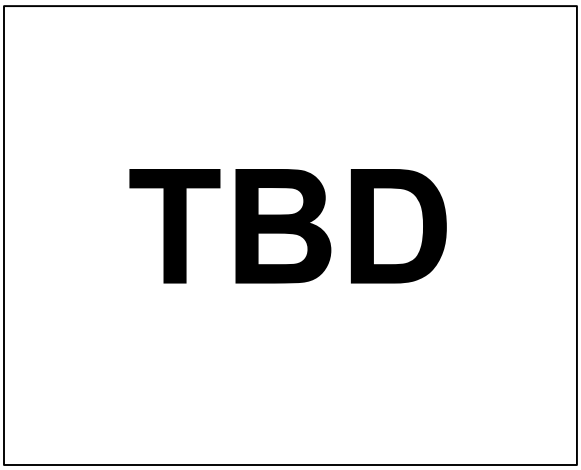


Figure 31. Phase B Current Channel Offset Distribution

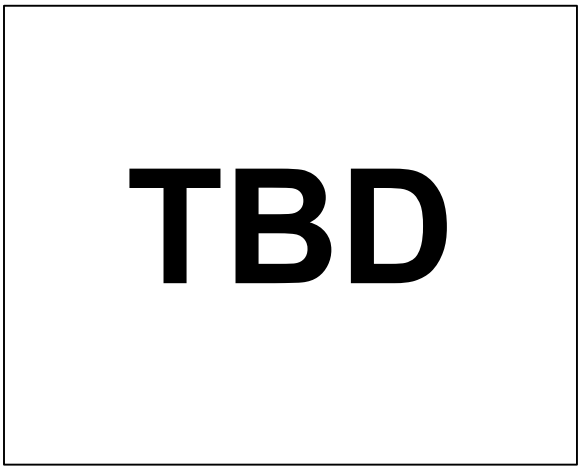


Figure 32. Phase C Current Channel Offset Distribution

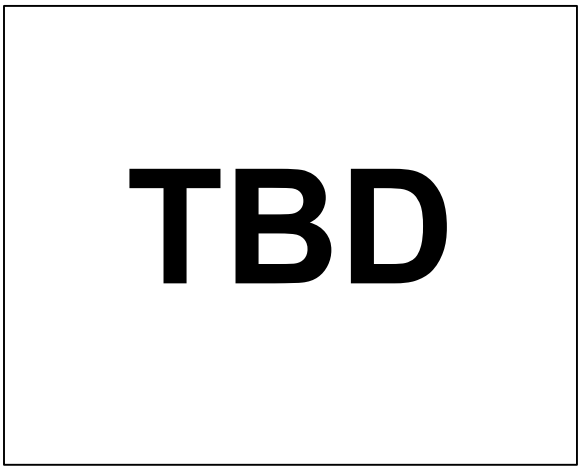


Figure 33. Phase A Voltage Channel Offset Distribution

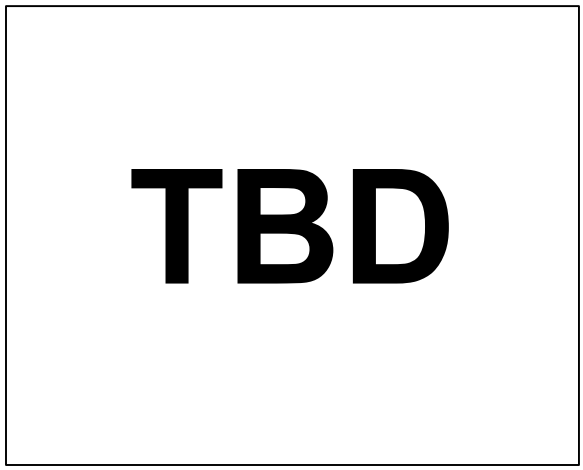


Figure 34. Phase B Voltage Channel Offset Distribution

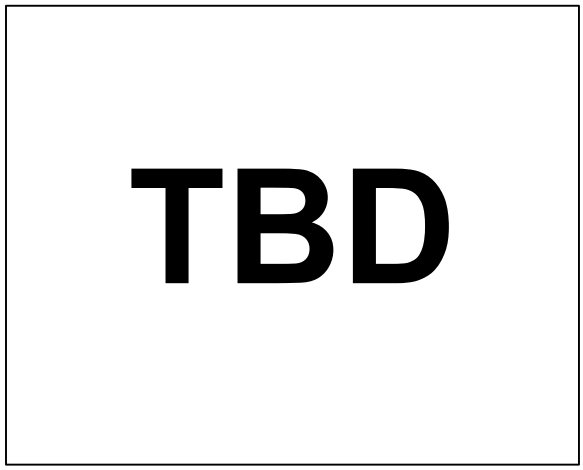


Figure 35. Phase C Voltage Channel Offset Distribution

TEST CIRCUIT

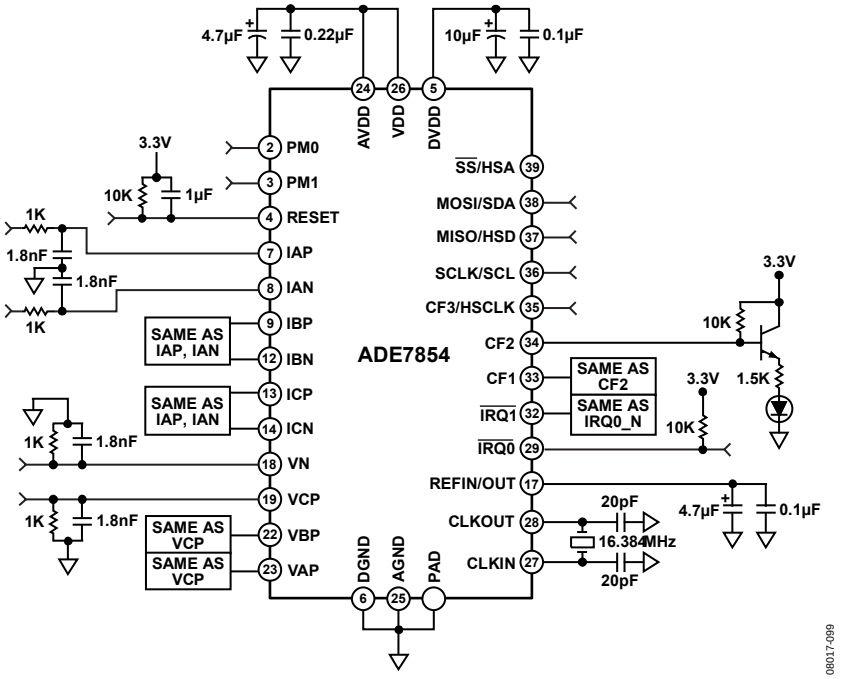


Figure 36. Test Circuit

TERMINOLOGY

Measurement Error

The error associated with the energy measurement made by the ADE7854 is defined by

$$Measurement\ Error = \frac{Energy\ Registered\ by\ ADE7858/7854 - True\ Energy}{True\ Energy} \times 100\% \quad (1)$$

Phase Error Between Channels

The high-pass filter (HPF) and digital integrator introduce a slight phase mismatch between the current and the voltage channel. The all-digital design ensures that the phase matching between the current channels and voltage channels in all three phases is within ±0.1° over a range of 45 Hz to 65 Hz and within ±0.2° over a range of 40 Hz to 1 kHz. This internal phase mismatch can be combined with the external phase error (from current sensor or component tolerance) and calibrated with the phase calibration registers.

Power Supply Rejection (PSR)

PSR quantifies the ADE7854 measurement error as a percentage of reading when the power supplies are varied. For the ac PSR measurement, a reading at nominal supplies (3.3 V) is taken. A second reading is obtained with the same input signal levels when an ac signal (TBD mV rms/TBD Hz) is introduced onto the supplies. Any error introduced by this ac signal is expressed as a percentage of reading (see the Measurement Error definition).

For the dc PSR measurement, a reading at nominal supplies (3.3 V) is taken. A second reading is obtained with the same input signal levels when the power supplies are varied by ±10%. Any error introduced is again expressed as a percentage of the reading.

ADC Offset Error

The ADC offset error refers to the dc offset associated with the analog inputs to the ADCs. It means that, with the analog inputs connected to AGND, the ADCs still see a dc analog input signal. The magnitude of the offset depends on the gain and input range selection (see the Typical Performance Characteristics section). However, the offset is removed from the current and voltage channels by an HPF, and the power calculation is not affected by this offset.

Gain Error

The gain error in the ADCs of the ADE7854 is defined as the difference between the measured ADC output code (minus the offset) and the ideal output code (see the Current Channel ADC section and the Voltage Channel ADC section). The difference is expressed as a percentage of the ideal code.

Gain Error Match

The gain error match is defined as the gain error (minus the offset) obtained when switching between a gain of 1, 2, 4, 8, or 16. It is expressed as a percentage of the output ADC code obtained under a gain of 1.

CF Jitter

The period of pulses at one of the CF1, CF2, or CF3 pins is continuously measured. The maximum, minimum, and average values of four consecutive pulses are computed as follows:

$$Maximum\ Value = Max(Period_0, Period_1, Period_2, Period_3)$$

$$Minimum\ Value = Min(Period_0, Period_1, Period_2, Period_3)$$

$$Average\ Value = \frac{Period_0, Period_1, Period_2, Period_3}{4}$$

The CF jitter is then computed as

$$CF_{JITTER} = \frac{Maximum\ Value - Minimum\ Value}{Average\ Value} \times 100[\%]$$

POWER MANAGEMENT

The ADE7854 has two modes of operation, which are determined by the state of the PM1 pin (see Table 7). This pin provides complete control of ADE7854 operation and can easily be connected to an external microprocessor I/O. The PM1 pin has internal pull-up resistors. Table 8 presents all characteristics of the power modes. Table 9 lists actions that are recommended before and after setting a new power mode.

POWER MODES

Table 7. Power Modes

Power Modes	PM1
PSM0, Normal Power Mode	0
PSM3, Sleep Mode	1

PSM0—Normal Power Mode

In PSM0 mode, the ADE7854 is fully functional. The PM1 pin is set low for the ADE7854 to enter this mode.

If the ADE7854 is in PSM3 mode and is switched into PSM0 mode, all control registers take the default values. The ADE7854 signals the end of the transition period by triggering the $\overline{\text{IRQ1}}$ interrupt pin low and setting Status Bit 15 (RSTDONE) in the STATUS1 register (Address 0xE503) to 1. This bit is set to 0 during the transition period and changes to 1 when the transition is complete. The status bit is cleared, and the $\overline{\text{IRQ1}}$ pin is set high by writing to the STATUS1register with the corresponding bit set to 1. Bit 15 (RSTDONE) in the MASK1 register (Address 0xE50B) does not have any functionality attached even if the $\overline{\text{IRQ1}}$ pin goes low when Status Bit 15 (RSTDONE) in the STATUS1 register is set to 1. This makes the RSTDONE interrupt unmaskable.

PSM3—Sleep Mode

In this mode, most of the internal circuits of the ADE7854 are turned off, and current consumption is at its lowest. The I²C, HSDC, and SPI ports are not functional in this mode. The $\overline{\text{RESET}}$, SCLK/SCL, MOSI/SDA, and $\overline{\text{SS}}$/HSA pins should be set high.

POWER-UP PROCEDURE

The ADE7854 contains an on-chip power supply monitor that supervises the power supply, VDD. At power-up, the chip is in an inactive state until VDD reaches 2 V ± 10%. As VDD crosses this threshold, the power supply monitor keeps the chip in this inactive state for 26 ms more, allowing VDD to achieve 3.3 V − 10%, the minimum recommended supply voltage. Because the PM1 pin has an internal pull-up resistor and the external microprocessor keeps it high, the ADE7854 always powers up in sleep mode (PSM3). Then, an external circuit (that is, the microprocessor) sets the PM1 pin low, allowing the ADE7854 to enter normal mode (PSM0). The passage from PSM3 mode (in which most of the internal circuitry is turned off) to PSM0 mode (in which all functionality is enabled) is completed in less than 40 ms (see Figure 37).

When the ADE7854 enters PSM0 mode, the I²C port is the active serial port. If the SPI port is used, the $\overline{\text{SS}}$ pin must be toggled three times high to low. This action selects the SPI port. If the I²C port is the active serial port, Bit 1 (I2C_LOCK) of the CONFIG2 register (Address 0xEC01) must be set to 1 to lock it in. Once locked in, the ADE7854 ignores spurious toggling of the $\overline{\text{SS}}$ pin, and an eventual switch to the SPI port is no longer possible. If the SPI port is the active serial port, any write to the CONFIG2 register locks the SPI port. Once locked, switching to the I²C port is no longer possible.

Only a power-down event or setting the $\overline{\text{RESET}}$ pin low resets the ADE7854 to use the I²C port. Once locked in, the serial port choice is maintained when the ADE7854 switches between the PSM0 and PSM3 power modes.

Immediately after entering PSM0, the ADE7854 sets all registers, including CONFIG2, to their default values. The ADE7854 signals the end of the transition period by triggering the $\overline{\text{IRQ1}}$ interrupt pin low and setting Status Bit 15 (RSTDONE) in the STATUS1 register (Address 0xE502) to 1. This bit is 0 during the transition period and changes to 1 when the transition ends.

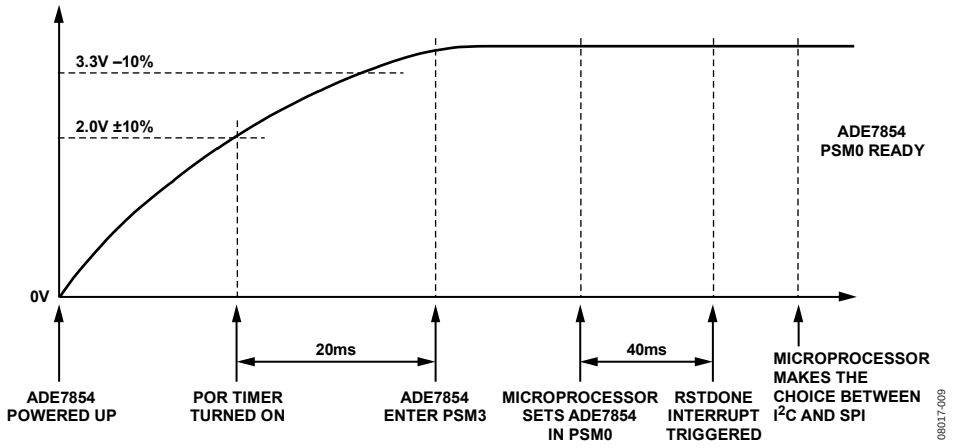


Figure 37. Power-Up Procedure

The status bit is cleared, and the $\overline{\text{IRQ1}}$ pin is set high again by writing to the STATUS1 register with the corresponding bit (RSTDONE) set to 1. Because the RSTDONE bit is an unmaskable interrupt, Status Bit 15 (RSTDONE) in the STATUS1 register must be cancelled for the $\overline{\text{IRQ1}}$ pin to return high. It is recommended to wait until the $\overline{\text{IRQ1}}$ pin goes low before accessing the STATUS1 register to test the state of the RSTDONE bit. As a good programming practice, it is also recommended at this point to cancel all other status flags in the STATUS1 and STATUS0 registers (Address 0xE502 and Address 0xE503, respectively) by writing a 1 to the corresponding bits.

Initially, the DSP is in idle mode. During this mode, no instructions are executed. This is the time to initialize all ADE7854 registers and then write 0x0001 into the RUN register (Address 0xE228) to start the digital signal processor (DSP) (see the Digital Signal Processor section for details about the RUN register).

If the supply voltage (VDD) falls below 2 V ± 10%, the ADE7854 goes into an inactive state, in which no measurements are executed.

RESET FUNCTIONALITY

Hardware Reset

The ADE7854 has a $\overline{\text{RESET}}$ pin. If the ADE7854 is in PSM0 mode and the $\overline{\text{RESET}}$ pin is set low, the ADE7854 enters into a hardware reset state. The ADE7854 must be in PSM0 mode for hardware reset to be considered. Setting the $\overline{\text{RESET}}$ pin low while the ADE7854 is in PSM3 mode does not have any effect. If the ADE7854 is in PSM0 mode and the $\overline{\text{RESET}}$ pin is toggled from high to low and then back to high after at least 10 µs, all the registers are set to their default values, including CONFIG2. The ADE7854 signals the end of the transition period by triggering the $\overline{\text{IRQ1}}$ interrupt pin low and setting Status Bit 15 (RSTDONE) in the STATUS1 register to 1. This bit is set to 0 during the transition period and changes to 1 when the transition ends. The status bit is cleared, and the $\overline{\text{IRQ1}}$ pin is returned high by writing to the STATUS1 register with the corresponding bit (RSDONE) set to 1.

After a hardware reset, the DSP is in idle mode, in which it does not execute instructions. Because the I^2C port is the default serial port of the ADE7854, it becomes active after a reset state. If the SPI is the port used by the external microprocessor, the procedure to enable it must be repeated immediately after the $\overline{\text{RESET}}$ pin is toggled high again (see the Serial Interfaces section).

Next, it is recommended to initialize all ADE7854 registers and then write 0x0001 to the RUN register to start the DSP (see the Digital Signal Processor section for details about the RUN register).

Software Reset

Bit 7 (SWRST) in the CONFIG register (Address 0xE618) manages the software reset functionality in PSM0 mode. The default value of this bit is 0. If this bit is set to 1, the ADE7854 enters a software reset state. In this state, almost all internal registers are set to their default values. In addition, the serial port, I^2C or SPI, that is in use remains unchanged if the lock-in procedure has been previously executed (see the Serial Interfaces section for details). The register that maintains its values, despite the SWRST bit being set to 1, is the CONFIG2 register. When the software reset ends, Bit 7 (SWRST) in the CONFIG register is cleared to 0, the $\overline{\text{IRQ1}}$ interrupt pin is set low, and Status Bit 15 (RSTDONE) in the STATUS1 register (Address 0xE503) is set to 1. This bit is 0 during the transition period and changes to 1 when the transition ends. The status bit is cleared, and the $\overline{\text{IRQ1}}$ pin is set high by writing to the STATUS1 register with the corresponding bit (RSTDONE) set to 1.

After a software reset ends, the DSP is in idle mode, which means that it does not execute any instruction. It is recommended to initialize all the ADE7854 registers and then write 0x0001 to the RUN register to start the DSP (see the Digital Signal Processor section for details about the RUN register).

Software reset functionality is not available in PSM3 mode.

Table 8. Power Modes and Related Characteristics

Power Mode	Registers	CONFIG2	I²C/SPI	Functionality
PSM0				
State After Hardware Reset	Set to default	Set to default	I²C enabled	All circuits are active; DSP is in idle mode
State After Software Reset	Set to default	Unchanged	Active serial port unchanged if lock-in procedure has been previously executed	All circuits are active; DSP is in idle mode
PSM3	Not available	Value set during PSM0 are unchanged	Disabled	Internal circuits shut down; serial ports not available.

Table 9. Recommended Actions When Changing Power Mode

Initial Power Mode	Recommended Actions Before Setting Next Power Mode	Next Power Mode	
		PSM0	PSM3
PSM0	Stop DSP by setting RUN[15:0] = 0x0000 Disable HSDC by clearing Bit 6 (HSDEN) to 0 in the CONFIG[15:0] register Mask interrupts by setting MASK0[31:0] = 0x0 and MASK1[31:0] = 0x0 Erase interrupt status flags in the STATUS0[31:0] and STATUS1[31:0] registers	N/A	No action required
PSM3	No action required	Wait until the $\overline{\text{IRQ1}}$ pin is triggered low Poll the STATUS1 register until Status Bit 15 (RSTDONE) is set to 1	N/A

THEORY OF OPERATION

ANALOG INPUTS

The ADE7854 provides six analog inputs that form current and voltage channels. The current channels consist of three pairs of fully differential voltage inputs: IAP and IAN, IBP and IBN, ICP and ICN. These voltage input pairs have a maximum differential signal of ±0.5 V. The maximum common-mode signal allowed on the inputs is ±25 mV. Figure 38 shows a schematic of the current channel inputs and their relationship to the maximum common-mode voltage.

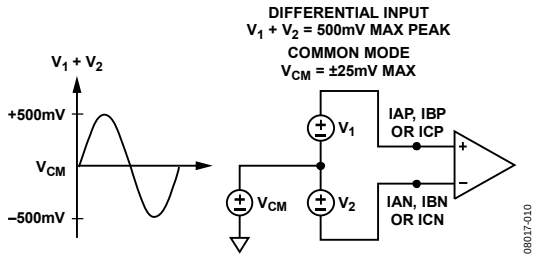


Figure 38. Maximum Input Level, Current Channels, Gain = 1

All inputs have a programmable gain amplifier (PGA) with a possible gain selection of 1, 2, 4, 8, or 16. As shown in Table 33, the gain of the IAx, IBx, and ICx inputs is set in the PGA1 bits of the GAIN register (Address 0xE60F[2:0]).

The voltage channel has three single-ended voltage inputs: VAP, VBP, and VCP. These single-ended voltage inputs have a maximum input voltage of ±0.5 V with respect to VN. In addition, the maximum signal level on the analog inputs for VxP and VN is ±0.5 V with respect to AGND. The maximum common-mode signal allowed on the inputs is ±25 mV. Figure 39 shows a schematic of the voltage channels inputs and their relationship to the maximum common-mode voltage.

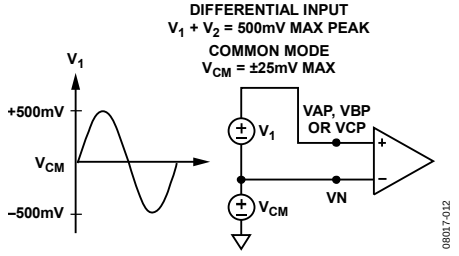


Figure 39. Maximum Input Level, Voltage Channels, Gain = 1

All inputs have a programmable gain with a possible gain selection of 1, 2, 4, 8, or 16. The setting is done using the PGA3 bits in the GAIN register (Address 0xE60F[8:6], see Table 33). Figure 40 shows how the gain selection from the GAIN register works in both current and voltage channels.

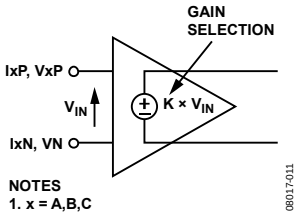


Figure 40. PGA in Current and Voltage Channels

ANALOG-TO-DIGITAL CONVERSION

The ADE7854 has six Σ-Δ ADCs. In PSM0 mode, all ADCs are active. In PSM3 mode, the ADCs are powered down to minimize power consumption.

For simplicity, the block diagram in Figure 41 shows a first-order Σ-Δ ADC. The converter consists of the Σ-Δ modulator and the digital low-pass filter.

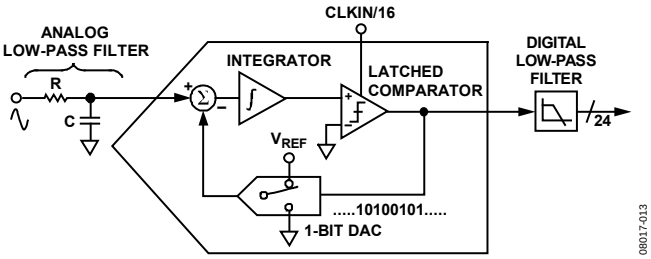


Figure 41. First-Order Σ-Δ ADC

The Σ-Δ modulator converts the input signal into a continuous serial stream of 1s and 0s at a rate determined by the sampling clock. In the ADE7854, the sampling clock is equal to 1.024 MHz (CLKIN/16). The 1-bit DAC in the feedback loop is driven by the serial data stream. The DAC output is subtracted from the input signal. If the loop gain is high enough, the average value of the DAC output (and, therefore, the bit stream) can approach that of the input signal level. For any given input value in a single sampling interval, the data from the 1-bit ADC is virtually meaningless. Only when a large number of samples are averaged is a meaningful result obtained. This averaging is carried out in the second part of the ADC, the digital low-pass filter. By averaging a large number of bits from the modulator, the low-pass filter can produce 24-bit data-words that are proportional to the input signal level.

The Σ-Δ converter uses two techniques to achieve high resolution from what is essentially a 1-bit conversion technique. The first is oversampling. Oversampling means that the signal is sampled at a rate (frequency) that is many times higher than the bandwidth of interest. For example, the sampling rate in the The ADE7854 is 1.024 MHz and the bandwidth of interest is 40 Hz to 2 kHz. Oversampling has the effect of spreading the quantization noise (noise due to sampling) over a wider bandwidth. With the noise spread more thinly over a wider bandwidth, the quantization noise in the band of interest is lowered (see Figure 42). However, oversampling alone is not efficient enough to improve the signal-to-noise ratio (SNR) in the bandwidth of interest.

For example, an oversampling ratio of 4 is required just to increase the SNR by only 6 dB (1 bit). To keep the oversampling ratio at a reasonable level, it is possible to shape the quantization noise so that the majority of the noise lies at the higher frequencies. In the Σ-Δ modulator, the noise is shaped by the integrator, which has a high-pass-type response for the quantization noise.

This is the second technique used to achieve high resolution. The result is that most of the noise is at the higher frequencies, where it can be removed by the digital low-pass filter. This noise shaping is shown in Figure 42.

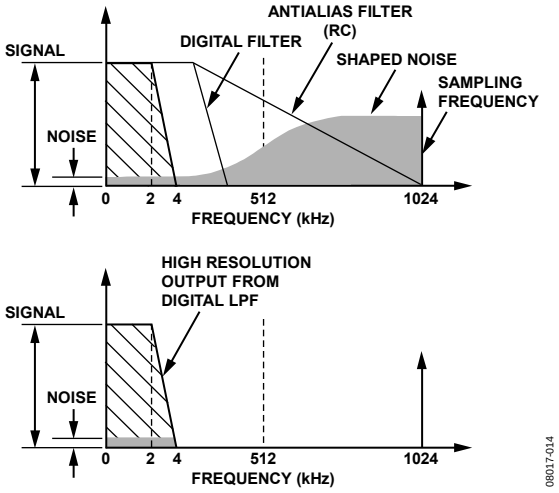


Figure 42. Noise Reduction Due to Oversampling and Noise Shaping in the Analog Modulator

Antialiasing Filter

Figure 41 also shows an analog low-pass filter (RC) on the input to the ADC. This filter is placed outside the ADE7854; its role is to prevent aliasing. Aliasing is an artifact of all sampled systems and is illustrated in Figure 43. Aliasing means that frequency components in the input signal to the ADC, which are higher than half the sampling rate of the ADC, appear in the sampled signal at a frequency below half the sampling rate. Frequency components (the arrows shown in black) above half the sampling frequency (also known as the Nyquist frequency, that is, 512 kHz) are imaged or folded back down below 512 kHz. This happens with all ADCs, regardless of the architecture.

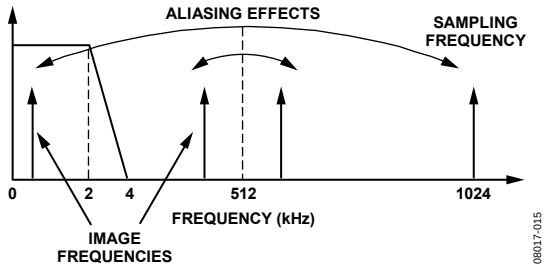


Figure 43. Aliasing Effects

In the example shown, only frequencies near the sampling frequency, that is, 1.024 MHz, move into the band of interest for metering, i.e., 40 Hz to 2 kHz. To attenuate the high frequency (near 1.024 MHz) noise and prevent the distortion of the band of interest, an LPF (low-pass filter) has to be introduced. For conventional current sensors, it is recommended that one RC filter with a corner frequency of 5 kHz be used, so that the attenuation is sufficiently high at the sampling frequency of 1.024 MHz. The 20 dB per decade attenuation of this filter is usually sufficient ficient to eliminate the effects of aliasing for conventional current sensors. However, for a di/dt sensor such as a Rogowski coil, the sensor has a 20 dB per decade gain. This gain neutralizes the 20 dB per decade attenuation produced by the LPF.

Therefore, when using a di/dt sensor, care should be taken to offset the 20 dB per decade gain. One simple approach is to cascade one additional RC filter, producing a −40 dB per decade attenuation.

ADC Transfer Function

All ADCs in the ADE7854 are designed to produce the same 24-bit signed output code for the same input signal level. With a full-scale input signal of 0.5 V and an internal reference of 1.2 V, the ADC output code is nominally 5,928,256 (0x5A7540). The code from the ADC can vary between 0x800000 (−8,388,608) and 0x7FFFFF (+8,388,607); this is equivalent to an input signal level of ±0.707 V. However, for specified performance, it is recommended not to exceed the nominal range of ±0.5V. The ADC performance is guaranteed only for input signals <±0.5 V.

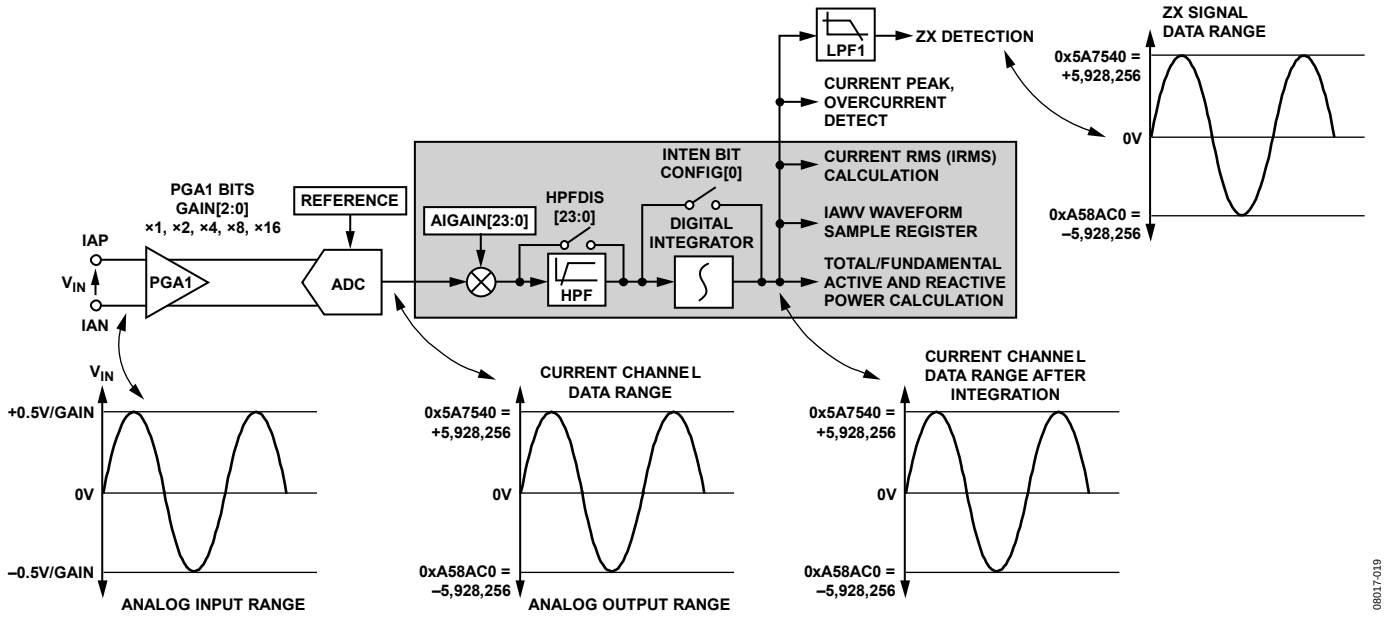


Figure 44. Current Channel Signal Path

CURRENT CHANNEL ADC

Figure 44 shows the ADC and signal processing path for the IAP and IAN inputs of the current channels (the same information applies to the IBP/IBN and ICP/ICN inputs). The ADC outputs are signed, twos complement, 24-bit data-words and are available at a rate of 8 kSPS. With the specified full-scale analog input signal of ±0.5 V, the ADC produces its maximum output code value. This diagram shows a full-scale voltage signal being applied to the differential inputs IAP and IAN. The ADC output swings between −5,928,256 (0xA58AC0) and +5,928,256 (0x5A7540).

Current Waveform Gain Registers

There is a multiplier in the signal path of each phase current. The current waveform can be changed ±100% by writing a correspondent twos complement number to the 24-bit signed current waveform gain registers (AIGAIN, Address 0x4380; BIGAIN, Address 0x4382; and CIGAIN, Address 0x4384). For example, if 0x400000 is written to those registers, the ADC output is scaled up by 50%. To scale the input by −50%, write 0xC00000 to the registers. Equation 1 describes mathematically the function of the current waveform gain registers.

$$Current\ Waveform = ADC\ Output \times \left(1 + \frac{Content\ of\ Current\ Gain\ Register}{2^{23}}\right) \quad (1)$$

Changing the content of the AIGAIN, BIGAIN, or CIGAIN registers affects all calculations based on its current; that is, it affects the corresponding phase active/reactive/apparent energy and current rms calculation. In addition, waveform samples are also scaled accordingly.

Note that the serial ports of the ADE7854 work on 32-, 16-, or 8-bit words, and the DSP works on 28 bits. The 24-bit AIGAIN, BIGAIN, and CIGAIN registers are accessed as 32-bit registers, with the four MSBs padded with 0s and sign extended to 28 bits (see Figure 45).

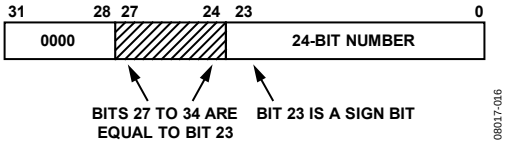


Figure 45. 24-Bit xIGAIN Registers Are Transmitted as 32-Bit Words

Current Channel High-Pass Filter (HPF)

The ADC outputs can contain a dc offset. This offset may create errors in power and rms calculations. High-pass filters (HPFs) are placed in the signal path of the phase currents and of the phase voltages. If enabled, the HPF eliminates any dc offset on the current channel. All filters are implemented in the DSP and, by default, they are all enabled: the 24-bit HPFDIS register (Address 0x43B6) is cleared to 0x00000000. All filters are disabled by setting the HPFDIS register to any nonzero value.

As previously stated, the serial ports of the ADE7854 work on 32-, 16-, or 8-bit words. The HPFDIS register is accessed as a 32-bit register with the eight MSBs padded with 0s (see Figure 46).

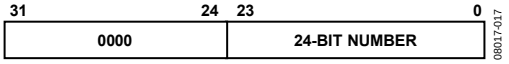


Figure 46. 24-Bit HPFDIS Register Is Transmitted as a 32-Bit Word

Current Channel Sampling

The waveform samples of the current channel are taken at the out-put of the HPF and stored in the 24-bit, signed IAWV, IBWV, and ICWV registers (Address 0xE50C, Address 0xE50D, and Address 0xE50E, respectively) at a rate of 8 kSPS. All power and rms calculations remain uninterrupted during this process. Status Bit 17 (DREADY) in the STATUS0 register (Address 0xE502) is set when the IAWV, IBWV, and ICWV registers are available to be read using the I²C or SPI serial ports. Setting Bit 17 (DREADY) in the MASK0 register (Address 0xE50A) enables an interrupt to be set when the DREADY flag is set (see the Digital Signal Processor (DSP) section).

As previously stated, the serial ports of the ADE7854 work on 32-, 16-, or 8-bit words. When the 24-bit, signed IAWV, IBWV, and ICWV registers are read from the ADE7854, they are transmitted as signed and extended to 32 bits (see Figure 47).

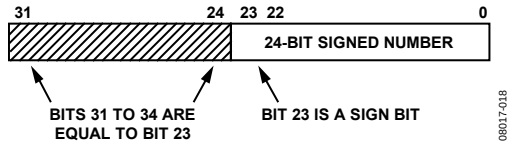


Figure 47. 24-Bit IxWV Registers Are Transmitted as 32-Bit Signed Words

The ADE7854 contains an HSDC port that is designed to provide fast access to the waveform sample registers (see the High Speed Data Capture Interface section for more information).

di/dt CURRENT SENSOR AND DIGITAL INTEGRATOR

The di/dt sensor detects magnetic field changes that are caused by the ac current. Figure 48 shows the principle of a di/dt current sensor.

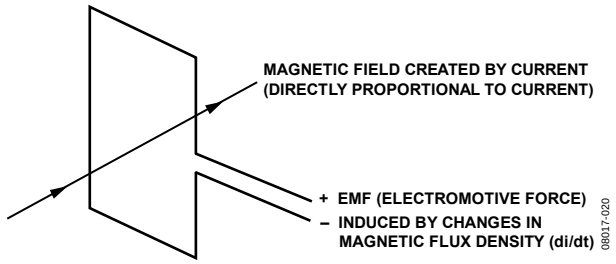


Figure 48. Principle of a di/dt Current Sensor

The flux density of a magnetic field induced by a current is directly proportional to the magnitude of the current. The changes in the magnetic flux density passing through a conductor loop generate an electromotive force (EMF) between the two ends of the loop. The EMF is a voltage signal that is proportional to the di/dt of the current. The voltage output from the di/dt current sensor is determined by the mutual inductance between the current carrying conductor and the di/dt sensor.

Due to the di/dt sensor, the current signal must be filtered before it can be used for power measurement. On each phase current datapath, there is a built-in digital integrator to recover the current signal from the di/dt sensor. The digital integrator is disabled by default when the ADE7854 is powered up and after a reset.

Setting Bit 0 (INTEN) of the CONFIG register (Address 0xE618) turns on the integrator. Figure 49 and Figure 50 show the magnitude and phase response of the digital integrator.

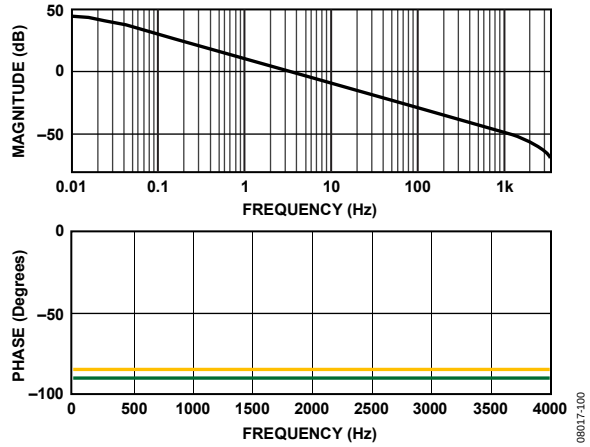


Figure 49. Combined Gain and Phase Response of the Digital Integrator

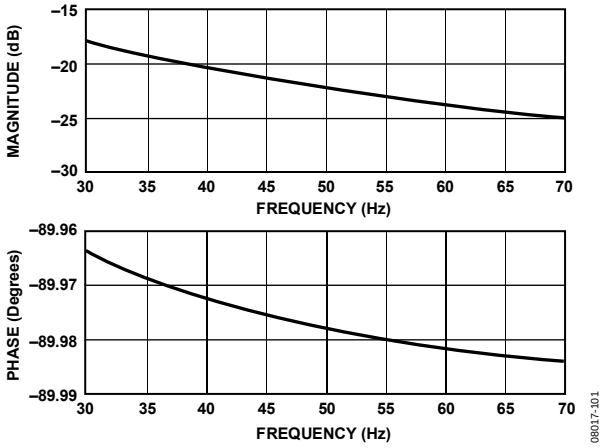


Figure 50. Combined Gain and Phase Response of the Digital Integrator (30 Hz to 70 Hz)

Note that the integrator has a −20 dB/dec attenuation and approximately −90° phase shift. When combined with a di/dt sensor, the resulting magnitude and phase response should be a flat gain over the frequency band of interest. However, the di/dt sensor has a 20 dB/dec gain associated with it and generates significant high frequency noise. An antialiasing filter of at least the second order is needed to prevent the noise alias from reappearing in the band of interest when the ADC is sampling (see the Antialiasing Filter section).

The 24-bit, signed DICOEFF register (Address 0x43B5) is used in the digital integrator algorithm. At power-up or after a reset, its value is 0x000000. Before turning on the integrator, this register must be initialized with 0xFF8000. The DICOEFF register is not used when the integrator is turned off, and, in this case, it can be left at 0x000000.

As previously stated, the serial ports of the ADE7854 work on 32-, 16-, or 8-bit words. Similar to the registers presented in Figure 45, the 24-bit, signed DICOEFF register (Address0x43B5) is accessed as a 32-bit register with the four MSBs padded with 0s and sign extended to 28 bits.

When the digital integrator is switched off, the ADE7854 can be used directly with a conventional current sensor, such as a current transformer (CT).

VOLTAGE CHANNEL ADC

Figure 51 shows the ADC and signal processing chain for the VAP input in the voltage channel. The VBP and VCP channels have similar processing chains. The ADC outputs are signed, twos complement, 24-bit words that are available at a rate of 8 kSPS. With the specified full-scale analog input signal of ±0.5 V, the ADC produces its maximum output code value. This diagram shows a full-scale voltage signal being applied to the differential inputs, VAP and VN. The ADC output swings between −5,928,256 (0xA558AC0) and +5,928,256 (0x5A7540).

Voltage Waveform Gain Registers

There is a multiplier in the signal path of each phase voltage. The voltage waveform can be changed by ±100% by writing a correspondent twos complement number to the 24-bit signed current waveform gain registers (AVGAIN, Address 0x4381; BVGAIN, Address 0x4383; and CVGAIN, Address 0x4385). For example, if 0x400000 is written to those registers, the ADC output is scaled up by 50%. To scale the input by −50%, write 0xC00000 to the registers. Equation 2 describes mathematically the function of the current waveform gain registers.

$$Voltage\ \ Waveform = ADC\ \ Output \times \left(1 + \frac{Content\ of\ Voltage\ Gain\ Register}{2^{23}}\right) \quad (2)$$

Changing the content of AVGAIN, BVGAIN, and CVGAIN affects all calculations based on its voltage; that is, it affects the corresponding phase active/reactive/apparent energy and voltage rms calculation. In addition, waveform samples are scaled accordingly.

As previously stated, the serial ports of the ADE7854 work on 32-, 16-, or 8-bit words, and the DSP works on 28 bits. As shown in Figure 45 with the xIGAIN registers, the AVGAIN, BVGAIN, and CVGAIN registers are accessed as 32-bit registers with the four MSBs padded with 0s and sign extended to 28 bits.

Voltage Channel HPF

As seen in the Current Channel High-Pass Filter (HPF) section, the ADC outputs may contain a dc offset that can create errors in power and rms calculations. HPFs are placed in the signal path of the phase voltages, similar to the ones in the current channels. The HPFDIS register (Address 0x43B6) can enable or disable the filters (see the Current Channel High-Pass Filter (HPF) section).

Voltage Channel Sampling

The waveform samples of the current channel are taken at the output of the HPF and stored in the 24-bit, signed VAWV, VBWV, and VCWV registers (Address 0xE510, Address 0xE511, and Address 0xE512, respectively) at a rate of 8 kSPS. All power and rms calculations remain uninterrupted during this process. Status Bit 17 (DREADY) in the STATUS0 register (Address 0xE502) is set when the VAWV, VBWV, and VCWV registers are available to be read using the I²C or SPI serial ports. Setting Bit 17 (DREADY) in the MASK0 register (Address 0xE50A) enables an interrupt to be set when the DREADY flag is set. See the Digital Signal Processor section for more information about the DREADY bit.

As previously stated, the serial ports of the ADE7854 work on 32-, 16-, or 8-bit words. Like the registers that are presented in Figure 46, the 24-bit, signed VAWV, VBWV, and VCWV registers are transmitted, signed, and extended to 32 bits.

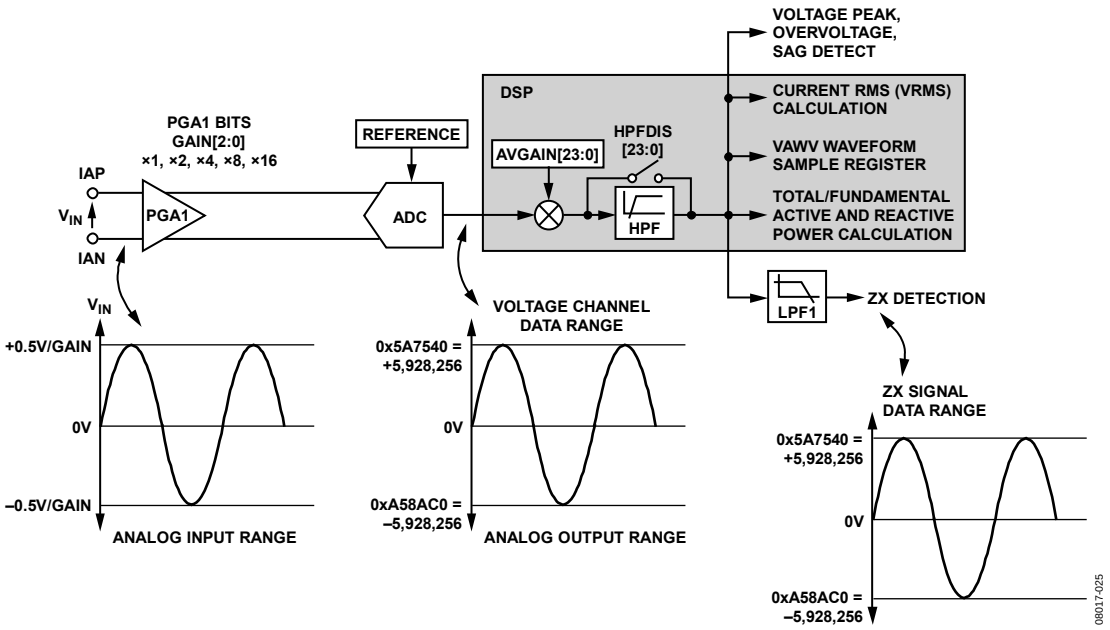


Figure 51. Voltage Channel Datapath

The ADE7854 contains an HSDC port that is designed to provide fast access to the waveform sample registers. See the High Speed Data Capture Interface section for more information.

CHANGING THE PHASE VOLTAGE DATAPATH

The ADE7854 can direct one phase voltage input to the computational datapath of another phase. For example, Phase A voltage can be introduced into the Phase B computational datapath, which means that all powers computed by the ADE7854 in Phase B are based on Phase A voltage and Phase B current.

Bits[9:8] (VTOIA) of the CONFIG register (Address 0xE618) manage the phase A voltage measured at the VAP pin. If VTOIA = 00 (default value), the voltage is directed to the Phase A computational datapath; if VTOIA = 01, the voltage is directed to the Phase B datapath; and if VTOIA = 10, the voltage is directed to the Phase C datapath. If VTOIA = 11, the ADE7854 behaves as though VTOIA = 00.

Bits[11:10] (VTOIB) of the CONFIG register manage the Phase B voltage measured at the VBP pin. If VTOIB = 00 (default value), the voltage is directed to the Phase B computational datapath; if VTOIB = 01, the voltage is directed to the Phase C datapath; and if VTOIB = 10, the voltage is directed to the Phase A datapath. If VTOIB = 11, the ADE7854 behaves as though VTOIB = 00.

Bits[13:12] (VTOIC) of the CONFIG register manage the Phase C voltage measured at the VCP pin. If VTOIC = 00 (default value), the voltage is directed to the Phase C computational datapath; if VTOIC = 01, the voltage is directed to the Phase A datapath; and if VTOIC = 10, the voltage is directed to the Phase B path. If VTOIC = 11, the ADE7854 behaves as though VTOIC = 00.

Figure 52 shows Phase A voltage used in the Phase B datapath, Phase B voltage used in the Phase C datapath, and Phase C voltage used in the Phase A datapath.

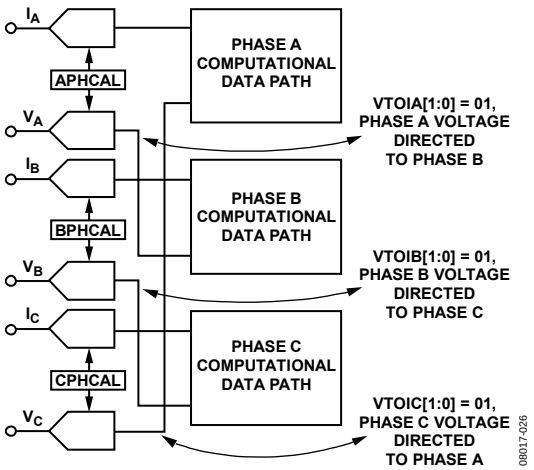


Figure 52. Phase Voltages Used in Different Datapaths

POWER QUALITY MEASUREMENTS

Zero-Crossing Detection

The ADE7854 has a zero-crossing (ZX) detection circuit on the current and voltage channels. Zero-crossing events are used as a time base for various power quality measurements and in the calibration process.

A zero crossing is generated from the output of LPF1. The low-pass filter is designed to eliminate all harmonics of 50 Hz and 60 Hz systems and help to identify the zero-crossing events on the fundamental components of both current and voltage channels. The digital filter has a pole at 80 Hz and is clocked at 256 kHz. As a result, there is a phase lag between the analog input signal (one of IAx, IBx, ICx, VAP, VBP, and VCP) and the output of LPF1. The error in ZX detection is 0.07° for 50 Hz systems and 0.085° for 60 Hz systems. The phase lag response of LPF1 results in a time delay of approximately 31.4° or 1.74 ms at 50 Hz between its input and output. The overall delay between the zero crossing on the analog inputs and the ZX detection obtained after LPF1 is approximately 39.6° or 2.2 ms at 50 Hz. The ADC and HPF introduce the additional delay. The LPF1 cannot be disabled to assure a good resolution of the ZX detection. Figure 53 shows how the zero-crossing signal is detected.

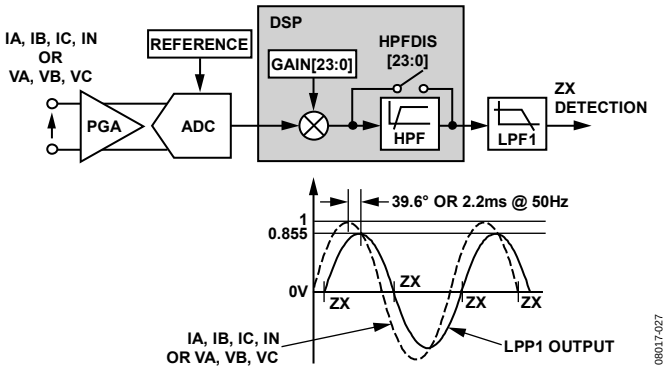


Figure 53. ZX Detection on Voltage and Current Channels

To provide additional protection from noise, input signals to the voltage channel with an amplitude of <10% of full scale do not generate zero-crossing events at all. The current channel ZX detection circuit is active for all input signals, independent of their amplitude.

The ADE7854 contains six ZX detection circuits, one for the voltage and current channels of each phase. Each circuit drives one flag in the STATUS1 register (Address 0xE503). If the circuit placed in the Phase A voltage channel detects one zero-crossing event, Bit 9 (ZXVA) in the STATUS1 register is set to 1. Similarly, the Phase B voltage circuit drives Bit 10 (ZXVB), the Phase C voltage circuit drives Bit 11 (ZXVC) and the circuits placed in the current channel drive (Bit 12 (ZXIA), Bit 13 (ZXIB), and Bit 14 (ZXIC)). If a ZX detection bit is set in the MASK1 register (Address 0xE50B), the $\overline{\text{IRQ1}}$ interrupt pin is driven low, and the corresponding status flag is set to 1. The status bit is cleared, and the $\overline{\text{IRQ1}}$ pin is set high again by writing to the STATUS1 register with the status bit set to 1.

Zero-Crossing Timeout

Every ZX detection circuit has an associated timeout register. This register is loaded with the value written into the 16-bit ZXTOUT register (Address 0xE60D) and is decremented by 1 LSB every 62.5 µs (16 kHz clock). The register is reset to the ZXTOUT value every time a zero crossing is detected. The default value of this register is 0xFFFF. If the timeout register decrements to 0 before a zero crossing is detected, one of Bits[8:3] of the STATUS1 register is set to 1. Bit 3 (ZXTOVA), Bit 4 (ZXTOVB), and Bit 5 (ZXTOVC) refer to Phase A, Phase B, and Phase C, respectively, of the voltage channel, and Bit 6 (ZXTOIA), Bit 7 (ZXTOIB), and Bit 8 (ZXTOIC) refer to Phase A, Phase B, and Phase C, respectively, of the current channel. If one of the ZXTOVx or ZXTOIx bits is set in the MASK1 register, the $\overline{\text{IRQ1}}$ interrupt pin is driven low when the corresponding status bit is set to 1. The status bit is cleared, and the $\overline{\text{IRQ1}}$ pin is set high again by writing to the STATUS1 register with the status bit set to 1.

The resolution of the ZXTOUT register is 62.5 µs (16 kHz clock) per LSB. Thus, the maximum time-out period for an interrupt is 4.096 sec: 2^{16}/16 kHz.

Figure 54 shows the mechanism of the zero-crossing timeout detection when the voltage or the current signal stays at a fixed dc level for more than 62.5 × ZXTOUT µs.

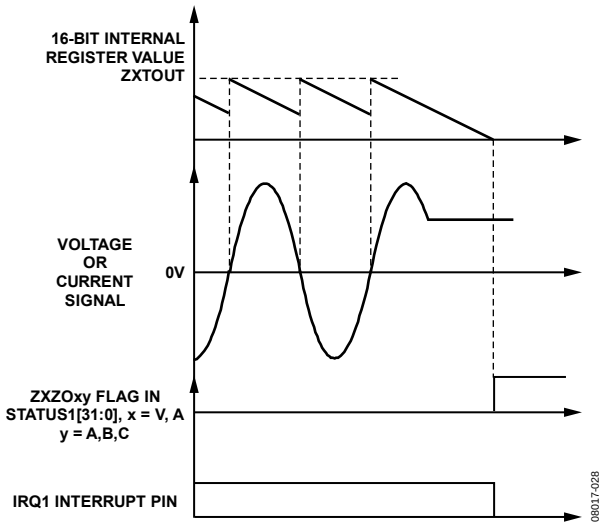


Figure 54. Zero-Crossing Timeout Detection

Phase Sequence Detection

The ADE7854 has an on-chip phase sequence error detection circuit. This detection works on phase voltages and considers only the zero crossings determined by their negative-to-positive transitions. The regular succession of these zero-crossing events is Phase A, followed by Phase B, followed by Phase C (see Figure 55). If the sequence of zero-crossing events is, instead, Phase A, followed by Phase C, followed by Phase B, Status Bit 19 (SEQERR) in the STATUS1 register is set. If Bit 19 (SEQERR) in the MASK1 register is set to 1 and a phase sequence error event is triggered, the $\overline{\text{IRQ1}}$ interrupt pin is driven low. The status bit is cleared, and the $\overline{\text{IRQ1}}$ pin is set high by writing to the STATUS1 register with the SEQERR status bit set to 1.

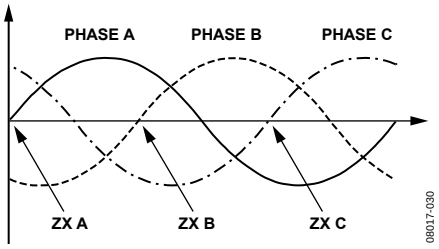


Figure 55. Phase Sequence Detection

The phase sequence error detection circuit is functional only when the ADE7854 is connected in a 3-phase, 4-wire, three-voltage sensors configuration, with the CONSEL bits in the ACCMODE register (Address 0xE701[5:4]) set to 00. In all other configurations, only two voltage sensors are used and, therefore, it is not recommended that the detection circuit be used. In these cases, the time intervals between phase voltages should be used to analyze the phase sequence (see the Time Interval Between Phases section).

Figure 56 shows an example in which Phase A voltage is not followed by Phase B voltage but, instead, by Phase C voltage. Every time a negative-to-positive zero crossing occurs, Status Bit 19 (SEQERR) in the STATUS1 (Address 0xE503) register is set to 1 because such zero crossings on Phase C, Phase B, or Phase A cannot come after zero crossings from Phase A, Phase C, or Phase B zero crossings, respectively.

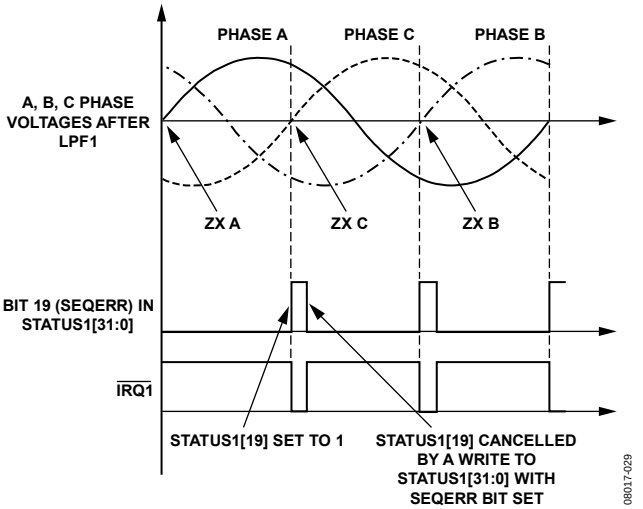


Figure 56. SEQERR Bit Set to 1 When Phase A Voltage Is Followed by Phase C Voltage

When a phase sequence error is detected, the time measurement between various phase voltages (see the Time Interval Between Phases section) can help to identify which phase voltage should be considered with another phase current in the computational datapath. Bits[9:8] (VTOIA), Bits[11:10] (VTOIB) and Bits[13:12] (VTOIC) in the CONFIG register (Address 0xE618) can be used to direct one phase voltage to the datapath of another phase (see the Changing the Phase Voltage Datapath section).

Time Interval Between Phases

The ADE7854 has the capability to measure the time delay between phase voltages, between phase currents, or between voltages and currents of the same phase. The negative-to-positive transitions identified by the zero-crossing detection circuit are used as start and stop measuring points. Only one set of such measurements is available at a time, based on Bits[10:9] (ANGLESEL) in the COMPMODE register (Address 0xE60E).

When the ANGLESEL bits are set to 00 (the default value), then the delays between voltages and currents on the same phase are measured. The delay between Phase A voltage and Phase A current is stored in the 16-bit, unsigned ANGLE0 register (Address 0xE601) (see Figure 57). In a similar way, the delays between voltages and currents on Phase B and Phase C are stored in the ANGLE1 register (Address 0xE602) and the ANGLE2 register (Address 0xE603), respectively.

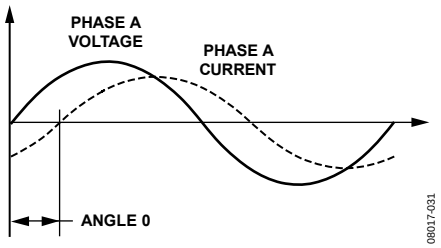


Figure 57. Delay Between Phase A Voltage and Current Is Stored in ANGLE0

When the ANGLESEL bits are set to 01, the delays between phase voltages are measured. The delay between Phase A voltage and Phase C voltage is stored in the ANGLE0 register. The delay between Phase B voltage and Phase C voltage is stored in the ANGLE1 register, and the delay between Phase A voltage and Phase B voltage is stored in the ANGLE2 register (see Figure 58).

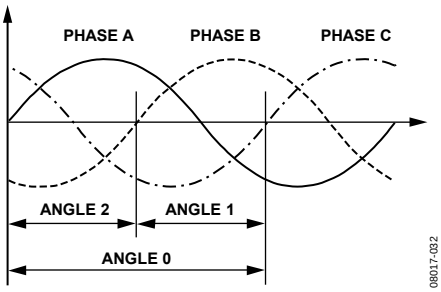


Figure 58. Delays Between Phase Voltages (Currents)

When the ANGLESEL bits are set to 10, the delays between phase currents are measured. Similar to delays between phase voltages, the delay between Phase A current and Phase C current is stored in the ANGLE0 register (Address 0xE601), the delay between Phase B current and Phase C current is stored in the ANGLE1 register (Address 0xE602), and the delay between Phase A current and Phase B current is stored in the ANGLE2 register (Address 0xE603) (see Figure 58).

The ANGLE0, ANGLE1, and ANGLE2 registers are 16-bit, unsigned registers with 1 LSB corresponding to 3.9 μs (256 kHz clock), which means a resolution of 0.07° (360° × 50 Hz/256 kHz) for 50 Hz systems and 0.084° (360° × 60 Hz/256 kHz) for 60 Hz systems. The delays between phase voltages or phase currents are used to characterize how balanced the load is. The delays between phase voltages and currents are used to compute the power factor on each phase (see Equation 3).

$$\cos\varphi_x = \cos\left[ANGLEx \times \frac{360° \times f_{LINE}}{256\ \text{kHz}} \right] \quad (3)$$

where x = 0, 1, or 2; and f_{LINE} is 50 Hz or 60 Hz.

Period Measurement

The ADE7854 provides the period measurement of the line in the voltage channel. Bits[1:0] (PERSEL) in the MMODE register (Address 0x E700) select the phase voltage used for this measurement. The PERIOD register (Address 0xE607) is a 16-bit, unsigned register that is updated every line period. Because of the LPF1 filter (see Figure 53), a settling time of 30 ms to 40 ms is associated with this filter before the measurement is stable.

The period measurement has a resolution of 3.9 μs/LSB (256 kHz clock), which represents 0.0195% (50 Hz/256 kHz) when the line frequency is 50 Hz. The value of the period register for 50 Hz networks is approximately 5,120 (256 kHz/50 Hz). The length of the register enables the measurement of line frequencies as low as 3.9 Hz (256 kHz/2^{16}). The period register is stable at ±1 LSB when the line is established, and the measurement does not change.

The following equations can be used to compute the line period and frequency using the PERIOD register:

$$T_L = \frac{PERIOD}{256E3}[\text{sec}] \quad (4)$$

$$f_L = \frac{256E3}{PERIOD}[\text{Hz}] \quad (5)$$

Phase Voltage Sag Detection

The ADE7854 can be programmed to detect when the absolute value of any phase voltage drops below a certain peak value for a number of half line cycles. The phase where this event took place is identified in Bits[14:12] (VSPHASE) of the PHSTATUS register at Address 0x600 (see Figure 59).

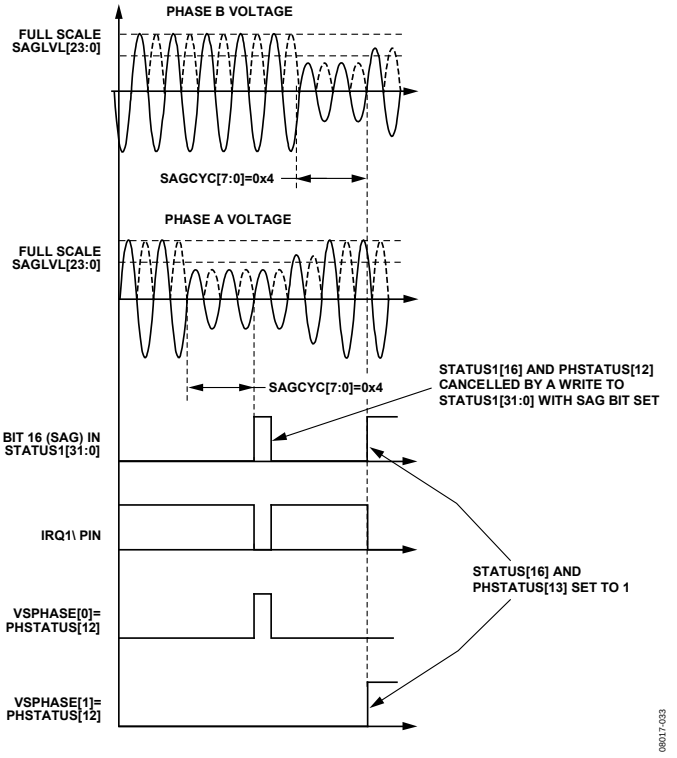


Figure 59. Sag Detection

Figure 59 shows Phase A voltage falling below a threshold that is set in the sag level register (SAGLVL, Address 0xE509) for four half-line cycles (SAGCYC = 4). When Status Bit 16 (SAG) in the STATUS1 register (Address 0xE503) is set to 1 to indicate the condition, Bit 12 (VSPHASE[0]) in the PHSTATUS register is set to 1 because the event happened on Phase A. Bit 16 (SAG) in the STATUS1 register and Bits[14:12] (VSPHASE[2:0], not VSPHASE[0] only) of the PHSTATUS register are erased by writing to the STATUS1 register with the SAG bit set to 1. The SAGCYC register (Address 0xE704) represents the number of half-line cycles the phase voltage must remain below the level indicated in SAGLVL register to trigger a sag condition. Zero is not a valid number for SAGCYC. For example, when the sag cycle (SAGCYC) contains 0x07, the SAG status flag in the STATUS1 register is set at the end of the seventh half-line cycle for which the line voltage falls below the threshold.

If Bit 16 (SAG) in the MASK1 register (Address 0xE50B) is set, the $\overline{\text{IRQ1}}$ interrupt pin is driven low in case of a sag event at the same time that Status Bit 16 (SAG) in the STATUS1 register (Address 0xE503) is set to 1. The SAG status bit in the STATUS1 register and all Bits[14:12] (VSPHASE[2:0]) of the PHSTATUS register (Address 0xE600) are cleared, and the $\overline{\text{IRQ1}}$ pin is set high again by writing to the STATUS1 register with the status bit set to 1.

When the Phase B voltage falls below the threshold indicated in the SAGLVL register (Address 0xE509) for two line cycles, the VSPHASE[1] bit in the PHSTATUS register is set to 1, and the VSPHASE[0] bit is cleared to 0. At the same moment, Status Bit 16 (SAG) in the STATUS1 register is set to 1 to indicate the condition.

Note that the internal zero-crossing counter is always active. By setting the SAGLVL register, the first sag detection result is, therefore, not accomplished across a full SAGCYC period. Writing to the SAGCYC register (Address 0xE704) when the SAGLVL register is already initialized resets the zero-crossing counter, thus ensuring that the first sag detection result is obtained across a full SAGCYC period.

The following procedure is recommended for managing sag events:

1. Enable the SAG interrupts in the MASK1 register by setting Bit 16 (SAG) to 1.
2. The $\overline{\text{IRQ1}}$ interrupt pin goes low when a sag event occurs.
3. The STATUS1 register is read with Bit 16 (SAG) set to 1.
4. The PHSTATUS register is read, identifying the phase or phases on which a sag event has occurred.
5. The STATUS1 register is written with Status Bit 16 (SAG) set to 1. In this moment, the SAG bit is erased, along with all Bits[14:12] (VSPHASE[2:0]) of the PHSTATUS register.

Sag Level Set

The content of the sag level register (SAGLVL) is compared to the absolute value of the output from the HPF. Writing 5,928,256 (0x5A7540) to the SAGLVL register puts the sag detection level at full scale (see the Voltage Channel ADC section), so the sag event is triggered continuously. Writing 0x00 or 0x01 puts the sag detection level at 0, so the sag event is never triggered.

As previously stated, the serial ports of the ADE7854 work on 32-, 16-, or 8-bit words. Similar to the register presented in Figure 46, the SAGLVL register is accessed as 32-bit registers with the eight MSBs padded with 0s.

Peak Detection

The ADE7854 records the maximum absolute values reached by the voltage and current channels over a certain number of half-line cycles and stores them in the 24 LSBs of the 32-bit IPEAK and VPEAK registers (Address 0xE500 and Address 0xE501, respectively). The PEAKCYC register (Address 0xE703) contains the number of half-line cycles used as a time base for the measurement. It uses the zero-crossing points identified by the ZX detection circuit. Bits[4:2] (PEAKSEL) in the MMODE register (Address 0xE700) select the phases on which the peak measurement is complete. Bit 2 selects Phase A, Bit 3 selects Phase B, and Bit 4 selects Phase C. Selecting more than one phase to monitor the peak values decreases proportionally the measurement period indicated in the PEAKCYC register because zero crossings from more phases are involved in the process.

When a new peak value is determined, one of Bits[26:24] (IPPHASE or VPPHASE) in the IPEAK and VPEAK registers, respectively, is set to 1, identifying the phase that triggered the peak detection event. For example, if a peak value has been identified on Phase A current, Bit 24 (IPPHASE[0]) in the IPEAK register is set to 1. If a new peak value is measured on Phase B, Bit 24 (IPPHASE[0]) of the IPEAK register is cleared to 0 and Bit 25 (IPPHASE[1]) of the IPEAK register is set to 1. Figure 60 shows the composition of the IPEAK and VPEAK registers.

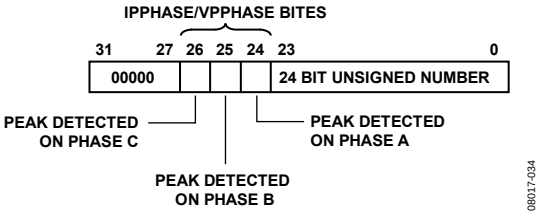


Figure 60. Composition of the IPEAK and VPEAK Registers

Figure 61 shows how the ADE7854 records the peak value on the current channel when measurements on Phase A and Phase B are enabled (the PEAKSEL[2:1] bits in the MMODE register are set to 011). PEAKCYC[7:0] is set to 16, meaning that the peak measurement cycle consists of four line periods. The maximum absolute value of Phase A is greatest during the first four line periods (PEAKCYC = 16). The maximum absolute value is written into the 24 LSBs of the IPEAK register, and Bit 24 (IPPHASE) of the IPEAK register is set to 1 at the end of the period.

The IPPHASE bit remains set to 1 for the duration of the second PEAKCYC period of four line cycles. The maximum absolute value of Phase B is the greatest during the second PEAKCYC period, so the max-imum absolute value is written into the 24 LSBs of the IPEAK register, and Bit 25 (IPPHASE[1]) in the IPEAK register is set to 1 at the end of the period.At the end of the peak detection period in the current channel, Status Bit 23 (PKI) in the STATUS1 register (Address 0xE503) is set to 1.

If Bit 23 (PKI) in the MASK1 register is set, the $\overline{\text{IRQ1}}$ interrupt pin is driven low at the end of the PEAKCYC period, and Status Bit 23 (PKI) in the STATUS1 register is set to 1. Similarly, at the end of the peak detection period in the voltage channel, Status Bit 24 (PKV) in the STATUS1 register is set to 1. If Bit 24 (PKV) in the MASK1 register is set, the $\overline{\text{IRQ1}}$ interrupt pin is driven low at the end of PEAKCYC period and Status Bit 24 (PKV) in the STATUS1 register is set to 1. To find the phase that triggered the interrupt, either the IPEAK register or the VPEAK register is read immediately after reading the STATUS1 register. Then the status bits are cleared, and the $\overline{\text{IRQ1}}$ pin is set high again by writing to the STATUS1 register with the status bit set to 1.

Note that the internal zero-crossing counter is always active. By setting Bits[4:2] (PEAKSEL[2:0]) in the MMODE register, the first peak detection result is, therefore, not accomplished across a full PEAKCYC period. Writing to the PEAKCYC register when the PEAKSEL[2:0] bits are set resets the zero-crossing counter, thus ensuring that the first peak detection result is obtained across a full PEAKCYC period.

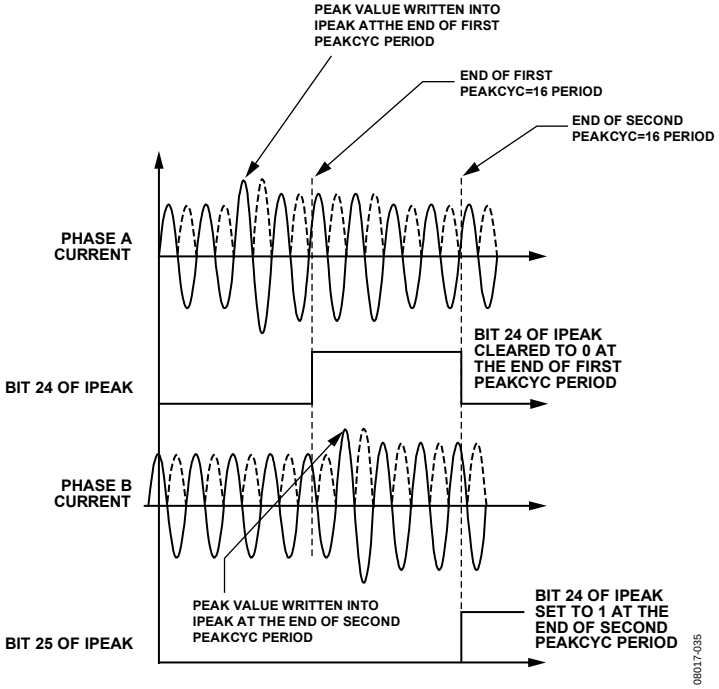


Figure 61. Peak Level Detection

Overvoltage and Overcurrent Detection

The ADE7854 detects when the instantaneous absolute value measured on the voltage and current channels is greater than the thresholds set in the unsigned, 24-bit OVLVL and OILVL regi-sters (Address 0xE508 and Address 0xE507, respectively). If Bit 18 (OV) in the MASK1 register is set, the $\overline{\text{IRQ1}}$ interrupt pin is driven low when an overvoltage event occurs. There are two status flags that are set when the $\overline{\text{IRQ1}}$ interrupt pin is driven low: Status Bit 18 (OV) in the STATUS1 register (Address 0xE503), and one of the following bits: Bit 11, Bit 10, or Bit 9 (OVPHASE[2:0]) in the PHSTATUS register (Address 0xE600), identifying the phase that generated the overvoltage.

Status Bit 18 (OV) in the STATUS1 register and all Bits[11:9] (OVPHASE[2:0]) in the PHSTATUS register are cleared, and the $\overline{\text{IRQ1}}$ pin is set high again by writing to the STATUS1 register with the status bit set to 1. Figure 62 shows overvoltage detection in Phase A voltage. When the absolute instantaneous value of the voltage goes above the threshold from the OVLVL register, Status Bit 18 (OV) in the STATUS1 register and Bit 9 (OVPHASE[0]) in the PHSTATUS register are set to 1. Bit 18 (OV) in the STATUS1 register and Bit 9 (OVPHASE[0]) in the PHSTATUS register are cancelled when the STATUS1 register is written with Status Bit 18 (OV) set to 1.

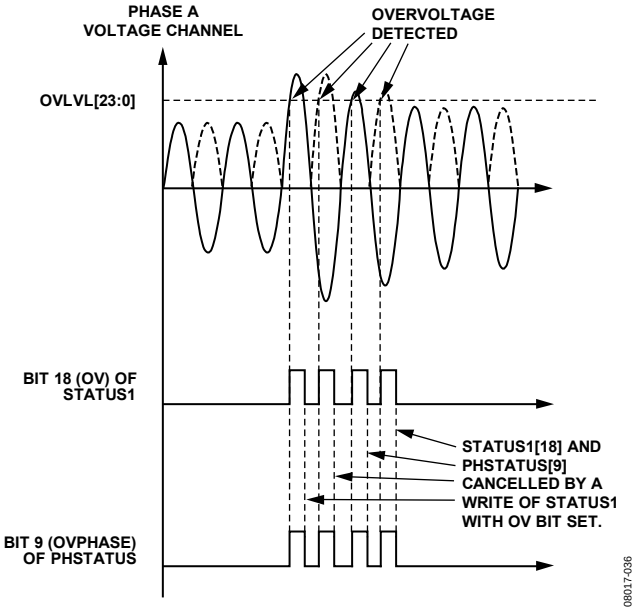


Figure 62. Overvoltage Detection

The following procedure is recommended for managing overvoltage events:

1. Enable the OV interrupts in the MASK1 register by setting Bit 18 (OV) to 1.
2. The $\overline{\text{IRQ1}}$ interrupt pin goes low when an overvoltage event occurs.
3. The STATUS1 register is read with Status Bit 18 (OV) set to 1.
4. The PHSTATUS register is read, identifying the phase or phases on which an overvoltage event has occurred.
5. The STATUS1 register is written with Status Bit 18 (OV) set to 1. At that moment, the OV bit is erased, along with all Bits[11:9] (OVPHASE[2:0]) of the PHSTATUS register.

If Bit 17 (OI) in the MASK1 register is set to 1 when an overcurrent event occurs, the $\overline{\text{IRQ1}}$ interrupt pin is driven low. At the same time, Status Bit 17 (OI) in the STATUS1 register and one of Bits[5:3] (OIPHASE[2:0]) in the PHSTATUS register is set, identifying which phase generated the interrupt. To find the phase that triggered the interrupt, the PHSTATUS register is read immediately after reading the STATUS1 register. Then Status Bit 17 (OI) in the STATUS1 register and Bits[5:3] (OIPHASE[2:0]) in the PHSTATUS register are cleared, and the $\overline{\text{IRQ1}}$ pin is set high again by writing to the STATUS1 register with the status bit set to 1. The process is similar to the overvoltage detection process.

Overvoltage and Overcurrent Level Set

The content of the 24-bit, unsigned overvoltage (OVLVL, Address 0xE508) and overcurrent (OILVL, Address 0xE507) registers is compared to the absolute value of the voltage and current channels. The maximum value of these registers is the maximum value of the HPF outputs: +5,928,256 (0x5A7540). When OVLVL or OILVL are equal to this value, the overvoltage or overcurrent conditions are never detected. Writing 0x0 to these registers signifies the overvoltage or overcurrent conditions are continuously detected, and the corresponding interrupts are triggered permanently.

As previously stated, the serial ports of the ADE7854 work on 32-, 16-, or 8-bit words. Like the register presented in Figure 46, the OILVL and OVLVL registers are accessed as 32-bit registers with the eight MSBs padded with 0s.

PHASE COMPENSATION

As discussed in the Current Channel ADC and Voltage Channel ADC sections, the datapath for both current and voltages is the same. The phase error between the current and voltage signals that is introduced by the ADE7854 is negligible. However, the ADE7854 must work with transducers that may have inherent phase errors. For example, a current transformer (CT) with a phase error of 0.1° to 3° is not uncommon. These phase errors can vary from part to part, and they must be corrected to perform accurate power calculations.

The errors associated with phase mismatch are particularly noticeable at low power factors. The ADE7854 provides a means of digitally calibrating these small phase errors. The ADE7854 allows a small time delay or time advance to be introduced into the signal processing chain to compensate for the small phase errors.

The phase calibration registers (APHCAL, BPHCAL, and CPHCAL) are 10-bit registers that can vary the time advance in the voltage channel signal path from +61.5 µs to −374.0 µs, respectively. Negative values written to the xPHCAL registers represent a time advance, and positive values represent a time delay. One LSB is equivalent to 0.976 µs of time delay or time advance (with a clock rate of 1.024 MHz). With a line frequency of 60 Hz, this gives a phase resolution of 0.0211° (360° × 60 Hz/1.024 MHz) at the fundamental, which corresponds to a total correction range of −8.079° to +1.329° at 60 Hz. At 50 Hz, the correction range is −6.732° to +1.107° and the resolution is 0.0176°(360° × 50 Hz/1.024 MHz).

Given a phase error of x degrees measured while using the phase voltage as the reference, the corresponding LSBs are computed by dividing x by the phase resolution (0.0211°/LSB for 60 Hz and 0.0176°/LSB for 50 Hz). The only acceptable results are between −383 and +63. Numbers outside this range are not accepted. If the result is negative, the absolute value is written into the xPHCAL registers; if the result is positive, 512 is added to it before writing the result into the xPHCAL registers.

$$yPHCAL = \begin{cases} \left| \dfrac{x}{Phase\_Resolution} \right|, x \le 0 \\ \dfrac{x}{Phase\_Resolution} + 512, x > 0 \end{cases} \quad (6)$$

Figure 64 illustrates how the phase compensation is used to remove an $x = -1°$ phase lead in the IAP/IAN inputs of the current channel from the external current transducer (which is an equivalent of 55.5 µs for 50 Hz systems). To cancel the lead (1°) in the current channel of Phase A, a phase lead must be introduced into the corresponding voltage channel. Using Equation 3, APHCAL is 57, rounded up from 56.8. The phase lead is achieved by introducing a time delay of 55.73 µs into the Phase A current.

As previously stated, the serial ports of the ADE7854 work on 32-, 16-, or 8-bit words. As shown in Figure 63, the 10-bit APHCAL, BPHCAL, and CPHCAL registers are accessed as 16-bit registers, with the six MSBs padded with 0s.

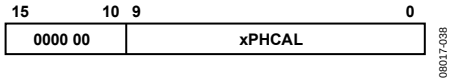


Figure 63. xPHCAL Registers Are Communicated as 16-Bit Registers

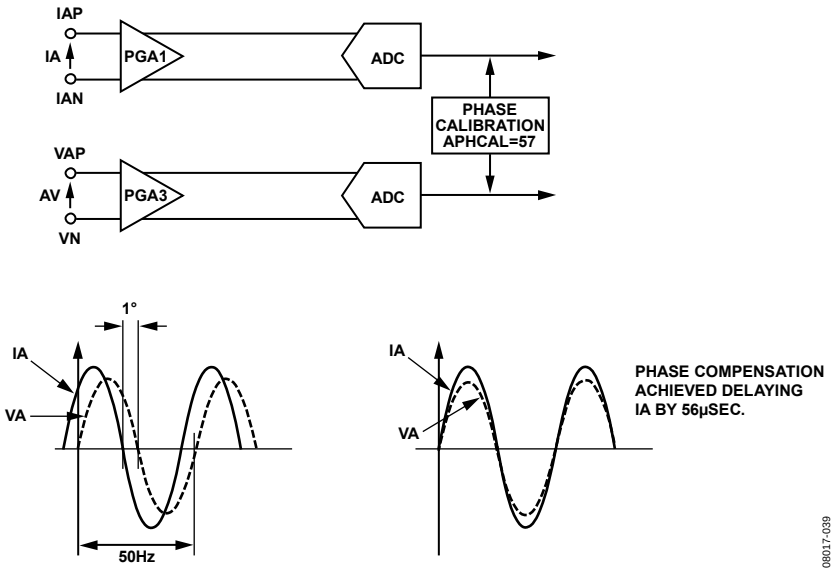


Figure 64. Phase Calibration on Voltage Channels

REFERENCE CIRCUIT

The nominal reference voltage at the $REF_{IN/OUT}$ pin is 1.2±1% V, which is the reference voltage used for the ADCs in the ADE7854. The $REF_{IN/OUT}$ pin can be overdriven by an external source; for example, by an external 1.2 V reference. The voltage of the ADE7854 reference drifts slightly with temperature; see the Specifications section for the temperature coefficient specification (in ppm/°C). The value of the temperature drift varies from part to part. Because the reference is used for all ADCs, any *x*% drift in the reference results in a 2*x* % deviation of the meter accuracy. The reference drift resulting from temperature changes is usually very small and, typically, much smaller than the drift of other components on a meter. Alternatively, the meter can be calibrated at multiple temperatures.

If Bit 0 (EXTREFEN) in the CONFIG2 register (Address 0xEC01) is cleared to 0 (the default value), the ADE7854 uses the internal voltage reference. If the bit is set to 1, the external voltage reference is used. The CONFIG2 register should be set during PSM0 mode. Its value is maintained during the PSM3 power mode.

DIGITAL SIGNAL PROCESSOR (DSP)

The ADE7854 contains a fixed function DSP that computes all power and rms values. It contains various memories: program memory ROM, program memory RAM, and data memory RAM.

The program used for the power and rms computations is stored in the program memory ROM, and the processor executes it every 8 kHz. The end of the computation is signaled by setting Status Bit 17 (DREADY) to 1 in the STATUS0 register (Address 0xE502). An interrupt attached to this flag can be enabled by setting Bit 17 (DREADY) in the MASK0 register (Address 0xE50A). If enabled, the $\overline{IRQ0}$ pin is set low and the DREADY status bit is set to 1 at the end of the computations. The status bit is cleared and the $\overline{IRQ0}$ pin is set back high by writing STATUS0 register with Bit 17 (DREADY) set to 1.

The registers used by the DSP are located in the data memory RAM, at addresses between 0x4000 and 0x43FF. The width of this memory is 28 bits.

As explained in the Power-Up Procedure section, at power-up or after a hardware or software reset, the DSP is in idle mode. No instruction is being executed. All the registers located in the data memory RAM are initialized at 0, their default values. The RUN register (Address 0xE228), which is used to start and stop the DSP, is cleared to 0x0000. The RUN register must be written with 0x0001 for the DSP to start code execution. It is recommended to first initialize all ADE7854 registers located in the data memory RAM with their desired values and then write 0x0001 to the RUN register. In this way, the DSP starts the computation from a desired configuration.

There is no obvious reason to stop the DSP if the ADE7854 is maintained in PSM0 normal mode. All ADE7854 registers, including ones located in the data memory RAM, can be modified without stopping the DSP. However, to stop the DSP, 0x0000 must be written into the RUN register. To restart the DSP, one of the following procedures must be followed:

- If the ADE7854 registers located in the data memory RAM have not been modified, write 0x0001 into the RUN register to start the DSP.
- If the ADE7854 registers located in the data memory RAM must be modified, first execute a software or a hardware reset, initialize all the ADE7854 registers at the desired values, and then write 0x0001 to the RUN register to start the DSP.

As mentioned in the Power Management section, when the ADE7854 switches out of PSM0 power mode into PSM3 sleep mode, it is recommended that the DSP be stopped by writing 0x0000 into the RUN register (see Table 9 for recommended actions when changing power modes).

ROOT MEAN SQUARE (RMS) MEASUREMENT

Root mean square (rms) is a measurement of the magnitude of an ac signal. Its definition can be both practical and mathematical. Defined practically, the rms value assigned to an ac signal is the amount of dc required to produce an equivalent amount of power in the load. Mathematically, the rms value of a continuous signal f(t) is defined as follows:

$$FRMS = \sqrt{\frac{1}{\mathrm{T}}\int_0^{\mathrm{T}} f^2(t)\mathrm{dt}} \tag{7}$$

For time sampling signals, rms calculation involves squaring the signal, taking the average, and obtaining the square root.

$$FRMS = \sqrt{\frac{1}{N}\sum_{n=1}^{N} f^2[n]} \tag{8}$$

Equation 8 implies that, for signals containing harmonics, the rms calculation contains the contribution of all harmonics, not just that of the fundamental. The first method is to low-pass filter the square of the input signal (LPF3) and take the square root of the result (see Figure 65), as follows:

$$f(t) = \sum_{k=1}^{\infty} F_k \sqrt{2}\sin\left(k\omega t + \gamma_k\right) \tag{9}$$

Then,

$$\begin{aligned} f^2(t) &= \sum_{k=1}^{\infty} F_k^2 - \sum_{k=1}^{\infty} F_k^2 \cos(2k\omega t + \gamma_k) + \\ &+ 2\sum_{\substack{k,m=1 \\ k\neq m}}^{\infty} 2 \times F_k \times F_m \sin\left(k\omega t + \gamma_k\right) \times \sin\left(m\omega t + \gamma_m\right) \end{aligned} \tag{10}$$

After the LPF3 and the execution of the square root, the rms value of f(t) is obtained, as follows:

$$F = \sqrt{\sum_{k=1}^{\infty} F_k^2} \tag{11}$$

The rms calculation based on this method is simultaneously processed on all six analog input channels. Each result is available in the following 24-bit registers: AIRMS, BIRMS, and CIRMS (Address 0x43C0, Address 0x43C2, and Address 0x43C4, respectively) and AVRMS, BVRMS, and CVRMS (Address 0x43C1, Address 0x43C3, and Address 0x43C5, respectively).

Current RMS Calculation

This section presents the first approach to compute the rms values of all phase currents.

Figure 65 shows the detail of the signal processing chain for the rms calculation on one of the phases of the current channel. The current channel rms value is processed from the samples used in the current channel. The current rms values are signed 24-bit values, and they are stored in the AIRMS, BIRMS, and CIRMS registers. The update rate of the current rms measurement is 8 kHz.

With the specified full-scale analog input signal of 0.5 V, the ADC produces an output code that is approximately ±5,928,256. The equivalent rms value of a full-scale sinusoidal signal is 4,191,910 (0x3FF6A6), independent of the line frequency. If the integrator is enabled, Bit 0 (INTEN) in the CONFIG register (Address 0xE618) is set to 1, and the equivalent rms value of a full-scale sinusoidal signal at 50 Hz is 4,191,910 (0x3FF6A6), and at 60 Hz it is 3,493,258 (0x354D8A).

The accuracy of the current rms is typically 0.1% error from the full-scale input down to 1/1000 of the full-scale input. Additionally, this measurement has a bandwidth of 2 kHz. It is recommended that the rms registers be read synchronous to the voltage zero crossings to ensure stability. The $\overline{\text{IRQ1}}$ interrupt can be used to indicate when a zero crossing has occurred (see the Interrupts section).

Table 10 shows the settling time for the IRMS measurement, which is the time it takes for the rms register to reflect the value at the input to the current channel.

Table 10. Settling Time for IRMS Measurement

Integrator Status	50 Hz Input Signals	60 Hz Input Signals
Integrator Off	530 ms	530 ms
Integrator On	550 ms	500 ms

As previously stated, the serial ports of the ADE7854 work on 32-, 16-, or 8-bit words. Like the register presented in Figure 46, the 24-bit, signed AIRMS, BIRMS, and CIRMS registers are accessed as 32-bit registers with the eight MSBs padded with 0s.

Current RMS Offset Compensation

The ADE7854 incorporates a current rms offset compensation register for each phase: AIRMSOS, BIRMSOS, and CIRMSOS. These are 24-bit signed registers and are used to remove offsets in the current rms calculations. An offset can exist in the rms calculation due to input noises that are integrated in the dc component of $I^2(t)$. One LSB of the current rms offset compensation register is equivalent to 128 LSBs of the square of the current rms register. Assuming that the maximum value from the current rms calculation is 4,191,400 with full-scale ac inputs (50 Hz), one LSB of the current rms offset represents 0.00036% of the rms measurement at 60 dB down from full scale. Calibration of the offset should be done at low current, and values at zero input should be ignored.

$$IRMS = \sqrt{IRMS_0^2 + IRMSOS \times 128} \quad (12)$$

where $IRMS_0$ is the rms measurement without offset correction.

As previously stated, the serial ports of the ADE7854 work on 32-, 16- or 8-bit words and the DSP works on 28 bits. Like the registers shown in Figure 45, the 24-bit, signed AIRMSOS, BIRMSOS, and CIRMSOS registers are accessed as 32-bit registers with the four MSBs padded with 0s and sign extended to 28 bits.

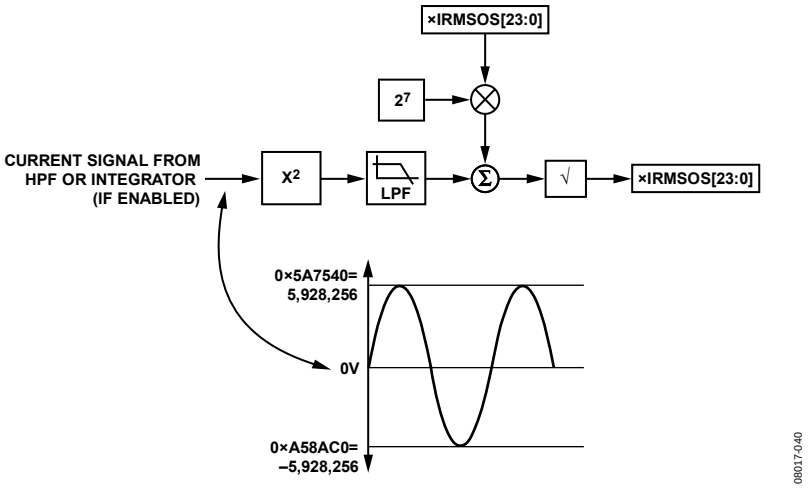


Figure 65. Current RMS Signal Processing

Voltage Channel RMS Calculation

Figure 66 shows the detail of the signal processing chain for the rms calculation on one of the phases of the voltage channel. The voltage channel rms value is processed from the samples used in the voltage channel. The voltage rms values are signed 24-bit values and they are stored in the AVRMS, BVRMS, and CVRMS registers. The update rate of the current rms measurement is 8 kHz.

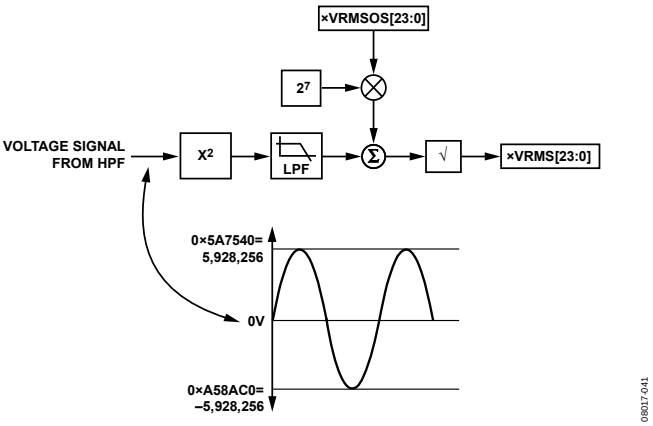


Figure 66. Voltage RMS Signal Processing

With the specified full-scale analog input signal of 0.5 V, the ADC produces an output code that is approximately ±5,928,256. The equivalent rms value of a full-scale sinusoidal signal is 4,191,910 (0x3FF6A6), independent of the line frequency.

The accuracy of the voltage rms is typically 0.1% error from the full-scale input down to 1/1000 of the full-scale input. In addition, this measurement has a bandwidth of 2 kHz. It is recommended that the rms registers be read synchronously with the voltage zero crossings to ensure stability. The $\overline{\text{IRQ1}}$ interrupt can be used to indicate when a zero crossing has occurred (see the Interrupts section).

Table 11 shows the settling time for the VRMS measurement, which is the time it takes for the rms register to reflect the value at the input to the voltage channel.

Table 11. Settling Time for VRMS Measurement

50 Hz Input Signals	60 Hz Input signals
530 ms	530 ms

As previously stated, the serial ports of the ADE7854 work on 32-, 16-, or 8-bit words. Like the register shown in Figure 46, the 24-bit, signed AVRMS, BVRMS, and CVRMS registers are accessed as 32-bit registers with the eight MSBs padded with 0s.

Voltage RMS Offset Compensation

The ADE7854 incorporates a voltage rms offset compensation for each AVRMSOS, BVRMSOS, and CVRMSOS phase. These are 24-bit, signed registers that are used to remove the offsets in the voltage rms calculations. An offset can exist in the rms calculation due to input noises that are integrated in the dc component of $V^2(t)$. One LSB of the voltage rms offset compensation register is equivalent to 128 LSBs of the square of the voltage rms register.

Assuming that the maximum value from the voltage rms calculation is 4,191,400 with full-scale ac inputs (50 Hz), 1 LSB of the current rms offset represents 0.00036% of the rms measurement at 60 dB down from full scale. Calibration of the offset should be accomplished at low current, and values at zero input should be ignored.

$$VRMS = \sqrt{VRMS_0^2 + VRMSOS \times 128} \quad (13)$$

where $VRMS_0$ is the rms measurement without offset correction.

As previously stated, the serial ports of the ADE7854 work on 32-, 16-, or 8-bit words, and the DSP works on 28 bits. Like the registers presented in Figure 45, the 24-bit AVRMSOS, BVRMSOS, and CVRMSOS registers are accessed as 32-bit registers with the four MSBs padded with 0s and sign extended to 28 bits.

ACTIVE POWER CALCULATION

The ADE7854 computes the total active power. Total active power considers in its calculation all fundamental and harmonic components of the voltages and currents.

Total Active Power Calculation

Electrical power is defined as the rate of energy flow from source to load. It is given by the product of the voltage and current waveforms. The resulting waveform is called the instantaneous power signal, and it is equal to the rate of energy flow at every instant of time. The unit of power is the watt or joules/sec. If an ac system is supplied by a voltage, v(t), and consumes the current, i(t), and each of them contains harmonics, then

$$v(t) = \sum_{k=1}^{\infty} V_k \sqrt{2} \sin\left(k\omega t + \varphi_k\right) \quad (14)$$

$$i(t) = \sum_{k=1}^{\infty} I_k \sqrt{2} \sin\left(k\omega t + \gamma_k\right)$$

where:

V_k and I_k are the rms voltage and current of each harmonic.

φ_k and γ_k are the phase delays of each harmonic.

The instantaneous power in an ac system is shown in the following equation (Equation 15):

$$p(t) = v(t) \cdot i(t) = \sum_{k=1}^{\infty} V_k I_k \cos\left(\varphi_k - \gamma_k\right) - \sum_{k=1}^{\infty} V_k I_k \cos\left(2k\omega t + \varphi_k - \gamma_k\right) +$$

$$+ \sum_{\substack{k,m=1 \\ k \neq m}}^{\infty} V_k I_m \left\{\cos\left[(k-m)\omega t + \varphi_k - \gamma_m\right] - \cos\left[(k+m)\omega t + \varphi_k + \gamma_m\right]\right\}$$

The average power over an integral number of line cycles (n) is given by the following equation:

$$P = \frac{1}{nT} \int_0^{nT} p(t)dt = \sum_{k=1}^{\infty} V_k I_k \cos\left(\varphi_k - \gamma_k\right) \quad (16)$$

where:

T is the line cycle period.

P is referred to as the total active or total real power.

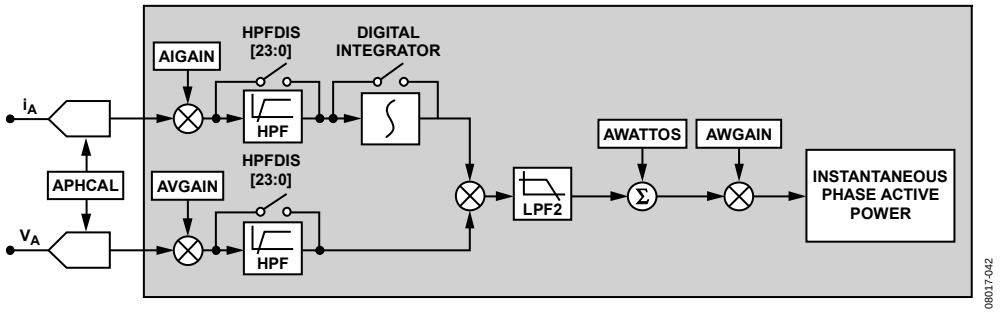


Figure 67. Total Active Power Datapath

Note that the total active power is equal to the dc component of the instantaneous power signal $p(t)$ in Equation 15; that is,

$$\sum_{k=1}^{\infty} V_k I_k \cos(\varphi_k - \gamma_k)$$

This is the expression used to calculate the total active power in the ADE7854 for each phase.

Figure 67 shows how the ADE7854 computes the total active power on each phase. First, it multiplies the current and voltage signals in each phase. Next, it extracts the dc component of the instantaneous power signal in each phase (Phase A, Phase B, and Phase C), using LPF2, the low-pass filter.

If the phase currents and voltages contain only the fundamental component, are in phase (that is, $\varphi_1 = \gamma_1 = 0$), and correspond to full-scale ADC inputs, multiplying them results in an instantaneous power signal that has a dc component, $V_1 \times I_1$, and a sinusoidal component, $V_1 \times I_1 \cos(2\omega t)$. Figure 68 shows the corresponding waveforms.

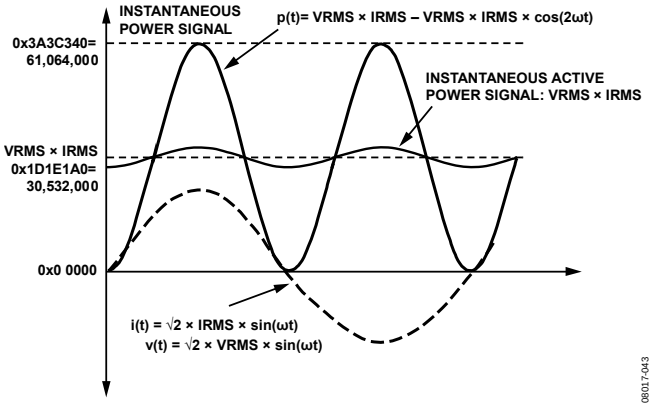


Figure 68. Active Power Calculation

Because LPF2 does not have an ideal brick wall frequency response (see Figure 69), the active power signal has some ripple due to the instantaneous power signal. This ripple is sinusoidal and has a frequency equal to twice the line frequency. Because the ripple is sinusoidal in nature, it is removed when the active power signal is integrated over time to calculate the energy.

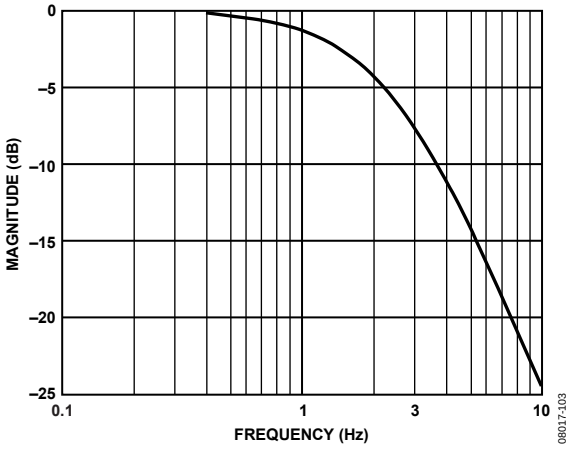


Figure 69. Frequency Response of the LPF Used to Filter Instantaneous Power in Each Phase

The ADE7854 stores the instantaneous total phase active powers in the AWATT, BWATT, and CWATT registers (Address 0xE513, Address 0xE514, and Address 0xE515, respectively).

They are expressed as follows:

$$xWATT = \sum_{k=1}^{\infty} \frac{U_k}{U_{FS}} \times \frac{I_k}{I_{FS}} \times \cos(\varphi_k - \gamma_k) \times PMAX \times \frac{1}{2^4} \quad (17)$$

where:
x stands for A, B, and C.
U_{FS} and I_{FS} are the rms values of the phase voltage and current when the ADC inputs are at full scale.
$PMAX$ = 33,516,139, which is the instantaneous power computed when the ADC inputs are at full scale and in phase.

The xWATT waveform registers can be accessed using various serial ports (see the Waveform Sampling Mode section).

Active Power Gain Calibration

Note that the average active power result from the LPF2 output in each phase can be scaled by ±100% by writing to the phase's watt gain 24-bit register, AWGAIN, BWGAIN, and CWGAIN (Address 0x4391, Address 0x4393, and Address 0x4395, respectively). The xWGAIN registers are placed in each phase of the total active power datapath. The watt gain registers are twos complement, signed registers and have a resolution of 2^{-23}/LSB. Equation 18 describes mathematically the function of the watt gain registers.

$$Average\ Power\ Data = LPF2\ Output \times \left(1 + \frac{Watt\ Gain\ Register}{2^{23}}\right) \quad (18)$$

The output is scaled by −50% by writing 0xC00000 to the watt gain registers and increased by +50% by writing 0x400000 to them. These registers can be used to calibrate the active power (or energy) calculation in the ADE7854 for each phase.

As previously stated, the serial ports of the ADE7854 work on 32, 16-, or 8-bit words, and the DSP works on 28 bits. Like the registers shown in Figure 45, the 24-bit, signed AWGAIN, BWGAIN, and CWGAIN registers are accessed as 32-bit registers, with the four MSBs padded with 0s and sign extended to 28 bits.

Active Power Offset Calibration

The ADE7854 also incorporates a watt offset 24-bit register on each phase and on each active power. The AWATTOS, BWATTOS, and CWATTOS registers (Address 0x4392, Address 0x4394, and Address 0x4396, respectively) compensate the offsets in the total active power calculations. These are signed, twos complement, 24-bit registers that are used to remove offsets in the active power calculations. An offset can exist in the power calculation due to crosstalk between channels on the PCB or in the chip itself. The offset calibration allows the contents of the active power register to be maintained at 0 when no power is being consumed. One LSB in the active power offset register is equivalent to 1 LSB in the active power multiplier output. With full-scale current and voltage inputs, the LPF2 output is PMAX = 33,516,139. At −80 dB from full scale (active power scaled down 10^4 times), 1 LSB of the active power offset register represents 0.032% of PMAX.

As previously stated, the serial ports of the ADE7854 work on 32-, 16-, or 8-bit words and the DSP works on 28 bits. Like the registers shown in Figure 45, the 24-bit, signed AWATTOS, BWATTOS, and CWATTOS registers are accessed as 32-bit registers with the four MSBs padded with 0s and sign extended to 28 bits.

Sign of Active Power Calculation

Note that the average active power is a signed calculation. If the phase difference between the current and voltage waveform is more than 90°, the average power becomes negative. Negative power indicates that energy is being injected back on the grid. The ADE7854 has a sign detection circuitry for total active power calculations. As shown in the Active Energy Calculation section, the active energy accumulation is performed in two stages. Every time a sign change is detected in the energy accumulation at the end of the first stage, that is, after the energy accumulated into the internal accumulator reaches the threshold of the WTHR1 and WTHR0 registers (Address 0x43AB and Address 0x43AC, respectively), a dedicated interrupt is triggered. The sign of each phase active power can be read in the PHSIGN register (Address 0xE617).

Bits[8:6] (REVAPC, REVAPB and REVAPA, respectively) in the STATUS0 register are set when a sign change occurs in the total active power.

Bits[2:0] (CWSIGN, BWSIGN, and AWSIGN, respectively) in the PHSIGN register are set simultaneously with the REVAPC, REVAPB, and REVAPA bits. They indicate the sign of the power. When they are 0, the total active power is positive. When they are 1, the total active power is negative.

Interrupts attached to Status Bits[8:6] (REVAPC, REVAPB, and REVAPA, respectively) in the STATUS0 register (Address 0xE502) can be enabled by setting Bit 8 (REVAPC), Bit 7 (REVAPB), and Bit 6 (REVAPA) in the MASK0 register (Address 0xE50A). If enabled, the $\overline{\text{IRQ0}}$ pin is set low and the status bit is set to 1 when a change of sign occurs. To find the phase that triggered the interrupt, the PHSIGN register is read immediately after reading the STATUS0 register. Then the status bit is cleared, and the $\overline{\text{IRQ0}}$ pin is set high again by writing to the STATUS0 register with the corresponding bit set to 1.

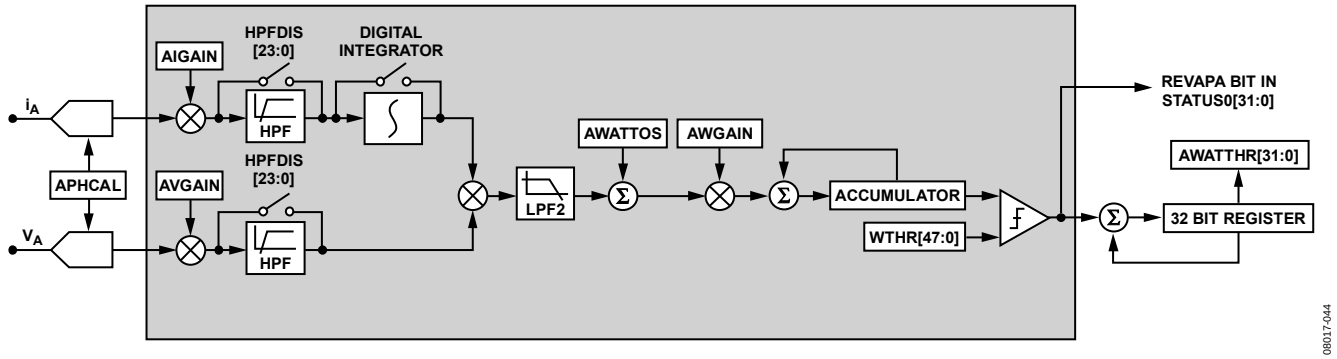


Figure 70. Total Active Energy Accumulation

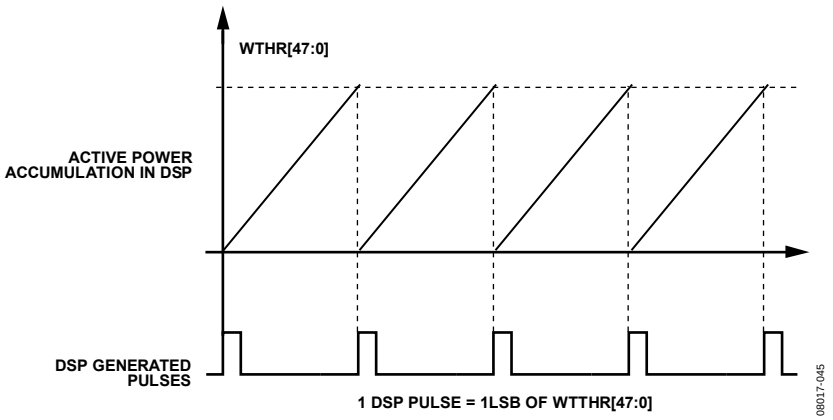


Figure 71. Active Power Accumulation Inside DSP

ACTIVE ENERGY CALCULATION

As previously stated, power is defined as the rate of energy flow. This relationship can be expressed mathematically as

$$Power = \frac{\mathrm{d}Energy}{dt} \quad (19)$$

Conversely, *Energy* is given as the integral of power.

$$Energy = \int p(t)dt \quad (20)$$

Total active energy accumulation is signed. Negative energy is subtracted from the active energy contents.

The ADE7854 achieves the integration of the active power signal in two stages (see Figure 70). The process is identical for both total and fundamental active powers. The first stage is performed inside the DSP: every 125 µs (at 8 kHz frequency), the instantaneous phase total or fundamental active power is accumulated into an internal register. When a threshold is reached, a pulse is generated at the processor port and the threshold is subtracted from the internal register. The sign of the energy at this time is considered the sign of the active power (see the Sign of Active Power Calculation section for details). The second stage is per-formed outside the DSP and consists of accumulating the pulses generated by the processor into internal 32-bit accumulation registers. The content of these registers is transferred to the watt-hr registers, AWATTHR, BWATTHR, and CWATTHR (Address 0xE400, Address 0xE401, and Address 0xE402, respectively) when these registers are accessed.

The AWATTHR, BWATTHR, and CWATTHR registers represent the phase total active powers. Figure 71 explains this process. The 48-bit, signed WTHR register (which comprises the WTHR1 and WTHR0 registers at Address 0x43AB and Address 0x43AC, respectively) contains the threshold. It is introduced by the user and is common for both total and fundamental phase active powers. Its value depends on how much energy is assigned to 1 LSB of watt-hour registers. Assume that a derivative of wh [10^n wh], where n is an integer, is desired as 1 LSB of WATTHR.

Then WTHR is computed, using the following expression:

$$WTHR = \frac{PMAX \times f_s \times 3600 \times 10^n}{U_{FS} \times I_{FS}} \quad (21)$$

where:

$PMAX$ = 33,516,139 = 0x1FF6A6B, which is the instantaneous power computed when the ADC inputs are at full scale.

f_s = 8 kHz, which is the frequency used by the DSP to compute the instantaneous power.

U_{FS} and I_{FS} are the rms values of the phase voltages and currents when the ADC inputs are at full scale.

The maximum value that can be written to WTHRx is $2^{47} - 1$. The minimum value is 0x0, but it is recommended that a value of ≥PMAX be written. Negative numbers should never be used.

WTHR1 and WRHR0 together form 48-bits. As previously stated, the serial ports of the ADE7854 work on 32-, 16-, or 8-bit words. As shown in Figure 72, the WTHRx registers are accessed as two 32-bit registers (WTHR1 and WTHR0), each having eight MSBs padded with 0s.

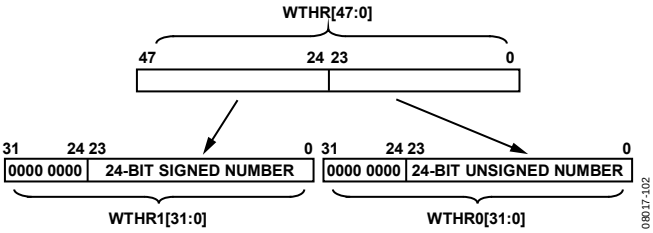


Figure 72. WTHR Register Is Communicated As Two 32-Bit Registers

This discrete time accumulation or summation is equivalent to integration in continuous time, as shown in the following equation:

$$Energy = \int p(t)dt = \lim_{T \to 0} \left\{ \sum_{n=0}^{\infty} p(nT) \times T \right\} \quad (22)$$

where:
n is the discrete time sample number.
T is the sample period.

In the ADE7854, the total phase active powers are accumulated in the 32-bit, signed AWATTHR, BWATTHR and CWATTHR registers (Address 0xE400, Address 0xE401, and Address 0xE402, respectively). The active energy register content can roll over to full-scale negative (0x80000000) and continue increasing in value when the active power is positive. Conversely, if the active power is negative, the energy register underflows to full-scale positive (0x7FFFFFFF) and continues decreasing in value.

Bit 0 (AEHF) in the STATUS0 register (Address 0xE502) is set when Bit 30 of one of the xWATTHR registers changes, signifying that one of these registers is half full. If the active power is positive, the watt-hr register becomes half full when it increments from 0x3FFF FFFF to 0x4000 0000. If the active power is negative, the watt-hr register becomes half full when it decrements from 0xC000 0000 to 0xBFFF FFFF.

Setting Bit 0 in the MASK0 register (Address 0xE50A) enables the AEHF interrupts. If enabled, the $\overline{\text{IRQ0}}$ pin is set low and the status bit is set to 1 when one of the xWATTHR energy registers (for the AEHF interrupt) becomes half full. The status bit is cleared, and the $\overline{\text{IRQ0}}$ pin is set to logic high by writing to the STATUS0 register with the corresponding bit set to 1.

Setting Bit 6 (RSTREAD) in the LCYCMODE register (Address 0xE) enables a read-with-reset for all watt-hr accumulation registers, that is, the registers are reset to 0 following a read operation.

Integration Time Under Steady Load

The discrete time sample period (T) for the accumulation register is 125 µs (1/8 kHz). With full-scale sinusoidal signals on the analog inputs and the watt gain registers set to 0x00000, the average word value from each LPF is PMAX = 33,516,139 = 0x1FF6A6B. If the WTHR[47:0] threshold is set at PMAX level, the DSP generates a pulse that is added at watt-hr registers every 125 µs.

The maximum value that can be stored in the watt-hr accumulation register before it overflows is $2^{31} - 1$ or 0x7FFFFFFF. The integration time is calculated as

$$Time = 0x7FFF,FFFF \times 125\ \mu s = 74\ h, 33\ min, 552\ sec \quad (23)$$

Energy Accumulation Modes

The active power accumulated in each 32-bit watt-hr accumulation register (AWATTHR, BWATTHR and CWATTHR) depends on the configuration of Bits[5:4] (CONSEL) in the ACCMODE register (Address 0xE701). The different configurations are listed in Table 12.

Table 12. Inputs to Watt-Hr Accumulation Registers

CONSEL	AWATTHR	BWATTHR	CWATTHR
00	VA × IA	VB × IB	VC × IC
01	VA × IA	0	VC × IC
10	VA × IA	VB × IB VB = –VA – VC	VC × IC
11	VA × IA	VB × IB VB = –VA	VC × IC

Depending on the polyphase meter service, the appropriate formula should be chosen to calculate the active energy. The American ANSI C12.10 standard defines the different configurations of the meter. Table 13 lists which mode should be chosen in each configuration.

Table 13. Meter Form Configuration

ANSI Meter Form		CONSEL
5S/13S	3-wire delta	01
6S/14S	4-wire wye	10
8S/15S	4-wire delta	11
9S/16S	4-wire wye	00

Bits[1:0] (WATTACC) in the ACCMODE register determine how the CF frequency output can be generated as a function of the total and fundamental active powers. While the watt-hr accumulation registers accumulate the active power in a signed format, the frequency output can be generated in signed mode or in absolute mode, a function of the WATTACC bits. See the Energy-to-Frequency Conversion section for details.

Line Cycle Active Energy Accumulation Mode

In line cycle energy accumulation mode, the energy accumulation is synchronized to the voltage channel zero crossings so that active energy is accumulated over an integral number of half line cycles. The advantage of summing the active energy over an integer number of line cycles is that the sinusoidal component in the active energy is reduced to 0. This eliminates any ripple in the energy calculation and allows the energy to be accumulated accurately over a shorter time. By using the line cycle energy accumulation mode, the energy calibration can be greatly simplified, and the time required to calibrate the meter can be significantly reduced. In line cycle energy accumulation mode, the ADE7854 transfers the active energy accumulated in the 32-bit internal accumulation registers into the xWATTHR registers (Address 0xE400, Address 0xE401, and Address 0xE402) after an integral number of line cycles, as shown in Figure 73. The number of half-line cycles is specified in the LINECYC register (Address 0xE60C).

The line-cycle energy accumulation mode is activated by setting Bit 0 (LWATT) in the LCYCMODE register (Address 0xE702). The energy accumulation over an integer number of half-line cycles is written to the watt-hr accumulation registers after the LINECYC number of half-line cycles is detected. When using the line-cycle accumulation mode, Bit 6 (RSTREAD) of the LCYCMODE register should be set to Logic 0 because the read-with-reset of the watt-hr registers is not available in this mode.

Phase A, Phase B, and Phase C zero crossings are included when counting the number of half-line cycles by setting the ZXSEL bits (Bit 5, Bit 4, and Bit 3, respectively) in the LCYCMODE register. Any combination of the zero crossings from all three phases can be used for counting the zero crossing. Only one phase should be selected at a time for inclusion in the zero-crossing count during line accumulation.

The number of zero crossings is specified by the 16-bit, unsigned LINECYC register. The ADE7854 can accumulate active power for up to 65,535 combined zero crossings. Note that the internal zero-crossing counter is always active. By setting Bit 0 (LWATT) in the LCYCMODE register, the first energy accumulation result is, therefore, incorrect. Writing to the LINECYC register when the LWATT bit is set resets the zero-crossing counter, thus ensuring that the first energy accumulation result is accurate.

At the end of an energy calibration cycle, Status Bit 5 (LENERGY) in the STATUS0 register (Address 0xE502) is set. If the corresponding bit in the MASK0 interrupt mask register (Address 0xE50A) is enabled, the $\overline{\text{IRQ0}}$ pin also goes active low. The status bit is cleared, and the $\overline{\text{IRQ0}}$ pin is set high by writing to the STATUS0 register with the corresponding bit set to 1.

Because the active power is integrated on an integer number of half-line cycles in this mode, the sinusoidal components are reduced to 0, eliminating any ripple in the energy calculation. Therefore, the total energy accumulated using the line-cycle accumulation mode is

$$e = \int_{t}^{t+nT} p(t)dt = nT\sum_{k=1}^{\infty} V_k I_k \cos(\varphi_k - \gamma_k) \quad (24)$$

where nT is the accumulation time.

Note that the line cycle active energy accumulation uses the same signal path as the active energy accumulation. The LSB size of these two methods is equivalent.

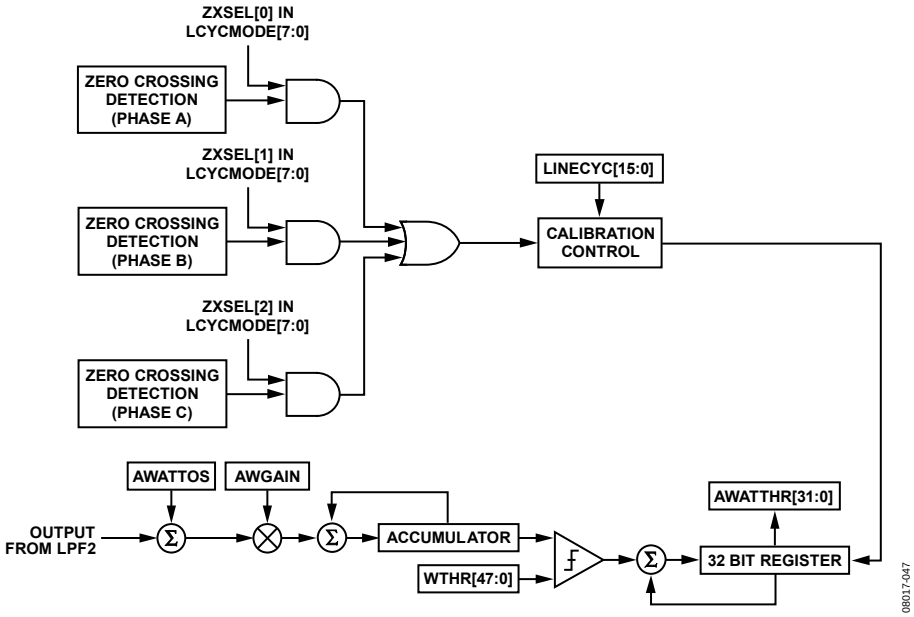


Figure 73. Line-Cycle Active Energy Accumulation Mode

APPARENT POWER CALCULATION

Apparent power is defined as the maximum power that can be delivered to a load. One way to obtain the apparent power is by multiplying the voltage rms value by the current rms value:

$$S = VRMS \times IRMS \quad (25)$$

where *S* is the apparent power and *VRMS* and *IRMS* are the rms voltage and current, respectively. It is also called the arithmetic apparent power.

The ADE7854 computes the arithmetic apparent power on each phase. Figure 74 shows the signal processing in each phase for the calculation of the apparent power in the ADE7854. Because VRMS and IRMS contain all harmonic information, the apparent power computed by the ADE7854 is a total apparent power.

The ADE7854 stores the instantaneous phase apparent powers into the AVA (Address 0xE51), BVA (Address 0xE51A), and CVA (Address 0xE51B) registers. Their expression follows:

$$xVA = \frac{U}{U_{FS}} \times \frac{I}{I_{FS}} \times PMAX \times \frac{1}{2^4} \quad (26)$$

where:
x is A, B, or C.
U and *I* are the rms values of the phase voltage and current.
U_{FS} and I_{FS} are the rms values of the phase voltage and current when the ADC inputs are at full scale.
PMAX = 33,516,139, which is the instantaneous power that is computed when the ADC inputs are at full scale and in phase.

The xVA waveform registers can be accessed using various serial ports. See the Waveform Sampling Mode section for more details.

The ADE7854 can compute the apparent power in an alternative way by multiplying the phase rms current by an rms voltage that is introduced externally. Refer to the Apparent Power Calculation Using VNOM section for details.

Apparent Power Gain Calibration

The average apparent power result in each phase can be scaled by ±100% by writing to the phase's 24-bit VAGAIN register (AVAGAIN, Address 0x438E; BVAGAIN, Address 0x438F; or CVAGAIN, Address 0x438F). The VAGAIN registers are twos complement, signed registers and have a resolution of 2^{-23}/LSB. The function of the VA gain registers is expressed mathematically as follows:

$$Average\ Apparent\ Power = VRMS \times IRMS \times \left(1 + \frac{VAGAIN\ Register}{2^{23}}\right) \quad (27)$$

The output is scaled by −50% by writing 0xC00000 to the VA gain registers and increased by +50% by writing 0x400000 to them. These registers can be used to calibrate the apparent power (or energy) calculation in the ADE7854 for each phase.

As previously stated, the serial ports of the ADE7854 work on 32-, 16-, or 8-bit words and the DSP works on 28 bits. Like the registers shown in Figure 45, the 24-bit AVAGAIN, BVAGAIN, and CVAGAIN registers are accessed as 32-bit registers, with the four MSBs padded with 0s and sign extended to 28 bits.

Apparent Power Offset Calibration

Each rms measurement includes an offset compensation register to calibrate and eliminate the dc component in the rms value (see the Root Mean Square (RMS) Measurement section). The voltage and current rms values are then multiplied together in the apparent power signal processing. Because no additional offsets are created in the multiplication of the rms values, there is no specific offset compensation in the apparent power signal processsing. The offset compensation of the apparent power measurement in each phase should be done by calibrating each individual rms measurement.

Apparent Power Calculation Using VNOM

The ADE7854 can compute the apparent power by multiplying the phase rms current by an rms voltage introduced externally in the 24-bit, unsigned VNOM register (Address 0xE520). When one of Bits[13:11] (VNOMCEN, VNOMBEN, or VNOMAEN) in the COMPMODE register (Address 0xE60E) is set to 1, the apparent power in the corresponding phase (Phase x for VNOMxEN) is computed in this way. When the VNOMxEN bits are cleared to 0, which is the default value, the arithmetic apparent power is computed.

The VNOM register contains a number determined by U, the desired rms voltage; and U_{FS}, the rms value of the phase voltage when the ADC inputs are at full scale; as follows:

$$VNOM = \frac{U}{U_{FS}} \times 4{,}191{,}400 \quad (28)$$

where U is usually the nominal phase rms voltage.

As previously stated, the serial ports of the ADE7854 work on 32-, 16-, or 8-bit words. Like the the register shown in Figure 46, the 24-bit VNOM register is accessed as a 32-bit register with the eight MSBs padded with 0s.

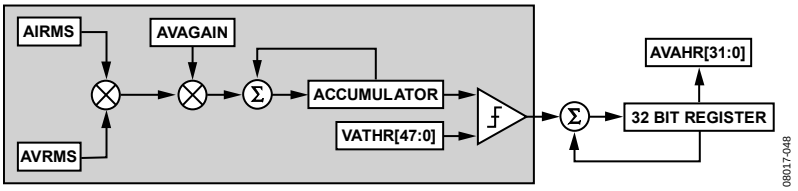


Figure 74. Apparent Power Data flow and Apparent Energy Accumulation

Apparent Energy Calculation

Apparent energy is defined as the integral of apparent power.

$$Apparent\ Energy = \int s(t)dt \quad (29)$$

Similar to active and reactive powers, the ADE7854 achieves the integration of the apparent power signal in two stages (see Figure 74). The first stage is done inside the DSP: every 125 µs (8 kHz frequency), the instantaneous phase apparent power is accumulated into an internal register. When a threshold is reached, a pulse is generated at the processor port and the threshold is subtracted from the internal register. The second stage is done outside the DSP and consists of accumulating the pulses generated by the processor into internal 32-bit accumulation registers. The content of these registers is transferred to va-hr registers xVAHR[31:0] when these registers are accessed.

This process is similar to the one shown in Figure 71 in the Active Energy Calculation section. The 48-bit VATHR (which comprises the VATHR1 and VATHR0 registers at Address 0x43A9 and Address 0x 43AA, respectively) contains the threshold. Its value depends on how much energy is assigned to 1LSB of VA-hour registers. Assume that a derivative of VAh [10^n VAh], where n is an integer, is desired as 1 LSB of VAHR.

Then VATHR can be computed using the following equation:

$$VATHR = \frac{PMAX \times f_s \times 3600 \times 10^n}{U_{FS} \times I_{FS}} \quad (30)$$

where:
$PMAX$ = 33,516,139 = 0x1FF6A6B, which is the instantaneous power computed when the ADC inputs are at full scale.
f_S = 8 kHz, the frequency with which the DSP computes the instantaneous power.
U_{FS} and I_{FS} are the rms values of phase voltages and currents when the ADC inputs are at full scale.

VATHR is a 48-bit combination of the VATHR1 and VATHR0 registers. As previously stated, the serial ports of the ADE7854 work on 32-, 16-, or 8-bit words. Like WTHR[47:0] shown in Figure 72, VATHR is accessed as two 32-bit registers (VATHR1 and VATHR0), each having the eight MSBs padded with 0s.

This discrete time accumulation or summation is equivalent to integration in continuous time, as shown in the following equation:

$$Apparent\ Energy = \int s(t)dt = \lim_{T \to 0} \left\{ \sum_{n=0}^{\infty} s(nT) \times T \right\} \quad (31)$$

where:
n is the discrete time sample number.
T is the sample period.

The phase apparent powers are accumulated in the 32-bit, signed AVAHR (Address 0xE40C), BVAHR (Address 0xE40C), and CVAHR (Address 0xE40D) registers. The apparent energy register content can roll over to full-scale negative (0x80000000) and continue increasing in value when the apparent power is positive. Conversely, if because of offset compensation in rms datapath, the apparent power is negative, the energy register underflows to full-scale positive (0x7FFFFFFF) and continues decreasing in value.

Status Bit 4 (VAEHF) in the STATUS0 register (Address 0xE502) is set when Bit 30 of one of the xVAHR registers changes, signifying that one of these registers is half full. Because the apparent power is always positive and the xVAHR registers are signed, the VA-hr registers become half full when they increment from 0x3FFFFFFF to 0x4000 0000. Interrupts attached to the VAEHF bit in the STATUS0 register can be enabled by setting Bit 4 in the MASK0 register (Address 0xE50A). If enabled, the $\overline{\text{IRQ0}}$ pin is set low and the status bit is set to 1 when one of the xVAHR energy registers becomes half full. The status bit is cleared, and the $\overline{\text{IRQ0}}$ pin is set high again by writing to the STATUS0 register with the corresponding bit set to 1.

Setting Bit 6 (RSTREAD) in the LCYCMODE register (Address 0xE702) enables a read-with-reset for all va-hr accumulation registers; that is, the registers are reset to 0 after a read operation.

Integration Time Under Steady Load

The discrete time sample period (T) for the accumulation register is 125 µs (1/8 kHz). With full-scale pure sinusoidal signals on the analog inputs, the average word value representing the apparent power is PMAX. If the VATHR[47:0] threshold is set at PMAX level, this means that the DSP generates a pulse that is added at the VA-hr registers every 125 µs.

The maximum value that can be stored in the va-hr accumulation register before it overflows is $2^{31} - 1$ or 0x7FFFFFFF. The integration time is calculated as follows:

$$Time = 0x7FFF,FFFF \times 125\ \mu s = 74\ h,\ 33\ min,\ 55\ sec \quad (32)$$

Energy Accumulation Mode

The apparent power accumulated in each VA-hr accumulation register (AVAHR, BVAHR, or CVAHR) depends on the configuration of Bits[5:4] (CONSEL) in the ACCMODE register (Address 0xE701). The different configurations are described in Table 14.

Table 14. Inputs to VA-Hr Accumulation Registers

CONSEL	AVAHR	BVAHR	CVAHR
00	AVRMS × AIRMS	BVRMS × BIRMS	CVRMS × CIRMS
01	AVRMS × AIRMS	0	CVRMS × CIRMS
10	AVRMS × AIRMS	BVRMS × BIRMS VB = –VA – VC	CVRMS × CIRMS
11	AVRMS × AIRMS	BVRMS × BIRMS VB = –VA	CVRMS × CIRMS

Line Cycle Apparent Energy Accumulation Mode

In line cycle energy accumulation mode, the energy accumulation can be synchronized to the voltage channel zero crossings so that the apparent energy can be accumulated over an integral number of half line cycles (see the Line Cycle Active Energy Accumulation Mode section for more information). In this mode, the ADE7854 transfers the apparent energy accumulated in the 32-bit internal accumulation registers into the xVAHR registers (Address 0xE40C, Address 0xE40D, and Address 0xE40E) after an integral number of line cycles, as shown in Figure 75. The number of half-line cycles is specified in the LINECYC register (Address 0xE60C).

The line cycle apparent energy accumulation mode is activated by setting Bit 2 (LVA) in the LCYCMODE register (Address 0xE702). The apparent energy accumulated over an integer number of zero crossings is written to the VA-hr accumulation registers after the LINECYC number of zero crossings is detected. When using the line cycle accumulation mode, Bit 6 (RSTREAD) of the LCYCMODE register should be set to Logic 0 because the read with reset of VA-hr registers is not available in this mode.

The Phase A, Phase B, and Phase C zero crossings are included when counting the number of half-line cycles by setting Bits[5:3] (ZXSEL[2:0]) in the LCYCMODE register. Any combination of the zero crossings from all three phases can be used for counting the zero crossing. Only one phase should be selected at a time for inclusion in the zero crossings count during calibration.

For details about setting the LINECYC register and the LENERGY interrupt associated with the line cycle accumulation mode, see the Line Cycle Active Energy Accumulation Mode section.

WAVEFORM SAMPLING MODE

The waveform samples of the current and voltage waveforms and the active and apparent power multiplier outputs are stored every 125 µs (at a rate of 8 kHz) into 24-bit signed registers that can be accessed through various serial ports of the ADE7854. Table 15 presents the list of the registers and their description.

Table 15. Waveform registers list

Register	Description	Register	Description
IAWV	Phase A current	AWATT	Phase A active power
IBWV	Phase B current	BWATT	Phase B active power
ICWV	Phase C current	CWATT	Phase C active power
VAWV	Phase A voltage	AVA	Phase A apparent power
VBWV	Phase B voltage	BVA	Phase B apparent power
VCWV	Phase C voltage	CVA	Phase C apparent power

Status Bit 17 (DREADY) in the STATUS0 register (Address 0xE502) can be used to signal when the registers listed in Table 15 can be read using the I²C or SPI serial ports. An interrupt attached to the flag can be enabled by setting Bit 17 (DREADY) in the MASK0 register (Address 0xE50A). Refer to the Digital Signal Processor (DSP) section for more information about the DREADY bit).

The ADE7854 contains an HSDC port that is specifically designed to provide fast access to the waveform sample registers. See the High Speed Data Capture Interface (HSDC) section for more information.

As previously stated, the serial ports of the ADE7854 work on 32-, 16-, or 8-bit words. All registers listed in Table 15 are transmitted, signed, and extended from 24 to 32 bits (see Figure 47).

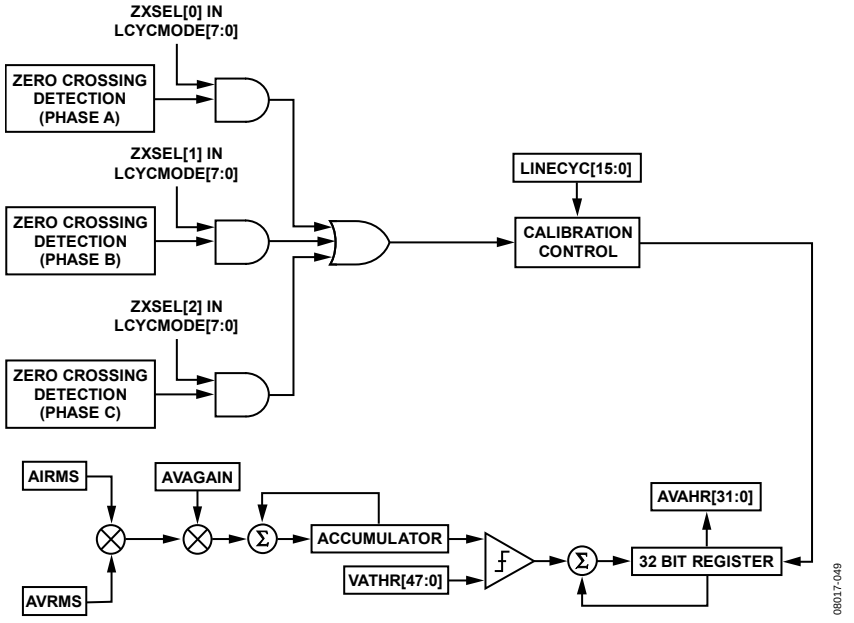


Figure 75. Line Cycle Apparent Energy Accumulation Mode

ENERGY-TO-FREQUENCY CONVERSION

The ADE7854 has three frequency output pins: CF1, CF2, and CF3.

The CF3 pin is multiplexed with the HSCLK pin of the HSDC interface. When HSDC is enabled, the CF3 functionality is disabled at the pin. CF1 and CF2 pins are always available. After initial calibration at manufacturing, the manufacturer or end customer verifies the energy meter calibration. One convenient way to verify the meter calibration is to provide an output frequency proportional to the active, reactive, or apparent powers under steady load conditions. This output frequency can provide a simple single-wire, optically isolated interface to external calibration equipment. Figure 76 shows the energy-to-frequency conversion in the ADE7854.

The DSP computes the instantaneous values of all phase powers: total active, fundamental active, total reactive, fundamental reactive, and apparent. The process in which the energy is sign accumulated in the various hr registers (watt-hr, var-hr and VA-hr) is described in the Active Energy Calculation sections. In the energy-to-frequency conversion process, the instantaneous powers are used to generate signals at the CF1, CF2, and CF3 frequency output pins.

One digital-to-frequency converter is used for every CFx pin. Every converter sums certain phase powers and generates a signal proportional to the sum. Two sets of bits decide which powers are converted.

First, Bits[2:0] (TERMSEL1[2:0]), Bits[5:3] (TERMSEL2[2:0]) and Bits[8:6] (TERMSEL3[2:0]) of the COMPMODE register (Address 0xE60E) determine which phases or which combination of phases are to be added. The TERMSEL1 bits relate to the CF1 pin; the TERMSEL2 bits relate to the CF2 pin, and the TERMSEL3 bits relate to the CF3 pin. The TERMSELx[0] bits manage Phase A. When set to 1, Phase A power is included in the sum of powers at the CFx converter. When cleared to 0, Phase A power is not included.

The TERMSELx[1] bits manage Phase B, and the TERMSELx[2] bits manage Phase C. Setting all TERMSELx bits to 1 means that all three phase powers are added at the CFx converter. Clearing all TERMSELx bits to 0 means that no phase power is added, and no CF pulse is generated.

Second, Bits[2:0] (CF1SEL[2:0]), Bits[5:3] (CF2SEL[2:0]), and Bits[8:6] (CF3SEL[2:0]) in the CFMODE register determine the type of power that is used at the inputs of CF1, CF2, and the respective CF3 converters. Table 16 shows the values that CFxSEL can have: total active or apparent powers.

By default, all the TERMSELx bits = 1; the CF1SEL bits = 000, the CF2SEL bits = 001, and the CF3SEL bits = 010. Therefore, by default, the CF1 digital-to-frequency converter produces signals that are proportional to the sum of all three phase total active powers, and CF3 produces signals that are proportional to the apparent powers. The CF2 digital-to-frequency converter does not produce a signal because its default setting is reserved.

Like the energy accumulation process, the energy-to-frequency conversion is accomplished in two stages. In the first stage, the instantaneous phase powers obtained from the DSP at a rate of 8 kHz are shifted left seven bits and then accumulated into an internal register at a rate of 1 MHz. When a threshold is reached, a pulse is generated and the threshold is subtracted from the internal register. The sign of the energy at that moment is considered the sign of the sum of the phase powers (see the Sign of the Sum of the Phase Powers in the CFx Datapath section). The threshold is the same threshold used in various active and apparent energy accumulators in DSP, WTHR[47:0] or VATHR[47:0], but this time it is shifted left seven bits. The advantage of accumulating the instantaneous powers at 1 MHz rate is that the ripple at the CFx pins is greatly diminished. The second stage consists of a frequency divider by the 16-bit, unsigned CFxDEN registers (Address 0xE611, Address 0xE612, and Address 0xE613). The values of CFxDEN depend on the meter constant (MC), measured in impulses/kwhr and how much energy is assigned to 1 LSB of the various energy registers: watt-hr and VA-hr. Assuming that a derivative of wh, [10^n wh], where n is a positive or negative integer, is desired as 1 LSB of WATTHR. Then CFxDEN is

$$CFxDEN = \frac{10^3}{MC[imp/kwh] \times 10^n} \quad (33)$$

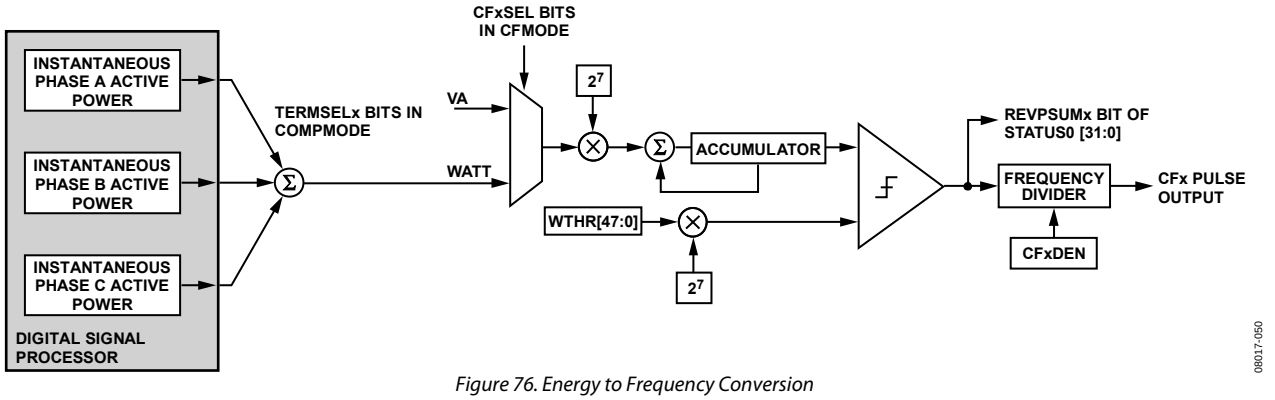


Figure 76. Energy to Frequency Conversion

The derivative of wh must be chosen in such a way as to obtain a CFxDEN that is greater than 1. If CFxDEN = 1, the CF stays active low for only 1 μs, so this number should be avoided. Fractional results cannot be accommodated by the frequency converter, so the result of the division must be rounded to the nearest integer. If CFxDEN is set equal to 0, then the ADE7854 considers it as equal to 1.

The pulse output for all digital to frequency converters stays low for 80 ms if the pulse period is larger than 160 ms (6.25 Hz). If the pulse period is smaller than 160 ms and CFxDEN is an even number, the duty cycle of the pulse output is exactly 50%. If the pulse period is smaller than 160 ms and CFxDEN is an odd number, the duty cycle of the pulse output is (1 + 1/CFxDEN) × 50%. The pulse output is active low and, preferably, should be connected to an LED as shown in Figure 77.

Bit 11 (CF3DIS), Bit 10 (CF2DIS), and Bit 9 (CF1DIS) of the CFMODE register (Address 0xE610) determine if the frequency converter output is generated at the CF3, CF2, or CF1 pin. When Bit CFxDIS is set to 1, which is the default value, the CFx pin is disabled and the pin stays high. When the CFxDIS bit is cleared to 0, the corresponding CFx output generates an active low signal.

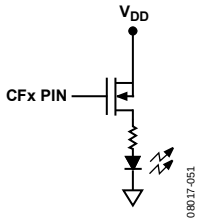


Figure 77. Recommended Connection for the CFx Pins

Bit 16 (CF3), Bit 15 (CF2), and Bit 14 (CF1) in the Mask 0 interrupt mask register (Address 0xE50A) manage the CF3, CF2, and CF1 related interrupts. When the CFx bits are set and a high-to-low transition occurs at the corresponding frequency converter output, an $\overline{\text{IRQ0}}$ interrupt is triggered; and a status bit in the STATUS0 register (Address 0xE502) is set to 1. The interrupt is available even if the CFx output is not enabled by the CFxDIS bits in the CFMODE register (Address 0xE610).

Synchronizing Energy Registers with the CFx Outputs

The ADE7854 contains a feature that allows synchronization of the content of the phase energy accumulation registers with the generation of a CFx pulse. When a high-to-low transition occurs at one frequency converter output, the contents of all internal phase energy registers that relate to the power being output at CFx pin are latched into the xWATTHR, xFVARHR, and xVAHR registers and then reset to 0. See Table 16 for the list of registers that are latched based on the CFxSEL bits in the CFMODE register. All three phase registers are latched independently from the TERMSELx bits of the COMPMODE register (Address 0xE60E). The process is shown in the example in Figure 78, where CF1SEL = 010 (apparent powers contribute at the CF1 pin) and CFCYC = 2.

The 8-bit, unsigned CFCYC register (Address 0xE705) contains the number of high-to-low transitions at the frequency converter that are output between two consecutive latches. Avoid writing a new value to the CFCYC register during a high-to-low transition at any CFx pin.

Bit 14 (CF3LATCH), Bit 13 (CF2LATCH), and Bit 12 (CF1LATCH) of the CFMODEregister enable this process when set to 1. When they are cleared to 0, which is the default state, no latch occurs. The process is available even when the CFx output is not enabled by the CFxDIS bits in the CFMODE register.

Table 16. CFxSEL Bits Description

CFxSEL	Description	Registers Latched When CFxLATCH = 1
000	CFx signal proportional to the sum of total phase active powers	AWATTHR, BWATTHR, and CWATTHR
001	Reserved	
010	CFx signal proportional to the sum of phase apparent powers	AVAHR, BVAHR, and CVAHR
011 to 111	Reserved	

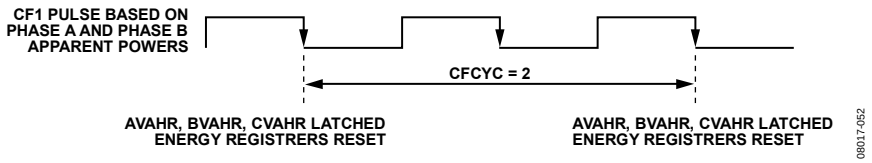


Figure 78. Synchronizing AVAHR and BVAHR with CF1

CFx Outputs for Various Accumulation Modes

The WATTACC bits in the ACCMODE register (Address 0xE701) determine the accumulation modes of the total active powers when signals proportional to the total active powers are chosen at the CFx pins (Bits CFxSEL = 000 or 011 in the CFMODE register). When WATTACC = 00 (the default value), the active powers are sign accumulated before entering the energy-to-frequency converter. Figure 79 shows an example of signed active power accumulation. Note that in this mode, the CF pulses are perfectly synchronized with the active energy accumulated in the watt-hr registers because the powers are sign accumulated in both datapaths.

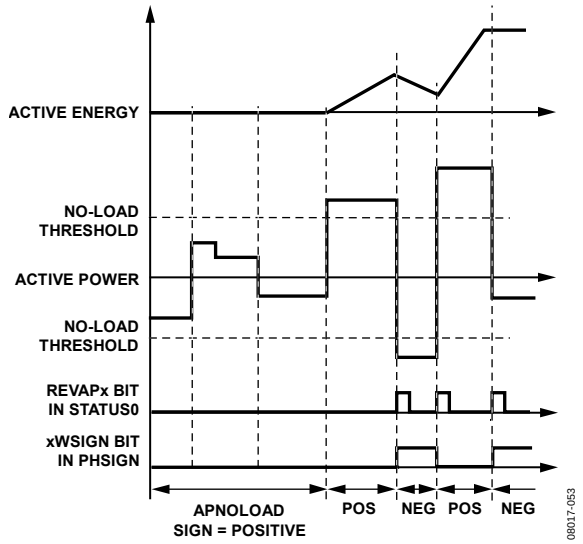


Figure 79. Active Power, Signed Accumulation Mode

When WATTACC = 11, the active powers are accumulated in absolute mode. When the powers are negative, they change sign and are accumulated together with the positive power. Figure 80 shows an example of absolute active power accumulation. Note that in this mode, the watt-hr registers continue to accumulate active powers in signed mode, even if the CF pulses are generated based on the absolute accumulation mode.

Sign of the Sum of the Phase Powers in the CFx Datapath

The ADE7854 has sign detection circuitry for the sum of the phase powers that are used in the CFx datapath. As shown in the Energy-to-Frequency Conversion section, the energy accumulation in the CFx datapath is executed in two stages. Every time a sign change is detected in the energy accumulation at the end of the first stage, that is, after the energy accumulated into the internal accumulator reaches one of the WTHR or VATHR thresholds, a dedicated interrupt can be triggered synchronously with the corresponding CF pulse. The sign of each sum can be read in the PHSIGN register (Address 0xE617).

Bit 18 (REVPSUM3), Bit 13 (REVPSUM2), and Bit 9 (REVPSUM1) of the STATUS0 register (Address 0xE502) are set to 1 when a sign change of the sum of powers occurs in CF3, CF2, or CF1 datapaths. To correlate these events with the pulses generated at the CFx pins after a sign change occurs, the REVPSUMx bits are set at the same time as an occurrence of a high-to-low transition at the CF3, CF2, and CF1 pins.

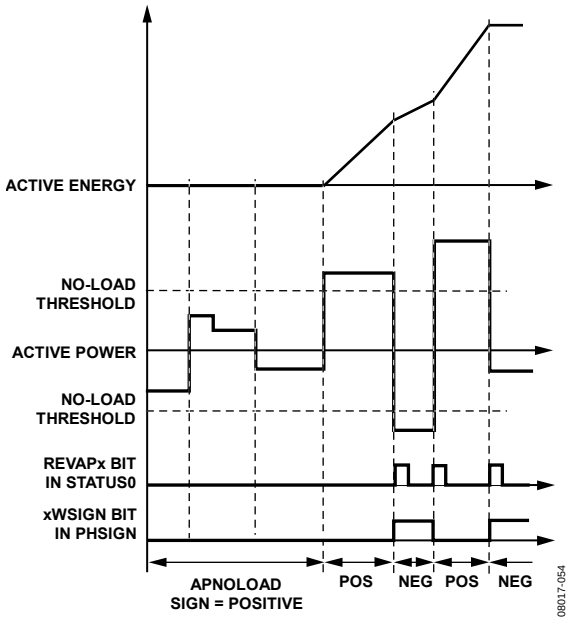


Figure 80. Active Power, Absolute Accumulation Mode

Bit 8 (SUM3SIGN), Bit 7 (SUM2SIGN), and Bit 3 (SUM1SIGN) of the PHSIGN register are set at the same time as the REVPSUM3, REVPSUM2, and REVPSUM1 bits and indicate the sign of the sum of phase powers. When cleared to 0, the sum is positive. When set to 1, the sum is negative.

Interrupts attached to Bit 18 (REVPSUM3), Bit 13 (REVPSUM2), and Bit 9 (REVPSUM1) in the STATUS0 register can be enabled by setting Bit 18, Bit 13, and Bit 9 in the MASK0 register (Address 0xE50A). If enabled, the $\overline{\text{IRQ0}}$ pin is set low and the status bit is set to 1 whenever a change of sign occurs. To find the phase that triggered the interrupt, the PHSIGN register is read immediately after reading STATUS0. Then the status bit is cleared, and the $\overline{\text{IRQ0}}$ pin is set high by writing to the STATUS0 register with the corresponding bit set to 1.

NO-LOAD CONDITION

The no-load condition is defined in metering equipment standards as occurring when the voltage is applied to the meter, and no current flows in the current circuit. To eliminate any creep effects in the meter, the ADE7854 contains two separate no-load detection circuits: one related to the total active powers, and one related to the apparent powers.

No-Load Detection Based on Total Active Power

This no-load condition is triggered when the absolute values of phase total active powers are less than or equal to a threshold indicated in the 24-bit, signed APNOLOAD register (Adress 0x43B1). In this case, the total active energy on that phase is not accumulated and no CF pulses are generated based on it. APNOLOAD represents the positive no-load level of total active power relative to PMAX, the maximum total active power obtained when full-scale voltages and currents are provided at the ADC inputs.

The following equation is used to compute the 24-bit, signed APNOLOAD value:

$$APNOLOAD = \frac{U_n}{U_{FS}} \times \frac{I_{NOLOAD}}{I_{FS}} \times PMAX \quad (34)$$

where:
PMAX = 33,516,139 = 0x1FF6A6B, which is the instantaneous power computed when the ADC inputs are at full scale.
U_{FS} and I_{FS} are the rms values of phase voltages and currents when the ADC inputs are at full scale.
U_n is the nominal rms value of phase voltage.
I_{NOLOAD} is the minimum rms value of phase current the meter starts measuring.

When APNOLOAD is set to negative values, the no-load detection circuit is disabled. Note that to ensure the good functionality of this no-load circuit, the 24-bit VARNOLOAD register (Address 0x43B2) must be set to 0x800000.

As previously stated, the serial ports of the ADE7854 work on 32-, 16-, or 8-bit words, and the DSP works on 28 bits. The 24-bit, signed APNOLOAD and VARNOLOAD registers are accessed as 32-bit registers with the four MSBs padded with 0s and sign extended to 28 bits. See Figure 45 for details.

Bit 0 (NLOAD) in the STATUS1 register (Address 0xE503) is set when this no-load condition in one of the three phases is triggered. Bits[2:0] (NLPHASE[2:0]) in the PHNOLOAD register (Address 0xE608) indicate the state of all phases relative to no-load condition and are set simultaneously with the NLOAD status bit in STATUS1. NLPHASE[0] indicates the state of Phase A; NLPHASE[1], the state of Phase B; and NLPHASE[2], the state of Phase C. When the NLPHASE[x] bit is cleared to 0, the phase is out of no-load condition. When set to 1, the phase is in no-load condition.

An interrupt attached to Status Bit 0 (NLOAD) in the STATUS1 register can be enabled by setting Bit 0 in the MASK1 register (Address 0xE50B). If enabled, the $\overline{\text{IRQ1}}$ pin is set low and the status bit is set to 1 when one of the three phases enters or exits this no-load condition. To find the phase that triggered the interrupt, the PHNOLOAD register is read immediately after reading the STATUS1 register. Then the status bit is cleared, and the $\overline{\text{IRQ1}}$ pin is set high again by writing to the STATUS1 register with the corresponding bit set to 1.

No-Load Detection Based on Apparent Power

This no-load condition is triggered when the absolute value of the phase apparent power is less than or equal to the threshold indicated in the 24-bit, signed VANOLOAD register (Address 0x43B0). In this case, the apparent energy of that phase is not accumulated, and no CF pulses are generated based on this energy. VANOLOAD represents the positive no-load level of apparent power relative to PMAX, the maximum apparent power obtained when full-scale voltages and currents are provided at the ADC inputs.

The following equation is used to compute the VANOLOAD signed 24-bit value:

$$VANOLOAD = \frac{U_n}{U_{FS}} \times \frac{I_{NOLOAD}}{I_{FS}} \times PMAX \quad (35)$$

where:
PMAX = 33,516,139 = 0x1FF6A6B, which is the instantaneous apparent power computed when the ADC inputs are at full scale.
U_{FS} and I_{FS} are the rms values of phase voltages and currents when the ADC inputs are at full scale.
U_n is the nominal rms value of phase voltage.
I_{NOLOAD} is the minimum rms value of phase current the meter starts measuring.

When VANOLOAD is set to negative values, the no-load detection circuit is disabled.

As previously stated, the serial ports of the ADE7854 work on 32-, 16-, or 8-bit words, and the DSP works on 28 bits. Like the registers shown in Figure 45, the signed 24-bit VANOLOAD register is accessed as a 32-bit registers with the four MSBs padded with 0s and sign extended to 28 bits.

Status Bit 2 (VANLOAD) in the STATUS1 register is set when this no-load condition in one of the three phases is triggered. Bits[8:6] (VANLPHASE[2:0]) in the PHNOLOAD register indicate the state of all phases relative to no-load condition and are set simultaneously with the VANLOAD status bit in the STATUS1 register. VANLPHASE[0] indicates the state of Phase A; VANLPHASE[1], the state of Phase B; and VANLPHASE[2], the state of Phase C. When the VANLPHASE bits are cleared to 0, the phase is out of no-load condition. When the VANLPHASE bits are set to 1, the phase is in no-load condition.

An interrupt attached to Bit 2 (VANLOAD) in the STATUS1 register can be enabled by setting Bit 2 in the MASK1 register. If enabled, the $\overline{\text{IRQ1}}$ pin is set low and the status bit is set to 1 when one of the three phases enters or exits this no-load condition. To find the phase that triggered the interrupt, the PHNOLOAD register is read immediately after reading the STATUS1 register. Then the status bit is cleared, and the $\overline{\text{IRQ1}}$ pin is set high again by writing to the STATUS1 register, with the corresponding bit set to 1.

CHECKSUM REGISTER

The 32-bit CHECKSUM register (Address 0xE51F) ensures that certain very important configuration registers maintain their desired value during PSM0, normal power mode.

The registers covered by this register are MASK0, MASK1, COMPMODE, GAIN, CFMODE, CF1DEN, CF2DEN, CF3DEN, CONFIG, MMODE, ACCMODE, LCYCMODE, HSDC_CFG, and six other 8-bit reserved internal registers that always have default values. The ADE7854 computes the cyclic redundancy check (CRC) based on the IEEE802.3 standard.

The registers are introduced one by one into a linear feedback shift register (LFSR)-based generator, starting with the LSB, as shown in Figure 81. The 32-bit result is written in the CHECKSUM register (Address 0xE51F). After power-up or a hardware/software reset, the CRC is computed on the default values of the registers. The result is 0x2689B124.

Figure 82 shows an example of LFSR. Bits a_0, a_1,…, a_{255} represent the bits from the list of registers presented above. a_0 is the LSB of the first internal register to enter LFSR, and a_{255} is the MSB of the MASK0 register (Address 0xE50A), the last register to enter LFSR. Following are the equations that govern LFSR:

$b_i(0)$ =1, i=0, 1, 2,…, 31, the initial state of the bits that form the CRC. b_0 is the LSB, b_{31} is the most significant.

g_i, i=0, 1, 2,…, 31 are the coefficients of the generating polynomial defined by IEEE802.3 standard

$$G(x) = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1 \quad (36)$$

$$g_0 = g_1 = g_2 = g_4 = g_5 = g_7 = 1$$
$$g_8 = g_{10} = g_{11} = g_{12} = g_{16} = g_{22} = g_{26} = 1 \quad (37)$$

All the other g_i coefficients are equal to 0.

$$FB(j) = a_{j-1} \oplus b_{31}(j-1) \quad (38)$$

$$b_0(j) = FB(j) \cdot g_0 \quad (39)$$

$$b_i(j) = FB(j) \cdot g_i \oplus b_{i-1}(j-1), i = 1,2,3,...,31 \quad (40)$$

The operations $\oplus$ and $\cdot$ represent the logic XOR and AND. Equation 38, Equation 39, and Equation 40 have to be repeated for j=1, 2,…, 256. The value written into the CHECKSUM register contains Bits $b_i(256)$, i = 0, 1,…, 31. The value of the CRC after the bits from the reserved internal register have passed through LFSR is 0x3A7ABC72. It is obtained at Step j = 48.

Two different approaches can be followed when using the CHECKSUM register. One is to compute the CRC based on the relationships shown in Equation 36 to Equation 40 and then compare the value against the CHECKSUM register. Another is to periodically read the CHECKSUM register. If two consecutive readings differ, it can be safely assumed that one of the registers has changed value and, therefore, the ADE7854 has changed configuration. The recommended response is to initiate a hardware/software reset that sets the values of all registers to the default, including the reserved registers, and then reinitialize the configuration registers.

INTERRUPTS

The ADE7854 has two interrupt pins, $\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$. Each pin is managed by a 32-bit interrupt mask register, MASK0 and MASK1 (Address 0xE50A and Address 0xE50B, respectively). To enable an interrupt, a bit in the MASKx register must be set to 1. To disable it, the bit must be cleared to 0. Two 32-bit status registers, STATUS0 and STATUS1 (Address 0xE502 and Address 0xE503, respectively) are associated with the interrupts. When an interrupt event occurs in the ADE7854, the corresponding flag in the interrupt status register is set to Logic 1 (see Table 26 and Table 27). If the mask bit for this interrupt in the interrupt mask register is set to Logic 1, the $\overline{\text{IRQx}}$ logic output goes active low. The flag bits in the interrupt status register are set, irrespective of the state of the mask bits. To determine the source of the interrupt, the MCU performs a read of the corresponding STATUSx register and identifies which bit is set to 1. To clear the flag in the status register, the STATUSx register should be written back to the ADE7854 with the flag set to 1. Practically speaking, after an interrupt pin goes low, the status register is read and the source of the interrupt is identified. Then, the status register is written back to the ADE7854 without any change to cancel the status flag. The $\overline{\text{IRQx}}$ pin remains low until the status flag is cancelled.

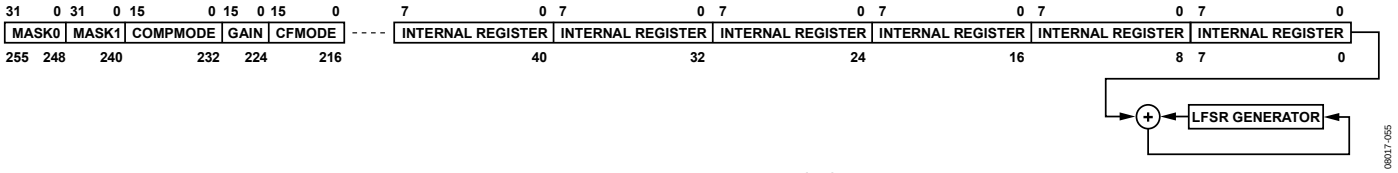


Figure 81. CHECKSUM Register Calculation

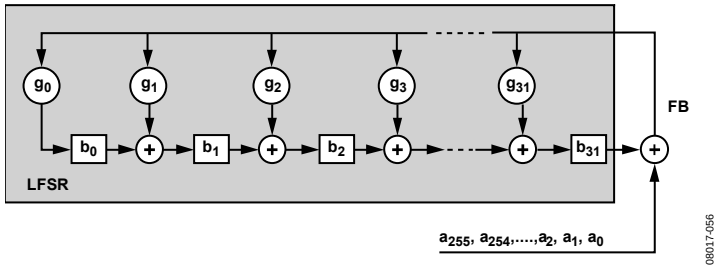


Figure 82. LFSR Generator Used in the CHECKSUM Register Calculation

By default, all interrupts are disabled. The RSTDONE interrupt is an exception. This interrupt can never be masked (disabled); and, therefore, Bit 15 (RSTDONE) in the MASK1 register (Address 0xE50B) does not have any functionality. The IRQ1 pin always goes low, and Status Bit 15 (RSTDONE) in the STATUS1 register (Address 0xE503) is set to 1 whenever a power-up or a hardware/software reset process ends. To cancel the status flag, the STATUS1 register must be written to with Bit 15 (RSTDONE) set to 1.

Some interrupts are used in conjunction with other status registers: Bit 0 (NLOAD) and Bit 2 (VANLOAD) in the MASK1 register work in conjunction with the status bits in the PHNOLAD register (Address 0xE608). Bit 16 (SAG), Bit 17 (OI), and Bit 18 (OV) in the MASK1 register work with the status bits in the PHSTATUS register (Address 0xE600). Bit 23 (PKI) and Bit 24 (PKV) in the MASK1 register work with the status bits in the IPEAK register and the VPEAK register (Address 0xE500 and Address 0xE501, respectively). Bit 8 (REVAPC), Bit 7 (REVAPB), and Bit 6 (REVAPA) and Bit 9 (REVPSUM1), Bit 13 (REVPSUM2), and Bit 18 (REVPSUM3) in the MASK0 register (Address 0xE50A) work with the status bits in the PHSIGN register (Address 0xE617). When the STATUSx register is read and one of these bits is set to 1, the status register associated with the bit is immediately read to identify the phase that triggered the interrupt. Only then is the STATUSx register written with the bit set to 1 to cancel the status flag.

Using the Interrupts with an MCU

Figure 83 shows a timing diagram that illustrates a suggested implementation of ADE7854 interrupt management using an MCU. At Time t_1, the IRQx pin goes active low, indicating that one or more interrupt events have occurred in the ADE7854. The IRQx pin should be tied to a negative-edge-triggered external interrupt on the MCU. Upon detection of the negative edge, the MCU should be configured to start executing its interrupt service routine (ISR). Upon entering the ISR, all interrupts should be disabled using the global interrupt mask bit. Next, the MCU external interrupt flag can be cleared to capture interrupt events that occur during the current ISR. When the MCU interrupt flag is cleared, a read from STATUSx (the interrupt status register) is carried out. The interrupt status register content is used to determine the source of the interrupt(s) and, hence, the appropriate action to be taken. Then, the same STATUSx content is written back into the ADE7854 to clear the status flag(s) and reset the IRQx line to logic high (t_2). If a subsequent interrupt event occurs during the ISR (t_3) that event is recorded by the MCU external interrupt flag being set again.

On returning from the ISR, the global interrupt mask bit is cleared (same instruction cycle) and the external interrupt flag uses the MCU to jump to its ISR once again. This ensures that the MCU does not miss any external interrupts.

Figure 84 shows a recommended timing diagram in which the status bits in the STATUSx registers work in conjunction with bits in other registers. As discussed previously in this section, when the IRQx pin goes active low, the STATUSx register is read. If one of the STATUSx bits is set to 1, a second status register is read immediately to identify the phase that triggered the interrupt. The name PHx in Figure 84 denotes one of the PHSTATUS, IPEAK, VPEAK, or PHSIGN registers. Finally, the STATUSx register is written back to the ADE7854 to clear the status flag(s).

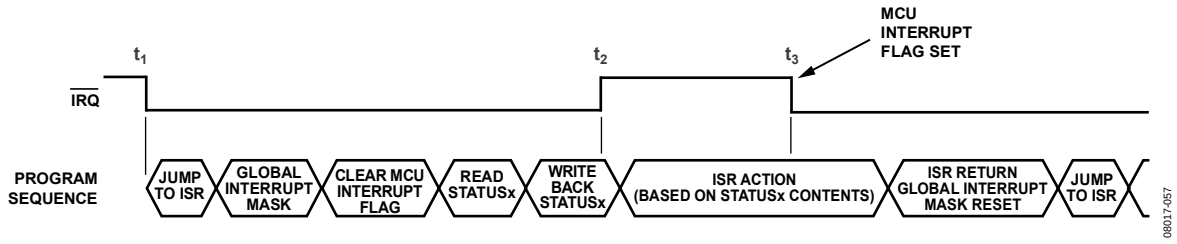


Figure 83. Interrupt Management

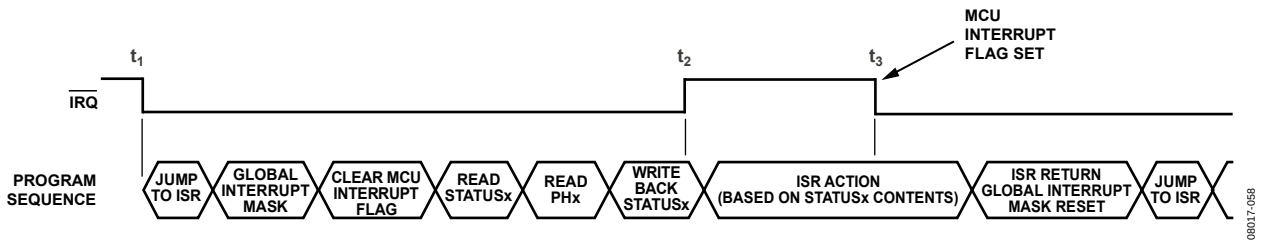


Figure 84. Interrupt Management When PHSTATUS, IPEAK, VPEAK or PHSIGN Registers Are Involved

SERIAL INTERFACES

The ADE7854 has three serial port interfaces: one fully licensed I²C interface, one Serial Peripheral Interface (SPI) and one High Speed Data Capture Port (HSDC). As the SPI pins are multiplexed with some of the pins of I²C and HSDC ports, the ADE7854 accepts two configurations: one using SPI port only and one using I²C port in conjunction with HSDC port.

Serial Interface Choice

After reset, the HSDC port is always disabled. The choice between I²C and SPI port is done by manipulating the $\overline{SS}$ pin after power up or after a hardware reset. If the $\overline{SS}$ pin is kept high, then the ADE7854 uses the I²C port until a new hardware reset is executed. If the $\overline{SS}$ pin is toggled high to low three times after power-up or after a hardware reset, the ADE7854 uses the SPI port until a new hardware reset is executed. This manipulation of the $\overline{SS}$ pin can be accomplished in two ways: one way is to use the $\overline{SS}$ pin of the master device (that is, the microcontroller) as a regular I/O pin and toggle it three times. Another way is to execute three SPI write operations to a location in the address space that is not allocated to a specific ADE7854 register (for example, 0xEBFF, where 8 bit writes can be executed). These writes allow the $\overline{SS}$ pin to toggle 3 times. See SPI Write Operation section for details on the write protocol involved.

After the serial port choice is done, it needs to be locked, so the active port remains in use until a hardware reset is executed in PSM0 normal mode or until a power down. If I²C is the active serial port, bit 1 (I2C_LOCK) of CONFIG2[7:0] must be set to 1 to lock it in. From this moment on, the ADE7854 ignores spurious togglings of the $\overline{SS}$ pin and an eventual switch into using SPI port is no longer possible. If SPI is the active serial port, any write to CONFIG2[7:0] register locks the port. From this moment on, a switch into using I²C port is no longer possible.

Once locked, the serial port choice is maintained when the ADE7854 changes between PSM0 and PSM3 power modes.

The functionality of the ADE7854 is accessible via several on-chip registers. The contents of these registers can be updated or read using the I²C or SPI interfaces. HSDC port provides the state of up to 13 registers representing instantaneous values of phase voltages and currents, active and apparent powers.

I²C Compatible Interface

The ADE7854 supports a fully licensed I²C interface. The I²C interface is implemented as a full hardware slave. SDA is the data I/O pin, and SCL is the serial clock. These two pins are shared with the MOSI and SCLK pins of the on-chip SPI interface. The maximum serial clock frequency supported by this interface is 400KHz.

The two pins used for data transfer, SDA and SCL are configured in a Wired-AND format that allows arbitration in a multi-master system.

The transfer sequence of an I²C system consists of a master device initiating a transfer by generating a START condition while the bus is idle. The master transmits the address of the slave device and the direction of the data transfer in the initial address transfer. If the slave acknowledges, then the data transfer is initiated. This continues until the master issues a STOP condition and the bus becomes idle.

I²C Write Operation

The write operation using I²C interface of the ADE7854 initiates when the master generates a start condition and consists of one byte representing the address of the ADE7854 followed by the 16-bit address of the target register and by the value of the register.

The most significant seveb bits of the address byte constitute the address of the ADE7854 and they are equal to b#0111000. Bit 0 of the address byte is the READ/$\overline{WRITE}$ bit. Because this is a write operation, it has to cleared to 0, so the first byte of the write operation is 0x70. After every byte is received, the ADE7854 generates an acknowledge. As registers may have 8, 16 or 32 bits, after the last bit of the register is transmitted and the ADE7854 acknowledges the transfer, the master generates a STOP condition. The addresses and the register content are sent MSB first. See Figure 85 for details of the I²C write operation.

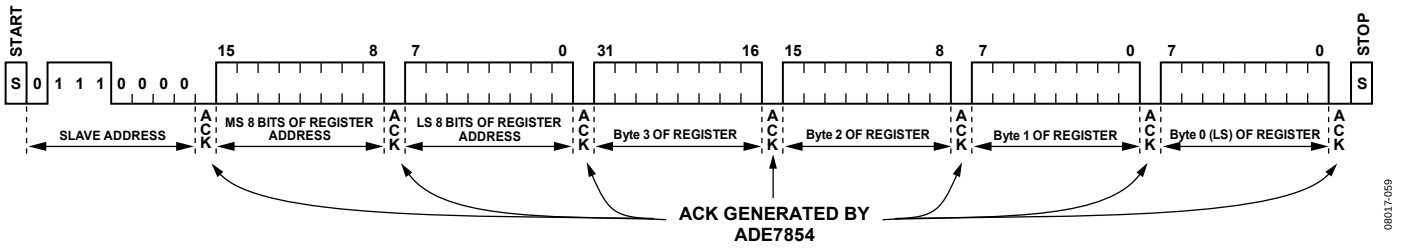


Figure 85. I²C Write Operation of a 32-Bit Register

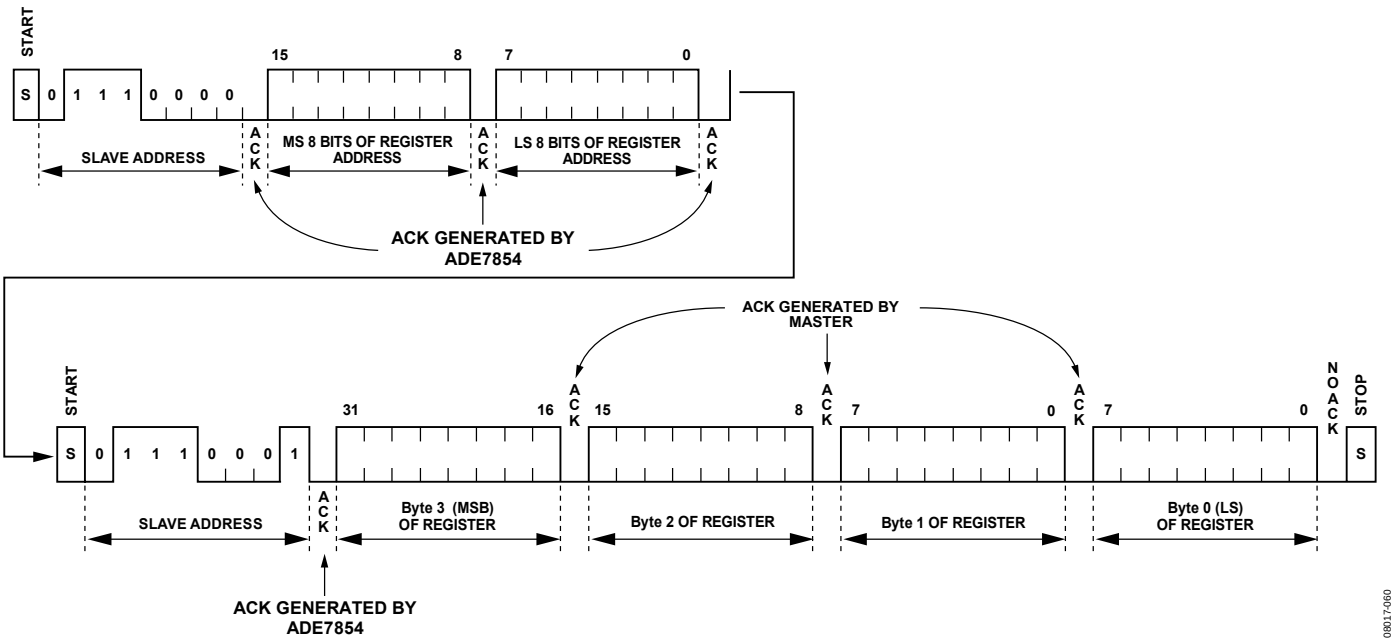


Figure 86. I²C Read Operation of a 32-Bit Register

I²C Read Operation

The read operation using the I²C interface of the ADE7854 is performed in two stages. The first stage sets the pointer to the address of the register. The second stage reads the content of the register.

As shown in Figure 86, the first stage initiates when the master generates a start condition. It consists of one byte that represents the address of the ADE7854, followed by the 16-bit address of the target register. The ADE7854 acknowledges every byte received. The address byte is similar to the address byte of a write operation and is equal to 0x70 (see the I2C Write Operation section). After the last byte of the register address has been sent and it has been acknowledged by the ADE7854, the second stage begins with the master generating a new start condition, followed by an address byte. The seven MSBs of this address byte constitute the address of the ADE7854; they are equal to b#0111000. Bit 0 of the address byte is the READ/WRITE bit. Because this is a read operation, Bit 0 must be set to 1, so the first byte of the read operation is 0x71. After this byte is received, the ADE7854 generates an acknowledge. Then the ADE7854 sends the value of the register, and, after every eight bits are received, the master generates an acknowledge. All the bytes are sent with the MSB first. Because registers can have 8, 16, or 32 bits, after the last bit of the register is received , the master does not acknowledge the transfer but, instead, generates a stop condition.

SPI-Compatible Interface

The serial peripheral interface (SPI) of the ADE7854 is always a slave of the communication and consists of four pins: SCLK, MOSI, MISO, and $\overline{SS}$. The serial clock for a data transfer is applied at the SCLK logic input. This logic input has a Schmitt trigger input structure that allows slow rising (and falling) clock edges to be used. All data transfer operations are synchronized to the serial clock. Data is shifted into the ADE7854 at the MOSI logic input on the falling edge of SCLK, and the ADE7854 samples it on the rising edge of SCLK. Data is shifted out of the ADE7854 at the MISO logic output on a falling edge of SCLK and can be sampled by the master device on the raising edge of SCLK. The MSB of the word is shifted in and out first. The maximum serial clock frequency supported by this interface is 2.5 MHz. MISO stays in a high impedance state when no data is transmitted from the ADE7854. Figure 87 shows details of the connection between the ADE7854 SPI and a master device containing an SPI interface.

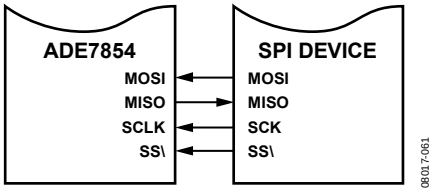


Figure 87. Connecting the SPI with an SPI Device

The $\overline{SS}$ logic input is the chip select input. This input is used when multiple devices share the serial bus. The $\overline{SS}$ input should be driven low for the entire data transfer operation. Bringing $\overline{SS}$ high during a data transfer operation aborts the transfer and places the serial bus in a high impedance state. A new transfer can then be initiated by bringing the $\overline{SS}$ logic input low again. However, because aborting a data transfer before completion leaves the accessed register in a state that cannot be guaranteed, every time a register is written, its value should be verified by reading it back.

The protocol is similar to the protocol used in the I²C interface.

SPI Read Operation

The read operation using the SPI interface of the ADE7854 initiates when the master sets the $\overline{SS}$ pin low and begins sending one byte representing the address of the ADE7854 on the MOSI line. The master sets data on the MOSI line starting with the first high-to-low transition of SCLK. The SPI of the ADE7854 samples data on the low-to-high transitions of SCLK. The seven MSBs of the address byte can have any value, but as a good programming practice, they should be different from b#0111000, which are the seven bits used in the I²C protocol. Bit 0 (READ/$\overline{WRITE}$) of the address byte must be set to 1 for a read operation. Next, the master sends the 16-bit address of the register that is read. After the ADE7854 receives the last address bit of the register on a low-to-high transition of SCLK, it begins to transmit its content on the MISO line before the next SCLK high-to-low transition occurs, so the master can sample the data on this SCLK transition. After the master receives the last bit, it sets the $\overline{SS}$ and SCLK lines high, and the communication ends. The MOSI and MISO data lines go into a high impedance state (see Figure 88 for the SPI read operation).

SPI Write Operation

The write operation using the SPI interface of the ADE7854 initiates when the master sets the $\overline{SS}$ pin low and begins sending one byte representing the address of the ADE7854 on the MOSI line. The master sets data on the MOSI line starting with the first high-to-low transition of SCLK. The SPI of the ADE7854 samples data on the low-to-high transitions of SCLK. The seven MSBs of the address byte can have any value, but as a good programming practice, they should be different from b#0111000, which are the seven bits used in the I²C protocol. Bit 0 (READ/$\overline{WRITE}$) of the address byte must be set to 0 for a write operation. Next, the master sends the 16-bit address of the register that is written to, as well as the 32-, 16-, or 8-bit value of that register, without losing any SCLK cycles. After the last bit is transmitted, the master sets the $\overline{SS}$ and SCLK lines high at the end of the SCLK cycle, and the communication ends. The MOSI and MISO data lines go into a high impedance state (see Figure 89 for the SPI write operation).

High Speed Data Capture Interface (HSDC)

The HSDC interface is disabled after default. It can be used only if the ADE7854 is configured with the I²C interface. The SPI interface cannot be used in conjunction with HSDC. Bit 6 (HSDCEN) in the CONFIG register (Address 0xE618) activates HSDC when set to 1. If the HSDCEN bit is cleared to 0, which is the default value, the HSDC interface is disabled. Setting HSDCEN = 1 when SPI is in use does not have any effect.

HSDC is an interface that is used to send up to thirteen 32-bit words to an external device, usually a microprocessor or a DSP. The words represent the instantaneous values of the phase currents and voltages, active and apparent powers. The registers that are transmitted are: IAWV, VAWV, IBWV, VBWV, ICWV, VCWV, AVA, BVA, CVA, AWATT, BWATT, and CWATT. All are 24-bit registers that are sign extended to 32-bits (see Figure 47). HSDC can be interfaced with SPI or other similar interfaces.

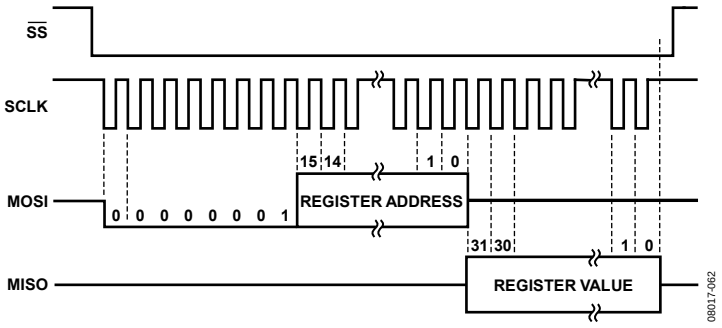


Figure 88. SPI Read Operation of a 32-Bit Register

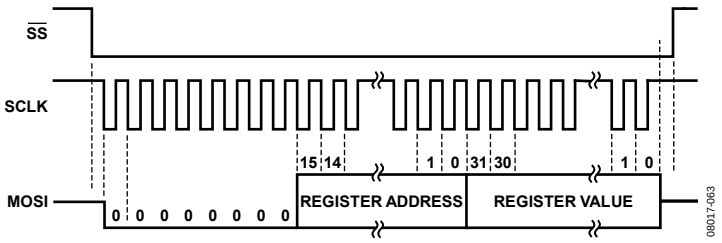


Figure 89. SPI Write Operation of a 32-Bit Register

HSDC is always a master of the communication and consists of three pins: HSA ($\overline{SS}$/HSA), HSD (MISO/HSD), and HSCLK (CF3/HSCLK). HSA represents the select signal. It stays active low or high when a word is transmitted and is usually connected to the select pin of the slave. HSD is used to send data to the slave and is usually connected to the data input pin of the slave. HSCLK is the serial clock line. It is generated by the ADE7854 and is usually connected to the serial clock input of the slave. Figure 90 shows details of the connection between the ADE7854 HSDC and slave devices containing SPI interfaces.

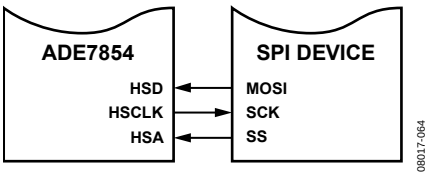


Figure 90. Connecting HSDC with an SPI

The HSDC communication is managed by the HSDC_CFG register at Address 0xE706 (see Table 17). It is recommended that the HSDC_CFG register be set to the desired value before enabling the port, using Bit 6 (HSDCEN) in the CONFIG register (Address 0xE618). In this way, the state of various pins belonging to the HSDC port do not take levels that are inconsistent with the desired HSDC behavior. After a hardware reset or after power-up, the MISO/HSD and $\overline{SS}$/HSA pins are set high.

Bit 0 (HCLK) in the HSDC_CFG register determines the serial clock frequency of the HSDC communication. When HCLK = 0, which is the default value, the clock frequency is 8 MHz. When HCLK = 1, the clock frequency is 4 MHz. A bit of data is transmitted for every HSCLK high-to-low transition. The slave device that receives data from HSDC samples the HSD line on the low-to-high transition of HSCLK.

The words can be transmitted as 32-bit packages or as 8-bit packages. When Bit 1 (HSIZE) in the HSDC_CFG register is set to 0 (the default value), the words are transmitted as 32-bit packages. When HSIZE = 1, the registers are transmitted as 8-bit packages. The HSDC interface transmits the words with the MSB first.

When set to 1, Bit 2 (HGAP) introduces a gap of seven HSCLK cycles between packages. When the HGAP bit is cleared to 0 (the default value), no gap is introduced between packages and the communication time is shortest. In this case, HSIZE does not have any influence on the communication, and a bit is put on the HSD line every HSCLK high-to-low transition.

Bits[4:3] (HXFER) of the HSDC_CFG register (Address 0xE706) determine how many words are transmitted. When HXFER = 00, which is the default value, 16 words are transmitted. When HXFER = 01, only the words representing the instantaneous values of phase currents and phase voltages are transmitted, and they are transmitted in the following order: IAWV, VAWV, IBWV, VBWV, ICWV, VCWV and one 32-bit word that is always equal to 0. When HXFER = 10, only the instantaneous values of the phase powers are transmitted, and they are transmitted in the following order: AVA, BVA, CVA, AWATT, BWATT, CWATT, followed by three 32-bit words that are always equal to 0. HXFER = 11 is reserved, and writing it is equivalent to writing 00, which is the default value.

Bit 5 (HSAPOL) determines the polarity of the HSA pin during the communication. When HSAPOL = 0, which is the default value, the HSA pin is active low during the communication. This means that HSA stays high when no communication is in progress. When the communication starts, HSA goes low and stays low until the communication ends. Then it returns high. When HSAPOL = 1, the HSA pin is active high during the communication. This means that HSA stays low when no communication is in progress. When the communication starts, HSA goes high and stays high until the communication ends. Then it returns low.

Table 17. HSDC_CFG Register (Address 0xE706)

Bit	Bit Name	Default Value	Description
[7:6]	Reserved	00	Reserved. These bits do not manage any functionality.
5	HSAPOL	0	0: HSACTIVE output pin is active low. 1: HSACTIVE output pin is active high.
[4:3]	HXFER	00	00: HSDC transmits 16 32-bit words in the following order: IAWV, VAWV, IBWV, VBWV, ICWV, VCWV, one 32-bit word equal to 0, AVA, BVA, CVA, AWATT, BWATT, CWATT and three 32-bit words equal to 0. 01: HSDC transmits the six instantaneous values of currents and voltages plus one 32-bit word that is always equal to 0 in the following order: IAWV, VAWV, IBWV, VBWV, ICWV, VCWV and one 32-bit word equal to 0. 10: HSDC transmits six instantaneous values of phase powers plus three 32-bit words that are always equal to 0 in the following order: AVA, BVA, CVA, AWATT, BWATT, CWATT and three 32-bit words that are equal to 0. 11: reserved. If set, the ADE7854 behaves as though HXFER = 00.
2	HGAP	0	0: no gap is introduced between packages. 1: a gap of seven HCLK cycles is introduced between packages.
1	HSIZE	0	0: HSDC transmits the 32-bit registers in 32-bit packages, MSB first 1: HSDC transmits the 32-bit registers in 8-bit packages, MSB first.
0	HCLK	0	0: HSCLK = 8 MHz. 1: HSCLK = 4 MHz.

Bits[7:6] of the HSDC_CFG register are reserved. Any value written to these bits has no effect on HSDC behavior.

Figure 91 shows the HSDC transfer protocol for HGAP = 0, HXFER = 00, and HSAPOL = 0. Note that the HSDC interface sets a bit on the HSD line every HSCLK high-to-low transition, and the value of the HSIZE bit is irrelevant.

Figure 92 shows the HSDC transfer protocol for HSIZE = 0, HGAP = 1, HXFER = 00 and HSAPOL = 0. Note that the HSDC interface introduces a gap of seven HSCLK cycles between every 32-bit word.

Figure 93 shows the HSDC transfer protocol for HSIZE = 1, HGAP = 1, HXFER = 00, and HSAPOL = 0. Note that the HSDC interface introduces a gap of seven HSCLK cycles between the 8-bit words.

Table 18 shows the time it takes to execute an HSDC data transfer for all HSDC_CFG settings. For some settings, the transfer time is less than 125 µs (at a frequency of 8 kHz), which is the update rate of the waveform sample registers. This means that the HSDC port transmits data every sampling cycle. For settings in which the transfer time is greater than 125 µs, the HSDC port transmits data in only the first of two consecutive 8 kHz sampling cycles. This means it transmits registers at an effective rate of 4 kHz.

Table 18. Communication Times for Various HSDC Settings

HXFER	HGAP	HSIZE[1]	HCLK	Communication Time (µs)
00	0	X	0	64
00	0	X	1	128
00	1	0	0	77.125
00	1	0	1	154.25
00	1	1	0	119.25
00	1	1	1	238.25
01	0	X	0	28
01	0	X	1	56
01	1	0	0	33.25
01	1	0	1	66.5
01	1	1	0	51.625
01	1	1	1	103.25
10	0	X	0	36
10	0	X	1	72
10	1	0	0	43
10	1	0	1	86
10	1	1	0	66.625
10	1	1	1	133.25

[1] X = don't care.

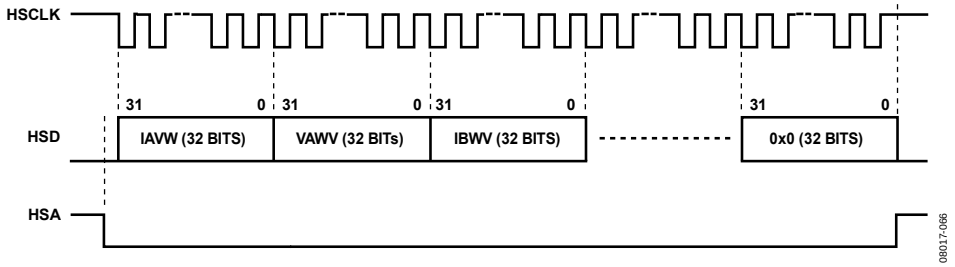


Figure 91. HSDC Communication for HGAP = 0, HXFER[1:0] = 00, and HSAPOL = 0; HSIZE Is Irrelevant

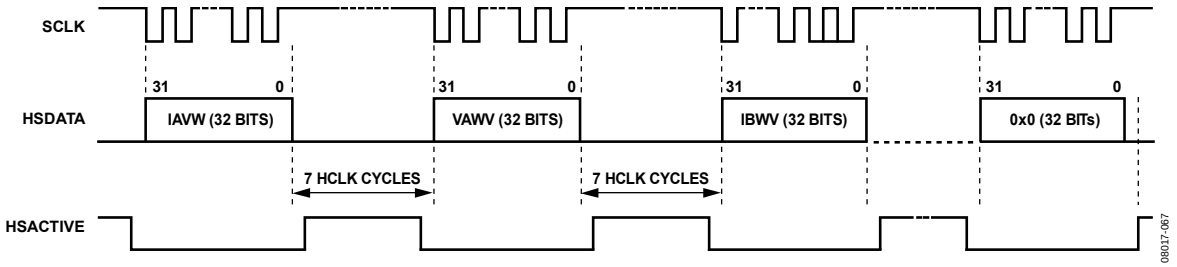


Figure 92. HSDC Communication for HSIZE = 0, HGAP = 1, HXFER[1:0] = 00, and HSAPOL = 0

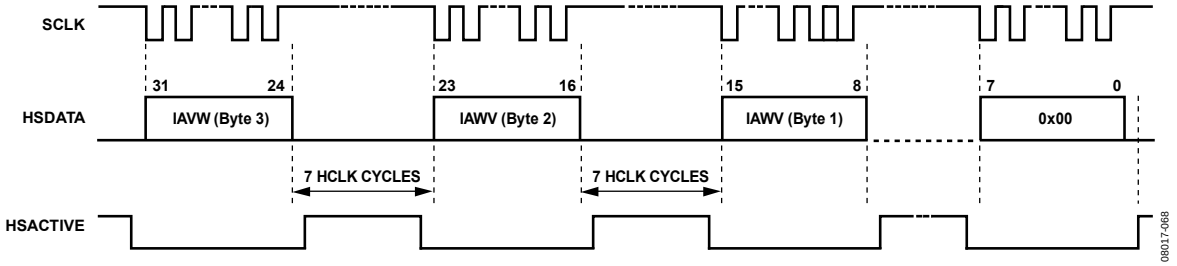


Figure 93. HSDC Communication for HSIZE = 1, HGAP = 1, HXFER[1:0] = 00, and HSAPOL = 0

REGISTERS

REGISTER MAPS

Table 19. Registers Located in DSP Data Memory RAM

Address	Name	R/W[1]	Bit Length	Bit Length During Communication[2]	Type[3]	Default Value	Description
0x4380	AIGAIN	R/W	24	32 ZPSE	S	0x000000	Phase A current gain adjust.
0x4381	AVGAIN	R/W	24	32 ZPSE	S	0x000000	Phase A voltage gain adjust.
0x4382	BIGAIN	R/W	24	32 ZPSE	S	0x000000	Phase B current gain adjust.
0x4383	BVGAIN	R/W	24	32 ZPSE	S	0x000000	Phase B voltage gain adjust.
0x4384	CIGAIN	R/W	24	32 ZPSE	S	0x000000	Phase C current gain adjust.
0x4385	CVGAIN	R/W	24	32 ZPSE	S	0x000000	Phase C voltage gain adjust.
0x4386	Reserved	N/A	N/A	N/A	N/A	0x000000	For proper operation, this memory location should be kept at 0x000000.
0x4387	AIRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase A current rms offset.
0x4388	AVRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase A voltage rms offset.
0x4389	BIRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase B current rms offset.
0x438A	BVRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase B voltage rms offset.
0x438B	CIRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase C current rms offset.
0x438C	CVRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase C voltage rms offset.
0x438D	Reserved	N/A	N/A	N/A	N/A	0x000000	For proper operation, this memory location should be kept at 0x000000.
0x438E	AVAGAIN	R/W	24	32 ZPSE	S	0x000000	Phase A apparent power gain adjust.
0x438F	BVAGAIN	R/W	24	32 ZPSE	S	0x000000	Phase B apparent power gain adjust.
0x4390	CVAGAIN	R/W	24	32 ZPSE	S	0x000000	Phase C apparent power gain adjust.
0x4391	AWGAIN	R/W	24	32 ZPSE	S	0x000000	Phase A total active power gain adjust.
0x4392	AWATTOS	R/W	24	32 ZPSE	S	0x000000	Phase A total active power offset adjust.
0x4393	BWGAIN	R/W	24	32 ZPSE	S	0x000000	Phase B total active power gain adjust.
0x4394	BWATTOS	R/W	24	32 ZPSE	S	0x000000	Phase B total active power offset adjust.
0x4395	CWGAIN	R/W	24	32 ZPSE	S	0x000000	Phase C total active power gain adjust.
0x4396	CWATTOS	R/W	24	32 ZPSE	S	0x000000	Phase C total active power offset adjust.
0x4397 to 0x43A8	Reserved	N/A	N/A	N/A	N/A	0x000000	These memory locations should be kept at 0x000000 for proper operation.
0x43A9	VATHR1	R/W	24	32 ZP	U	0x000000	24 MSBs of VATHRx[47:0] threshold used in phase apparent power datapath.
0x43AA	VATHR0	R/W	24	32 ZP	U	0x000000	24 LSBs of the VATHRx[47:0] threshold used in the phase apparent power datapath.
0x43AB	WTHR1	R/W	24	32 ZP	U	0x000000	24 MSBs of the WTHRx[47:0] threshold used in the phase total active power datapath.
0x43AC	WTHR0	R/W	24	32 ZP	U	0x000000	24 LSBs of the WTHRx[47:0] threshold used in the phase total active power datapath.
0x43AD to 0x43AF	Reserved	N/A	N/A	N/A	N/A	0x000000	For proper operation, this memory location should be kept at 0x000000.
0x43B0	VANOLOAD	R/W	24	32 ZPSE	S	0x000000	No-load threshold in the apparent power datapath.
0x43B1	APNOLOAD	R/W	24	32 ZPSE	S	0x000000	No-load threshold in the total active power datapath.
0x43B2	VARNOLOAD	R/W	24	32 ZPSE	S	0x000000	This register must be set to 0x800000 to ensure correct functionality of the no-load detection circuit based on total active power (see the No-Load Detection Based on Total Active Power section for details).
0x43B3 to 0x43B4	Reserved	N/A	N/A	N/A	N/A	0x000000	For proper operation, these memory locations should not be written.

Address	Name	R/W[1]	Bit Length	Bit Length During Communication[2]	Type[3]	Default Value	Description
0x43B5	DICOEFF	R/W	24	32ZPSE	S	0x0000000	Register used in the digital integrator algorithm; if the integrator is turned on, it must be set to 0xFF8000.
0x43B6	HPFDIS	R/W	24	32 ZP	U	0x000000	Disables/enables the HPF in the current datapath (see the Register Bit Descriptions section).
0x43B7 to 0x43BF	Reserved	N/A	N/A	N/A	N/A	0x000000	For proper operation, these memory locations should be kept at 0x000000.
0x43C0	AIRMS	R	24	32 ZP	S	NA	Phase A current rms value.
0x43C1	AVRMS	R	24	32 ZP	S	NA	Phase A voltage rms value.
0x43C2	BIRMS	R	24	32 ZP	S	NA	Phase B current rms value.
0x43C3	BVRMS	R	24	32 ZP	S	NA	Phase B voltage rms value.
0x43C4	CIRMS	R	24	32 ZP	S	NA	Phase C current rms value.
0x43C5	CVRMS	R	24	32 ZP	S	NA	Phase C voltage rms value.
0x43C6 to 0x43FF	Reserved	N/A	N/A	N/A	N/A	0x000000	For proper operation, these memory locations should not be written to.

[1] R = read; W = write.
[2] 32 ZPSE is a 24-bit, signed register that is transmitted as a 32-bit word, with the four MSBs padded with 0s and sign extended to 28 bits; 32 ZP is a 28- or 24-bit, signed or unsigned register that is transmitted as a 32-bit word with four or eight MSBs, respectively, that are padded with 0s.
[3] U = unsigned register, S = signed register in twos complement format.

Table 20. Internal DSP Memory RAM Registers

Address	Name	R/W[1]	Bit Length	Bit Length During Communication	Type[2]	Default Value	Description
0xE203	Reserved	R/W	16	16	U	0x0000	For proper operation, do not write to this memory location.
0xE228	RUN	R/W	16	16	U	0x0000	The RUN register starts and stops the DSP (see the Digital Signal Processor section).

[1] R = read, W = write.
[2] U = unsigned register.

Table 21. Billable Registers

Address	Name	R/W[1]	Bit Length	Bit Length During Communication	Type[2]	Default Value	Description
0xE400	AWATTHR	R	32	32	S	0x00000000	Phase A total active energy accumulation.
0xE401	BWATTHR	R	32	32	S	0x00000000	Phase B total active energy accumulation.
0xE402	CWATTHR	R	32	32	S	0x00000000	Phase C total active energy accumulation.
0xE403 to 0xE40B	Reserved	R	N/A	N/A	N/A	Can have any value	Reserved.
0xE40C	AVAHR	R	32	32	S	0x00000000	Phase A apparent energy accumulation.
0xE40D	BVAHR	R	32	32	S	0x00000000	Phase B apparent energy accumulation.
0xE40E	CVAHR	R	32	32	S	0x00000000	Phase C apparent energy accumulation.

[1] R = read, W = write.
[2] S = signed register in twos complement format.

Table 22. Configuration and Power Quality Registers

Address	Name	R/W[1]	Bit Length	Bit Length During Communication[2]	Type[3]	Default Value	Description
0xE500	IPEAK	R	32	32	U	NA	Current peak register (see Figure 60 and Table 24).
0xE501	VPEAK	R	32	32	U	NA	Voltage peak register (see Figure 60 and Table 25).
0xE502	STATUS0	R	32	32	U	NA	Interrupt Status Register 0 (see Table 26).
0xE503	STATUS1	R	32	32	U	NA	Interrupt Status Register 1 (see Table 27).
0xE504 to 0xE506	Reserved	N/A	N/A	N/A	N/A	N/A	Reserved
0xE507	OILVL	R/W	24	32 ZP	U	0xFFFFFF	Overcurrent threshold.
0xE508	OVLVL	R/W	24	32 ZP	U	0xFFFFFF	Overvoltage threshold.
0xE509	SAGLVL	R/W	24	32 ZP	U	0x000000	Voltage sag level threshold.
0xE50A	MASK0	R/W	32	32	U	0x00000000	Interrupt Enable Register 0 (see Table 28).
0xE50B	MASK1	R/W	32	32	U	0x00000000	Interrupt Enable Register 1 (see Table 29).
0xE50C	IAWV	R	24	32 SE	S	NA	Instantaneous value of Phase A current.
0xE50D	IBWV	R	24	32 SE	S	NA	Instantaneous value of Phase B current.
0xE50E	ICWV	R	24	32 SE	S	NA	Instantaneous value of Phase C current.
0xE50F	Reserved	R					
0xE510	VAWV	R	24	32 SE	S	NA	Instantaneous value of Phase A voltage.
0xE511	VBWV	R	24	32 SE	S	NA	Instantaneous value of Phase B voltage.
0xE512	VCWV	R	24	32 SE	S	NA	Instantaneous value of Phase C voltage.
0xE513	AWATT	R	24	32 SE	S	NA	Instantaneous value of Phase A total active power.
0xE514	BWATT	R	24	32 SE	S	NA	Instantaneous value of Phase B total active power.
0xE515	CWATT	R	24	32 SE	S	NA	Instantaneous value of Phase B total active power.
0xE516-0xE518	Reserved	R					
0xE519	AVA	R	24	32 SE	S	NA	Instantaneous value of Phase A apparent power.
0xE51A	BVA	R	24	32 SE	S	NA	Instantaneous value of Phase Bapparent power.
0xE51B	CVA	R	24	32 SE	S	NA	Instantaneous value of Phase B apparent power.
0xE51C to 0xE51E	Reserved	R					
0xE51F	CHECKSUM	R	32	32	U	0x2689B124	Checksum verification (see the Checksum Register section for details).
0xE520	VNOM	R/W	24	32 ZP	S	0x000000	Nominal phase voltage rms used in the alternative computation of the apparent power.
0xE521 to 0xE52E	Reserved	N/A	N/A	N/A	N/A	N/A	For proper operation, do not write to these addresses.
0xE600	PHSTATUS	R	16	16	U	NA	Phase peak register (see Table 30 for details).
0xE601	ANGLE0	R	16	16	U	NA	Time Delay 0 (see the Time Interval Between Phases section for details).
0xE602	ANGLE1	R	16	16	U	NA	Time Delay 1 (see the Time Interval Between Phases section for details).
0xE603	ANGLE2	R	16	16	U	NA	Time Delay 2 (see the Time Interval Between Phases section for details).
0xE604 to 0xE606	Reserved	N/A	N/A	N/A	N/A	N/A	For proper operation, do not write to these addresses.
0xE607	PERIOD	R	16	16	U	NA	Network line period.

Address	Name	R/W[1]	Bit Length	Bit Length During Communication[2]	Type[3]	Default Value	Description
0xE608	PHNOLOAD	R	16	16	U	N/A	Phase no-load register (see Table 31).
0xE609 to 0xE60B	Reserved	N/A	N/A	N/A	N/A	N/A	For proper operation, do not write to these addresses.
0xE60C	LINECYC	R/W	16	16	U	0xFFFF	Line cycle accumulation mode count.
0xE60D	ZXTOUT	R/W	16	16	U	0xFFFF	Zero-crossing timeout count.
0xE60E	COMPMODE	R/W	16	16	U	0x01FF	Computation mode register (see Table 32).
0xE60F	GAIN	R/W	16	16	U	0x0000	PGA gains at ADC inputs (see Table 33).
0xE610	CFMODE	R/W	16	16	U	0x0E88	CFx configuration register (see Table 34).
0xE611	CF1DEN	R/W	16	16	U	0x0000	CF1 denominator.
0xE612	CF2DEN	R/W	16	16	U	0x0000	CF2 denominator.
0xE613	CF3DEN	R/W	16	16	U	0x0000	CF3 denominator.
0xE614	APHCAL	R/W	10	16 ZP	U	0x0000	Phase calibration of Phase A (see Table 35).
0xE615	BPHCAL	R/W	10	16 ZP	U	0x0000	Phase calibration of Phase B (see Table 35).
0xE616	CPHCAL	R/W	10	16 ZP	U	0x0000	Phase calibration of Phase C (see Table 35).
0xE617	PHSIGN	R	16	16	U	NA	Power sign register (see Table 36).
0xE618	CONFIG	R/W	16	16	U	0x0000	ADE7854 configuration register (see Table 37).
0xE700	MMODE	R/W	8	8	U	0x16	Measurement mode register (see Table 38).
0xE701	ACCMODE	R/W	8	8	U	0x00	Accumulation mode register (see Table 39).
0xE702	LCYCMODE	R/W	8	8	U	0x78	Line accumulation mode behavior (see Table 40).
0xE703	PEAKCYC	R/W	8	8	U	0x00	Peak detection half line cycles.
0xE704	SAGCYC	R/W	8	8	U	0x00	Sag detection half line cycles.
0xE705	CFCYC	R/W	8	8	U	0x01	Number of CF pulses between two consecutive energy latches (see the Synchronizing Energy Registers with the CFx Outputs section.
0xE706	HSDC_CFG	R/W	8	8	U	0x00	HSDC configuration register (see Table 41).
0xEBFF	Reserved	N/A	8	8	N/A	N/A	This address can be used in manipulating the $\overline{SS}$ pin when SPI is chosen as the active port (see the Serial Interfaces section for details).
0xEC00	Reserved	N/A	N/A	N/A	N/A	N/A	For proper operation, do not write to this address.
0xEC01	CONFIG2	R/W	8	8	U	0x00	Second configuration register (see Table 42).

[1] R = read, W = write.
[2] 32 ZP = 24- or 20-bit signed or unsigned register that is transmitted as a 32-bit word with 8 or 12 MSBs, respectively, that are padded with 0s.
32 SE = 24-bit signed register that is transmitted as a 32-bit word, sign extended to 32 bits
16 ZP = 10-bit unsigned register that is transmitted as a 16-bit word, with six MSBs that are padded with 0s.
[3] U = unsigned, S = signed.

REGISTER BIT DESCRIPTIONS

Table 23. HPFDIS Register (Address 0x43B6)

Bit	Bit Name	Default Value	Description
[23:0]	HPFDIS	0x00000000	When HPFDIS = 0x00000000, all high-pass filters in the voltage and current channels are enabled. When the register is set to any nonzero value, all high-pass filters are disabled.

Table 24. IPEAK Register (Address 0xE500)

Bit	Bit Name	Default value	Description
[31:27]	Reserved	00000	Reserved. These bits are always set to 0.
26	IPPHASE[2]	0	1: Phase C current generated the value of the IPEAKVAL bits.
25	IPPHASE[1]	0	1: Phase B current generated the value of the IPEAKVAL bits.
24	IPPHASE[0]	0	1: Phase A current generated the value of the IPEAKVAL bits.
[23:0]	IPEAKVAL	0x0	These bits contain the peak value determined in the current channel.

Table 25. VPEAK Register (Address 0xE501)

Bit	Bit Name	Default Value	Description
[31:27]	Reserved	00000	Reserved. These bits are always set to 0.
26	VPPHASE[2]	0	1: Phase C voltage generated the value of the VPEAKVAL bits.
25	VPPHASE[1]	0	1: Phase B voltage generated the value of the VPEAKVAL bits.
24	VPPHASE[0]	0	1: Phase A voltage generated the value of the VPEAKVAL bits.
[23:0]	VPEAKVAL	0	These bits contain the peak value determined in the voltage channel.

Table 26. STATUS0 Register (Address 0xE502)

Bit	Bit Name	Default Value	Description
[31:19]	Reserved	0 0000 0000 0000	Reserved. These bits are always set to 0.
18	REVPSUM3	0	1: the sum of all phase powers in the CF3 datapath has changed sign. The sign itself is indicated in Bit 8 (SUM3SIGN) of the PHSIGN register (see Table 36).
17	DREADY	0	1: all periodical (at 8 kHz rate) DSP computations are complete.
16	CF3		1: a high-to-low transition has occurred at the CF3 pin; that is, an active low pulse has been generated. The bit is set even if the CF3 output is disabled by setting Bit 11 (CF3DIS) to 1 in the CFMODE register. The type of power used at the CF3 pin is determined by Bits[8:6] (CF3SEL) in the CFMODE register (see Table 34).
15	CF2		1: a high-to-low transition has occurred at the CF2 pin; that is, an active low pulse has been generated. The bit is set even if the CF2 output is disabled by setting Bit 10 (CF2DIS) to 1 in the CFMODE register. The type of power used at the CF2 pin is determined by Bit[5:3] (CF2SEL) in the CFMODE register (see Table 34).
14	CF1		1: a high-to-low transition has occurred at the CF1 pin; that is, an active low pulse has been generated. The bit is set even if the CF1 output is disabled by setting Bit 9 (CF1DIS) to 1 in the CFMODE register. The type of power used at the CF1 pin is determined by Bits[2:0] (CF1SEL) in the CFMODE register (see Table 34).
13	REVPSUM2	0	1: the sum of all phase powers in the CF2 datapath has changed sign. The sign itself is indicated in Bit 7 (SUM2SIGN) of the PHSIGN register (see Table 36).
[12:10]	Reserved	000	Reserved. These bits are always set to 0.
9	REVPSUM1	0	1: the sum of all phase powers in the CF1 datapath has changed sign. The sign itself is indicated in Bit 3 (SUM1SIGN) of the PHSIGN register (see Table 36).
8	REVAPC	0	1: Phase C total active power has changed sign. The sign itself is indicated in Bit 2 (CWSIGN) of the PHSIGN register (see Table 36).
7	REVAPB	0	1: Phase B total active power has changed sign. The sign itself is indicated in Bit 1 (BWSIGN) of the PHSIGN[15:0] register (see Table 36).
6	REVAPA	0	1: Phase A total active power has changed sign. The sign itself is indicated in Bit 0 (AWSIGN) of the PHSIGN register (see Table 36).
5	LENERGY	0	1: in line energy accumulation mode, it indicates the end of an integration over an integer number of half-line cycles set in the LINECYC register.
4	VAEHF	0	1: Bit 30 of any one of the apparent energy registers (AVAHR, BVAHR, or CVAHR) has changed.
[3:1]	Reserved	000	Reserved. These bits are always set to 0.
0	AEHF	0	1: Bit 30 of one of the total active energy registers (AWATTHR, BWATTHR, or CWATTHR) has changed.

Table 27. STATUS1 Register (Address 0xE503)

Bit	Bit Name	Default Value	Description
[31:25]	Reserved	000 0000	Reserved. These bits are always set to 0.
24	PKV	0	1: the period used to detect the peak value in the voltage channel has ended. The VPEAK register (Address 0xE501) contains the peak value and the phase where the peak has been detected (see Table 25).
23	PKI	0	1: the period used to detect the peak value in the current channel has ended. The IPEAK register (Address 0xE500) contains the peak value and the phase where the peak has been detected (see Table 24).
22	Reserved	0	Reserved.
21	Reserved	1	Reserved.
20	Reserved	0	Reserved. This bit is always set to 0.
19	SEQERR	0	1: a negative-to-positive zero crossing on the Phase A voltage was not followed by a negative-to-positive zero crossing on Phase B voltage but, instead, by a negative-to-positive zero crossing on the Phase C voltage.
18	OV	0	1: an overvoltage event has occurred on one of the phases indicated by Bits[11:9] (OVPHASE[2:0]) in the PHSTATUS register (see Table 30).
17	OI	0	1: an overcurrent event has occurred on one of the phases indicated by Bits[5:3] (OIPHASE[2:0]) in the PHSTATUS register (see Table 30).
16	SAG	0	1: a SAG event has occurred on one of the phases indicated by Bits[14:12] (VSPHASE[2:0]) in the PHSTATUS register (see Table 30).
15	RSTDONE	1	In case of a software reset command (that is, Bit 7 (SWRST) is set to 1 in the CONFIG register at Address 0xE618), a transition from PSM3 to PSM0, or a hardware reset, this bit is set to 1 at the end of the transition process and after all registers have changed value to their default. The $\overline{\text{IRQ1}}$ pin goes low to signal this event because this interrupt cannot be disabled.
14	ZXIC	0	1: a zero crossing is detected on the Phase C current.
13	ZXIB	0	1: a zero crossing is detected on the Phase B current.
12	ZXIA	0	1: a zero crossing is detected on the Phase A current.
11	ZXVC	0	1: a zero crossing is detected on the Phase C voltage.
10	ZXVB	0	1: a zero crossing is detected on the Phase B voltage.
9	ZXVA	0	1: a zero crossing is detected on the Phase A voltage.
8	ZXTOIC	0	1: a zero crossing on the Phase C current is missing.
7	ZXTOIB	0	1: a zero crossing on the Phase B current is missing.
6	ZXTOIA	0	1: a zero crossing on the Phase A current is missing.
5	ZXTOVC	0	1: a zero crossing on the Phase C voltage is missing.
4	ZXTOVB	0	1: a zero crossing on the Phase B voltage is missing.
3	ZXTOVA	0	1: a zero crossing on the Phase A voltage is missing.
2	VANLOAD	0	1: at least one phase has entered no-load condition based on apparent power. The phase is indicated in Bits[8:6] (VANLPHASE) in the PHNOLOAD register (see Table 31).
1	Reserved	0	This bit is always set to 0.
0	NLOAD	0	1: at least one phase has entered a no-load condition based on total active power. The phase is indicated in Bits[2:0] (NLPHASE) in the PHNOLOAD register (see Table 31).

Table 28. MASK0 Register (Address 0xE50A)

Bit	Bit Name	Default Value	Description
[31:19]	Reserved	00 0000 0000 0000	Reserved. These bits do not manage any functionality.
18	REVPSUM3	0	1: interrupt enabled when the sum of all phase powers in the CF3 datapath changes sign.
17	DREADY	0	1: interrupt enabled when all periodical (at 8 kHz rate) DSP computations finish.
16	CF3		1: interrupt enabled when a high-to-low transition occurs at the CF3 pin; that is, an active low pulse is generated. The interrupt can be enabled even if the CF3 output is disabled by setting Bit 11 (CF3DIS) to 1 in the CFMODE register. The type of power used at the CF3 pin is determined by Bits[8:6] (CF3SEL) in the CFMODE register (see Table 34).
15	CF2		1: interrupt enabled when a high-to-low transition occurs at CF2 pin; that is, an active low pulse is generated. The interrupt can be enabled even if the CF2 output is disabled by setting Bit 10 (CF2DIS) to 1 in the CFMODE register. The type of power used at the CF2 pin is determined by Bits[5:3] (CF2SEL) in the CFMODE register (see Table 34).
14	CF1		1: interrupt enabled when a high-to-low transition occurs at the CF1 pin; that is, an active low pulse is generated. The interrupt can be enabled even if the CF1 output is disabled by setting Bit 9 (CF1DIS) to 1 in the CFMODE register. The type of power used at the CF1 pin is determined by Bits[2:0] (CF1SEL) in the CFMODE register (see Table 34).
13	REVPSUM2	0	1: interrupt enabled when the sum of all phase powers in the CF2 datapath changes sign.
[12:10]	Reserved	000	Reserved. These bits do not manage any functionality.
9	REVPSUM1	0	1: interrupt enabled when the sum of all phase powers in the CF1 datapath changes sign.
8	REVAPC	0	1: interrupt enabled when the Phase C active power register changes sign.
7	REVAPB	0	1: interrupt enabled when the Phase B active power register changes sign.
6	REVAPA	0	1: interrupt enabled when the Phase A active power register changes sign.
5	LENERGY	0	1: in line energy accumulation mode, it enables an interrupt at the end of an integration over an integer number of half-line cycles set in the LINECYC register.
4	VAEHF	0	1: interrupt enabled when Bit 30 of any one of the apparent energy registers (AVAHR, BVAHR, or CVAHR) switches from 0 to 1 or vice versa.
[1:3]	Reserved	000	Reserved. These bits do not manage any functionality.
0	AEHF	0	When this bit is set to 1, it enables an interrupt when Bit 30 of any one of the total active energy registers (AWATTHR, BWATTHR, or CWATTHR) changes from 0 to 1 or vice versa.

Table 29. MASK1 Register (Address 0xE50B)

Bit	Bit Name	Default Value	Description
[31:25]	Reserved	000 0000	Reserved. These bits do not manage any functionality.
24	PKV	0	1: interrupt enabled when the period used to detect the peak value in the voltage channel has ended.
23	PKI	0	1: interrupt enabled when the period used to detect the peak value in the current channel has ended.
[20:22]	Reserved	000	Reserved. These bits do not manage any functionality.
19	SEQERR	0	1: interrupt enabled when a negative-to-positive zero crossing on Phase A voltage is not followed by a negative-to-positive zero crossing on Phase B voltage but, instead, by a negative-to-positive zero crossing on Phase C voltage.
18	OV	0	1: interrupt enabled when an overvoltage event occurs on one of the phases indicated by Bits[11:9] (OVPHASE[2:0]) in the PHSTATUS register (see Table 30).
17	OI	0	1: interrupt enabled when an overcurrent event occurs on one of the phases indicated by Bits[5:3] (OIPHASE[2:0]) in the PHSTATUS register (see Table 30).
16	SAG	0	1: interrupt enabled when a SAG event occurs on one of the phases indicated by Bits[14:12] (VSPHASE[2:0]) in the PHSTATUS register (see Table 30).
15	RSTDONE	0	Because the RSTDONE interrupt cannot be disabled, this bit does not have any functionality attached to it. It can be set to 1 or cleared to 0 without having any effect.
14	ZXIC	0	1: interrupt enabled when a zero crossing is detected on Phase C current.
13	ZXIB	0	1: interrupt enabled when a zero crossing is detected on Phase B current.
12	ZXIA	0	1: interrupt enabled when a zero crossing is detected on Phase A current.
11	ZXVC	0	1: interrupt enabled when a zero crossing is detected on Phase C voltage.
10	ZXVB	0	1: interrupt enabled when a zero crossing is detected on Phase B voltage.
9	ZXVA	0	1: interrupt enabled when a zero crossing is detected on Phase A voltage.
8	ZXTOIC	0	1: interrupt enabled when a zero crossing on Phase C current is missing.
7	ZXTOIB	0	1: interrupt enabled when a zero crossing on Phase B current is missing.
6	ZXTOIA	0	1: interrupt enabled when a zero crossing on Phase A current is missing.
5	ZXTOVC	0	1: interrupt enabled when a zero crossing on Phase C voltage is missing.
4	ZXTOVB	0	1: interrupt enabled when a zero crossing on Phase B voltage is missing.
3	ZXTOVA	0	1: interrupt enabled when a zero crossing on Phase A voltage is missing.
2	VANLOAD	0	1: interrupt enabled when at least one phase enters no-load condition based on apparent power.
1	Reserved	0	Reserved. This bit does not manage any functionality.
0	NLOAD	0	1: interrupt enabled when at least one phase enters no-load condition based on total active and reactive powers.

Table 30. PHSTATUS Register (Address 0xE600)

Bit	Bit Name	Default Value	Description
15	Reserved	0	Reserved. This bit is always set to 0.
14	VSPHASE[2]	0	When this bit is set to 1, Phase C voltage generated Status Bit 16 (SAG) in the STATUS1 register.
13	VSPHASE[1]	0	When this bit is set to 1, Phase B voltage generated Status Bit 16 (SAG) in the STATUS1 register.
12	VSPHASE[0]	0	When this bit is set to 1, Phase A voltage generated Status Bit 16 (SAG) in the STATUS1 register.
11	OVPHASE[2]	0	When this bit is set to 1, Phase C voltage generated Status Bit 18 (OV) in the STATUS1 register.
10	OVPHASE[1]	0	When this bit is set to 1, Phase B voltage generated Status Bit 18 (OV) in the STATUS1 register.
9	OVPHASE[0]	0	When this bit is set to 1, Phase A voltage generated Status Bit 18 (OV) in the STATUS1 register.
[8:6]	Reserved	000	Reserved. These bits are always set to 0.
5	OIPHASE[2]	0	When this bit is set to 1, Phase C current generated Status Bit 17 (OI) in the STATUS1 register.
4	OIPHASE[1]	0	When this bit is set to 1, Phase B current generated Status Bit 17 (OI) in the STATUS1 register.
3	OIPHASE[0]	0	When this bit is set to 1, Phase A current generated Status Bit 17 (OI) in the STATUS1 register.
[2:0]	Reserved	000	Reserved. These bits are always set to 0.

Table 31. PHNOLOAD Register (Address 0xE608)

Bit	Bit Name	Default Value	Description
[15:9]	Reserved	000 0000	Reserved. These bits are always set to 0.
8	VANLPHASE[2]	0	0: Phase C is out of no-load condition based on apparent power. 1: Phase C is in no-load condition based on apparent power. This bit is set together with Status Bit 2 (VANLOAD) in the STATUS1 register.
7	VANLPHASE[1]	0	0: Phase B is out of no-load condition based on apparent power. 1: Phase B is in no-load condition based on apparent power. This bit is set together with Status Bit 2 (VANLOAD) in the STATUS1 register.
6	VANLPHASE[0]	0	0: Phase A is out of no-load condition based on apparent power. 1: Phase A is in no-load condition based on apparent power. This bit is set together with Status Bit 2 (VANLOAD) in the STATUS1 register.
[3:5]	Reserved	000	Reserved. These bits are always set to 0.
2	NLPHASE[2]	0	0: Phase C is out of no-load condition based on total active powers. 1: Phase C is in no-load condition based on total active powers. This bit is set together with Status Bit 0 (NLOAD) in the STATUS1 register.
1	NLPHASE[1]	0	0: Phase B is out of no-load condition based on total active powers. 1: Phase B is in no-load condition based on total active powers. This bit is set together with Status Bit 0 (NLOAD) in the STATUS1 register.
0	NLPHASE[0]	0	0: Phase A is out of no-load condition based on total active powers. 1: Phase A is in no-load condition based on total active powers. This bit is set together with Status Bit 0 (NLOAD) in the STATUS1 register.

Table 32. COMPMODE Register (Address 0xE60E)

Bit	Bit Name	Default Value	Description
15	Reserved	0	Reserved. This bit does not manage any functionality.
14	Reserved	0	Reserved. This bit does not manage any functionality.
13	VNOMCEN	0	0: the apparent power on Phase C is computed regularly. 1: the apparent power on Phase C is computed using the VNOM register instead of the regular measured rms phase voltage.
12	VNOMBEN	0	0: the apparent power on Phase B is computed regularly. 1: the apparent power on Phase B is computed using the VNOM register instead of the regular measured rms phase voltage.
11	VNOMAEN	0	0: the apparent power on Phase A is computed regularly. 1: the apparent power on Phase A is computed using the VNOM register instead of the regular measured rms phase voltage.
[10:9]	ANGLESEL[1:0]	00	00: the angles between phase voltages and phase currents are measured. 01: the angles between phase voltages are measured. 10: the angles between phase currents are measured. 11: no angles are measured.
8	TERMSEL3[2]	1	Phase C is included in the CF3 output calculations.
7	TERMSEL3[1]	1	Phase B is included in the CF3 output calculations.
6	TERMSEL3[0]	1	Setting all TERMSEL3[2:0] bits to 1 signifies that the sum of all three phases is included in the CF3 output. Phase A is included in the the CF3 output calculations.
5	TERMSEL2[2]	1	Phase C is included in the CF2 output calculations.
4	TERMSEL2[1]	1	Phase B is included in the CF2 output calculations.
3	TERMSEL2[0]	1	Setting all TERMSEL2[2:0] bits to 1 signifies that the sum of all three phases is included in the CF2 output. Phase A is included in the CF2 output calculations.
2	TERMSEL1[2]	1	Phase C is included in the CF1 output calculations.
1	TERMSEL1[1]	1	Phase B is included in the CF1 output calculations.
0	TERMSEL1[0]	1	Setting all TERMSEL1[2:0] bits to 1 signifies that the sum of all three phases is included in the CF1 output. Phase A is included in the CF1 output calculations.

Table 33. GAIN Register (Address 0xE60F)

Bit	Bit Name	Default Value	Description
[15:9]	Reserved	000 0000	Reserved. These bits do not manage any functionality.
[8:6]	PGA3	000	Phase voltage gain selection. 000: gain = 1. 001: gain = 2. 010: gain = 4. 011: gain = 8. 100: gain = 16. 101, 110, 111: reserved. When set, the ADE7854 behaves as though PGA3 = 000.
[5:3]	Reserved	000	Reserved. These bits do not manage any functionality.
[2:0]	PGA1	000	Phase current gain selection. 000: gain = 1. 001: gain = 2. 010: gain = 4. 011: gain = 8. 100: gain = 16. 101, 110, 111: reserved. When set, the ADE7854 behaves as though PGA1 = 000.

Table 34. CFMODE Register (Address 0xE610)

Bit	Bit Name	Default Value	Description
15	Reserved	0	Reserved. This bit does not manage any functionality.
14	CF3LATCH	0	1: the content of the corresponding energy registers is latched when a CF3 pulse is generated (see the Synchronizing Energy Registers with the CFx Outputs section).
13	CF2LATCH	0	1: the content of the corresponding energy registers is latched when a CF2 pulse is generated (see the Synchronizing Energy Registers with the CFx Outputs section).
12	CF1LATCH	0	1: the content of the corresponding energy registers is latched when a CF1 pulse is generated (see the Synchronizing Energy Registers with the CFx Outputs section).
11	CF3DIS	1	1: the CF3 output is disabled. However, the respective digital-to-frequency converter remains enabled. 0: the CF3 output is enabled.
10	CF2DIS	1	1: the CF2 output is disabled. However, the respective digital-to-frequency converter remains enabled. 0: the CF2 output is enabled.
9	CF1DIS	1	1: the CF1 output is disabled. However, the respective digital-to-frequency converter remains enabled. 0: the CF1 output is enabled.
[8:6]	CF3SEL	010	000: the CF3 frequency is proportional to the sum of total active powers on each phase that is identified by Bits[8:6] (TERMSEL3) in the COMPMODE register. 001: if selected, the CF3 pin is set low permanently. 010: the CF3 frequency is proportional to the sum of the apparent powers on each phase that is identified by Bits[8:6] (TERMSEL3) in the COMPMODE register. 011,100: if selected, the CF3 pin is set low permanently. 101,110,111: reserved. When set, the ADE7854 behaves as though CF3SEL[2:0] = 000.
[5:3]	CF2SEL	001	000: the CF2 frequency is proportional to the sum of the total active powers on each phase that is identified by Bits[5:3] (TERMSEL2) in the COMPMODE register. 001: if selected, the CF2 pin is set low permanently. 010: the CF2 frequency is proportional to the sum of the apparent powers on each phase that is identified by Bits[5:3] (TERMSEL2) in the COMPMODE register. 011, 100: if selected, the CF2 pin is set low permanently. 101, 110, 111: reserved. When set, the ADE7854 behaves as though CF2SEL[2:0] = 000.
[2:0]	CF1SEL	000	000: the CF1 frequency is proportional to the sum of the total active power on each phase that is identified by Bits[2:0] (TERMSEL1) in the COMPMODE register. 001: if selected, the CF1 pin is set low permanently. 010: the CF1 frequency is proportional to the sum of the apparent power on each phase that is identified by Bits[2:0] (TERMSEL1) in the COMPMODE register. 011, 100: if selected, the CF1 pin is set low permanently. 101, 110, 111: reserved. When set, the ADE7854 behaves as though CF1SEL[2:0] = 000.

Table 35. APHCAL, BPHCAL, CPHCAL Registers (Address 0xE614, Address 0xE615, and Address 0xE616)

Bit	Bit Name	Default Value	Description
[15:10]	Reserved	000000	Reserved. These bits do not manage any functionality.
[9:0]	xPHCALVAL	0000000000	If current channel compensation is necessary, these bits can vary only between 0 and 383. If voltage channel compensation is necessary, these bits can vary only between 512 and 575. If the xPHCALVAL bits are set with numbers between 384 and 511, the compensation behaves as though the xPHCALVAL bits are set between 256 and 383. If the xPHCALVAL bits are set with numbers between 512 and 1023, the compensation behaves as though the xPHCALVAL bits are set between 384 and 511.

Table 36. PHSIGN Register (Address 0xE617)

Bit	Bit Name	Default Value	Description
[15:9]	Reserved	000 0000	Reserved. These bits are always set to 0.
8	SUM3SIGN	0	0: the sum of all phase powers in the CF3 datapath is positive. 1: the sum of all phase powers in the CF3 datapath is negative. Phase powers in the CF3 datapath are identified by Bits[8:6] (TERMSEL3) of the COMPMODE register (Address 0xE60E) and by Bits[8:6] (CF3SEL) of the CFMODE register (Address 0xE610).
7	SUM2SIGN	0	0: the sum of all phase powers in the CF2 datapath is positive. 1: the sum of all phase powers in the CF2 datapath is negative. Phase powers in the CF2 datapath are identified by Bits[5:3] (TERMSEL2) of the COMPMODE register (Address 0xE60E) and by Bits[5:3] (CF2SEL) of the CFMODE register (Address 0xE610).
[6:4]	Reserved	000	Reserved. These bits are always set to 0.
3	SUM1SIGN	0	0: the sum of all phase powers in the CF1 datapath is positive. 1: the sum of all phase powers in the CF1 datapath is negative. Phase powers in the CF1 datapath are identified by Bits[2:0] (TERMSEL1) of the COMPMODE register (Address 0xE60E) and by Bits[2:0] (CF1SEL) of the CFMODE register (Address 0xE610).
2	CWSIGN	0	0: total active power on Phase C is positive. 1: total active power identified on Phase C is negative.
1	BWSIGN	0	0: total active power on Phase B is positive. 1: total active power on Phase B is negative.
0	AWSIGN	0	0: total active power on Phase A is positive. 1: total active power on Phase A is negative.

Table 37. CONFIG Register (Address 0xE618)

Bit	Bit Name	Default Value	Description
[15:14]	Reserved	0	Reserved. These bits do not manage any functionality.
[13:12]	VTOIC	00	These bits decide which phase voltage is considered together with the Phase C current in the power path. 00 = Phase C voltage. 01 = Phase A voltage. 10 = Phase B voltage. 11 = reserved. When set, the ADE7854 behaves as though VTOIC = 00.
[11:10]	VTOIB	00	These bits decide which phase voltage is considered together with the Phase B current in the power path. 00 = Phase B voltage. 01 = Phase C voltage. 10 = Phase A voltage. 11 = reserved. When set, the ADE7854 behaves as though VTOIB = 00.
[9:8]	VTOIA	00	These bits decide which phase voltage is considered together with the Phase A current in the power path. 00 = Phase A voltage. 01 = Phase B voltage. 10 = Phase C voltage. 11 = reserved. When set, the ADE7854 behaves as though VTOIA = 00.
7	SWRST	0	1: initiates a software reset.

Bit	Bit Name	Default Value	Description
6	HSDCEN	0	1: the HSDC serial port is enabled, and HSCLK functionality is chosen at the CF3/HSCLK pin. 0: HSDC is disabled and CF3 functionality is chosen at the CF3/HSCLK pin.
5	MOD2SHORT	0	1: the current channel ADCs behave as though the voltage inputs are connected to ground.
4	MOD1SHORT	0	1: the voltage channel ADCs behave as though the voltage inputs are connected to ground.
3	SWAP	0	1: the voltage channel outputs are swapped with the current channel outputs. Thus, the current channel information is present in the voltage channel registers, and vice versa.
[2:1]	Reserved	000	Reserved. These bits do not manage any functionality.
0	INTEN	0	Integrator enable. 1: the internal digital integrator is enabled for use in meters utilizing Rogowski coils on all 3-phase current inputs. 0: the internal digital integrator is disabled.

Table 38. MMODE Register (Address 0xE700)

Bit	Bit Name	Default Value	Description
[7:5]	Reserved	000	Reserved. These bits do not manage any functionality.
4	PEAKSEL[2]	1	1: Phase C is selected for the voltage and current peak registers.
3	PEAKSEL[1]	1	1: Phase B is selected for the voltage and current peak registers.
2	PEAKSEL[0]	1	1: Phase A is selected for the voltage and current peak registers. The PEAKSEL[2:0] bits can all be set to 1 simultaneously to allow peak detection on all three phases at the same time. If more than one of the PEAKSEL[2:0] bits are set to 1, the peak measurement period indicated in the PEAKCYC register (Address 0xE703) decreases accordingly because zero crossings are detected on more than one phase.
[1:0]	PERSEL	00	00: Phase A is selected as the source of the voltage line period measurement. 01: Phase B is selected as the source of the voltage line period measurement. 10: Phase C is selected as the source of the voltage line period measurement. 11: reserved. When set, the ADE7854 behaves as though PERSEL = 00.

Table 39. ACCMODE Register (Address 0xE701)

Bit	Bit Name	Default Value	Description				
[7:6]	Reserved	00	Reserved. These bits should be kept at 00 for proper operation.				
[5:4]	CONSEL	00	These bits are used to select the inputs to the energy accumulation registers. 00: 3-phase, 4-wire system with three voltage sensors. 01: 3-phase, 3-wire delta connection. 10: 3-phase, 4-wire system with two voltage sensors. 11: 3-phase, 4-wire delta connection.				
			Energy Registers	**CONSEL = 00**	**CONSEL = 01**	**CONSEL = 10**	**CONSEL = 11**
			AWATTHR	$VA \times IA$	$VA \times IA$	$VA \times IA$	$VA \times IA$
			BWATTHR	$VB \times IB$	0	$VB = -VA - VC$ $VB \times IB$	$VB = -VA$ $VB \times IB$
			CWATTHR	$VC \times IC$	$VC \times IC$	$VC \times IC$	$VC \times IC$
			AVAHR	$VA_{rms} \times IA_{rms}$	$VA_{rms} \times IA_{rms}$	$VA_{rms} \times IA_{rms}$	$VA_{rms} \times IA_{rms}$
			BVAHR	$VB_{rms} \times IB_{rms}$	0	$VB_{rms} \times IB_{rms}$	$VB_{rms} \times IB_{rms}$
			CVAHR	$VC_{rms} \times IC_{rms}$	$VC_{rms} \times IC_{rms}$	$VC_{rms} \times IC_{rms}$	$VC_{rms} \times IC_{rms}$
[3:2]	Reserved	00	Reserved. These bits do not manage any functionality.				
[1:0]	WATTACC	00	00: signed accumulation mode of the total active powers. 01: reserved. When set, the ADE7854 behaves as though WATTACC = 00. 10: reserved. When set, the ADE7854 behaves as though WATTACC =00. 11: absolute accumulation mode of the total active powers.				

Table 40. LCYCMODE Register (Address 0xE702)

Bit	Bit Name	Default Value	Description
7	Reserved	0	Reserved. This bit does not manage any functionality.
6	RSTREAD	1	0: read-with-reset function of the xWATTHR and xVAHR registers is disabled. This bit should be cleared to 0 when Bit 2 or Bit 0 (LVA or LWATT) is set to 1. 1: read-with-reset of all xWATTHR and xVAHR registers is enabled. A read of these registers resets them to 0.
5	ZXSEL[2]	1	0: Phase C is not selected for zero-crossing counts in the line cycle accumulation mode. 1: Phase C is selected for zero-crossing counts in the line cycle accumulation mode.
4	ZXSEL[1]	1	0: Phase B is not selected for zero-crossing counts in the line cycle accumulation mode. 1: Phase B is selected for zero-crossing counts in the line cycle accumulation mode.
3	ZXSEL[0]	1	0: Phase A is not selected for zero-crossing counts in the line cycle accumulation mode. 1: Phase A is selected for zero-crossing counts in the line cycle accumulation mode. If more than one phase is selected for zero-crossing detection, the accumulation time is shortened accordingly.
2	LVA	0	0: the VA-hr accumulation registers (AVAHR, BVAHR, and CVAHR) are placed in regular accumulation mode. 1: the VA-hr accumulation registers (AVAHR, BVAHR, and CVAHR) are placed into line-cycle accumulation mode.
1	Reserved	0	Reserved. This bit does not manage any functionality.
0	LWATT	0	0: the watt-hr accumulation registers (AWATTHR, BWATTHR, and CWATTHR) are placed in regular accumulation mode. 1: the watt-hr accumulation registers (AWATTHR, BWATTHR, and CWATTHR) are placed in line cycle accumulation mode.

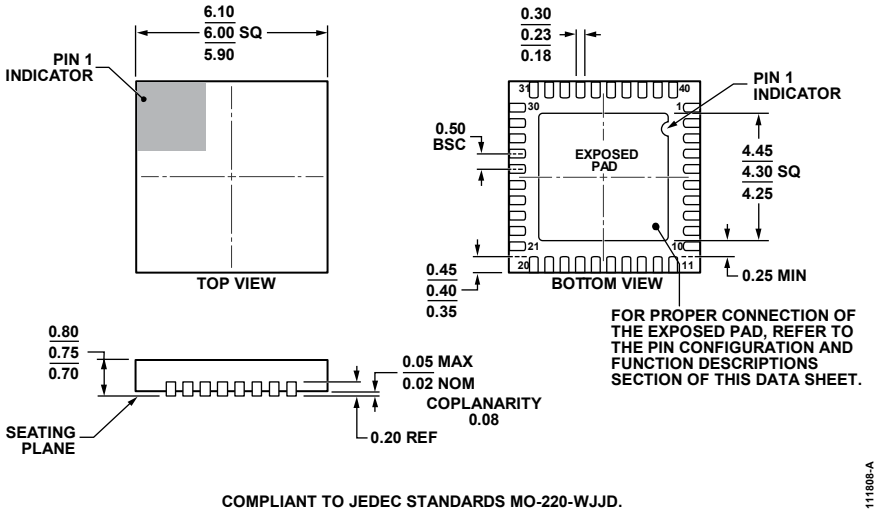
Table 41. HSDC_CFG Register (Address 0xE706)

Bit	Bit Name	Default Value	Description
[7:6]	Reserved	00	These bits do not manage any functionality.
5	HSAPOL	0	0: the HSACTIVE output pin is active low. 1: the HSACTIVE output pin is active high.
[4:3]	HXFER	00	00: HSDC transmits 16 32-bit words in the following order: IAWV, VAWV, IBWV, VBWV, ICWV, VCWV, one 32-bit word equal to 0, AVA, BVA, CVA, AWATT, BWATT, CWATT, and three 32-bit words that are equal to 0. 01: HSDC transmits the six instantaneous values of currents and voltages plus one 32-bit word that is always equal to 0 in the following order: IAWV, VAWV, IBWV, VBWV, ICWV, VCWV, and one 32-bit word equal to 0. 10: HSDC transmits six instantaneous values of phase powers plus three 32-bit words that are always equal to 0 in the following order: AVA, BVA, CVA, AWATT, BWATT, CWATT, and three 32-bit words that are equal to 0. 11: reserved. If set, the ADE7854 behaves as though HXFER = 00.
2	HGAP	0	0: no gap is introduced between packages. 1: a gap of seven HCLK cycles is introduced between packages.
1	HSIZE	0	0: HSDC transmits the 32-bit registers in 32-bit packages, MSB first. 1: HSDC transmits the 32-bit registers in 8-bit packages, MSB first.
0	HCLK	0	0: HSCLK = 8 MHz. 1: HSCLK = 4 MHz.

Table 42. CONFIG2 Register (Address 0xEC01)

Bit	Bit Name	Default Value	Description
[7:2]	Reserved	00000	Reserved. These bits do not manage any functionality.
1	I2C_LOCK	0	When this bit is set to 0, the $\overline{SS}$/HSA pin can be toggled three times to activate the SPI port. If I^2C is the active serial port, this bit must be set to 1 to lock it in. From then on, spurious togglings of the $\overline{SS}$ pin and an eventual switch to the SPI port are no longer possible. If SPI is the active serial port, any write to the CONFIG2 register locks the port. From then on, a switch to the I^2C port is no longer possible. Once locked, the serial port choice is maintained when the ADE7854 switches between the PSM0 and PSM3 power modes.
0	EXTREFEN	0	0: the internal voltage reference is used in the ADCs. 1: an external reference is connected to Pin 17 ($REF_{IN/OUT}$)

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WJJD.

Figure 94. 40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
6 mm × 6 mm Body, Very Very Thin Quad
(CP-40-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADE7854ACPZ[1]	−40°C to +85°C	40-Lead LFCSP_WQ	CP-40-10
ADE7854ACPZ-RL[1]	−40°C to +85°C	40-Lead LFCSP_WQ, 13″Tape & Reel	CP-40-10
EVAL-ADE7854EBZ[1]		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

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D08017-0-8/09(PrD)

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