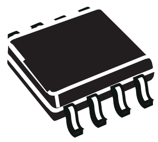
LED5000

3 A monolithic step-down current source with dimming capability

Datasheet - production data



HSOP8

Applications

- High brightness LED driving
- Street lighting
- Signage
- Halogen bulb replacement
- General lighting

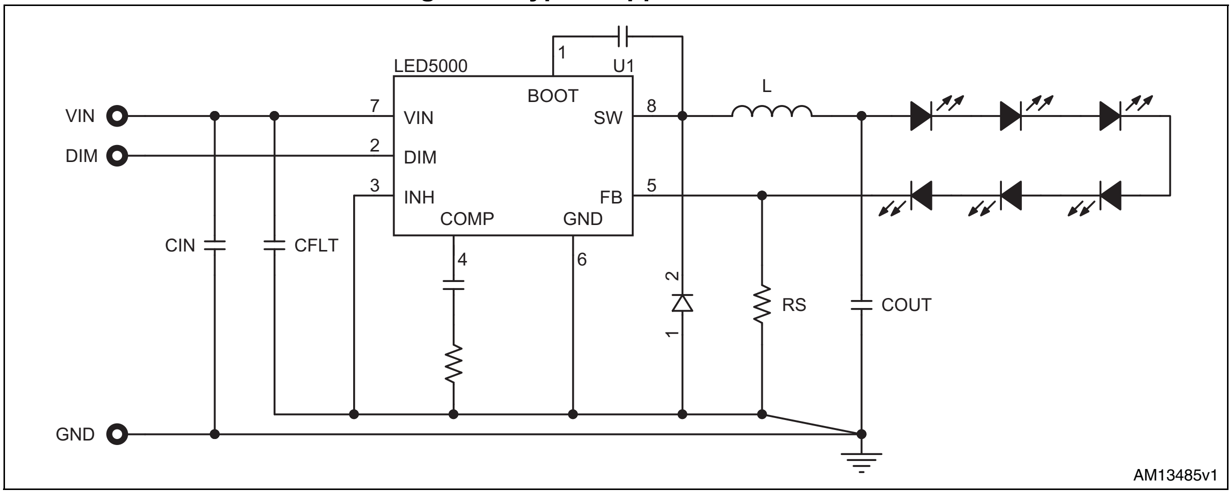
Features

- 5.5 V to 48 V operating input voltage range
- 850 kHz fixed switching frequency
- 200 mV typ. current sense voltage drop
- Buck / buck-boost / floating boost topologies
- PWM dimming
- ± 3% output current accuracy overtemperature
- 200 mΩ typical R_{DSON}
- Peak current mode architecture
- Short-circuit protection
- Compliant with ceramic output capacitors
- Inhibit for zero current consumption
- Thermal shutdown

Description

The LED5000 device is an 850 kHz fixed switching frequency monolithic step-down DC-DC converter designed to operate as a precise constant current source with an adjustable current capability up to 3 A DC. The embedded PWM dimming circuitry features LED brightness control. The regulated output current level is set by connecting a sensing resistor to the feedback pin. The 200 mV typical R_{SENSE} voltage drop enhances performance in terms of efficiency. The size of the overall application is minimized thanks to the high switching frequency and its compatibility with ceramic output capacitors. The device is fully protected against overheating, overcurrent and output short-circuit. The LED5000 is available in an HSOP8 package.

Figure 1. Typical application circuit



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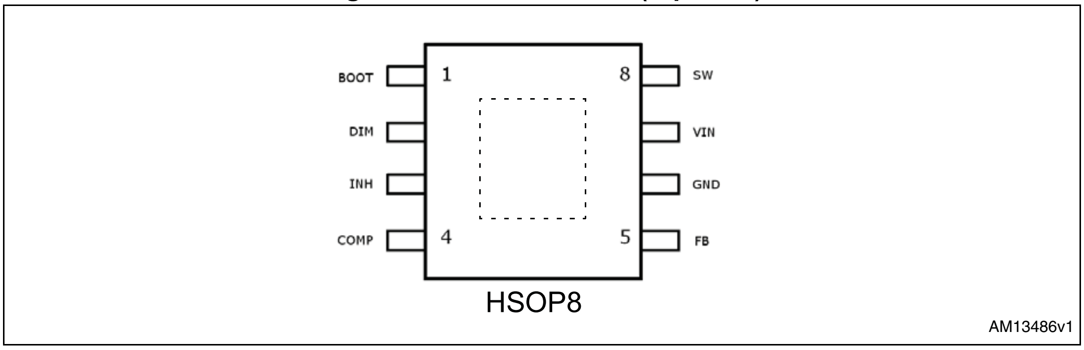
1 Pin settings

1.1 Pin connection

Figure 2. Pin connection (top view)



1.2 Pin description

Table 1. Pin description

	Type	Description
1	BOOT	Analog circuitry power supply connection
2	DIM	Dimming control input. Logic low prevents the switching activity, logic high enables it. A square wave on this pin implements LEDs current PWM dimming. Connect to VIN if not used (see *Section 5.8 on page 22*).
3	INH	Inhibit pin. Connect to GND if not used.
4	COMP	Analog circuitry
5	FB	Feedback input. Connect a proper sensing resistor to set the LED current.
6	GND	Ground connection
7	VIN	Power input voltage
8	SW	Switching node
-	e.p.	Exposed pad to be connected to GND to increase the package thermal performance and the device noise immunity.

2 Maximum ratings

2.1 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	Power supply input voltage	-0.3 to 52	V
V_{INH}	Inhibit input	-0.3 to 7	V
V_{DIM}	Dimming input	-0.3 to (V_{IN} + 0.3)	V
V_{COMP}	Comp output	-0.3 to 3	V
BOOT	Bootstrap pin	-0.3 to 55	V
SW	Switching node	-1 to (V_{IN} + 0.3)	V
V_{FB}	Feedback voltage	-0.3 to 3	V
T_J	Operating junction temperature range	-40 to 150	°C
T_{STG}	Storage temperature range	-65 to 150	°C
T_{LEAD}	Lead temperature (soldering 10 sec.)	260	°C

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ JA}$(1)	Thermal resistance junction ambient	40	°C/W

1. Device soldered to the STEVAL-ILL056V1 demonstration board.

2.3 ESD protection

Table 4. ESD protection

Symbol	Test condition	Value	Unit
ESD	HBM	4	KV
	MM	500	V

3 Electrical characteristics

All tests performed at T_J = 25 °C, V_{CC} = 12 V, V_{INH} = 0 V unless otherwise specified. The specification is guaranteed from -40 to +125 °C - T_J temperature range by design, characterization and statistical correlation.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage range			5.5		48	V
$R_{DS(on)}$	MOSFET on resistance	I_{SW} = 1 A			0.2	0.4	Ω
I_{SW}	Maximum limiting current			3.7	4.5	5.2	A
t_{HICCUP}	Hiccup time				16		ms
f_{SW}	Switching frequency			600	850	1000	kHz
	Duty cycle		(1)		90		%
$T_{ON\ MIN}$	Minimum conduction time of the power element		(1)		90		ns
$T_{OFF\ MIN}$	Minimum conduction time of the external diode		(1)	75	90	120	ns
DC characteristics							
V_{FB}	Voltage feedback			194	200	206	mV
I_{FB}	FB biasing current				50		nA
I_q	Quiescent current	V_{DIM} > 1.5 V			1.3	2	mA
		V_{DIM} > 1.5 V, V_{IN} = 48 V			1.7	2.4	mA
$I_{qst\text{-}by}$	Standby quiescent current	V_{INH} > 1.5 V		12	16	34	µA
Inhibit							
V_{INH}	Inhibit levels	Device ON V_{IN} = 5.5 V to 48 V				0.5	V
		Device OFF V_{IN} = 5.5 V to 48 V		1.5			V
I_{INH}	Inhibit biasing current	V_{INH} = 5 V		0.7	1.6	2.5	µA
Dimming							
V_{DIM}	Dimming levels	Switching activity V_{IN} = 5.5 V to 48 V		2.2			V
		Switching activity prevented V_{IN} = 5.5 V to 48 V				0.5	V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
Error amplifier							
V_{OH}	High level output voltage	V_{FB} = 0 V		3			V
V_{OL}	Low level output voltage	V_{FB} = 400 mV				150	mV
$I_{o\ source}$	Source output current	V_{COMP} = 1.5 V; V_{FB} = 0 V		16	23	30	µA
$I_{o\ sink}$	Sink output current	V_{COMP} = 1.5 V; V_{FB} = 0.4 V		16	23	30	µA
Ib	Source bias current	V_{FB} = 250 mV			50		nA
	DC open loop gain	$R_L = \infty$	(1)		90		dB
gm	Transconductance	I_{COMP} = TBD; V_{COMP} = TBD			220		µS
Thermal shutdown							
T_{SHDWN}	Thermal shutdown temperature		(1)	140	150	160	°C
T_{HYS}	Thermal shutdown hysteresis		(1)		15		°C

1. Parameter guaranteed by design.

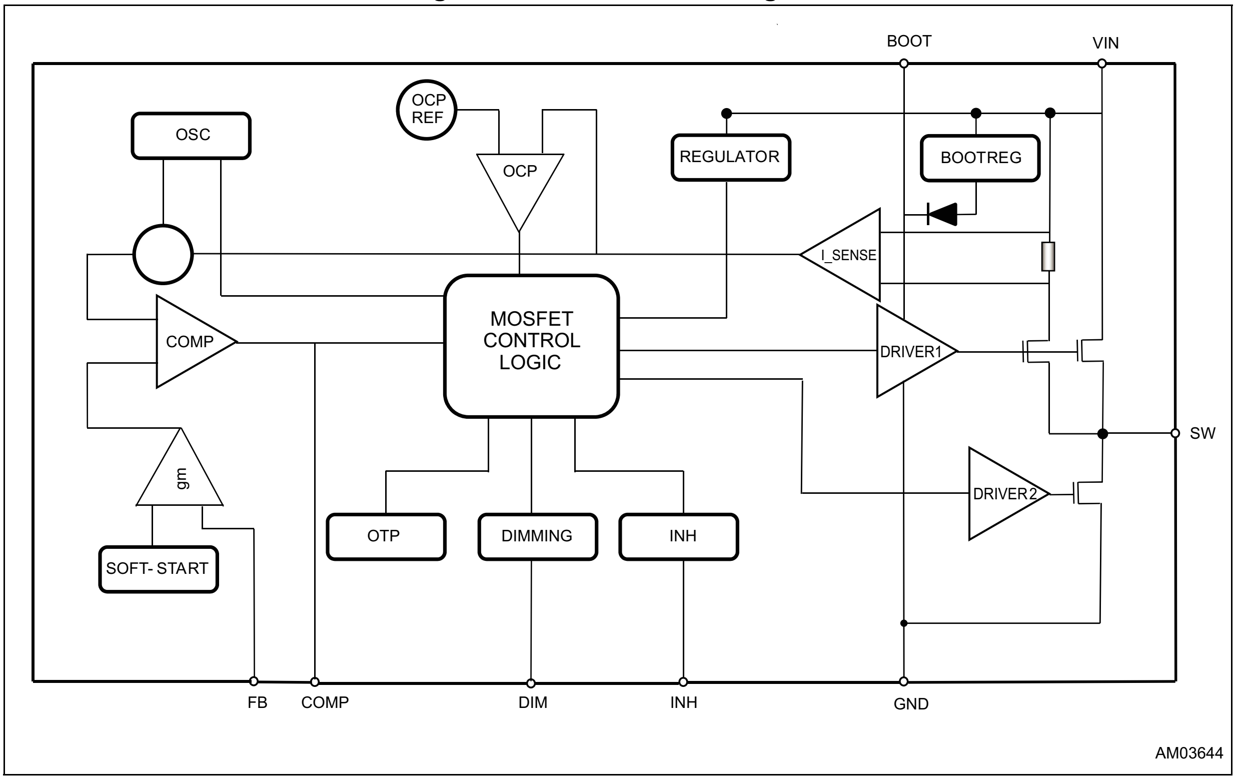
4 Functional description

The LED5000 is based on a “peak current mode” architecture with fixed frequency control. As a consequence the intersection between the error amplifier output and the sensed inductor current generates the control signal to drive the power switch.

The main internal blocks shown in the block diagram in *Figure 3* are:

- A fully integrated sawtooth oscillator with a typical frequency of 850 kHz
- A transconductance error amplifier
- A high side current sense amplifier to track the inductor current
- A pulse width modulator (PWM) comparator and the circuitry necessary to drive the internal power element
- The soft-start circuitry to decrease the inrush current at power-up
- The dimming block to implement PWM dimming
- The inhibit block for standby operation
- The current limitation circuit based on the pulse-by-pulse current and the HICCUP protection
- The bootstrap circuitry to drive the embedded NMOS switch
- A circuit to implement the thermal protection function

Figure 3. LED5000 block diagram



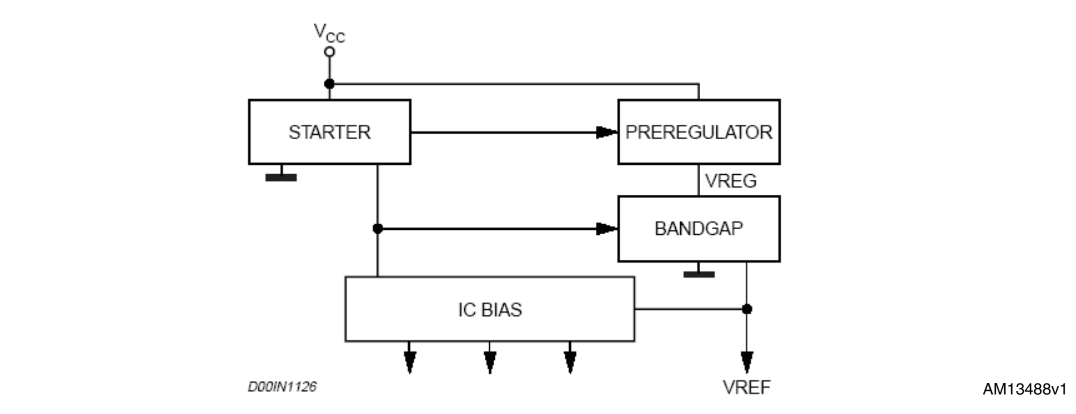
4.1 Power supply and voltage reference

The internal regulator circuit consists of a startup circuit, an internal voltage pre-regulator, the bandgap voltage reference and the bias block that provides current to all the blocks. The starter supplies the startup current to the entire device when the input voltage goes high and the device is enabled (inhibit pin connected to ground). The pre-regulator block supplies the bandgap cell with a pre-regulated voltage that has a very low supply voltage noise sensitivity.

4.2 Voltage monitor

An internal block continuously senses the V_{cc}, V_{ref} and V_{bg}. If the monitored voltages are good, the regulator begins operating. There is also a hysteresis on the V_{cc}(UVLO).

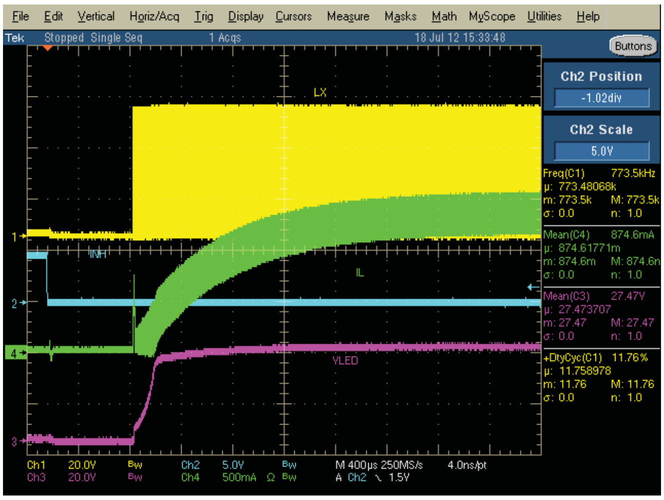
Figure 4. Internal circuit



4.3 Soft-start

The startup phase is implemented ramping the reference of the embedded error amplifier in 1 msec typ. time. It minimizes the inrush current and decreases the stress of the power components at power up.

Figure 5. Soft-start open



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During normal operation a new soft-start cycle takes place in case of:

- thermal shutdown event
- UVLO event

The soft-start is disabled during the dimming operation to maximize the dimming performance.

4.4 Dimming block

The DIM input features the LED brightness control with the PWM dimming operation (see *Section 5.8 on page 22*).

4.5 Inhibit block

The inhibit block features the standby mode accordingly with *Table 5: Electrical characteristics on page 8*. The INH pin high level disables the device so the power consumption is reduced to less than 40 µA. The INH pin is 5 V tolerant.

4.6 Error amplifier

The voltage error amplifier is the core of the loop regulation. It is a transconductance operational amplifier whose non inverting input is connected to the internal voltage reference (200 mV), while the inverting input (FB) is connected to the output current sensing resistor.

Table 6. Uncompensated error amplifier characteristics

Description	Values
Transconductance	220 µS
Low frequency gain	90 dB

The error amplifier output is compared with the inductor current sense information to perform PWM control.

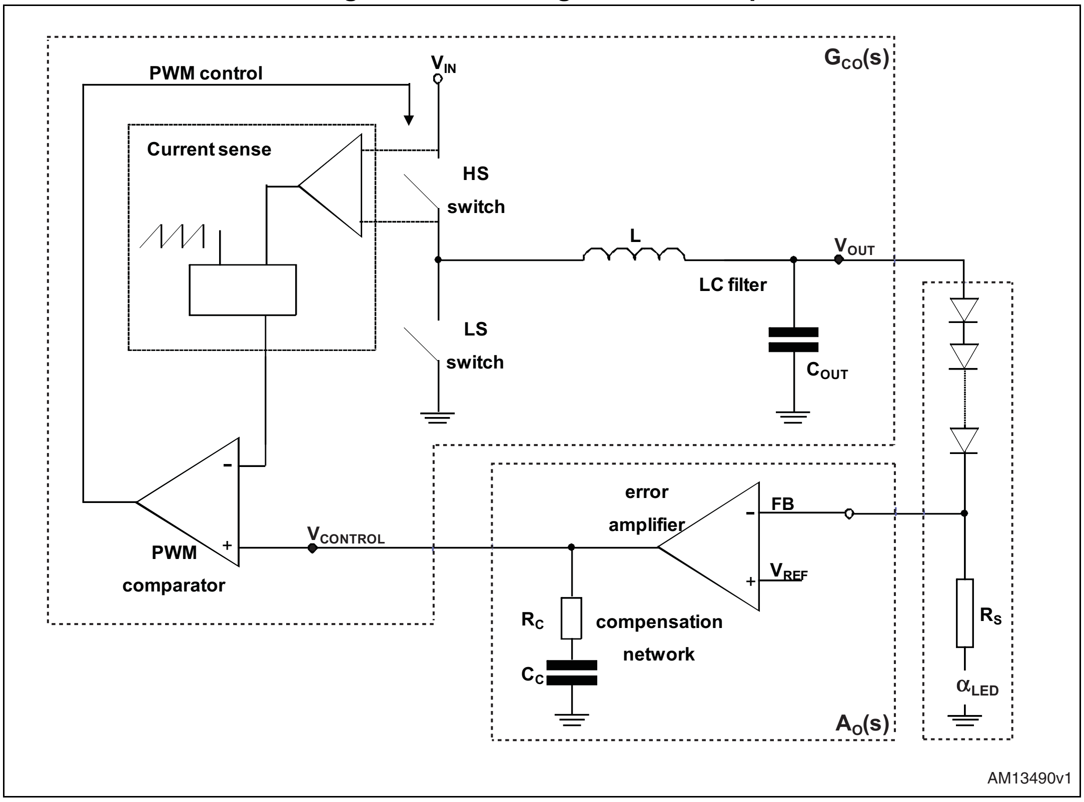
4.7 Thermal shutdown

The shutdown block generates a signal that disables the power stage if the temperature of the chip goes higher than a fixed internal threshold (150 ± 10 °C typical). The sensing element of the chip is close to the PDMOS area, ensuring fast and accurate temperature detection. A 15 °C typical hysteresis prevents the device from turning ON and OFF continuously during the protection operation.

5 Application notes - buck conversion

5.1 Closing the loop

Figure 6. Block diagram of the loop



5.2 $G_{CO}(s)$ control to output transfer function

The accurate control to output transfer function for a buck peak current mode converter can be written as:

Equation 1

$$G_{CO}(s) = \frac{R_{LOAD}}{R_{CS}} \cdot \frac{1}{1 + \frac{R_0 \cdot T_{SW}}{L} \cdot [m_C \cdot (1 - D) - 0.5]} \cdot \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_p}\right)} \cdot F_H(s)$$

where R_{LOAD} represents the load resistance (see Section 5.4 on page 18), R_{CS} the equivalent sensing resistor of the current sense circuitry equal to 0.38, ω_p the single pole introduced by the LC filter and ω_z the zero given by the ESR of the output capacitor.

$F_H(s)$ accounts the sampling effect performed by the PWM comparator on the output of the error amplifier that introduces a double pole at one half of the switching frequency.

Equation 2

$$\omega_Z = \frac{1}{ESR \cdot C_{OUT}}$$

where *ESR* is the equivalent series resistor to the output capacitor.

Equation 3

$$\omega_P = \frac{1}{R_{LOAD} \cdot C_{OUT}} + \frac{m_C \cdot (1 - D) - 0.5}{L \cdot C_{OUT} \cdot f_{SW}}$$

where:

Equation 4

$$\begin{cases} m_C = 1 + \frac{S_e}{S_n} \\ S_e = V_{pp} \cdot f_{SW} \\ S_n = \frac{V_{IN} - V_{OUT}}{L} \cdot R_{CS} \end{cases}$$

S_n represents the slope of the sensed inductor current, S_e the slope of the external ramp (V_{PP} peak to peak amplitude equal to 1.2 V) that implements the slope compensation to avoid sub-harmonic oscillations at duty cycle over 50%.

The sampling effect contribution $F_H(s)$ is:

Equation 5

$$F_H(s) = \frac{1}{1 + \frac{s}{\omega_n \cdot Q_P} + \frac{s^2}{\omega_n^2}}$$

where:

Equation 6

$$\omega_n = \pi \cdot f_{SW}$$

and

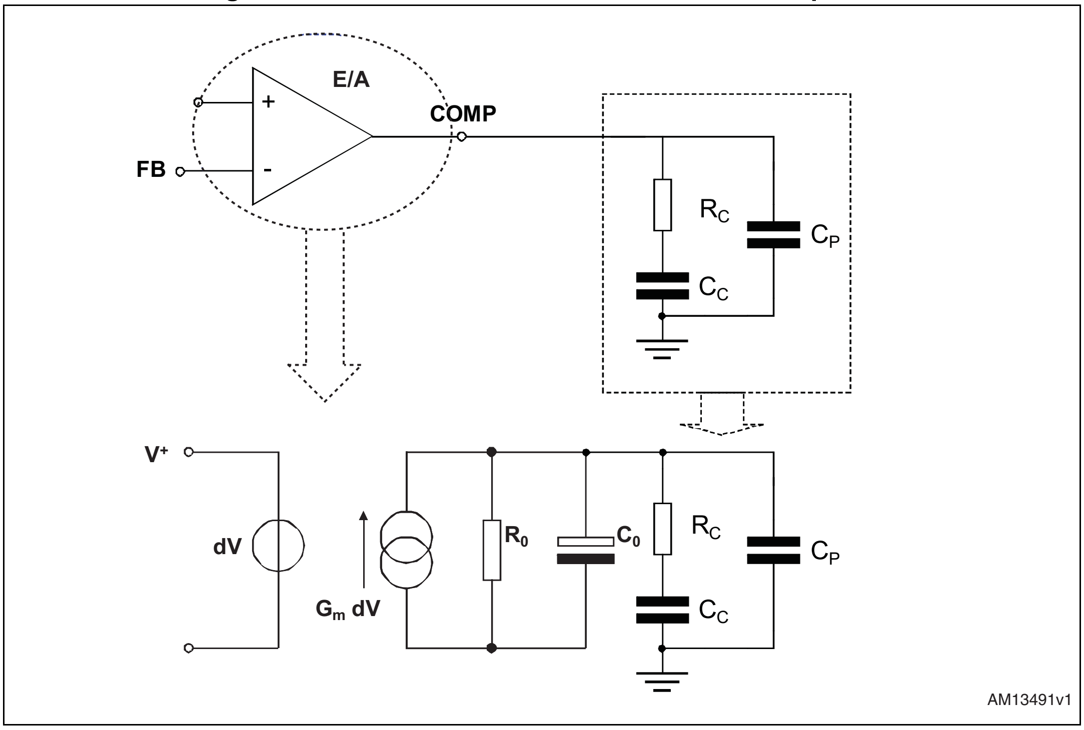
Equation 7

$$Q_P = \frac{1}{\pi \cdot [m_C \cdot (1 - D) - 0.5]}$$

5.3 Error amplifier compensation network

The external compensation network connected at the output of the error amplifier is dimensioned to stabilize the system depending on the application conditions.

Figure 7. Transconductance embedded error amplifier



R_C and C_C introduce a pole and a zero in the open loop gain. C_P does not significantly affect system stability but it can be useful to reduce the noise at the output of the error amplifier.

The transfer function of the error amplifier and its compensation network is:

Equation 8

$$A_0(s) = \frac{A_{V0} \cdot (1 + s \cdot R_c \cdot C_c)}{s^2 \cdot R_0 \cdot (C_0 + C_p) \cdot R_c \cdot C_c + s \cdot (R_0 \cdot C_c + R_0 \cdot (C_0 + C_p) + R_c \cdot C_c) + 1}$$

Where $A_{V0} = G_m \cdot R_0$ (R_O = output resistor of OTA = 200 * 10 ^ 6 Ω).

The poles of this transfer function are (if $C_c >> C_0 + C_P$):

Equation 9

$$f_{P\,LF} = \frac{1}{2 \cdot \pi \cdot R_0 \cdot C_c}$$

Equation 10

$$f_{P\,HF} = \frac{1}{2 \cdot \pi \cdot R_c \cdot (C_0 + C_p)}$$

whereas the zero is defined as:

Equation 11

$$F_Z = \frac{1}{2 \cdot \pi \cdot R_c \cdot C_c}$$

5.4 LED small signal model

Once the system reaches the working condition the LEDs composing the row are biased and their equivalent circuit can be considered as a resistor for frequencies << 1 MHz.

The LED manufacturer typically provides the equivalent dynamic resistance of the LED biased at a different DC current. This parameter is required to study the behavior of the system in the small signal analysis.

For instance, the equivalent dynamic resistance of Luxeon III Star from Lumiled measured with different biasing current levels is reported below:

$$r_{LED} \quad \begin{cases} 1.3\Omega & I_{LED} = 350mA \\ 0.9\Omega & I_{LED} = 700mA \end{cases}$$

In case the LED datasheet does not provide the equivalent resistor value, it can be easily derived as the tangent to the diode I - V characteristic in the present working point (see *Figure 8*).

Figure 8. Equivalent series resistor

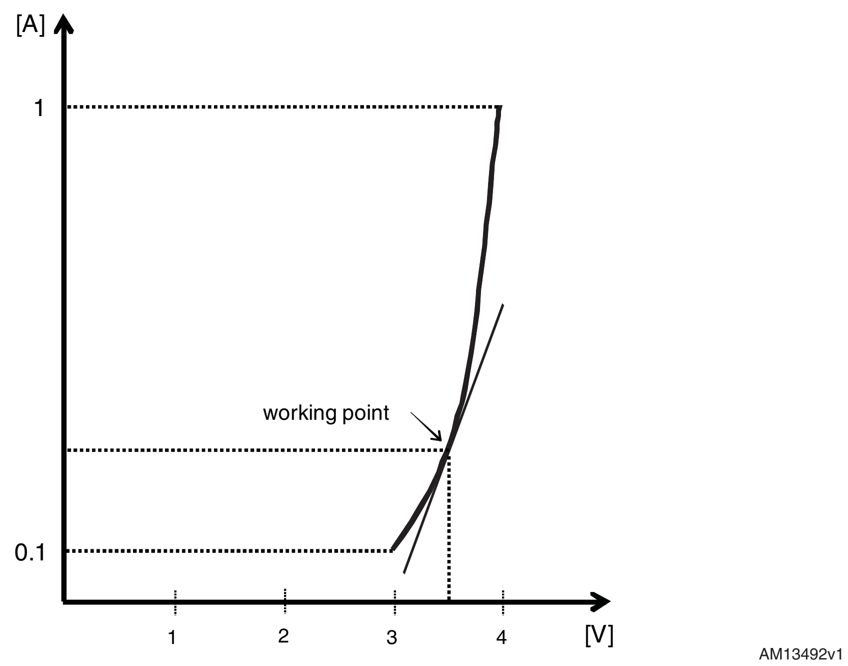


Figure 9 shows the equivalent circuit of the LED constant current generator.

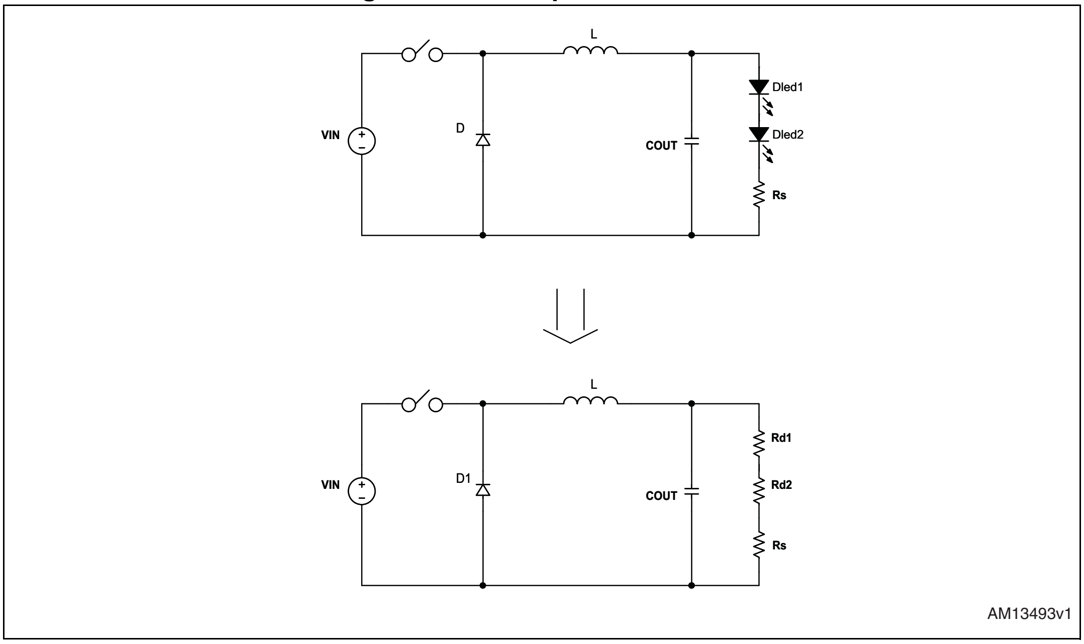
The equivalent loading resistor in the LEDs working point is:

Equation 12

$$R_{LOAD} = n_{LED} \cdot r_{LED} + R_S$$

where R_S is the resistor put in series to the LED string.

Figure 9. Load equivalent circuit



As a consequence the LED equivalent circuit gives the $\alpha_{LED}(s)$ term correlating the output voltage with the high impedance FB input:

Equation 13

$$\alpha_{LED}(n_{LED}) = \frac{R_{SENSE}}{n_{LED} \cdot r_{LED} + R_{SENSE}}$$

5.5 Total loop gain

In summary, the open loop gain can be expressed as:

Equation 14

$$G(s) = G_{CO}(s) \cdot A_0(s) \cdot \alpha_{LED}(n_{LED})$$

5.6 Compensation network design

The maximum bandwidth of the system can be designed up to $f_{SW}/6$ to guarantee a valid small signal model.

Equation 15

$$\frac{\omega_P}{2 \cdot \pi} < BW \leq BW_{MAX} = \frac{f_{SW}}{6}$$

where ω_P (*Equation 3*) is the pole introduced by the power components. The following calculations are valid in the hypothesis that BW > ω_P which is the typical condition.

With the power components selected in accordance with *Section 5.9: Component selection on page 25* and given the BW specification, the components composing the compensation network can be calculated as:

Equation 16

$$R_C = \frac{1 + \frac{R_{LOAD} \cdot T_{SW}}{L} \cdot [m_C \cdot (1 - D) - 0.5]}{f_P} \cdot \frac{BW \cdot R_{CS}}{G_m \cdot R_S}$$

where the term m_C is represented in *Equation 4 on page 15*, R_{LOAD} the equivalent loading resistor (*Equation 12*), R_S the resistor put in series to the LED string, G_m the error amplifier transconductance and R_{CS} the equivalent sensing resistor of the current sense circuitry equal to 0.38 (*Table 5: Electrical characteristics on page 8*).

Equation 17

$$C_C = \frac{K}{R_C \cdot BW}$$

where *K* represents the leading position of the F_Z (*Equation 11*) with respect to the system bandwidth. In general, a value of 2 gives enough phase margin to the overall small loop transfer function.

5.7 Example of system design

Design specification:

V_{IN} = 48 V, V_{FW_LED} = 3.7 V, n_{LED} = 10, r_{LED} = 1.1 Ω, I_{LED} = 1 A, $I_{LED\ RIPPLE}$ = 2%.

The inductor and capacitor value are dimensioned to meet the $I_{LED\ RIPPLE}$ specification (see *Section 5.9.2 on page 25* for output capacitor and inductor selection guidelines):

L = 22 µH, C_{OUT} = 1.0 µF mlcc (negligible ESR).

In accordance with *Section 5.9.1 on page 25* the sensing resistor value is:

Equation 18

$$R_S = \frac{200\ mV}{1\ A} = 200\ m\Omega$$

Assuming a system bandwidth of:

Equation 19

$$BW = 70\ kHz < BW_{MAX}$$

The ideal values of the components making up the compensation network are:

Equation 20

$$R_C = 43\ k\Omega \qquad C_C = 650\ pF$$

Final component selection is based on commercial values and a small capacitor C_P is added to reduce noise at the error amplifier output. C_P slightly decreases the BW and phase margin.

Equation 21

$$R_C = 47\ k\Omega \qquad C_C = 680\ pF \qquad C_C = 12\ pF$$

The gain and phase margin bode diagrams are plotted, respectively, in *Figure 10* and *Figure 11*.

Figure 10. Module plot

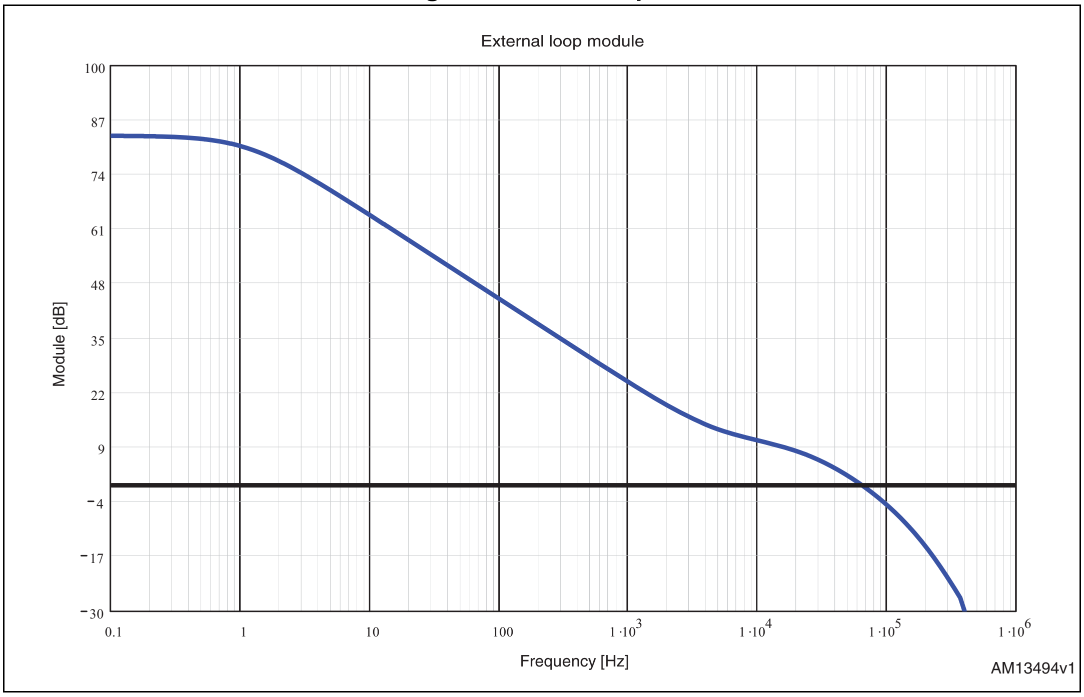
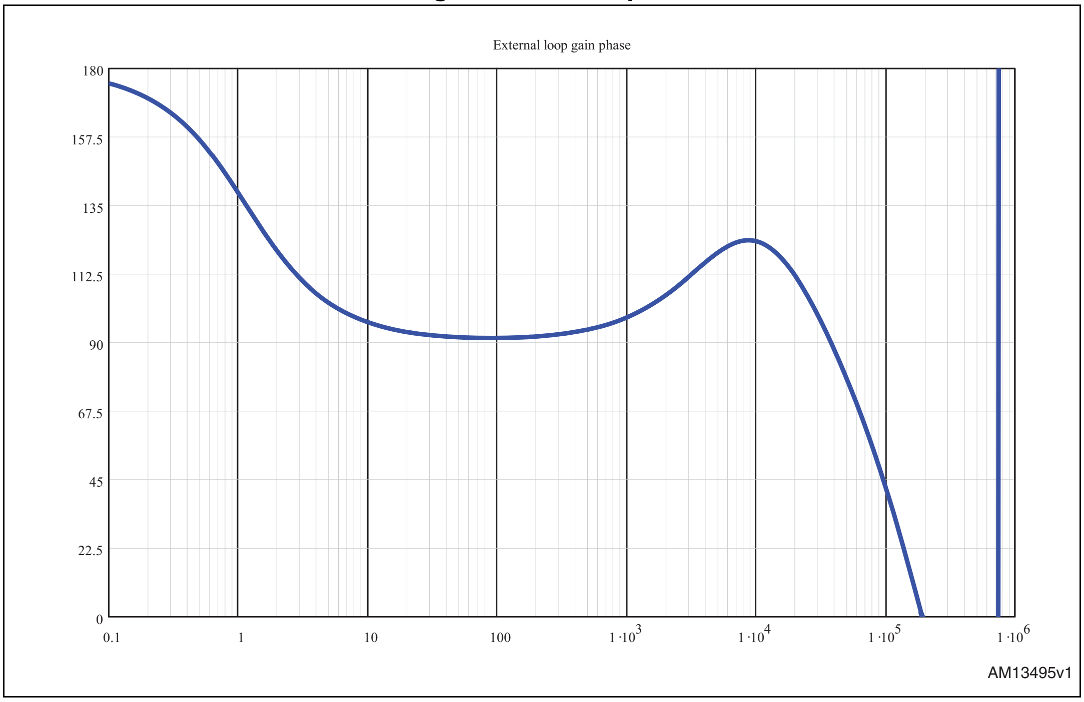


Figure 11. Phase plot



The cut-off frequency and the phase margin are:

Equation 22

$$f_C = 65\text{ kHz} \qquad pm = 66°$$

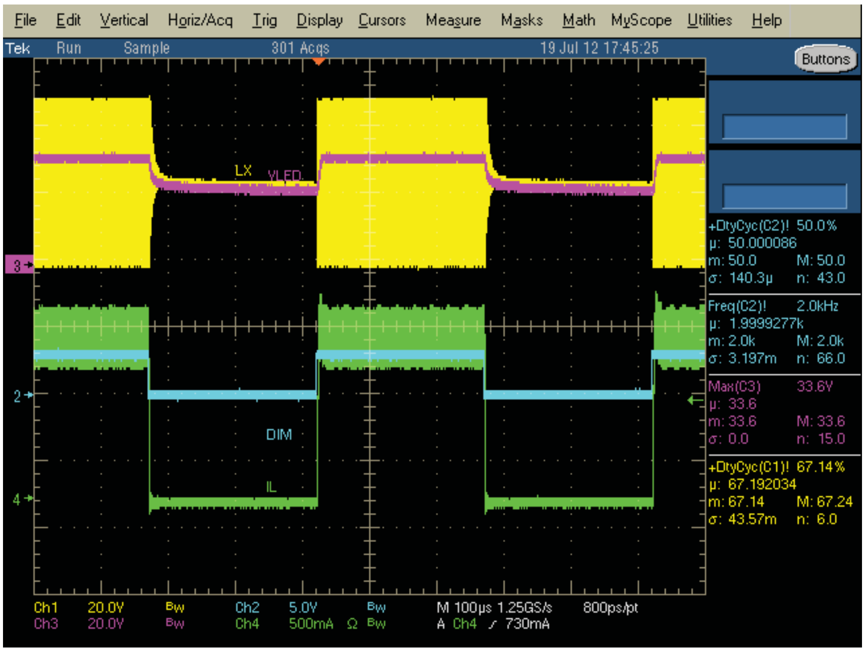
5.8 Dimming operation

The dimming input disables the switching activity, masking the PWM comparator output.

The inductor current dynamic performance when dimming input goes high depends on the designed system response. The best dimming performance is obtained by maximizing the bandwidth and phase margin, when possible.

As a general rule, the output capacitor minimization improves dimming performance.

Figure 12. dimming operation example



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In fact, when dimming enables the switching activity, a small capacitor value is fast charged with low inductor value. As a consequence, the LEDs current rising edge time is improved and the inductor current oscillation reduced. An oversized output capacitor value requires extra current for fast charge so generating an inductor current overshoot and oscillations.

The switching activity is prevented as soon as the dimming signal goes low. Nevertheless, the LED current drops to zero only when the voltage stored in the output capacitor goes below a minimum voltage determined by the selected LEDs. As a consequence, a big capacitor value makes the LED current falling time worse than a smaller one.

The LED5000 device embeds dedicated circuitry to improve LED current rising edge time.

Figure 13. LED rising edge operation

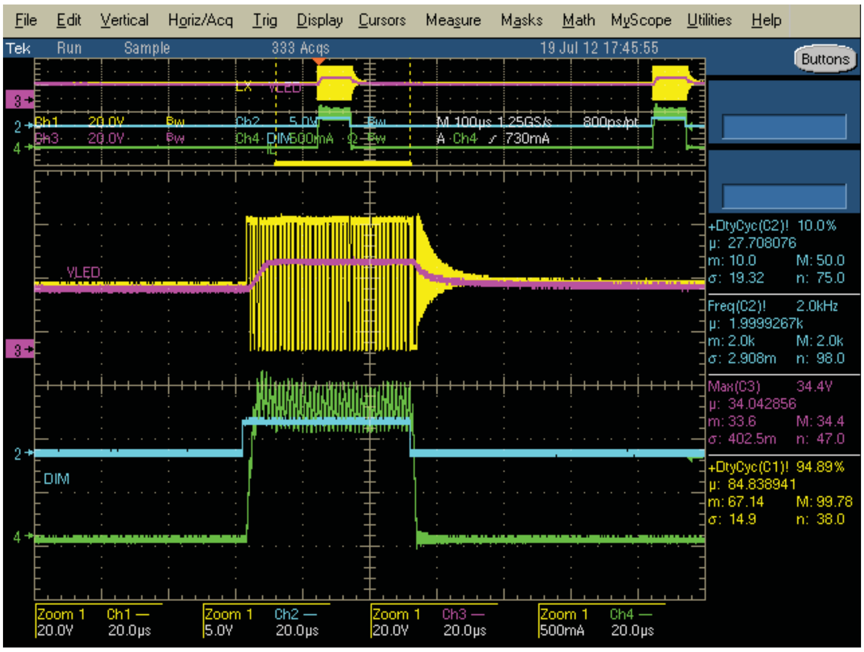

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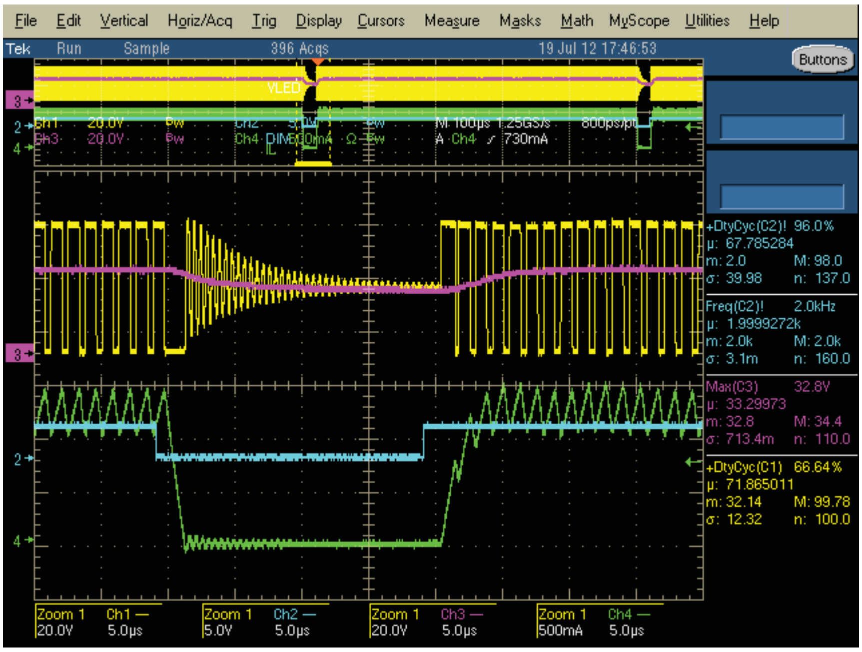
Figure 14. LED rising edge operation (zoom)



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Dimming frequency vs. dimming depth

As seen in *Section 5.8* the LEDs current rising and falling edge time mainly depends on the system bandwidth (T_{RISE}) and the selected output capacitor value (T_{RISE} and T_{FALL}).

The dimming performance depends on the minimum current pulse shape specification of the final application. The ideal minimum current pulse has rectangular shape, in any case it degenerates into a trapezoid or, at worst, into a triangle, depending on the ratio (T_{RISE} + T_{FALL})/ T_{DIM}.

Equation 23

$$\underset{\textbf{rectangle}}{\frac{T_{RISE}+T_{FALL}}{T_{DIM}} \ll 1} \rightarrow \underset{\textbf{trapezoid}}{\frac{T_{RISE}+T_{FALL}}{T_{DIM}} < 1} \rightarrow \underset{\textbf{triangle}}{\frac{T_{RISE}+T_{FALL}}{T_{DIM}} = 1}$$

The small signal response in *Figure 14* is considered as an example.

Equation 24

$$\begin{cases} T_{RISE} \cong 5\mu s \\ T_{FALL} \cong 2\mu s \end{cases}$$

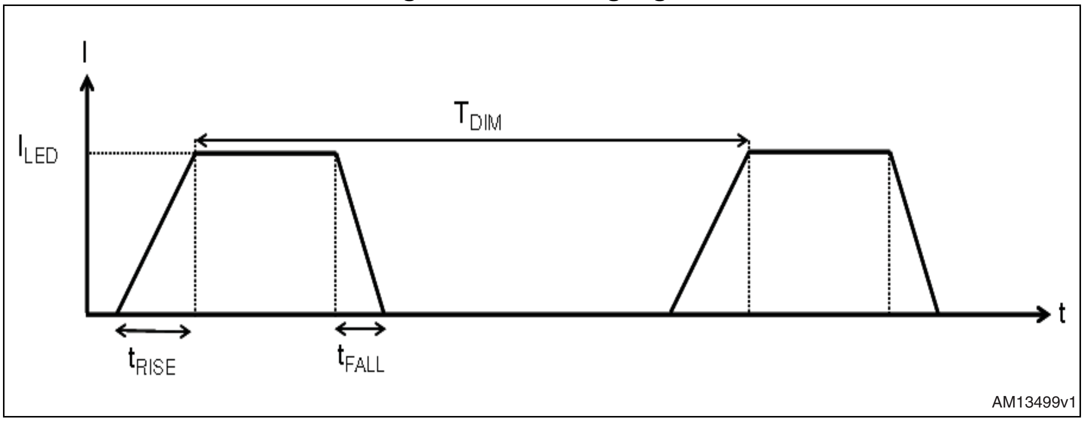
Assuming the minimum current pulse (T_{MIN_PULSE}) shape specification as:

Equation 25

$$T_{RISE} + T_{FALL} = 0.75 \cdot T_{MIN\_PULSE} = 0.75 \cdot D_{MIN} \cdot T_{DIMMING}$$

where $T_{DIMMING}$ represents the dimming period and D_{MIN} the minimum duty cycle which gives the T_{MIN_PULSE} charge. In the given example T_{MIN_PULSE} = 9 µs.

Figure 15. dimming signal



Given T_{MIN_PULSE} it is possible to calculate the maximum dimming depth given the dimming frequency or vice versa.

For example, assuming a 10 KHz dimming frequency the maximum dimming depth is 9% or given a 5% dimming depth it follows a 5.5 KHz maximum f_{DIM}.

The LED5000 dimming performance is strictly dependent on the system small signal response. As a consequence, an optimized compensation network (good phase margin and bandwidth maximized) and minimized C_{OUT} value are crucial for best performance. Once the external power components and the compensation network are selected, a direct measurement to determine T_{RISE}, T_{FALL} (see *Equation 24*) is necessary to certify the achieved dimming performance.

5.9 Component selection

5.9.1 Sensing resistor

In closed loop operation the LED5000 feedback pin voltage is 200 mV, so the sensing resistor calculation is expressed as:

Equation 26

$$R_S = \frac{200\ mV}{I_{LED}}$$

Since the main loop (see *Section 5.1 on page 14*) regulates the sensing resistor voltage drop, the average current is regulated into the LEDs. The integration period is at minimum 5 * T_{SW} since the system bandwidth can be dimensioned up to $f_{SW}/5$ at maximum.

A system loop based on a peak current mode architecture features consistent advantages in comparison with simpler closed loop regulation schemes like the hysteretic or the constant ON/OFF control.

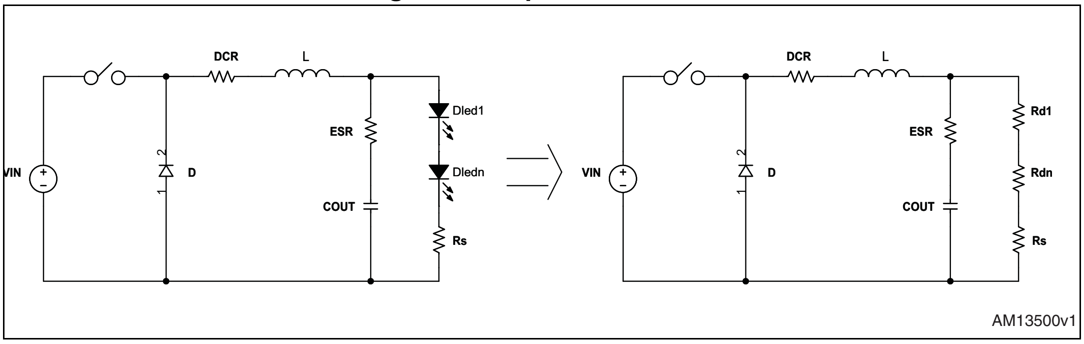
The system performs the output current regulation over a period which is at least five times longer than the switching frequency. The output current regulation neglects the ripple current contribution and its reliance on external parameters like input voltage and output voltage variations (line transient and LED forward voltage spread). This performance cannot be achieved with simpler regulation loops like hysteretic control.

For the same reason, the switching frequency is constant over the application conditions, that helps to tune the EMI filtering and to guarantee the maximum LED current ripple specification in the application range. This performance cannot be achieved using constant ON/OFF time architectures.

5.9.2 Inductor and output capacitor selection

The output capacitor filters the inductor current ripple that, given the application condition, depends on the inductor value. As a consequence the LED current ripple, that is the main specification for a switching current source, depends on the inductor and output capacitor selection.

Figure 16. Equivalent circuit



The LED ripple current can be calculated as the inductor ripple current ratio flowing into the output impedance using the Laplace transform (see *Figure 11 on page 21*):

Equation 27

$$\Delta I_{RIPPLE}(s) = \frac{\frac{8}{\pi^2} \cdot \Delta I_L \cdot (1 + s \cdot ESR \cdot C_{OUT})}{1 + s \cdot (R_S + ESR + n_{LED} \cdot R_{LED}) \cdot C_{OUT}}$$

where the term $8/\pi^2$ represents the main harmonic of the inductor current ripple (which has a triangular shape) and ΔI_L is the inductor current ripple.

Equation 28

$$\Delta I_L = \frac{V_{OUT}}{L} \cdot T_{OFF} = \frac{n_{LED} \cdot V_{FW\_LED} + 200mV}{L} \cdot T_{OFF}$$

so L value can be calculated as:

Equation 29

$$L = \frac{n_{LED} \cdot V_{FW\_LED} + 200mV}{\Delta I_L} \cdot T_{OFF} = \frac{n_{LED} \cdot V_{FW\_LED} + 200mV}{\Delta I_L} \cdot \left(1 - \frac{n_{LED} \cdot V_{FW\_LED} + 200mV}{V_{IN}}\right)$$

where T_{OFF} is the OFF time of the embedded high switch, given by 1 - D.

As a consequence the lower is the inductor value (so higher the current ripple), the higher would be the C_{OUT} value to meet the specification.

A general rule to dimension L value is:

Equation 30

$$\frac{\Delta I_L}{I_{LED}} \leq 0.5$$

Finally the required output capacitor value can be calculated equalizing the LED current ripple specification with the module of the Fourier transformer (see *Equation 27*) calculated at f_{SW} frequency.

Equation 31

$$|\Delta I_{RIPPLE}(s = j \cdot \omega)| = \Delta I_{RIPPLE\_SPEC}$$

Example 1(see *Section 5.6 on page 19*):

V_{IN} = 48 V, I_{LED} = 700 mA, $\Delta I_{LED}/I_{LED}$ = 2%, V_{FW_LED} = 3.7 V, n_{LED} = 10.

A lower inductor value maximizes the inductor current slew rate for better dimming performance. *Equation 30* becomes:

Equation 32

$$\frac{\Delta I_L}{I_{LED}} = 0.5$$

which is satisfied selecting a 10 µH inductor value.

The output capacitor value has to be dimensioned according to *Equation 31*.

Finally, given the selected inductor value, a 1 µF ceramic capacitor value keeps the LED current ripple ratio lower than the 2% of the nominal current. An output ceramic capacitor type (negligible ESR) is suggested to minimize the ripple contribution given a fixed capacitor value.

Table 7. Inductor selection

Manufacturer	Series	Inductor value (µH)	Saturation current (A)
Wurth Elektronik	WE-HCI 7040	1 to 4.7	20 to 7
	WE-HCI 7050	4.9 to 10	20 to 4.0
Coilcraft	XPL 7030	2.2 to 10	29 to 7.2

5.9.3 Input capacitor

The input capacitor must be able to support the maximum input operating voltage and the maximum RMS input current.

Since step-down converters draw current from the input in pulses, the input current is squared and the height of each pulse is equal to the output current. The input capacitor has to absorb all this switching current, whose RMS value can be up to the load current divided by two (worst case, with duty cycle of 50%). For this reason, the quality of these capacitors has to be very high to minimize the power dissipation generated by the internal ESR, thereby improving system reliability and efficiency. The critical parameter is usually the RMS current rating, which must be higher than the RMS current flowing through the capacitor. The maximum RMS input current (flowing through the input capacitor) is:

Equation 33

$$I_{RMS} = I_O \cdot \sqrt{D - \frac{2 \cdot D^2}{\eta} + \frac{D^2}{\eta^2}}$$

Where η is the expected system efficiency, D is the duty cycle and I_O is the output DC current. Considering $\eta = 1$ this function reaches its maximum value at D = 0.5 and the equivalent RMS current is equal to I_O divided by 2. The maximum and minimum duty cycles are:

Equation 34

$$D_{MAX} = \frac{V_{OUT} + V_F}{V_{INMIN} - V_{SW}}$$

and

Equation 35

$$D_{MIN} = \frac{V_{OUT} + V_F}{V_{INMAX} - V_{SW}}$$

Where V_F is the freewheeling diode forward voltage and V_{SW} the voltage drop across the internal PDMOS. Considering the range D_{MIN} to D_{MAX}, it is possible to determine the max. I_{RMS} going through the input capacitor.

Capacitors that can be considered are:

- Electrolytic capacitors:

These are widely used due to their low price and their availability in a wide range of RMS current ratings.

The only drawback is that, considering ripple current rating requirements, they are physically larger than other capacitors.

- Ceramic capacitors:

If available for the required value and voltage rating, these capacitors usually have a higher RMS current rating for a given physical dimension (due to very low ESR).

The drawback is the considerably high cost.

- Tantalum capacitors:

Small tantalum capacitors with very low ESR are becoming more available. However, they can occasionally burn if subjected to very high current during charge.

Therefore, it is suggested to avoid this type of capacitor for the input filter of the device as they could be stressed by a high surge current when connected to the power supply.

Table 8. List of ceramic capacitors for the LED5000

Manufacturer	Series	Capacitor value (µF)	Rated voltage (V)
Taiyo Yuden	UMK325BJ106MM-T	10	50
Murata	GRM42-2 X7R 475K 50	4.7	50

In case the selected capacitor is ceramic (so neglecting the ESR contribution), the input voltage ripple can be calculated as:

Equation 36

$$V_{IN\,PP} = \frac{I_O}{C_{IN} \cdot f_{SW}} \cdot \left[\left(1 - \frac{D}{\eta}\right) \cdot D + \frac{D}{\eta} \cdot (1 - D)\right]$$

5.10 Layout considerations

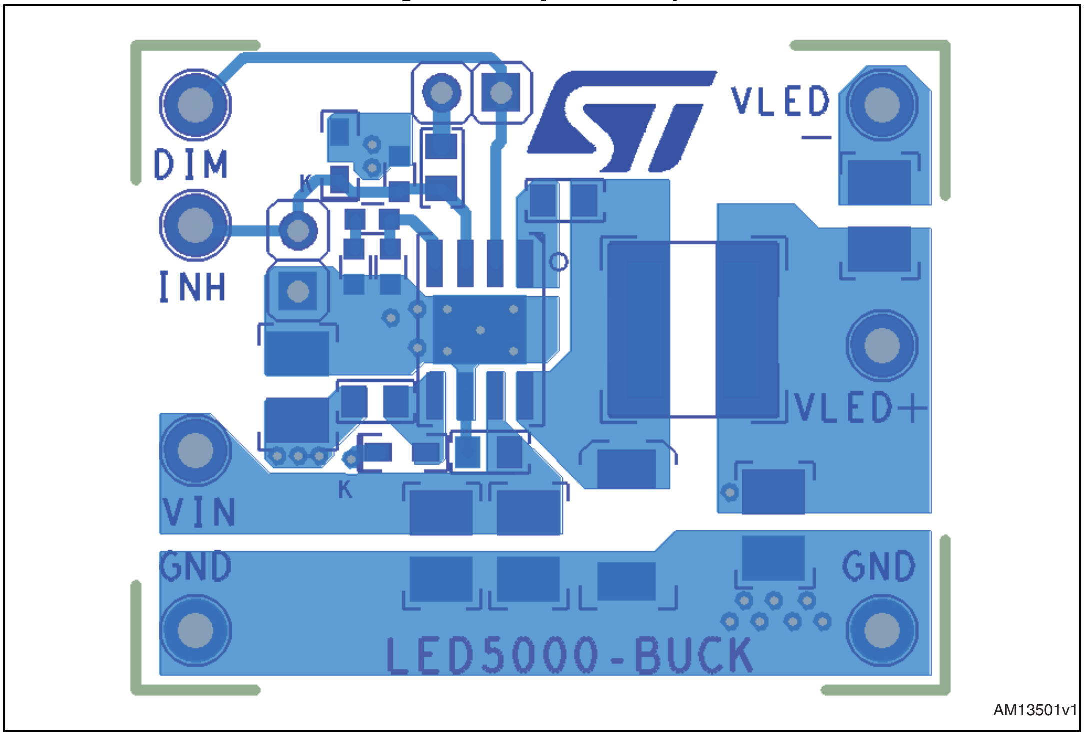
The layout of switching DC-DC converters is very important to minimize noise and interference. Power-generating portions of the layout are the main cause of noise and so high switching current loop areas should be kept as small as possible and lead lengths as short as possible.

High impedance paths (in particular the feedback connections) are susceptible to interference, so they should be as far as possible from the high current paths. A layout example is provided in *Figure 17*.

The input and output loops are minimized to avoid radiation and high frequency resonance problems. The feedback pin to the sensing resistor path must be designed as short as possible to avoid pick-up noise. Another important issue is the ground plane of the board. Since the package has an exposed pad, it is very important to connect it to an extended ground plane in order to reduce the thermal resistance junction to ambient and increase the noise immunity during the switching operation.

In addition, to increase the design noise immunity, different signal and power grounds should be designed in the layout (see *Section 5.13: Application circuit on page 34*). The signal ground serves the small signal components, the device analog ground pin, the exposed pad and a small filtering capacitor connected to the VCC pin. The power ground serves the device ground pin and the input filter. The different grounds are connected underneath the output capacitor. Neglecting the current ripple contribution, the current flowing through this component is constant during the switching activity and so this is the cleanest ground point of the buck application circuit.

Figure 17. Layout example



5.11 Thermal considerations

The dissipated power of the device is tied to three different sources:

- Conduction losses due to the R_{DSON}, which are equal to:

Equation 37

$$P_{ON} = R_{RDSON\_HS} \cdot (I_{OUT})^2 \cdot D$$

Where *D* is the duty cycle of the application. Note that the duty cycle is theoretically given by the ratio between V_{OUT} ($n_{LED} * V_{LED}$ + 200 mV) and V_{IN}, but in practice it is substantially higher than this value to compensate for the losses in the overall application.

For this reason, the conduction losses related to the R_{DSON} increase compared to an ideal case.

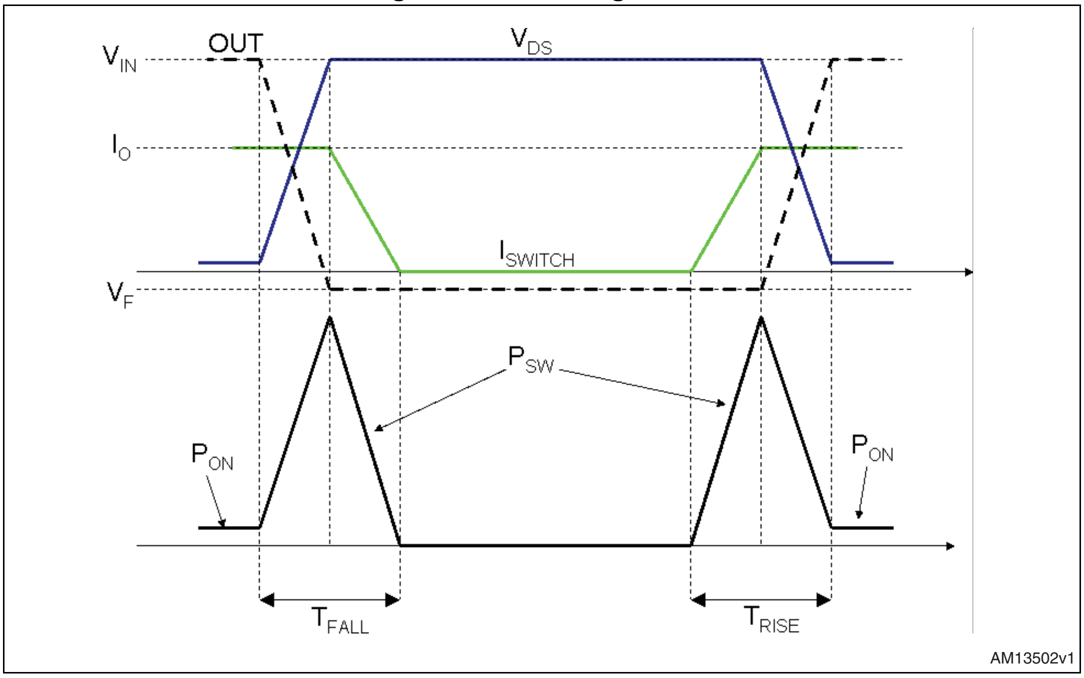
- Switching losses due to turning ON and OFF. These are derived using *Equation 38*:

Equation 38

$$P_{SW} = V_{IN} \cdot I_{OUT} \cdot \frac{(T_{RISE} + T_{FALL})}{2} \cdot F_{SW} = V_{IN} \cdot I_{OUT} \cdot T_{SW\_EQ} \cdot F_{SW}$$

Where T_{RISE} and T_{FALL} represent the switching times of the power element that cause the switching losses when driving an inductive load (see *Figure 18*). T_{SW} is the equivalent switching time.

Figure 18. Switching losses



- Quiescent current losses.

Equation 39

$$P_Q = V_{IN} \cdot I_Q$$

Example 2 (see *Section 5.6 on page 19*):

V_{IN} = 42 V, V_{FW_LED} = 3.7 V, n_{LED} = 8, I_{LED} = 1500 mA.

The typical output voltage is:

Equation 40

$$V_{OUT} = n_{LED} \cdot V_{FW\_LED} + V_{FB} = 29.4V$$

R_{DSON_HS} has a typical value of 200 Ω at 25 °C.

For the calculation we can estimate R_{DSON_HS} = 300 mΩ as a consequence of T_J increase during the operation.

T_{SW_EQ} is approximately 12 ns.

I_Q has a typical value of 2.4 mA at V_{IN} = 48 V.

The overall internal losses are:

Equation 41

$$P_{TOT} = R_{DSON\_HS} \cdot (I_{OUT})^2 \cdot D + V_{IN} \cdot I_{OUT} \cdot f_{SW} \cdot T_{SW\_EQ} + V_{IN} \cdot I_Q$$

where T_{SW_EQ} = (T_{RISE} + T_{FALL})/2 = 12 nS.

Equation 42

$$P_{TOT} = 0.3 \cdot 1.5^2 \cdot 0.7 + 42 \cdot 1.5 \cdot 12 \cdot 10^{-9} \cdot 850 \cdot 10^3 + 42 \cdot 2.4 \cdot 10^{-3} \cong 1.2W$$

The junction temperature of the device will be:

Equation 43

$$T_J = T_A + Rth_{J-A} \cdot P_{TOT}$$

Where T_A is the ambient temperature and $Rth_{J\text{-}A}$ is the thermal resistance junction to ambient. The junction to ambient ($Rth_{J\text{-}A}$) thermal resistance of the device assembled in the HSOP8 package and mounted on the evaluation is about 40 °C/W.

Assuming the ambient temperature around 40 °C, the estimated junction temperature is:

$$T_J = 40 + 1.2W \cdot 40 \cdot \frac{°C}{W} \cong 110°C$$

5.12 Short-circuit protection

In overcurrent protection mode, when the peak current reaches the current limit threshold, the device disables the power element and it is able to reduce the conduction time down to the minimum value (approximately 100 nsec typical) to keep the inductor current limited. This is the pulse-by-pulse current limitation to implement constant current protection feature.

In overcurrent condition, the duty cycle is strongly reduced and, in most applications, this is enough to limit the switch current to the current threshold.

The inductor current ripple during ON and OFF phases can be written as:

- ON phase

Equation 44

$$\Delta I_{L\ TON} = \frac{V_{IN} - V_{OUT} - (DCR_L + R_{DSON\ HS}) \cdot I}{L}(T_{ON})$$

- OFF phase

Equation 45

$$\Delta I_{L\ TON} = \frac{-(V_{OUT} + DCR_L \cdot I + V_{FW\ DIODE})}{L}(T_{OFF})$$

where DCR_L is the series resistance of the inductor and $V_{FWDIODE}$ is the forward voltage drop across the external rectifying diode.

The pulse-by-pulse current limitation is effective to implement constant current protection when:

Equation 46

$$|\Delta I_{L\ TON}| = |\Delta I_{L\ TOFF}|$$

From *Equation 44* and *Equation 45* we can gather that the implementation of the constant current protection becomes more critical the lower is the V_{OUT} and the higher is V_{IN}.

In fact, in short-circuit condition the voltage applied to the inductor during the OFF time becomes equal to the voltage drop across parasitic components (typically the DCR of the inductor and the forward voltage of the diode) since V_{OUT} is negligible, while during T_{ON} the voltage applied the inductor is maximized and it is approximately equal to V_{IN}.

In general the worst case scenario is a heavy short-circuit at the output with maximum input voltage. *Equation 44* and *Equation 45* in overcurrent conditions can be simplified to:

Equation 47

$$\Delta I_{L\ TON} = \frac{V_{IN} - (DCR_L + R_{DSON\ HS}) \cdot I}{L}(T_{ON\ MIN}) \cong \frac{V_{IN}}{L}(90ns)$$

considering T_{ON} that has been already reduced to its minimum.

Equation 48

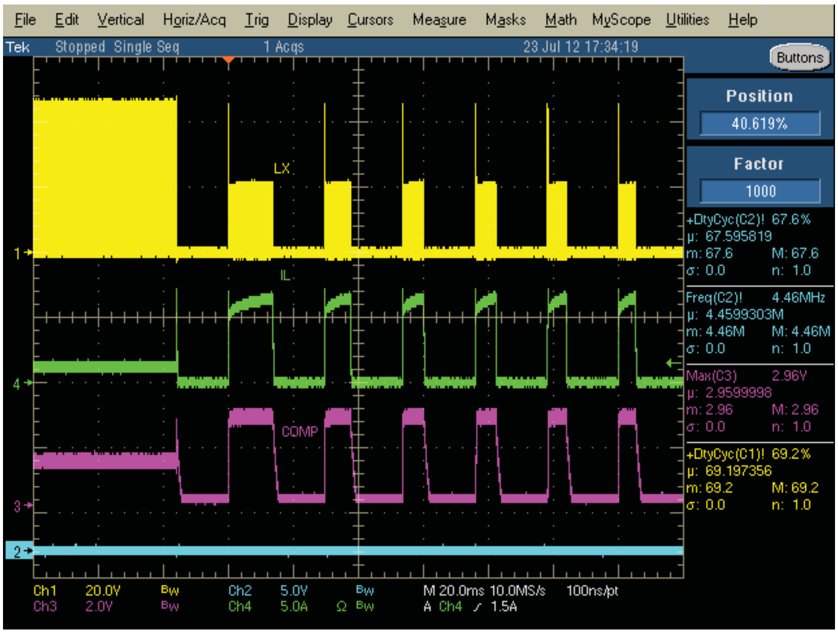
$$\Delta I_{L\ TOFF} = \frac{-(DCR_L \cdot I + V_{FW\ DIODE})}{L}(T_{SW} - 90ns) \cong \frac{-(DCR_L \cdot I + V_{FW\ DIODE})}{L}(1.18\mu s)$$

where $T_{SW} = 1/f_{SW}$ considering the nominal f_{SW}.

At high input voltage $\Delta I_{L\ TON}$ could be higher than $\Delta I_{L\ TOFF}$ and so the inductor current could escalate. As a consequence, the system typically meets *Equation 46* at a current level higher than the nominal value thanks to the increased voltage drop across stray components. In most application conditions the pulse-by-pulse current limitation is effective to limit the inductor current. Whenever the current escalates, a second level current protection called “hiccup mode” is enabled. The hiccup protection offers an additional protection against heavy short-circuit condition at very high input voltage even considering the spread of the minimum conduction time of the power element. In case the hiccup current level (6.2 A typical) is triggered the switching activity is prevented for 16 msec typ. (see hiccup time in *Table 5: Electrical characteristics on page 8*).

Figure 19 shows the operation of the constant current protection when a short-circuit is applied at the output at the maximum input voltage.

Figure 19. constant current protection triggering hiccup mode



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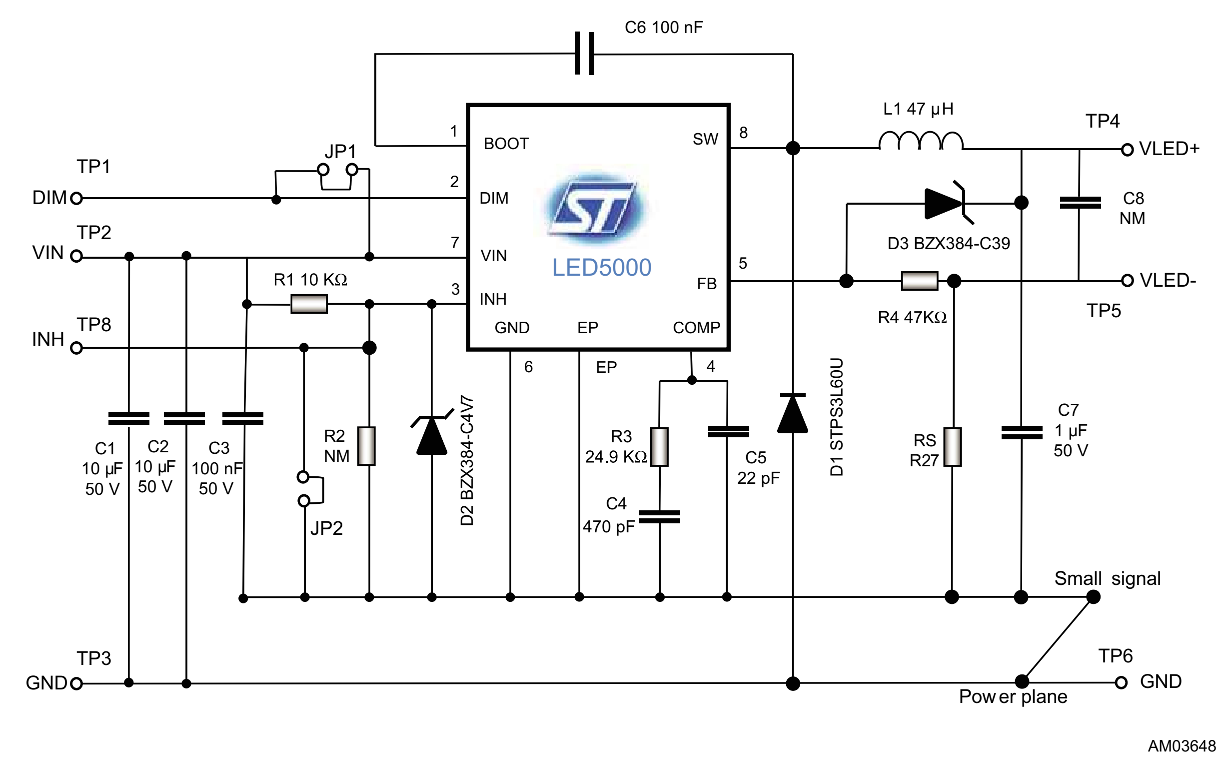
5.13 Application circuit

Figure 20. Evaluation board application circuit



The network D3, R4, RS implements an inexpensive overvoltage protection. R4 effect can be neglected during normal operation since the FB biasing current is negligible (tens of nA, see *Table 5: Electrical characteristics on page 8*) but it limits the current flowing in the Zener diode D3. In case the load is disconnected or in case of open LED:

Equation 49

$$V_{OUT} = V_{FB} + V_{ZENER\_DIODE}$$

$$I_{ZENER\_DIODE} = \frac{V_{FB}}{R_S + R_1}$$

R1 must be dimensioned to limit the D1 rated power so it is an inexpensive small signal Zener diode.

The overvoltage limits the output voltage in case of LED disconnection so protecting LEDs when the string is reconnected with the device enabled. In case the OVP is not implemented, a large amount of non-controlled current could flow through the LEDs during the output capacitor discharging phase, thereby damaging the devices.

Table 9. Component list

Reference	Part number	Description	Manufacturer
C1, C2	C3225X7S1H106M	10 µF 50 V (size 1210)	TDK
C3, C6		100 nF 50 V (size 0805)	
C4		470 pF 50 V (size 00603)	
C5		22 pF 50 V (size 0603)	
C7	C3216X7R1H105K	1 µF 50 V (size 1206)	TDK
C8		Not mounted	
D1	STPS3L60U	3 A 60 V	ST
D2	BZX384-C4V7		
D3	BZX384-C39		
L1	XFL6060-473ME	47 µH I_{SAT} = 1.8 A (10% drop) I_{RMS} = 3.7 A (40 °C rise) (size 7.3 x 7.3 x 4.1 mm)	Coilcraft
R_S	ERJ14BSFR27U	0.27 Ω 1% (size 1206)	Panasonic
R1		10 kΩ 1% (size 0603)	
R2		Not mounted	
R3		24.9 kΩ 1% (size 0603)	
R4		47 kΩ 1% (size 0603)	

Figure 21. PCB layout (component side)

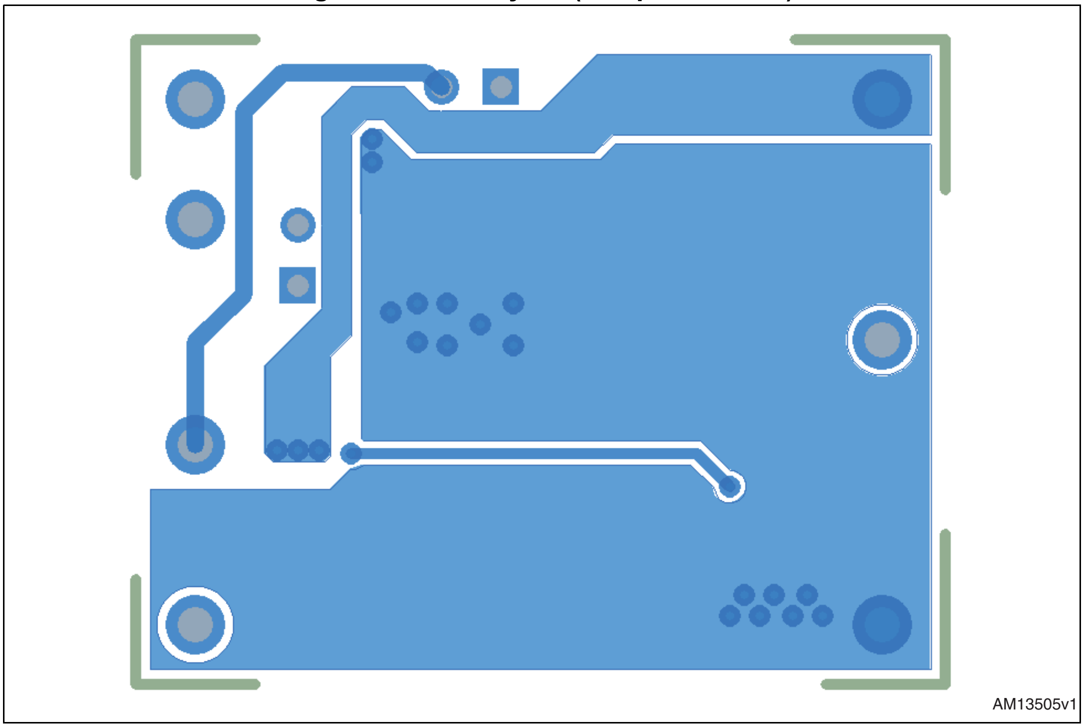
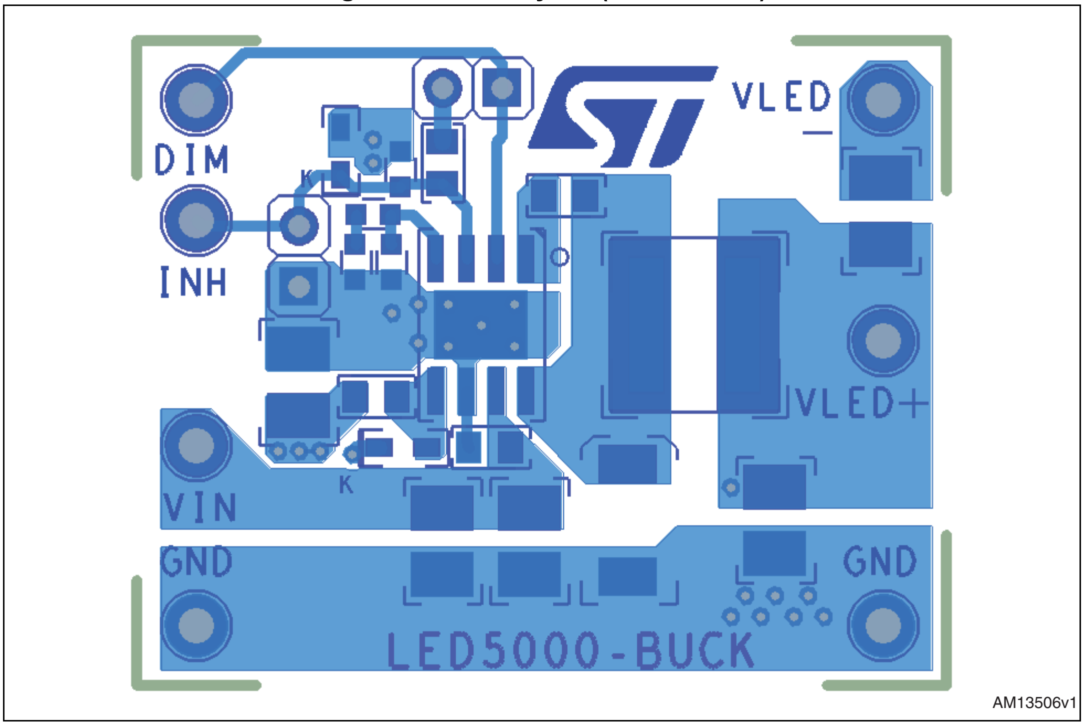


Figure 22. PCB layout (bottom side)



6 Application notes - alternative topologies

Thanks to the wide input voltage range, the adjustable external compensation network and enhanced dimming capability, the LED5000 device is suitable to implement boost and buck-boost topologies.

6.1 Inverting buck-boost

The buck-boost topology fits the application with an input voltage range that overlaps the output voltage, which is the voltage drop across the LEDs and the sensing resistor.

The inverting buck-boost (see *Figure 23*) requires the same component count as the buck conversion and it is more efficient than the positive buck-boost. A current generator based on this topology implies two main application constraints:

- the output voltage is negative so the LEDs must be reversed
- the device GND floats with the negative output voltage. The device is supplied between V_{IN} and V_{OUT} (< 0). As a consequence:

Equation 50

$$V_{IN\_MAX\ LED5000} = V_{IN} - V_{OUT}$$

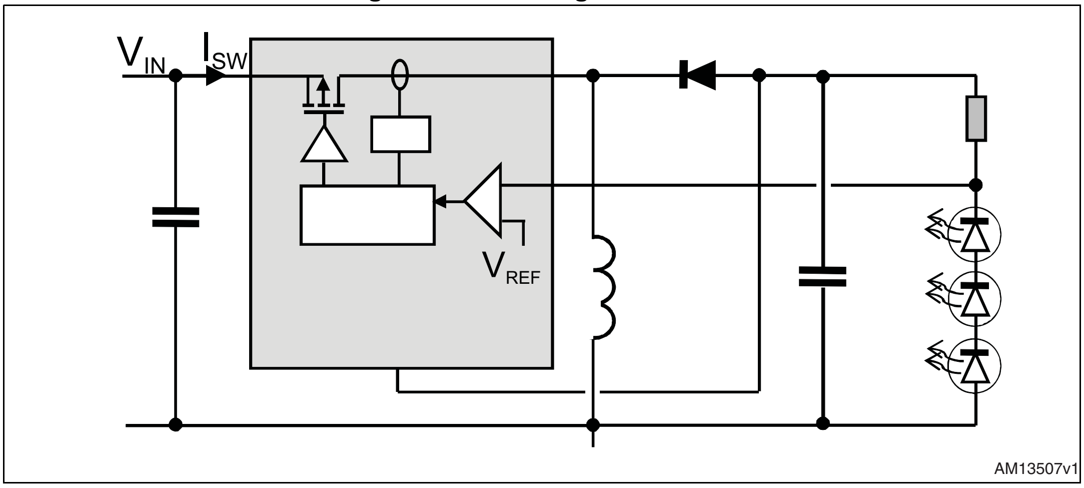
so:

Equation 51

$$V_{IN} = V_{IN\_MAX\ LED5000} + V_{OUT} = 48 + V_{OUT}$$

where $V_{OUT} < 0$.

Figure 23. Inverting buck-boost



Example 3

$V_{IN\ RANGE}$ = 12 - 24 V, V_{FW_LED} = 3.7 V, n_{LED} = 5 so V_{OUT} = 18.7 V.

Since the maximum operating voltage of the LED5000 is 48 V, according to *Equation 51* the maximum input voltage of the application is 48 - 18.7 = 29.3 V.

The output voltage is given by:

Equation 52

$$V_{OUT} = -V_{IN} \cdot \frac{D_{IDEAL}}{1 - D_{IDEAL}}$$

where the ideal duty cycle D_{IDEAL} for the buck-boost converter is:

Equation 53

$$D_{IDEAL} = \frac{-V_{OUT}}{V_{IN} - V_{OUT}}$$

However, due to power losses (mainly switching and conduction losses), the real duty cycle is always higher than this. The real value (which can be measured in the application) should be used in the following formulas.

The peak current flowing in the embedded switch is:

Equation 54

$$I_{SW} = \frac{I_{LOAD}}{1 - D_{REAL}} + \frac{I_{RIPPLE}}{2} = \frac{I_{LOAD}}{1 - D_{REAL}} + \frac{V_{IN}}{2 \cdot L} \cdot \frac{D}{f_{SW}}$$

while its average current level is equal to:

Equation 55

$$I_{SW} = \frac{I_{LOAD}}{1 - D_{REAL}}$$

This is due to the fact that the current flowing through the internal power switch is delivered to the output only during the OFF phase.

The switch peak current must be lower than the minimum current limit of the overcurrent protection (see *Table 5: Electrical characteristics on page 8* for details) while the average current must be lower than the rated DC current of the device.

As a consequence, the maximum output current is:

Equation 56

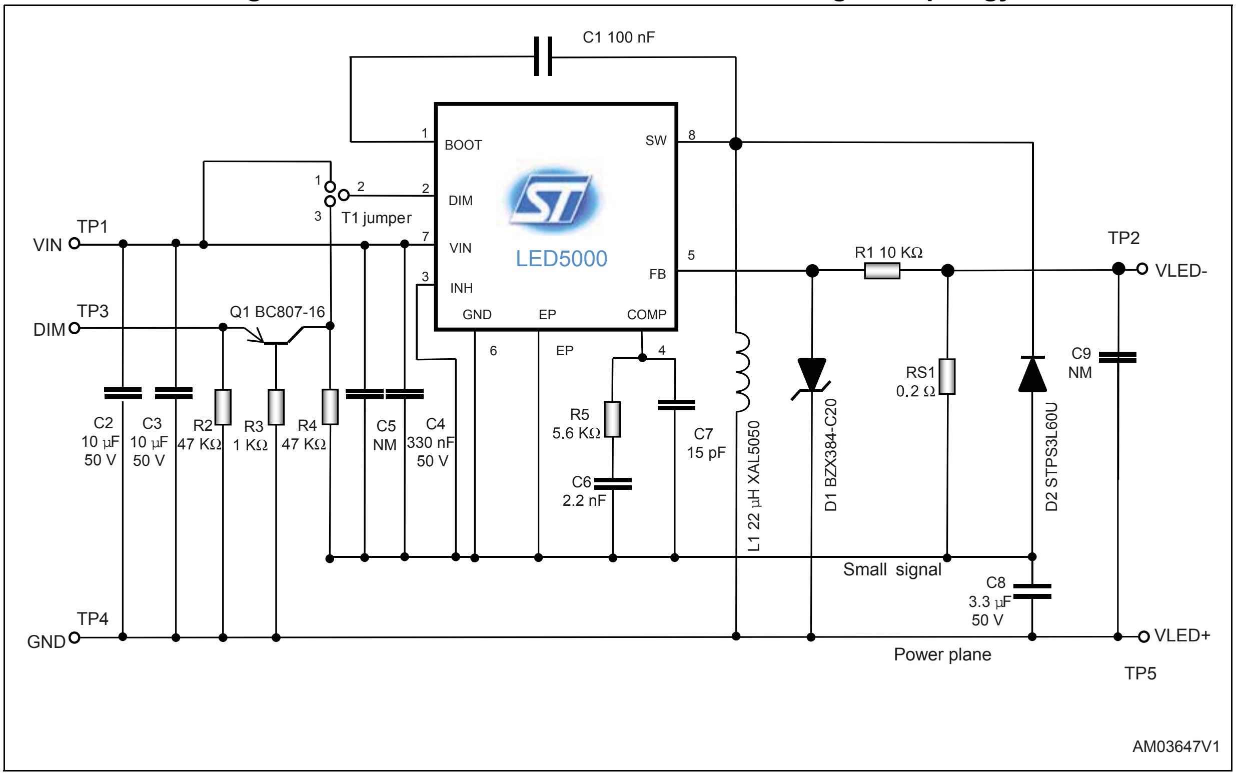
$$I_{LOAD\ MAX} \cong I_{SW\ MAX} \cdot (1 - D_{REAL})$$

where $I_{SW\ MAX}$ represents the rated current of the device.

The current capability is reduced by the term (1 - D_{REAL}) and so, for example, with a duty cycle of 0.5, and considering an average current through the switch of 3 A, the maximum output current deliverable to the load is 1.5 A.

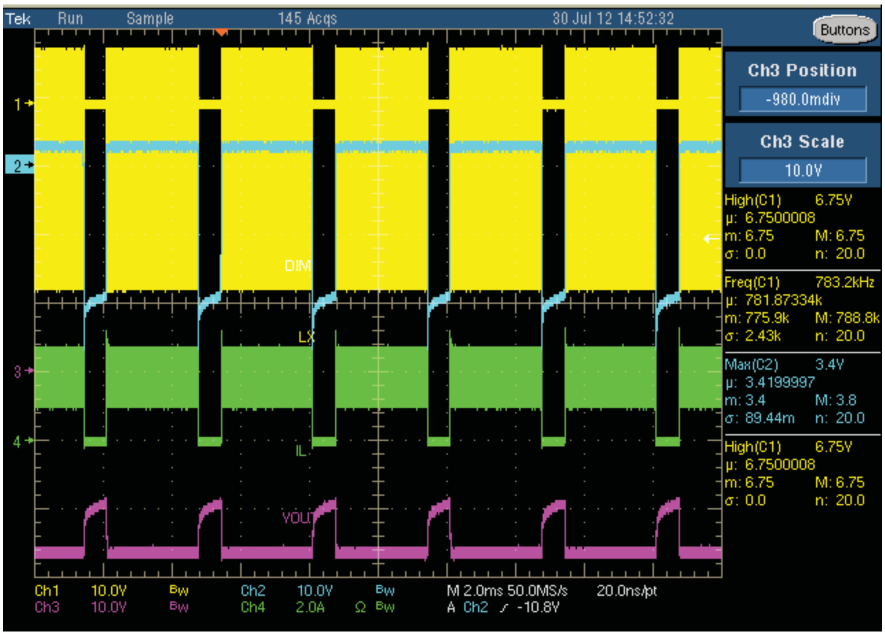
Figure 24 shows the schematic circuit for an LED current source based on inverting buck-boost topology. The input voltage ranges from 10 to 26 V and it can drive a string composed of 5 LEDs with1 A DC.

Figure 24. LED current source based on inverting BB topology



The circuitry Q1, R2, R3, R4 implements a level shifter to convert the dimming signal voltage levels (referred to GND) to the device rails, since the LED5000 local ground is referred to the negative output voltage (given by the voltage drop across the LEDs and the sensing resistor). *Figure 25* shows the dimming operation: the light blue trace represents the DIM pin, the yellow the SW (high level is V_{IN}, low level is $-V_{OUT}$), the green trace the inductor current (see *Equation 54*) and the purple is the output voltage.

Figure 25. Inverting BB dimming operation



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The network D1, R1, RS implements an inexpensive overvoltage protection. R1 effect can be neglected during normal operation since the FB biasing current is negligible (tens of nA, see *Table 5: Electrical characteristics on page 8*) but it limits the current flowing in the Zener diode D1. In case the load is disconnected or in case of an open LED:

Equation 57

$$V_{OUT} = V_{FB} + V_{ZENER\_DIODE}$$

$$I_{ZENER\_DIODE} = \frac{V_{FB}}{R_S + R_1}$$

R1 must be dimensioned to limit the D1 rated power so it is an inexpensive small signal Zener diode.

The overvoltage protection plays an important role for the inverting buck-boost topology. In fact, in case of open row, the output voltage tends to diverge thus exceeding the input voltage absolute maximum rate and the device would be damaged (see *Equation 50*). The overvoltage protection limits V_{OUT} and thereby it protects the device in case of load disconnection.

To design the compensation network for the inverting buck-boost topology please refer to paragraph *Chapter 6.4: Compensation network design for alternative topologies on page 48*.

Figure 26. Inverting BB PCB layout (component side)

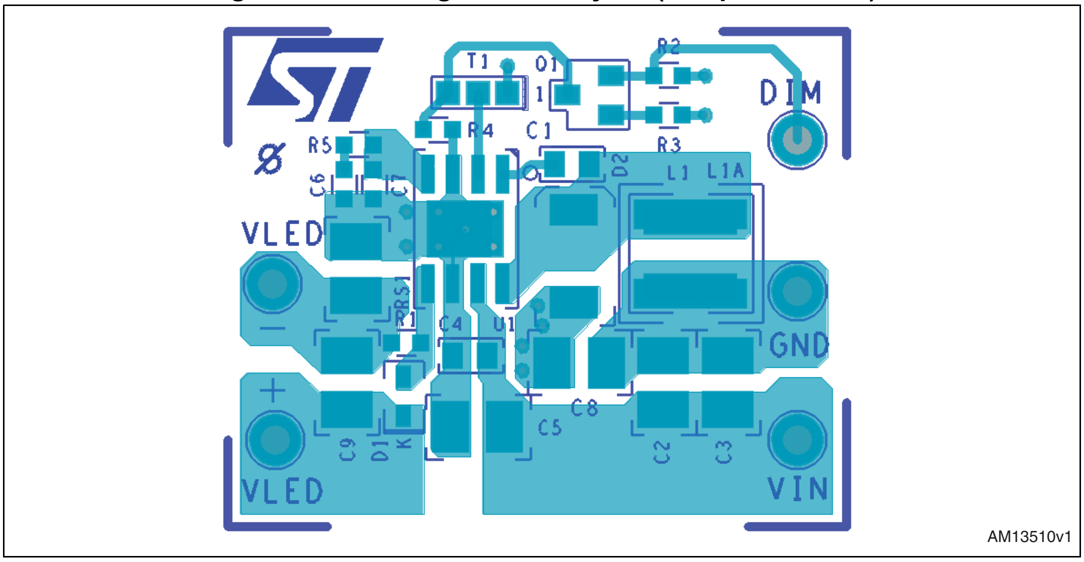
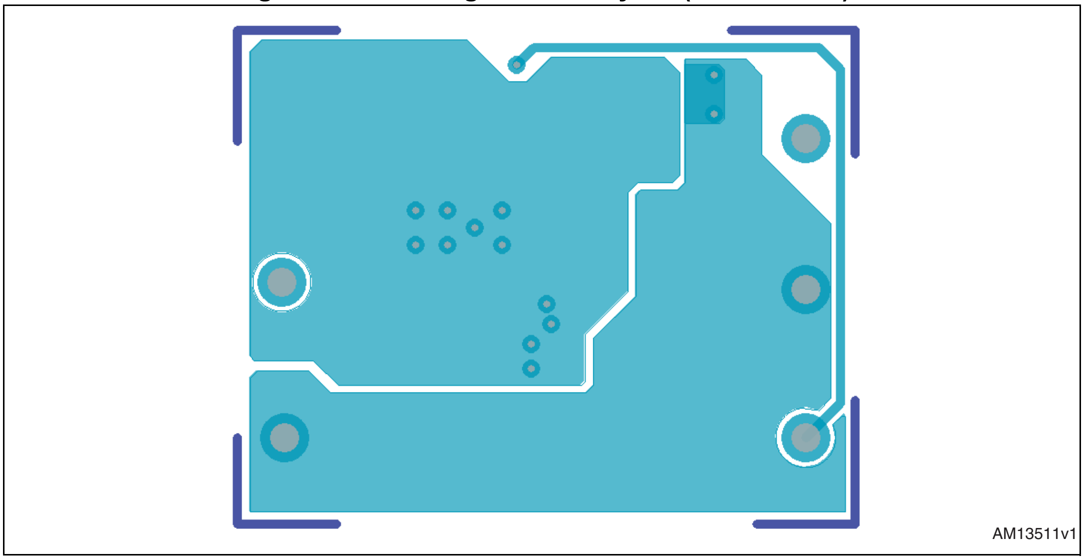


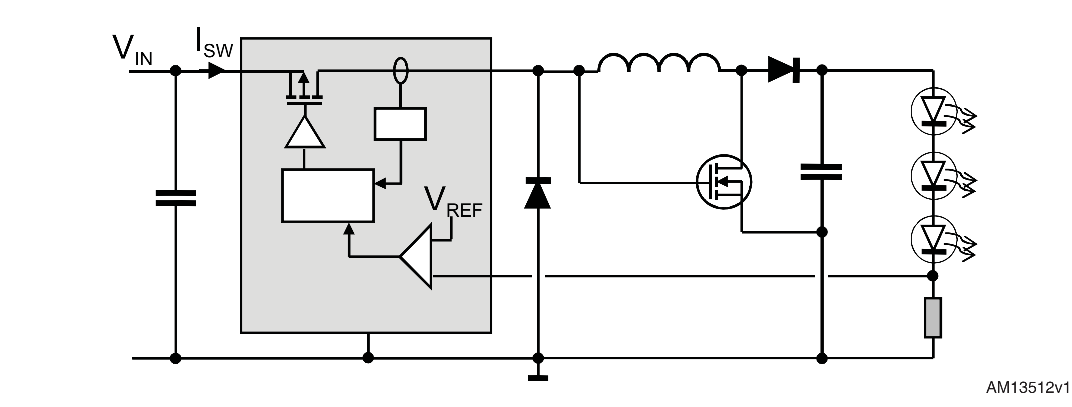
Figure 27. Inverting BB PCB layout (bottom side)



6.2 Positive buck-boost

Positive buck-boost fits those applications that require a buck-boost topology (i.e.: the input voltage range crosses the output voltage value) and where the inverting buck-boost is not suitable because of the main constraints for the final application (refer to *Section 6.1*). As a consequence the inverting buck-boost is the preferred option because it requires less components and it has higher efficiency compared to the positive buck-boost topology.

Figure 28. Positive buck-boost



The positive buck-boost implementation (*Figure 28*) requires one more diode and an external power switch than inverting buck-boost. The device is not floating, referred to GND, and it is supplied with the input voltage of the application (the input voltage in inverting buck-boost topology is instead V_{IN} - V_{OUT}, refer to *Section 6.1* for details). The LED5000 device does not see the output voltage during the switching activity so V_{OUT} can be higher than the maximum input voltage.

The equations for the positive buck-boost are similar to those seen for the inverting.

Equation 58

$$V_{OUT} = V_{IN} \cdot \frac{D_{IDEAL}}{1 - D_{IDEAL}}$$

where the ideal duty cycle D_{IDEAL} for the buck-boost converter is:

Equation 59

$$D_{IDEAL} = \frac{V_{OUT}}{V_{IN} + V_{OUT}}$$

However, due to power losses (mainly switching and conduction losses), the real duty cycle is always higher than this. The real value (which can be measured in the application) should be used in the following formulas.

The peak current flowing in the embedded switch is:

Equation 60

$$I_{SW} = \frac{I_{LOAD}}{1 - D_{REAL}} + \frac{I_{RIPPLE}}{2} = \frac{I_{LOAD}}{1 - D_{REAL}} + \frac{V_{IN}}{2 \cdot L} \cdot \frac{D}{f_{SW}}$$

while its average current level is equal to:

Equation 61

$$I_{SW} = \frac{I_{LOAD}}{1 - D_{REAL}}$$

This is due to the fact that the current flowing through the internal power switch is delivered to the output only during the OFF phase.

The switch peak current must be lower than the minimum current limit of the overcurrent protection (see *Table 5: Electrical characteristics on page 8* for details) while the average current must be lower than the rated DC current of the device.

As a consequence, the maximum output current is:

Equation 62

$$I_{LOAD\ MAX} \cong I_{SW\ MAX} \cdot (1 - D_{REAL})$$

where $I_{SW\ MAX}$ represents the rated current of the device.

The current capability is reduced by the term (1 - D_{REAL}) and so, for example, with a duty cycle of 0.5, and considering an average current through the switch of 3 A, the maximum output current deliverable to the load is 1.5 A.

Figure 29 shows the circuit schematic for an LED current source based on positive buck-boost topology. The input voltage ranges from 18 to 30 V and it can drive a string composed of 7 LEDs with 0.7 A DC (V_{FW_LED} = 3.75 V so V_{OUT} = 26.4 V).

The network D5, R4, R_S implements an inexpensive overvoltage protection. R4 effect can be neglected during the normal operation since the FB biasing current is negligible (tens of nA, see *Table 5: Electrical characteristics on page 8*) but it limits the current flowing in the Zener diode D5. In case the load is disconnected or in case of open LED:

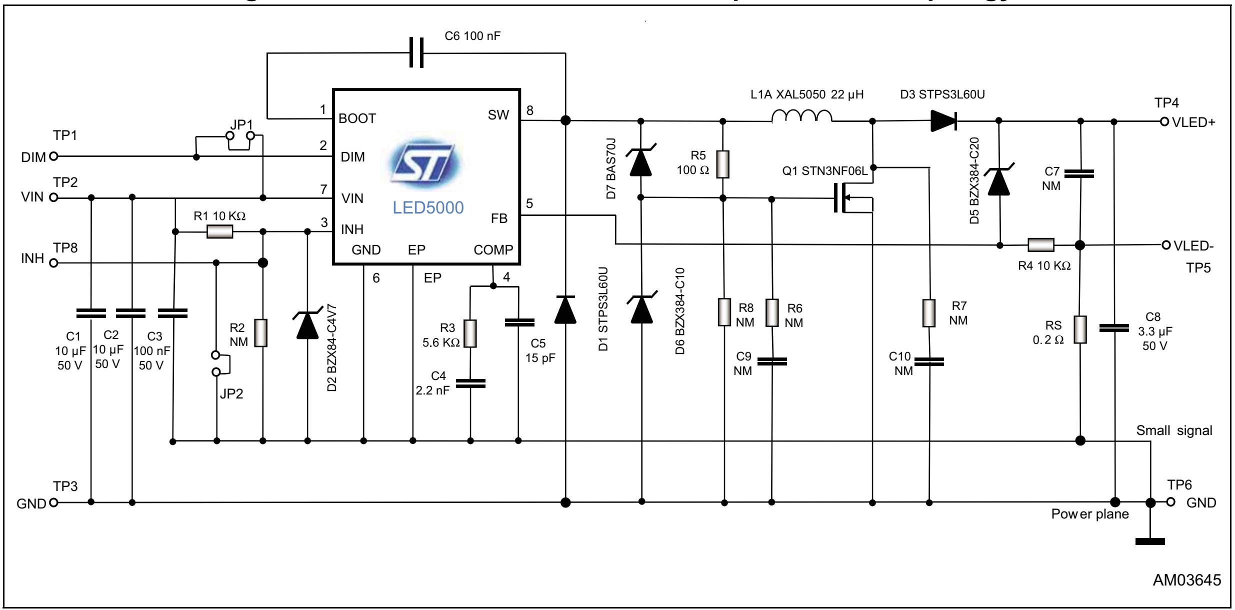
Equation 63

$$V_{OUT} = V_{FB} + V_{ZENER\_DIODE}$$

$$I_{ZENER\_DIODE} = \frac{V_{FB}}{R_S + R_4}$$

R4 must be dimensioned to limit the D5 rated power so it is an inexpensive small signal Zener diode.

Figure 29. LED current source based on positive BB+ topology



In case of open row, the positive output voltage tends to diverge, exceeding the D3 maximum reverse voltage and so the diode would be damaged. The overvoltage protection limits V_{OUT} and it protects the power components in case of load disconnection.

The network D4, R8 implements a level shifter to drive the gate of the transistor Q1. The voltage at Q1 is:

Equation 64

$$V_{Q1\ GATE} = V_{SW} - V_{DZ4} = V_{SW} - 15V$$

Considering the V_{IN} range 18 to 30 V:

Equation 65

$$V_{Q1\ GATE\ MIN} = V_{SW} - V_{DZ4} = 18V - 15V = 3V$$
$$V_{Q1\ GATE\ MAX} = V_{SW} - V_{DZ4} = 30V - 16V = 15V$$

The gate is driven inside the component specification. R8 can be dimensioned to discharge the gate when V_{SW} is low.

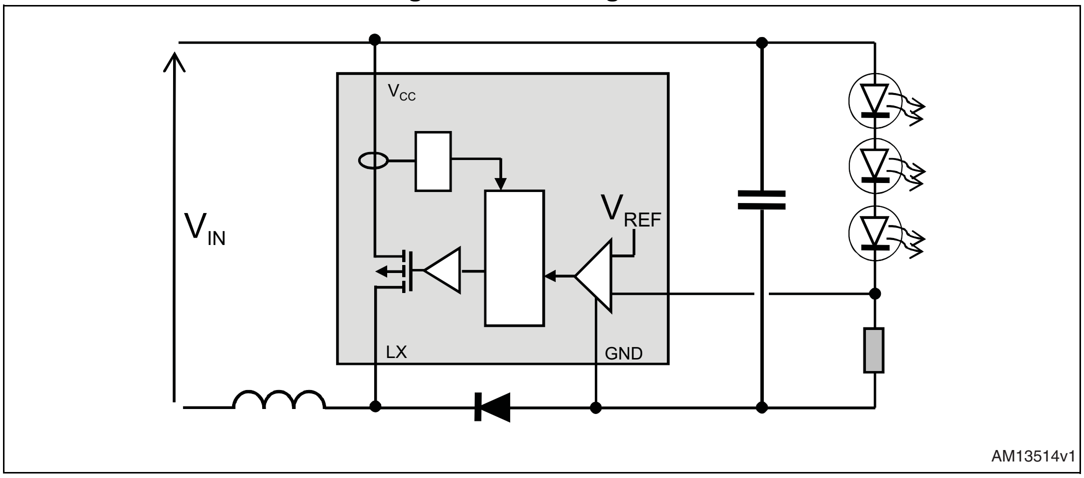
In case the input voltage range of the application is not suitable to implement a level shifter to drive Q1, a dissipative clamping network (like R5, D6) must be used.

To design the compensation network for the positive buck-boost topology please refer to *Section 6.4: Compensation network design for alternative topologies on page 48*.

6.3 Floating boost

The floating boost topology (see *Figure 30*) serves those applications with an input voltage range narrower than the output voltage, that is the voltage drop across the LEDs and the sensing resistor (i.e.: $V_{IN} < V_{OUT}$). The topology is called floating since the output voltage is referred to V_{IN} and not GND, but this is typically suitable for a floating load like a string of LEDs.

Figure 30. Floating boost



The device is supplied by the output voltage so the maximum voltage drop across the LEDs string is 48 V. The direct path of the boost conversion (C_{OUT}, V_{DIODE}, L) guarantees the proper startup when the input voltage is:

Equation 66

$$V_{IN\_START} = V_{OP\_MIN} + V_{DIODE} = 5.5V + V_{DIODE}$$

where V_{OP_MIN} is the minimum operating voltage.

The equations for the floating boost are:

Equation 67

$$V_{OUT} = \frac{V_{IN}}{1 - D_{IDEAL}}$$

The ideal duty cycle D_{IDEAL} for the boost converter is:

Equation 68

$$D_{IDEAL} = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

As seen for the buck-boost topologies (*Section 6.1 on page 37* and *Section 6.2 on page 41*), due to power losses the real duty cycle is always higher than the ideal. The real value (that can be measured in the application) should be used in the following formulas to estimate the switch current.

The peak current flowing in the embedded switch is:

Equation 69

$$I_{SW} = \frac{I_{LOAD}}{1 - D_{REAL}} + \frac{I_{RIPPLE}}{2} = \frac{I_{LOAD}}{1 - D_{REAL}} + \frac{V_{IN}}{2 \cdot L} \cdot \frac{D}{f_{SW}}$$

while its average current level is equal to:

Equation 70

$$I_{SW} = \frac{I_{LOAD}}{1 - D_{REAL}}$$

This is due to the fact that the current flowing through the internal power switch is delivered to the output only during the OFF phase.

The switch peak current must be lower than the minimum current limit of the overcurrent protection (see *Table 5: Electrical characteristics on page 8* for details) while the average current must be lower than the rated DC current of the device.

As a consequence, the maximum output current depends on the application conditions:

Equation 71

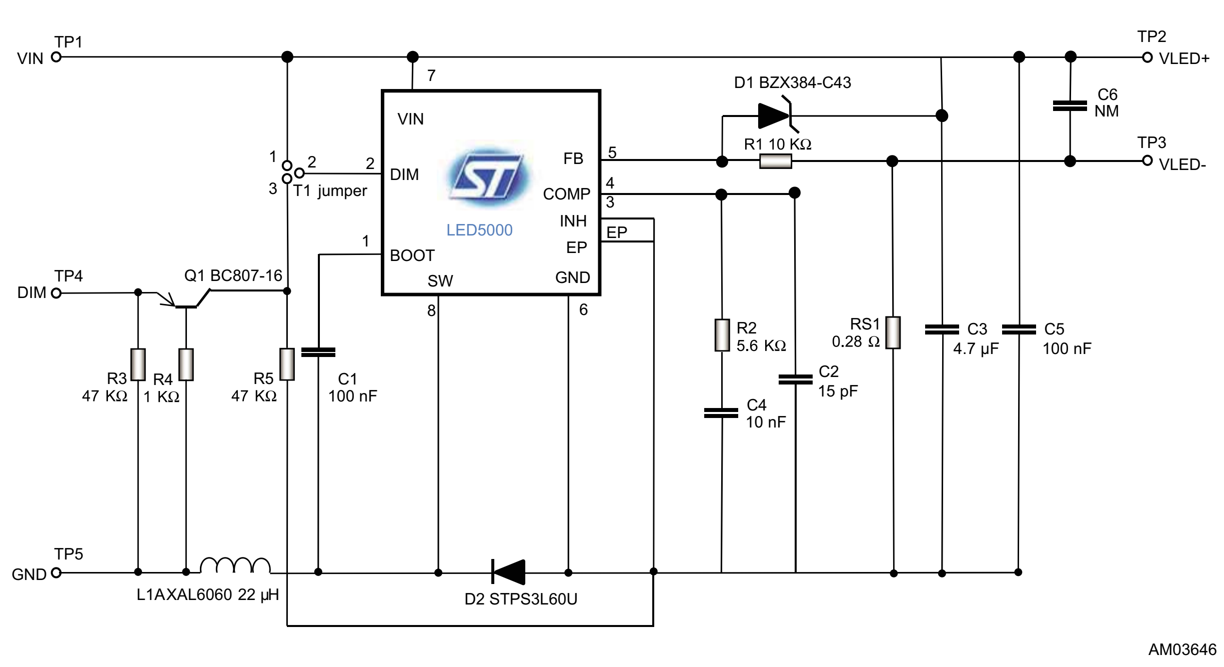
$$I_{LOAD\ MAX} \cong I_{SW\ MAX} \cdot (1 - D_{REAL})$$

where $I_{SW\ MAX}$ represents the rated current of the device.

The current capability is reduced by the term (1-D_{REAL}) and so, for example, with a duty cycle of 0.5, and considering an average current through the switch of 3 A, the maximum output current deliverable to the load is 1.5 A.

Figure 31 shows the circuit schematic for an LED current source based on the floating boost topology. The input voltage ranges from 12 to 36 V and it can drive a string composed of 11 LEDs with 0.7 A DC (V_{FW_LED} = 3.74 V so V_{OUT} = 41 V).

Figure 31. LED current source based on floating boost topology



The network D1, R1, R_S implements an inexpensive overvoltage protection. R1 effect can be neglected during the normal operation since the FB biasing current is negligible (tens of nA, see *Table 5: Electrical characteristics on page 8*) but it limits the current flowing in the Zener diode D1. In case the load is disconnected or in case of open LED:

Equation 72

$$V_{OUT} = V_{FB} + V_{ZENER\_DIODE}$$

$$I_{ZENER\_DIODE} = \frac{V_{FB}}{R_S + R_1}$$

R1 must be dimensioned to limit the D1 rated power so it is an inexpensive small signal Zener diode.

The circuitry Q1, R3, R4, R5 implements a level shifter to convert the dimming signal voltage levels (referred to GND) to the device rails, since the LED5000 local ground is floating. The LED5000 local GND level is:

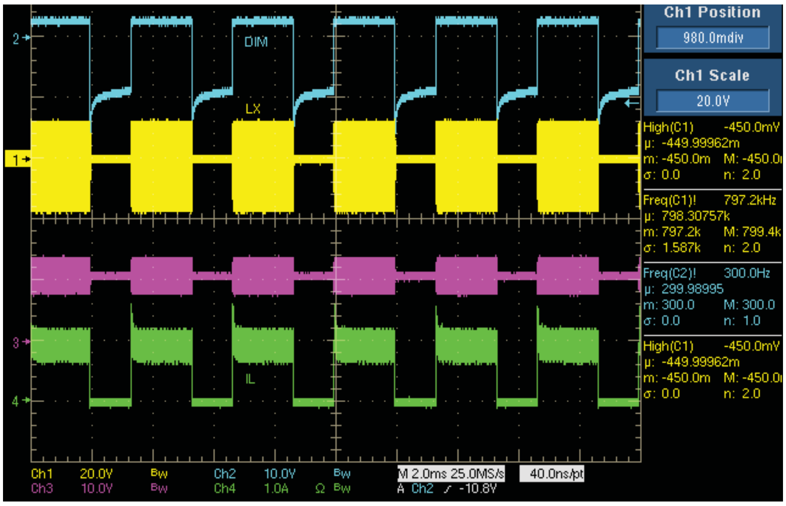
Equation 73

$$V_{LGND} = V_{IN} - V_{OUT}$$

where V_{LGND} represent the local GND value.

Figure 25 on page 40 shows the dimming operation: the light blue trace represents the DIM pin, the yellow the SW (high level is V_{IN}, low level is $V_{IN} - V_{OUT}$), the green trace the inductor current (see *Equation 69*) and the purple is the output voltage.

Figure 32. Floating BB dimming operation



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To design the compensation network for the boost topology please refer to *Section 6.4: Compensation network design for alternative topologies*.

Figure 33. Floating boost PCB layout (component side)

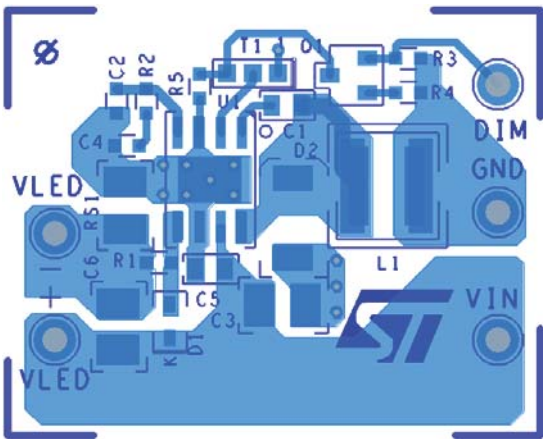

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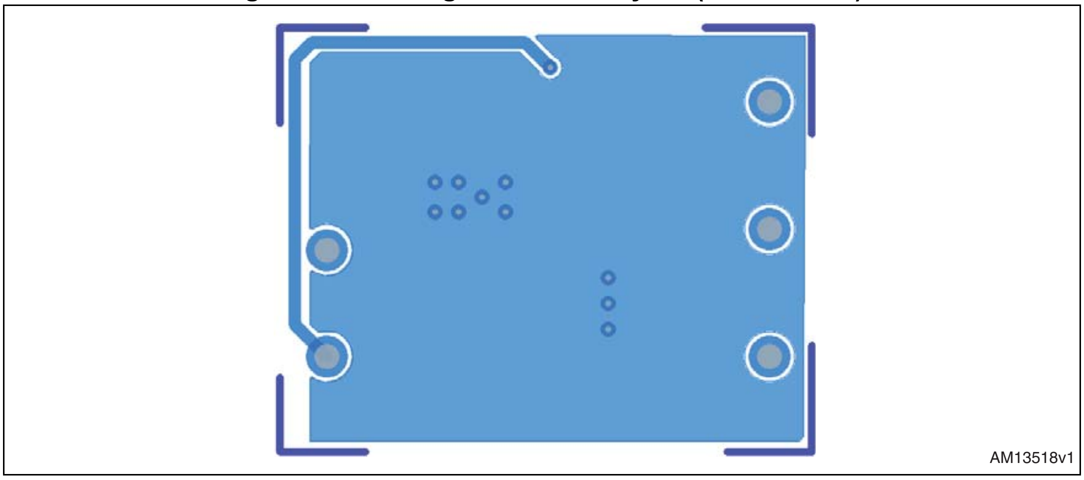
Figure 34. Floating boost PCB layout (bottom side)



6.4 Compensation network design for alternative topologies

The small signal analysis for the alternative topologies can be written as:

Equation 74

$$G_{CO}(s) = \frac{R_{LOAD}}{R_{CS}} \cdot \frac{(1-D)}{K_{Dx}} \cdot \frac{\left(1 - \frac{s}{\omega_{Z\_RHP}}\right) \cdot \left(1 + \frac{s}{\omega_Z}\right)}{\left(1 + \frac{s}{\omega_p}\right)} \cdot F_H(s)$$

that shares similar terms with *Equation 1 on page 14* which is valid for the buck (see *Equation 1*). In addition K_{DX} depends on the topology (different for boost and buck-boost) and ω_{Z_RHP} (*Equation 75*) is a zero in the right half plane:

Equation 75

$$\omega_{Z\_RHP} = \frac{R_{OUT} \cdot (1-D)^2}{L}$$

The RHP (right half plane) zero has the same 20 dB/dec rising gain magnitude as a conventional zero, but with 90 degree phase drop instead of lead. This characteristic cannot be compensated with the error amplifier network so the loop gain is designed to roll off at lower frequency in order to keep its contribution outside the small signal analysis.

ω_{Z_RHP} (see *Equation 75*) depends on the equivalent output resistance, inductor value and the duty cycle. As a consequence the minimum ω_{Z_RHP} over the input voltage range determines the maximum system bandwidth:

Equation 76

$$BW \leq BW_{MAX} = \frac{1}{K} \cdot \frac{\omega_{Z\_RHP\_MIN}}{2 \cdot \pi} \ll \frac{f_{SW}}{6}$$

the system phase margin depends on K.

This paragraph provides the equations to calculate the components of the compensation network once selected the power components and given the BW specification.

Table 10 summarizes the K_D, K_m, K parameters useful for the next calculations of the compensation network.

The DC gain of the total small loop is:

Equation 77

$$A_0 = G_m \cdot R_{EA} \cdot (1-D) \cdot \frac{R_S}{R_{CS}} \cdot \frac{1}{K_D}$$

where G_m is the error amplifier transconductance, R_{EA} the equivalent output resistance of the error amplifier, R_{CS} the internal current sense gain (for these parameters refer to *Table 5 on page 8*), R_S the sensing resistor value, and K_D can be calculated from *Table 10*.

The calculation of the components composing the compensation network depends on the relative position of the pole f_p (see *Equation 3 on page 15*) and the designed bandwidth BW.

Equation 78

$$f_p = \frac{\omega_p}{2 \cdot \pi} = \frac{1}{2 \cdot \pi} \cdot \frac{K_D}{C_O \cdot R_{LOAD}}$$

Table 10. BB and boost parameters

	Boost	Buck-boost
K_D	$1 + \frac{R_{LOAD}}{\frac{V_{OUT}}{I_{LED}}} + \frac{R_{LOAD} \cdot (1-D)^2}{R_{CS}} \cdot \left(\frac{1}{K_m} + \frac{K}{(1-D)}\right)$	$1 + \frac{R_{LOAD} \cdot D}{\frac{V_{OUT}}{I_{LED}}} + \frac{R_{LOAD} \cdot (1-D)^2}{R_{CS}} \cdot \left(\frac{1}{K_m} + \frac{K}{(1-D)}\right)$
K_m	$\frac{1}{(0.5-D) \cdot R_{CS} \cdot \frac{T_{SW}}{L} + \frac{V_{OUT} - V_{IN}}{V_{OUT}} \cdot R_{CS} \cdot \frac{T_{SW}}{L}}$	$\frac{1}{(0.5-D) \cdot R_{CS} \cdot \frac{T_{SW}}{L} + \frac{V_{OUT}}{V_{IN} + V_{OUT}} \cdot R_{CS} \cdot \frac{T_{SW}}{L}}$
k	$0.5 \cdot R_{CS} \cdot \frac{T_{SW}}{L} \cdot D \cdot (1-D)$	$0.5 \cdot R_{CS} \cdot \frac{T_{SW}}{L} \cdot D \cdot (1-D)$

6.4.1 f_p < BW

In case the pole f_p is inside the system bandwidth BW, the component values composing the compensation network can be calculated as:

Equation 79

$$R_C = \frac{R_{EA}}{A_0} \cdot \frac{BW}{f_p}$$

and

Equation 80

$$C_C = \frac{K}{2 \cdot \pi \cdot R_C \cdot BW}$$

Where *K* represents the leading position of the F_Z (*Equation 11 on page 17*) in respect to the system bandwidth. In general a decade (K = 10) gives enough phase margin to the overall small loop transfer function.

6.4.2 f_p > BW

In case the pole f_p is outside the system bandwidth BW, the component values composing the compensation network can be calculated as:

Equation 81

$$R_C = \frac{R_{EA}}{A_0} \cdot \frac{BW}{f_p}$$

and

Equation 82

$$C_C = \frac{K}{2 \cdot \pi \cdot R_C \cdot f_p}$$

where *K* represents the leading position of the F_Z (*Equation 11 on page 17*) in respect to the pole f_p.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Figure 35. HSOP8 package outline

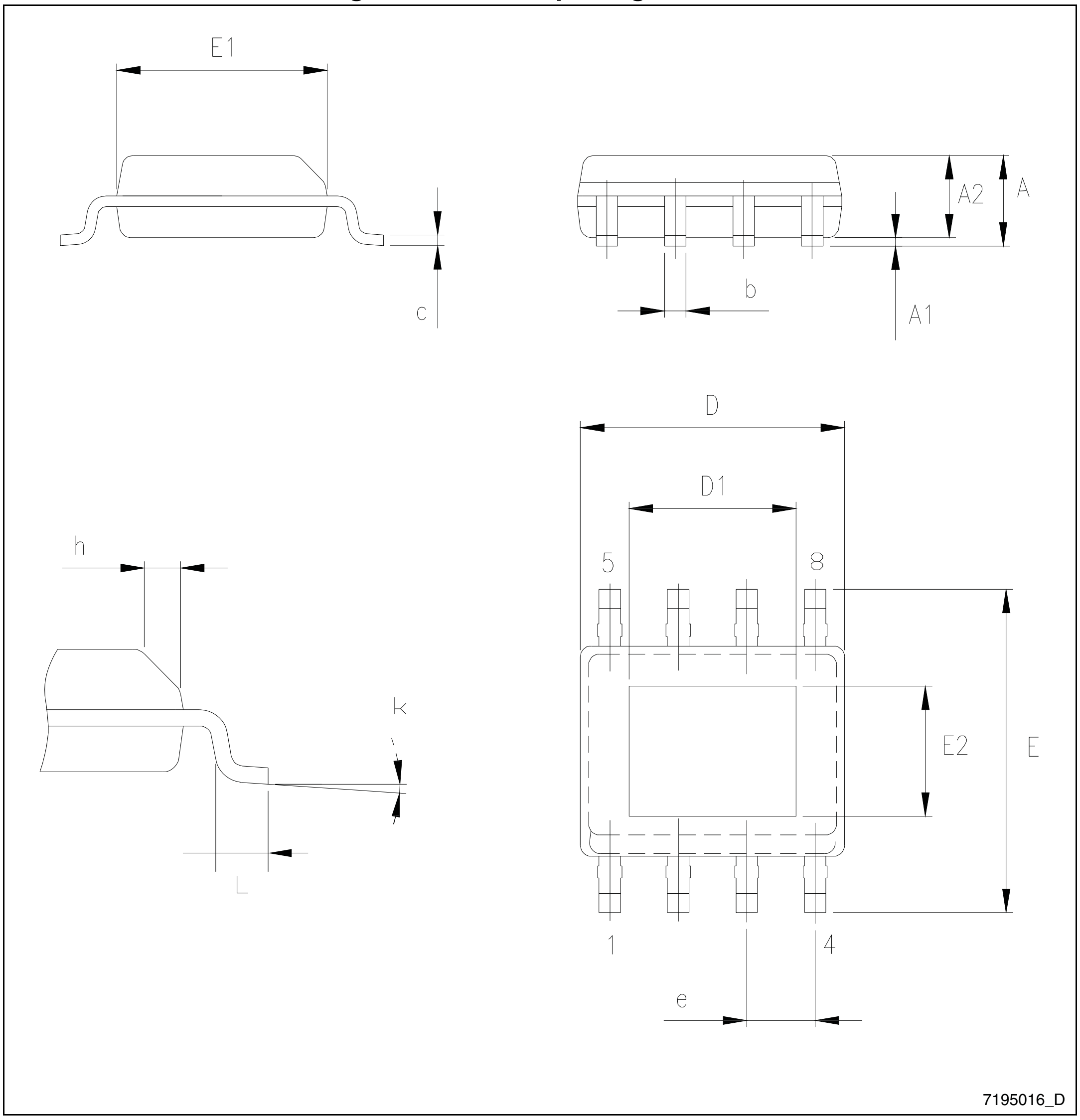


Table 11. HSOP8 package mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A			1.75
A1			0.15
A2	1.25		
b	0.38		0.51
c	0.17		0.25
D	4.80	4.90	5.00
D1	3.10	3.30	3.50
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
E2	2.20	2.40	2.60
e		1.27	
h	0.30		0.50
L	0.45		0.80
k	0°		8°

8 Ordering information

Table 12. Order code

Order code	Package	Packing
LED5000PHR	HSOP8	Tube

9 Revision history

Table 13. Document revision history

Date	Revision	Changes
31-Jan-2013	1	Initial release.
27-Feb-2014	2	Updated package name in package photo on page 1 (replaced “HPSO8” by “HSOP8”). Updated *Section : Features on page 1* (replaced “200 mW” by “200 mΩ” in “typical R_{DSON}”). Updated *Table 3 on page 7* (added note *1* below *Table 3*). Updated *Figure 3 on page 10* (replaced by a new block diagram). Updated *Table 6 on page 13* (changed “transconductance“ from 2200 µS to 220 µS). Updated *Section 5.2 on page 14* [updated text below *Equation 1* - added “equal to 0.38”. Added “where: ESR is the equivalent series resistor to the output capacitor.” below *Equation 2 on page 15*. Added “equal to 1.2 V” below *Equation 4 on page 15* to “(V_{PP} peak to peak amplitude)”]. Updated *Section 5.3* (updated text below *Equation 8 on page 16* - replaced “Where $A_{vo} = G_m \cdot R_o$” by “Where $A_{V0} = G_m \cdot R_0$ (R_O = output resistor of OTA = 200 * 10 ^ 6 Ω)”. Updated *Section 5.4* (updated *Equation 12 on page 18* - replaced “R_{SENSE}” by “R_S”, added “where R_S is the resistor put in series to the LED string” below *Equation 12*). Updated *Section 5.6* (updated text below *Equation 16 on page 20* - replaced text “R_S the sensing resistor value” by “R_S the resistor put in series to the LED string” and “R_{CS} the current sense gain” by “R_{CS} the equivalent sensing resistor of the current sense circuitry equal to 0.38”). Updated *Section 5.7 on page 20* (replaced “r_{LED}= 1.1 W” by “r_{LED}= 1.1 Ω“ in “Design specification”) . Updated *Equation 29 on page 26* (added equations). Updated *Equation 41 on page 31* (replaced “T_{SW}“ by “T_{SW_EQ}“, added text “where: $T_{SW\_EQ} = (T_{RISE} + T_{FALL})/2$ = 12 nS” below *Equation 41*). Updated text below *Equation 43 on page 31* (updated package name - replaced “HPSO8” by “HSOP8”, replaced “60” of “the estimated junction temperature” by “40”). Updated *Figure 20 on page 34* (replaced by a new application circuit - replaced “R56” by “R27”). Updated *Table 9 on page 35* [replaced “MSS7341”-473MLD” by “XFL6060-473ME”, “I_{SAT} = 1.0 A (30% drop)” by “I_{SAT} = 1.8 A (10% drop)” and “I_{RMS} = 1.85 A (40 °C rise)” by “I_{RMS} = 3.7 A (40 °C rise)”. of “L1“ component]. Updated *Figure 24 on page 39*, *Figure 29 on page 43* and *Figure 31 on page 46* (replaced by new figures). Updated *Section 7 on page 51* (updated titles, reversed order of *Figure 35* and *Table 11*, minor modifications). Updated package name in *Table 12 on page 53* (replaced “HPSO8” by “HSOP8”). Updated cross-references throughout document. Minor modifications throughout document.
28-Apr-2014	3	Updated *Section 6.1: Inverting buck-boost on page 37* (replaced 10 LEDs by 5 LEDs in text above *Figure 24 on page 39*).
30-Sep-2014	4	Updated *Figure 24 on page 39* (replaced by new figure).

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