MAX7033

315MHz/433MHz ASK Superheterodyne Receiver with AGC Lock

General Description

The MAX7033 fully integrated low-power CMOS superheterodyne receiver is ideal for receiving amplitude shift-keyed (ASK) data in the 300MHz to 450MHz frequency range. The receiver has an RF input signal range of -114dBm to 0dBm. With few external components and a low-current power-down mode, it is ideal for cost-sensitive and power-sensitive applications typical in consumer markets. The MAX7033 consists of a low-noise amplifier (LNA), a fully differential image-rejection mixer, an on-chip phase-locked loop (PLL) with integrated voltage-controlled oscillator (VCO), a 10.7MHz IF limiting amplifier stage with received-signal-strength indicator (RSSI), and analog baseband data-recovery circuitry. The MAX7033 also has a discrete one-step automatic gain control (AGC) that reduces the LNA gain by 35dB when the RF input signal exceeds -62dBm. The AGC circuitry offers an externally controlled hold feature.

The MAX7033 is available in 28-pin TSSOP and 32-pin TQFN packages and is specified over the extended (-40°C to +105°C) temperature range.

Applications

- Security Systems
- Garage Door Openers
- Home Automation
- Remote Controls
- Local Telemetry
- Wireless Sensors

Features

- Optimized for 315MHz or 433MHz Band
- Operates from Single +3.3V or +5.0V Supplies
- High Dynamic Range with On-Chip AGC
- AGC Hold Circuit
- 1ms AGC Release Time
- Selectable Image-Rejection Center Frequency
- Selectable x64 or x32 f_{LO}/f_{XTAL} Ratio
- Low 5.2mA Operating Supply Current
- < 3.5µA Low-Current Power-Down Mode for Efficient Power Cycling
- 250µs Startup Time
- Built-In 44dB RF Image Rejection
- Better than -114dBm Receive Sensitivity
- -40°C to +105°C Operation

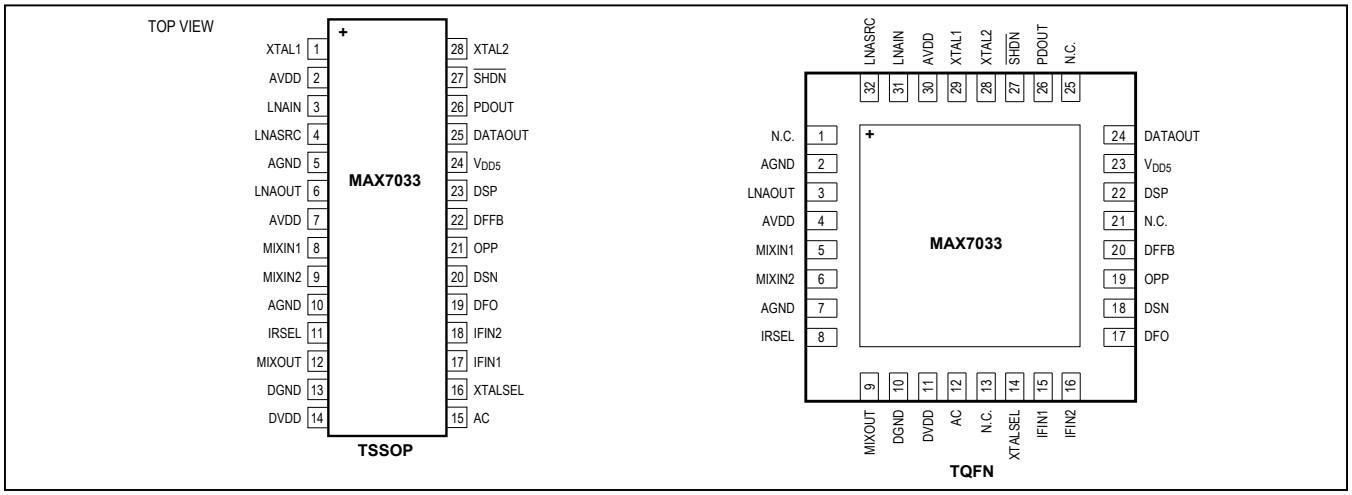
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX7033EUI+	-40°C to +105°C	28 TSSOP
MAX7033ETJ+	-40°C to +105°C	32 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Typical Application Circuit appears at end of data sheet.

Pin Configurations



maxim integrated™

Absolute Maximum Ratings

V_{DD5} to AGND .....-0.3V to +6.0V
AVDD to AGND .....-0.3V to +4.0V
DVDD to DGND.....-0.3V to +4.0V
AGND to DGND .....-0.1V to +0.1V
IRSEL, DATAOUT, XTALSEL,
AC, $\overline{SHDN}$ to AGND ..... -0.3V to (V_{DD5} + 0.3V)
All Other Pins to AGND.....-0.3V to (V_{DVDD} + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
28-Pin TSSOP (derate 12.8mW/°C above +70°C).1025.6mW
32-Thin QFN (derate 21.3mW/°C above +70°C) ...1702.1mW
Operating Temperature Range..... -40°C to +105°C
Junction Temperature.....+150°C
Storage Temperature Range..... -60°C to +150°C
Lead Temperature (soldering 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (+3.3V Operation)

(*Typical Application Circuit*, V_{AVDD} = V_{DVDD} = V_{DD5} = +3.0V to +3.6V, no RF signal applied, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{DD5} = +3.3V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V_{AVDD}, V_{DVDD}	+3.3V nominal supply voltage		3.0	3.3	3.6	V
Supply Current	I_{DD}	$V_{\overline{SHDN}}$ = V_{DVDD}	f_{RF} = 315MHz		5.2	6.23	mA
			f_{RF} = 433MHz		5.7	6.88	
Shutdown Supply Current	$I_{\overline{SHDN}}$	$V_{\overline{SHDN}}$ = 0V, $V_{XTALSEL}$ = 0V	f_{RF} = 315MHz		2.6		µA
			f_{RF} = 433MHz		3.5	8.0	
Input-Voltage Low	V_{IL}					0.4	V
Input-Voltage High	V_{IH}			V_{DVDD} - 0.4			V
Input Logic Current High	I_{IH}				10		µA
Image-Reject Select Voltage (Note 2)		f_{RF} = 433MHz, V_{IRSEL} = V_{DD5}		V_{DD5} - 0.4			V
		f_{RF} = 375MHz, V_{IRSEL} = V_{DD5}/2		1.1		V_{DD5} - 1.0	
		f_{RF} = 315MHz, V_{IRSEL} = 0V				0.4	
DATAOUT Output-Voltage Low	V_{OL}	I_{SINK} = 10µA			0.125		V
DATAOUT Output-Voltage High	V_{OH}	I_{SOURCE} = 10µA		V_{DVDD} - 0.125			V

DC Electrical Characteristics (+5.0V Operation)

(*Typical Application Circuit*, V_{DD5} = +4.5V to +5.5V, no RF signal applied, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DD5} = +5.0V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD5}	+5.0V nominal supply voltage		4.5	5.0	5.5	V
Supply Current	I_{DD}	$V_{\overline{SHDN}}$ = V_{DD5}	f_{RF} = 315MHz		5.2	6.4	mA
			f_{RF} = 433MHz		5.7	6.76	
Shutdown Supply Current	$I_{\overline{SHDN}}$	$V_{\overline{SHDN}}$ = 0V, $V_{XTALSEL}$ = 0V	f_{RF} = 315MHz		3.7		µA
			f_{RF} = 433MHz		4.2	9.8	
Input-Voltage Low	V_{IL}					0.4	V

Electrical Characteristics (continued)

(*Typical Application Circuit*, V_{DD5} = +4.5V to +5.5V, no RF signal applied, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DD5} = +5.0V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input-Voltage High	V_{IH}		V_{DD5} - 0.4			V
Input Logic Current High	I_{IH}			15		µA
Image-Reject Select Voltage (Note 2)		f_{RF} = 433MHz, V_{IRSEL} = V_{DD5}	V_{DD5} - 0.4			V
		f_{RF} = 375MHz, V_{IRSEL} = V_{DD5}/2	1.1		V_{DD5} - 1.5	
		f_{RF} = 315MHz, V_{IRSEL} = 0V			0.4	
DATAOUT Output-Voltage Low	V_{OL}	I_{SINK} = 10µA		0.125		V
DATAOUT Output-Voltage High	V_{OH}	I_{SOURCE} = 10µA	V_{DD5} - 0.125			V

AC Electrical Characteristics

(*Typical Application Circuit*, V_{AVDD} = V_{DVDD} = V_{DD5} = +3.0V to +3.6V, all RF inputs are referenced to 50Ω, f_{RF} = 315MHz, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{DD5} = +3.3V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS							
Startup Time	t_{ON}	Time for valid signal detection after $V_{\overline{SHDN}}$ = V_{DVDD}			250		µs
Receiver Input Frequency	f_{RF}			300		450	MHz
Maximum Receiver Input Level		Modulation depth > 18dB			0		dBm
Sensitivity (Note 3)		Average carrier power level			-120		dBm
		Peak power level			-114		
AGC Hysteresis		LNA gain from low to high			8		dB
		Switching time from low to high gain			1		ms
Maximum Data Rate		Manchester coded			33		kbps
		NRZ coded			66		
LNA IN HIGH-GAIN MODE							
Input Impedance	Z_{IN_LNA}	Normalized to 50Ω	f_{RF} = 433MHz		1 - j3.4		
			f_{RF} = 375MHz		1 - j3.9		
			f_{RF} = 315MHz		1 - j4.7		
1dB Compression Point	$P1dB_{LNA}$				-22		dBm
Input-Referred 3rd-Order Intercept	$IIP3_{LNA}$				-12		dBm
LO Signal Feedthrough to Antenna					-80		dBm
Noise Figure	NF_{LNA}				3		dB

Electrical Characteristics (continued)

(*Typical Application Circuit*, V_{AVDD} = V_{DVDD} = V_{DD5} = +3.0V to +3.6V, all RF inputs are referenced to 50Ω, f_{RF} = 315MHz, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{DD5} = +3.3V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LNA IN LOW-GAIN MODE							
Input Impedance	Z_{IN_LNA}	Normalized to 50Ω (Note 4)	f_{RF} = 433MHz		1 - j3.4		
			f_{RF} = 375MHz		1 - j3.9		
			f_{RF} = 315MHz		1 - j4.7		
1dB Compression Point	$P1dB_{LNA}$				-10		dBm
Input-Referred 3rd-Order Intercept	$IIP3_{LNA}$				-7		dBm
LO Signal Feedthrough to Antenna					-80		dBm
Noise Figure	NF_{LNA}				3		dB
Voltage-Gain Reduction		AGC enabled (depends on tank Q)			35		dB
MIXER							
Input-Referred 3rd-Order Intercept	$IIP3_{MIX}$				-18		dBm
Output Impedance	Z_{OUT_MIX}				330		Ω
Noise Figure	NF_{MIX}				16		dB
Image Rejection (Not Including LNA Tank)		f_{RF} = 433MHz, V_{IRSEL} = V_{DVDD}			42		dB
		f_{RF} = 375MHz, V_{IRSEL} = V_{DVDD}/2			44		
		f_{RF} = 315MHz, V_{IRSEL} = 0V			44		
LNA/Mixer Voltage Gain		330Ω IF filter load	LNA in high-gain mode		48		dB
			LNA in low-gain mode		13		
INTERMEDIATE FREQUENCY (IF)							
Input Impedance	Z_{IN_IF}				330		Ω
Operating Frequency	f_{IF}	Bandpass response			10.7		MHz
3dB Bandwidth					10		MHz
RSSI Linearity					±0.5		dB
RSSI Dynamic Range					80		dB
RSSI Level		P_{RFIN} < -120dBm			1.15		V
		P_{RFIN} > 0dBm, AGC enabled			2.2		
AGC Threshold		LNA gain from low to high			1.39		V
		LNA gain from high to low			1.98		
DATA FILTER							
Maximum Bandwidth					50		kHz
DATA SLICER							
Comparator Bandwidth					100		kHz

Electrical Characteristics (continued)

(*Typical Application Circuit*, V_{AVDD} = V_{DVDD} = V_{DD5} = +3.0V to +3.6V, all RF inputs are referenced to 50Ω, f_{RF} = 315MHz, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{DD5} = +3.3V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum Load Capacitance	C_{LOAD}				10		pF
Output High Voltage					V_{DD5}		V
Output Low Voltage					0		V
CRYSTAL OSCILLATOR							
Crystal Frequency (Note 5)	f_{XTAL}	f_{RF} = 433MHz	$V_{XTALSEL}$ = 0V		6.6128		MHz
			$V_{XTALSEL}$ = VDD5		13.2256		
		f_{RF} = 315MHz	$V_{XTALSEL}$ = 0V		4.7547		
			$V_{XTALSEL}$ = VDD5		9.5094		
Crystal Tolerance					50		ppm
Input Capacitance		From each pin to ground			6.2		pF

Note 1: 100% tested at T_A = +25°C. Guaranteed by design and characterization over temperature.

Note 2: IRSEL is internally set to 375MHz IR mode. It can be left open when the 375MHz image-rejection setting is desired. Bypass to AGND with a 1nF capacitor in a noisy environment.

Note 3: BER = 2 x 10^{-3}, Manchester encoded, data rate = 4kbps, IF bandwidth = 280kHz.

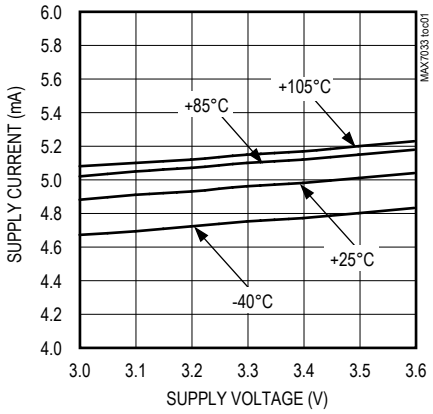
Note 4: Input impedance is measured at the LNAIN pin. Note that the impedance includes the 15nH inductive degeneration connected from the LNA source to ground. The equivalent input circuit is 50Ω in series with 2.2pF.

Note 5: Crystal oscillator frequency for other RF carrier frequency within the 300MHz to 450MHz range is (f_{RF} - 10.7MHz)/64 for $V_{XTALSEL}$ = 0V, and (f_{RF} - 10.7MHz)/32 for XTALSEL = V_{DD5}.

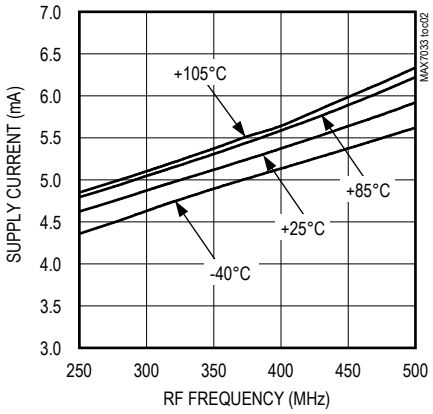
Typical Operating Characteristics

(*Typical Application Circuit*, V_{AVDD} = V_{DVDD} = V_{DD5} = +3.3V, f_{RF} = 315MHz, T_A = +25°C, unless otherwise noted.)

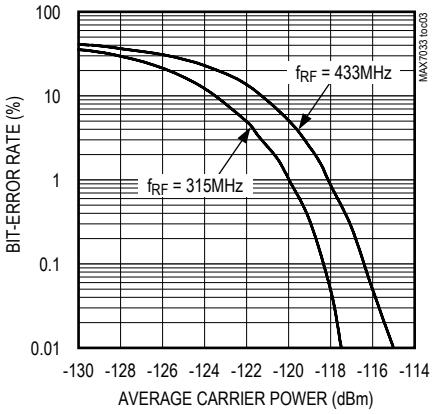
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. RF FREQUENCY



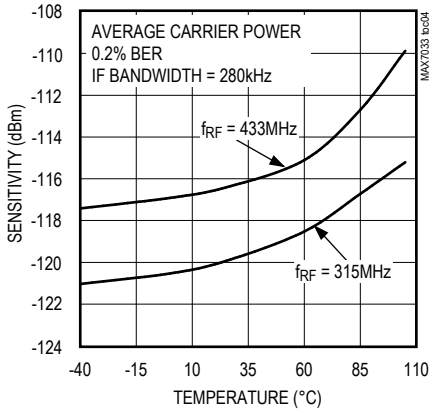
BIT-ERROR RATE vs. AVERAGE CARRIER POWER



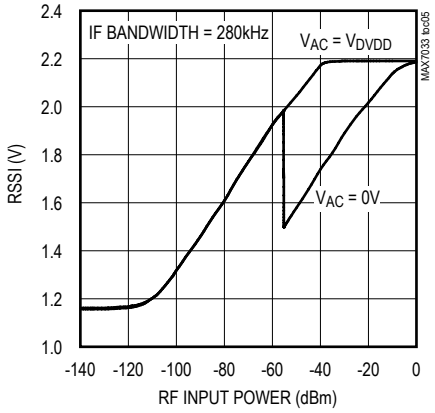
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, $V_{AVDD} = V_{DVDD} = V_{DD5} = +3.3V$, $f_{RF} = 315MHz$, $T_A = +25°C$, unless otherwise noted.)

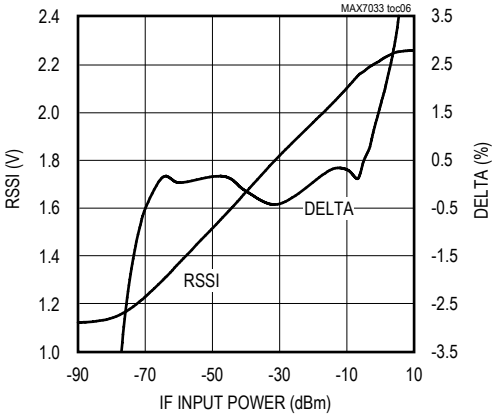
SENSITIVITY vs. TEMPERATURE



RSSI vs. RF INPUT POWER



RSSI AND DELTA vs. IF INPUT POWER



LNA/MIXER VOLTAGE GAIN vs. IF FREQUENCY

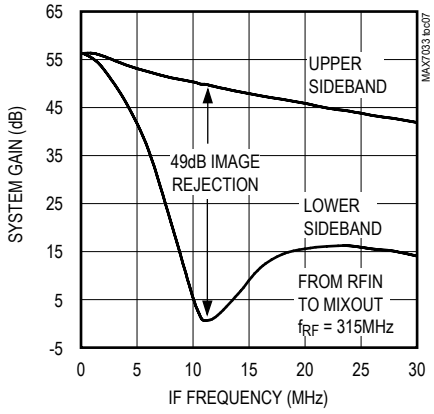


IMAGE REJECTION vs. RF FREQUENCY

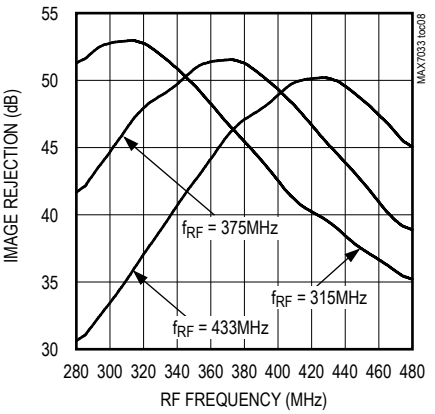
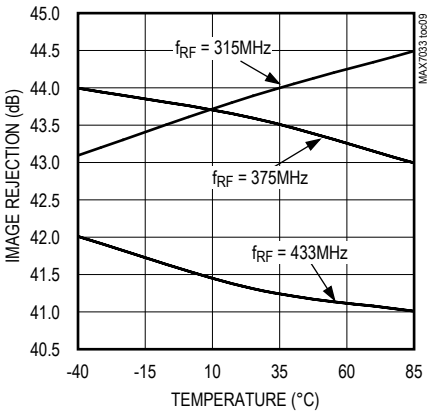


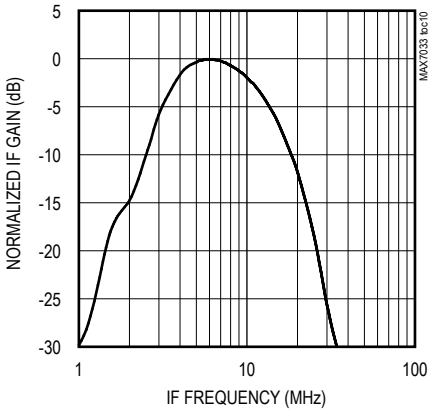
IMAGE REJECTION vs. TEMPERATURE



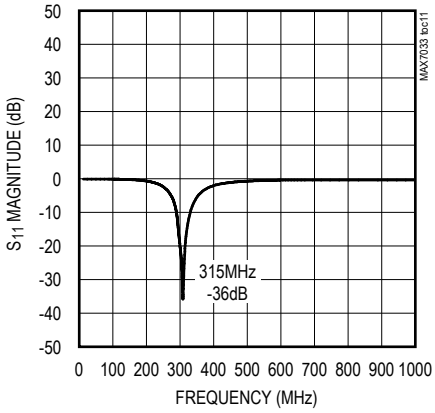
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, $V_{AVDD} = V_{DVDD} = V_{DD5} = +3.3V$, $f_{RF} = 315MHz$, $T_A = +25°C$, unless otherwise noted.)

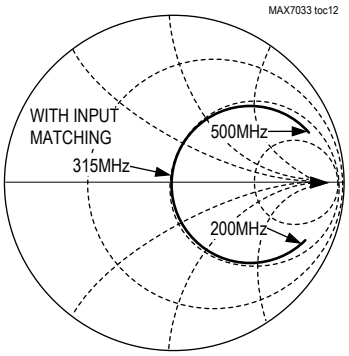
NORMALIZED IF GAIN vs. IF FREQUENCY



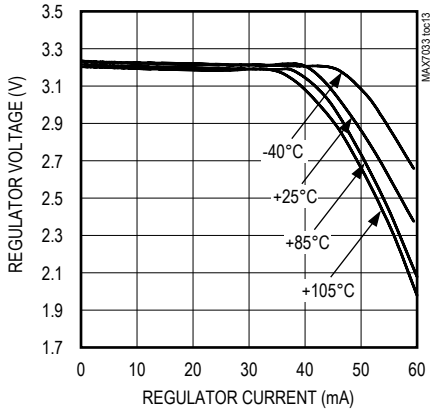
S_{11} LOG MAGNITUDE PLOT OF RFIN



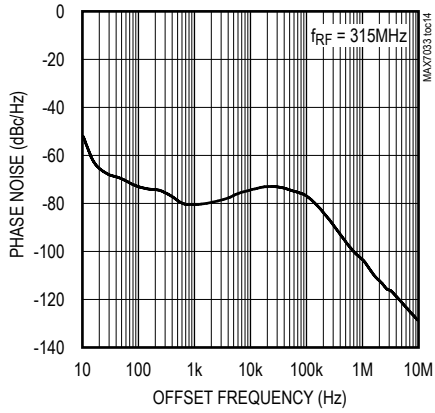
S_{11} SMITH CHART PLOT OF RFIN



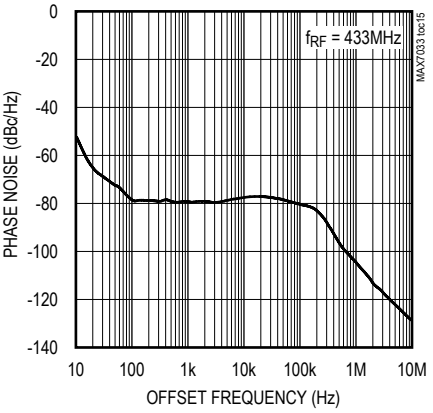
REGULATOR VOLTAGE vs. REGULATOR CURRENT



PHASE NOISE vs. OFFSET FREQUENCY



PHASE NOISE vs. OFFSET FREQUENCY



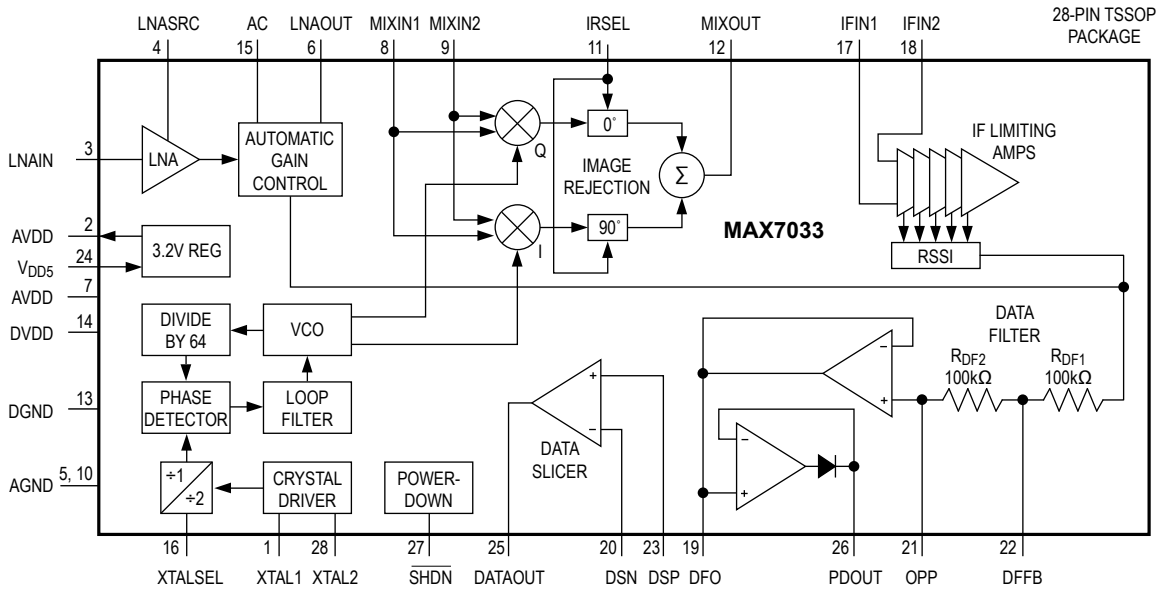
Pin Description

PIN		NAME	FUNCTION
TSSOP	TQFN		
1	29	XTAL1	Crystal Input 1 (see the *Phase-Locked Loop* section)
2, 7	4, 30	AVDD	Positive Analog Supply Voltage. For +5V operation, pin 2 is the output of an on-chip +3.2V low-dropout regulator, and should be bypassed to AGND with a 0.1µF capacitor as close as possible to the pin. Pin 7 must be externally connected to the supply from pin 2, and bypassed to AGND with a 0.01µF capacitor as close as possible to the pin (see the *Voltage Regulator* section and the *Typical Application Circuit*).
3	31	LNAIN	Low-Noise Amplifier Input (see the *Low-Noise Amplifier* section)
4	32	LNASRC	Low-Noise Amplifier Source for External Inductive Degeneration. Connect inductor to ground to set the LNA input impedance (see the *Low-Noise Amplifier* section).
5, 10	2, 7	AGND	Analog Ground
6	3	LNAOUT	Low-Noise Amplifier Output. Connect to mixer input through an LC tank filter (see the *Low-Noise Amplifier* section).
8	5	MIXIN1	1st Differential Mixer Input. Connect to LC tank filter from LNAOUT.
9	6	MIXIN2	2nd Differential Mixer Input. Connect through a 100pF capacitor to V_{DD3} side of the LC tank.
11	8	IRSEL	Image-Rejection Select. Set V_{IRSEL} = 0V to center image rejection at 315MHz. Leave IRSEL unconnected to center image rejection at 375MHz. Set V_{IRSEL} = V_{DD5} to center image rejection at 433MHz.
12	9	MIXOUT	330Ω Mixer Output. Connect to the input of the 10.7MHz bandpass filter.
13	10	DGND	Digital Ground
14	11	DVDD	Positive Digital Supply Voltage. Connect to both of the AVDD pins. Bypass to DGND with a 0.01µF capacitor as close as possible to the pin (see the *Typical Application Circuit*).
15	12	AC	Automatic Gain Control. See Figure 1. Internally pulled down to AGND with a 100kΩ resistor.
16	14	XTALSEL	Crystal Divider Ratio Select. Drive XTALSEL low to select f_{LO}/f_{XTAL} ratio of 64, or drive XTALSEL high to select f_{LO}/f_{XTAL} ratio of 32.
17	15	IFIN1	1st Differential Intermediate-Frequency Limiter Amplifier Input. Bypass to AGND with a 1500pF capacitor as close to the pin as possible.
18	16	IFIN2	2nd Differential Intermediate-Frequency Limiter Amplifier Input. Connect to the output of a 10.7MHz bandpass filter.
19	17	DFO	Data Filter Output
20	18	DSN	Negative Data Slicer Input
21	19	OPP	Noninverting Op-Amp Input for the Sallen-Key Data Filter
22	20	DFFB	Data-Filter Feedback Node. Input for the feedback of the Sallen-Key data filter.
23	22	DSP	Positive Data Slicer Input
24	23	V_{DD5}	+5V Supply Voltage. Bypass to AGND with a 0.01µF capacitor as close as possible to the pin. For +5V operation, V_{DD5} is the input to an on-chip voltage regulator whose +3.2V output appears at the pin 2 AVDD pin (see the *Voltage Regulator* section and the *Typical Application Circuit*).
25	24	DATAOUT	Digital Baseband Data Output
26	26	PDOUT	Peak-Detector Output
27	27	$\overline{SHDN}$	Power-Down Select Input. Drive high to power up the IC. Internally pulled down to AGND with a 100kΩ resistor.

Pin Description (continued)

PIN		NAME	FUNCTION
TSSOP	TQFN		
28	28	XTAL2	Crystal Input 2. Can also be driven with an external reference oscillator (see the *Crystal Oscillator* section).
—	1, 13, 21, 25	N.C.	No Connection
—	—	EP	Exposed Pad (TQFN Only). Connect EP to GND.

Functional Diagram



Detailed Description

The MAX7033 CMOS superheterodyne receiver and a few external components provide the complete receive chain from the antenna to the digital output data. Depending on signal power and component selection, data rates as high as 33kbps Manchester (66kbps NRZ) can be achieved.

The MAX7033 is designed to receive binary ASK data modulated in the 300MHz to 450MHz frequency range. ASK modulation uses a difference in amplitude of the carrier to represent logic 0 and logic 1 data.

Voltage Regulator

For operation with a single +3.0V to +3.6V supply voltage, connect AVDD, DVDD, and V_{DD5} to the supply voltage. For operation with a single +4.5V to +5.5V supply voltage, connect V_{DD5} to the supply voltage. An on-chip voltage regulator drives one of the AVDD pins to approximately +3.2V. For proper operation, DVDD and both the AVDD pins must be connected together. Bypass V_{DD5}, DVDD, and the pin 7 AVDD pin to AGND with 0.01µF capacitors, and the pin 2 AVDD pin to AGND with a 0.1µF capacitor, all placed as close as possible to the pins.

Low-Noise Amplifier

The LNA is an nMOS cascode amplifier with off-chip inductive degeneration, with a 3.0dB noise figure and an IIP3 of -12dBm. The gain and noise figures are dependent on both the antenna matching network at the LNA input and the LC tank network between the LNA output and the mixer inputs.

The off-chip inductive degeneration is achieved by connecting an inductor from LNASRC to AGND. This inductor sets the real part of the input impedance at LNAIN, allowing for a more flexible input impedance match, such as a typical PCB trace antenna. A nominal value for this inductor with a 50Ω input impedance is 15nH, but is affected by PCB trace.

The LC tank filter connected to LNAOUT comprises L3 and C2 (see the *Typical Application Circuit*). Select L3 and C2 to resonate at the desired RF input frequency. The resonant frequency is given by:

$$f_{RF} = \frac{1}{2\pi\sqrt{L_{TOTAL} \times C_{TOTAL}}}$$

where:

L_{TOTAL} = L3 + $L_{PARASITICS}$.

C_{TOTAL} = C2 + $C_{PARASITICS}$.

$L_{PARASITICS}$ and $C_{PARASITICS}$ include inductance and capacitance of the PCB traces, package pins, mixer input impedance, LNA output impedance, etc. These parasitics at high frequencies cannot be ignored, and can have a dramatic effect on the tank filter center frequency. Lab experimentation should be done to optimize the center frequency of the tank.

Automatic Gain Control

When the AC pin is low, the automatic gain-control (AGC) circuit monitors the RSSI output. As the RSSI output reaches 1.98V, which corresponds to RF input level of -62dBm, the AGC switches on the LNA gain reduction resistor. The resistor reduces the LNA gain by 35dB, thereby reducing the RSSI output by about 500mV. The LNA resumes high-gain mode when the RSSI level drops back below 1.39V (approximately -70dBm at RF input) for 1ms. The AGC has a hysteresis of 8dB. With the AGC function, the MAX7033 can reliably produce an ASK output for RF input levels up to 0dBm with modulation depth of 18dB.

When the AC pin is high and $\overline{SHDN}$ goes high, the AGC circuit is disabled and the LNA is always in high gain mode. The AGC function can be resumed by bringing the AC pin low when $\overline{SHDN}$ is high.

The MAX7033 features an AGC lock function that is asserted when the level at the AC pin transitions from low to high while $\overline{SHDN}$ is high. Locking the AGC locks the LNA in the current gain state. As shown in Figure 1, the AGC lock function can be enabled or disabled as long as the $\overline{SHDN}$ pin is high. Changing the state of AC when $\overline{SHDN}$ is low has no effect.

Mixer

A unique feature of the MAX7033 is the integrated image rejection of the mixer. This device eliminates the need for a costly front-end SAW filter for most applications. Advantages of not using a SAW filter are increased sensitivity, simplified antenna matching, less board space, and lower cost.

The mixer cell is a pair of double balanced mixers that perform an IQ downconversion of the RF input to the 10.7MHz IF from a low-side injected LO (i.e., $f_{LO} = f_{RF} - f_{IF}$). The image-rejection circuit then combines these signals to achieve 44dB of image rejection. Low-side injection

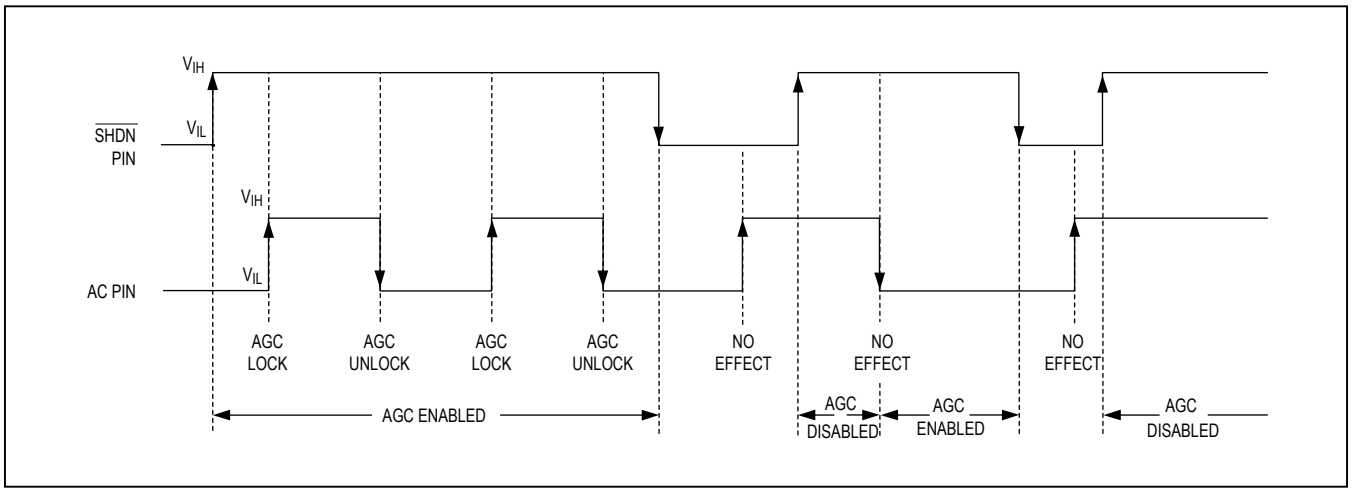


Figure 1. AGC Lock Activation Cycles

is required due to the on-chip image-rejection architecture. The IF output is driven by a source follower biased to create a driving-point impedance of 330Ω; this provides a good match to the off-chip 330Ω ceramic IF filter.

The IRSEL pin is a logic input that selects one of the three possible image-rejection frequencies. When V_{IRSEL} = 0V, the image rejection is tuned to 315MHz. V_{IRSEL} = V_{DD5}/2 tunes the image rejection to 375MHz, and V_{IRSEL} = V_{DD5} tunes the image rejection to 433MHz. The IRSEL pin is internally set to V_{DD5}/2 (image rejection at 375MHz) when it is left unconnected, thereby eliminating the need for an external V_{DD5}/2 voltage.

Phase-Locked Loop

The PLL block contains a phase detector, charge pump, integrated loop filter, VCO, asynchronous 64x clock divider, and crystal oscillator driver. Besides the crystal, this PLL does not require any external components. The VCO generates a low-side LO. The relationship between the RF, IF, and crystal frequencies is given by:

$$f_{XTAL} = \frac{f_{RF} - f_{IF}}{32 \times M}$$

where:

M = 1 ($V_{XTALSEL}$ = V_{DD5}) or 2 ($V_{XTALSEL}$ = 0V)

To allow the smallest possible IF bandwidth (for best sensitivity), minimize the tolerance of the reference crystal.

Table 1. Component Values for Typical Application Circuit

COMPONENT	VALUE FOR f_{RF} = 433MHz	VALUE FOR f_{RF} = 315MHz	DESCRIPTION
C1	100pF	100pF	5%
C2	2pF	4pF	± 0.1pF
C3	100pF	100pF	5%
C4	100pF	100pF	5%
C5	1500pF	1500pF	10%
C6	220pF	220pF	5%
C7	470pF	470pF	5%
C8	0.47µF	0.47µF	20%
C9	220pF	220pF	10%
C10	0.01µF	0.01µF	20%
C11	0.1µF	0.1µF	20%
C12	15pF	15pF	Depends on XTAL
C13	15pF	15pF	Depends on XTAL
C14	0.01µF	0.01µF	20%
C15	0.01µF	0.01µF	20%
L1	56nH	120nH	5% or better*
L2	15nH	15nH	5% or better*
L3	15nH	27nH	5% or better*
R1	5.1kΩ	5.1kΩ	5%
R2	Open	Open	—
R3	Short	Short	—
X1 (÷64)	6.6128MHz**	4.7547MHz**	Crystek or Hong Kong Crystal
X1 (÷32)	13.2256MHz**	9.5094MHz**	Crystek or Hong Kong Crystal
Y1	10.7MHz ceramic filter	10.7MHz ceramic filter	Murata

**Wire wound recommended.*

***Crystal frequencies shown are for ÷64 ($V_{XTALSEL}$ = 0V) and ÷32 ($V_{XTALSEL}$ = V_{DD})*

Intermediate Frequency and RSSI

The IF section presents a differential 330Ω load to provide matching for the off-chip ceramic filter. The six internal AC-coupled limiting amplifiers produce an overall gain of approximately 65dB, with a bandpass-filter-type response centered near the 10.7MHz IF frequency 1 with a 3dB bandwidth of approximately 10MHz. The RSSI circuit demodulates the IF by producing a DC output proportional to the log of the IF signal level, with a slope of approximately 14.2mV/dB (see the *Typical Operating Characteristics*).

Applications Information

Crystal Oscillator

The crystal oscillator in the MAX7033 is designed to present a capacitance of approximately 3pF between the XTAL1 and XTAL2. If a crystal designed to oscillate with a different load capacitance is used, the crystal is pulled away from its stated operating frequency, introducing an error in the reference frequency. Crystals designed to operate with higher differential load capacitance always pull the reference frequency higher. For example, a 4.7547MHz crystal designed to operate with a 10pF load capacitance oscillates at 4.7563MHz with the MAX7033, causing the receiver to be tuned to 315.1MHz rather than 315.0MHz, an error of about 100kHz, or 320ppm.

In actuality, the oscillator pulls every crystal. The crystal's natural frequency is really below its specified frequency, but when loaded with the specified load capacitance, the crystal is pulled and oscillates at its specified frequency. This pulling is already accounted for in the specification of the load capacitance. Additional pulling can be calculated if the electrical parameters of the crystal are known. The frequency pulling is given by:

$$f_P = \frac{C_M}{2}\left(\frac{1}{C_{CASE}+C_{LOAD}} - \frac{1}{C_{CASE}+C_{SPEC}}\right)\times 10^6$$

where:

f_P is the amount the crystal frequency pulled in ppm.

C_M is the motional capacitance of the crystal.

C_{CASE} is the case capacitance.

C_{SPEC} is the specified load capacitance.

C_{LOAD} is the actual load capacitance.

When the crystal is loaded as specified, i.e., C_{LOAD} = C_{SPEC}, the frequency pulling equals zero.

It is possible to use an external reference oscillator in place of a crystal to drive the VCO. AC-couple the external oscillator to XTAL2 with a 1000pF capacitor. Drive XTAL2 with a signal level of approximately -10dBm. AC-couple XTAL1 to ground with a 1000pF capacitor.

Data Filter

The data filter is implemented as a 2nd-order lowpass Sallen-Key filter. The pole locations are set by the combination of two on-chip resistors and two external capacitors. Adjusting the value of the external capacitors changes the corner frequency to optimize for different data rates. The corner frequency should be set to approximately 1.5 times the fastest expected data rate from the transmitter. Keeping the corner frequency near the data rate rejects any noise at higher frequencies, resulting in an increase in receiver sensitivity.

The configuration shown in Figure 2 can create a Butterworth or Bessel response. The Butterworth filter offers a very flat amplitude response in the passband and a rolloff rate of 40dB/decade for the two-pole filter. The Bessel filter has a linear phase response, which works well for filtering digital data. To calculate the value of C5 and C6, use the following equations, along with the coefficients in Table 2:

$$C5 = \frac{b}{a(100k)(\pi)(f_C)}$$

$$C6 = \frac{a}{4(100k)(\pi)(f_C)}$$

where f_C is the desired 3dB corner frequency.

Table 2. Coefficents to Calculate C5 and C6

FILTER TYPE	a	b
Butterworth (Q = 0.707)	1.414	1.000
Bessel (Q = 0.577)	1.3617	0.618

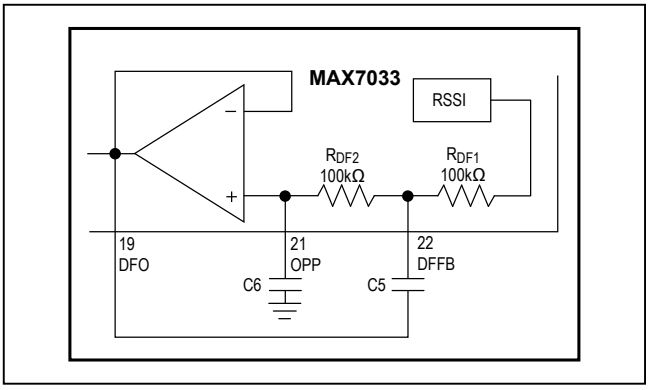


Figure 2. Sallen-Key Lowpass Data Filter

For example, to choose a Butterworth filter response with a corner frequency of 5kHz:

$$C5 = \frac{1.000}{(1.414)(100k\Omega)(3.14)(5kHz)} \approx 450pF$$

$$C6 = \frac{1.414}{(4)(100k\Omega)(3.14)(5kHz)} \approx 225pF$$

Choosing standard capacitor values changes C5 to 470pF and C6 to 220pF, as shown in the *Typical Application Circuit*.

Data Slicer

The data slicer takes the analog output of the data filter and converts it to a digital signal. This is achieved by using a comparator and comparing the analog input to a threshold voltage. One input is supplied by the data filter output. Both comparator inputs are accessible offchip to allow for different methods of generating the slicing threshold, which is applied to the second comparator input.

The suggested data slicer configuration uses a resistor (R1) connected between DSN and DSP with a capacitor (C4) from DSN to DGND (Figure 3). This configuration averages the analog output of the filter and sets the threshold to approximately 50% of that amplitude. With this configuration, the threshold automatically adjusts as the analog signal varies, minimizing the possibility for errors in the digital data. The values of R1 and C4 affect how fast the threshold tracks to the analog amplitude. Be sure to keep the corner frequency of the RC circuit much lower than the lowest expected data rate.

Note that a long string of zeros or ones can cause the threshold to drift. This configuration works best if a coding scheme, such as Manchester coding, which has an equal number of zeros and ones, is used.

To prevent continuous toggling of DATAOUT in the absence of an RF signal due to noise, add hysteresis to the data slicer as shown in Figure 4.

Peak Detector

The peak-detector output (PDOUT), in conjunction with an external RC filter, creates a DC output voltage equal to the peak value of the data signal. The resistor provides a path for the capacitor to discharge, allowing the peak detector to dynamically follow peak changes of the data-filter output voltage. For faster data slicer response, use the circuit shown in Figure 5.

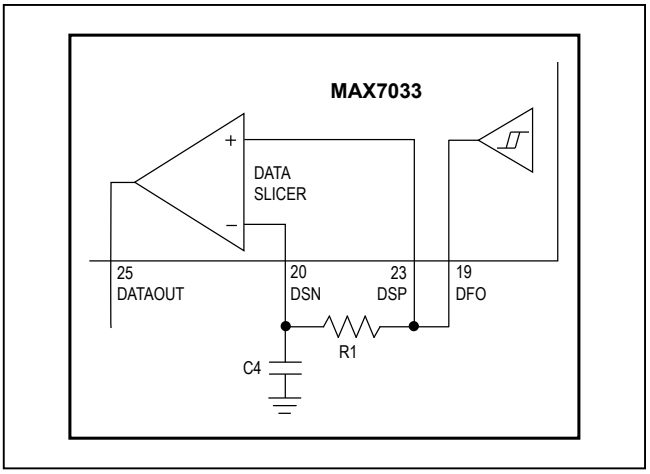


Figure 3. Generating Data Slicer Threshold

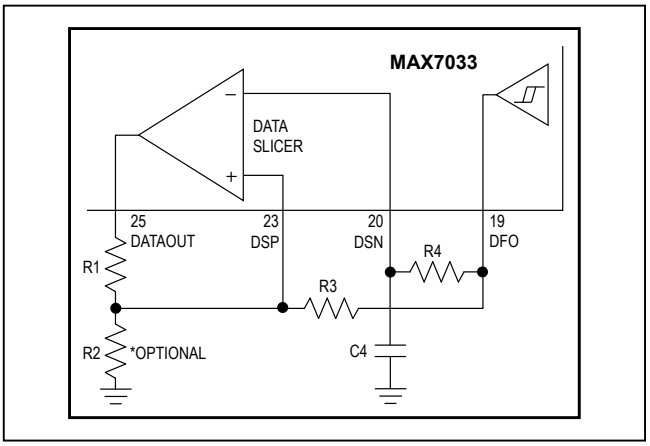


Figure 4. Generating Data Slicer Hysteresis

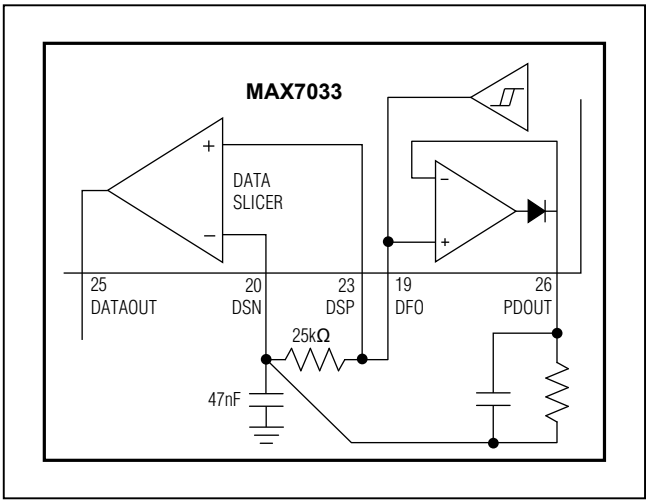


Figure 5. Using PDOUT for Faster Startup

Layout Considerations

A properly designed PCB is an essential part of any RF/microwave circuit. On high-frequency inputs and outputs, use controlled-impedance lines and keep them as short as possible to minimize losses and radiation. At high frequencies, trace lengths that are on the order of λ/10 or longer act as antennas.

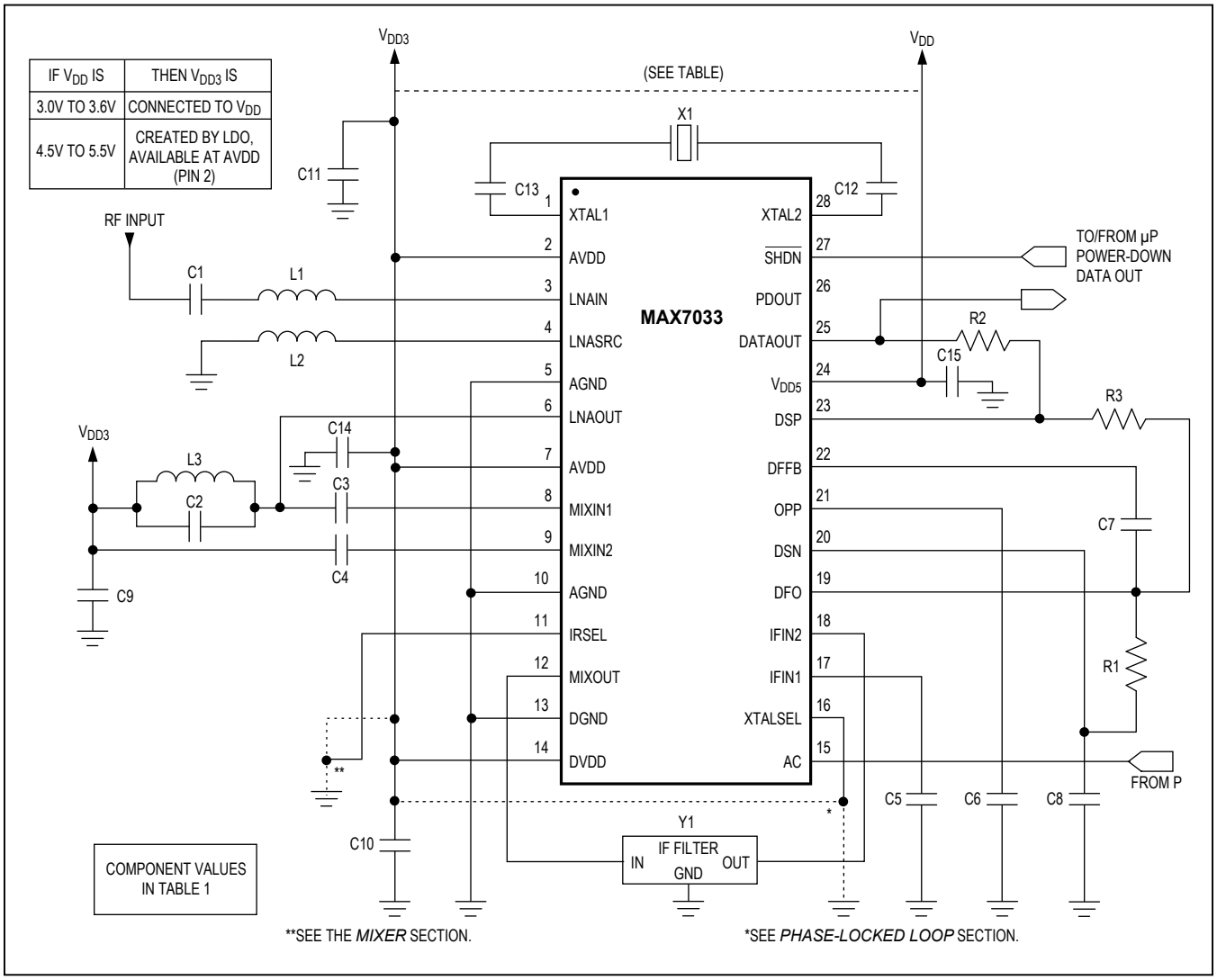
Keeping the traces short also reduces parasitic inductance. Generally, 1in of a PCB trace adds about 20nH of parasitic inductance. The parasitic inductance can have a dramatic effect on the effective inductance of a passive component. For example, a 0.5in trace connecting a 100nH inductor adds an extra 10nH of inductance or 10%.

To reduce the parasitic inductance, use wider traces and a solid ground or power plane below the signal traces. Also, use low-inductance connections to ground on all GND pins, and place decoupling capacitors close to all power-supply pins.

Control Interface Considerations

When operating the MAX7033 with a +4.5V to +5.5V supply voltage, the $\overline{SHDN}$ and AC pins can be driven by a microcontroller with either 3V or 5V interface logic levels. When operating the MAX7033 with a +3.0V to +3.6V supply, only 3V logic from the microcontroller is allowed.

Typical Application Circuit



Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
28 TSSOP	U28+1	21-0066	90-0171
32 TQFN-EP	T3255+3	21-0140	90-0001

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/04	Initial release	—
1	1/11	Updated *Ordering Information*, *Pin Configurations*, *Absolute Maximum Ratings*, *DC Electrical Characteristics*, *AC Electrical Characteristics*, *Typical Operating Characteristics*, *Pin Description*, *Functional Diagram*, *Voltage Regulator and Layout Considerations sections*, *Typical Application Circuit*, *Chip Information*, and *Package Information*	1–9, 13, 14, 15
2	9/11	Updated input impedance values in *AC Electrical Characteristics* table; updated TOC3 and TOC4 labels in *Typical Operating Characteristics*; clarified equations in *Pin Description* and *Phase-Locked Loop* and *Crystal Oscillator* sections; updated components in Table 1; and added new *Control Interface Considerations* section	3–6, 11–14
3	4/14	Updated *Applications* and *General Description*	1

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