19-3195; Rev 1; 2/05

MAXIM

Dual, Low-Power, 500Mbps ATE Driver/Comparator with 35mA Load

General Description

The MAX9967 dual, low-power, high-speed, pin electronics driver/comparator/load (DCL) IC includes, for each channel, a three-level pin driver, a dual comparator, variable clamps, and an active load. The driver features a wide voltage range and high-speed operation, includes high-impedance and active-termination (3rd-level drive) modes, and is highly linear even at low-voltage swings. The dual comparator provides low dispersion (timing variation) over a wide variety of input conditions. The clamps provide damping of high-speed device-under-test (DUT) waveforms when the device is configured as a high-impedance receiver. The programmable load supplies up to 35mA of source and sink current. The load facilitates contact/continuity testing, at-speed parametric testing of IOH and IOL, and pullup of high-output-impedance devices.

The MAX9967A provides tight matching of gain and offset for the drivers, and offset for the comparators and active load, allowing reference levels to be shared across multiple channels in cost-sensitive systems. Use the MAX9967B for system designs that incorporate independent reference levels for each channel.

The MAX9967 provides high-speed, differential control inputs with optional internal termination resistors that are compatible with ECL, LVPECL, LVDS, and GTL. ECL/LVPECL or flexible open-collector outputs with optional internal pullup resistors are available for the comparators. These features significantly reduce the discrete component count on the circuit board.

A 3-wire, low-voltage, CMOS-compatible serial interface programs the low-leakage, slew-rate limit, and tri-state/terminate operational configurations of the MAX9967.

The MAX9967's operating range is -1.5V to +6.5V with power dissipation of only 1.15W per channel. The device is available in a 100-pin, 14mm x 14mm body, and 0.5mm pitch TQFP. An exposed 8mm x 8mm die pad on the top of the package facilitates efficient heat removal. The device is specified to operate with an internal die temperature of +70°C to +100°C, and features a die temperature monitor output.

Applications

Low-Cost Mixed-Signal/System-on-Chip ATE

Commodity Memory ATE

PCI or VXI Programmable Digital Instruments

Features

- ♦ **Low Power Dissipation: 1.15W/Channel (typ)**
- ♦ **High Speed: 500Mbps at $3V_{P-P}$**
- ♦ **Programmable 35mA Active-Load Current**
- ♦ **Low Timing Dispersion**
- ♦ **Wide -1.5V to +6.5V Operating Range**
- ♦ **Active Termination (3rd-Level Drive)**
- ♦ **Low Leakage Mode: 60nA**
- ♦ **Integrated Clamps**
- ♦ **Interfaces Easily with Most Logic Families**
- ♦ **Integrated PMU Connection**
- ♦ **Digitally Programmable Slew Rate**
- ♦ **Internal Termination Resistors**
- ♦ **Low Gain and Offset Error**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9967ADCCQ*	0°C to +70°C	100 TQFP-EPR**
MAX9967AGCCQ*	0°C to +70°C	100 TQFP-EPR**
MAX9967ALCCQ	0°C to +70°C	100 TQFP-EPR**
MAX9967AMCCQ*	0°C to +70°C	100 TQFP-EPR**
MAX9967AQCCQ*	0°C to +70°C	100 TQFP-EPR**
MAX9967ARCCQ*	0°C to +70°C	100 TQFP-EPR**
MAX9967BDCCQ	0°C to +70°C	100 TQFP-EPR**
MAX9967BGCCQ	0°C to +70°C	100 TQFP-EPR**
MAX9967BLCCQ	0°C to +70°C	100 TQFP-EPR**
MAX9967BMCCQ	0°C to +70°C	100 TQFP-EPR**
MAX9967BQCCQ*	0°C to +70°C	100 TQFP-EPR**
MAX9967BRCCQ	0°C to +70°C	100 TQFP-EPR**

*Future product—contact factory for availability.
**EPR = Exposed pad reversed (TOP).

Pin Configuration and Typical Application Circuits appear at end of data sheet.
Selector Guide appears at end of data sheet.

Dual, Low-Power, 500Mbps ATE Driver/Comparator with 35mA Load

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +11.5V
V_{EE} to GND .....-7.0V to +0.3V
V_{CC} - V_{EE} .....-0.3V to +18V
GS to GND .....±1V
DUT_, LDH_, LDL_ to GND .....-2.5V to +7.5V
DATA_, NDATA_, RCV_, NRCV_, LDEN_, NLDEN_ to GND .....-2.5V to +5.0V
DATA_ to NDATA_, RCV_ to NRCV_, LDEN_ to NLDEN_ .....±1.5V
$V_{CCO\_}$ to GND .....-0.3V to +5V
SCLK, DIN, $\overline{CS}$, $\overline{RST}$, TDATA_, TRCV_, TLDEN_ to GND .....-1.0V to +5V
DHV_, DLV_, DTV_, CHV_, CLV_, COM_, FORCE_, SENSE_ to GND .....-2.5V to +7.5V
CPHV_ to GND .....-2.5V to +8.5V
CPLV_ to GND .....-3.5V to +7.5V
DHV_ to DLV_ .....±10V
DHV_ to DTV_ .....±10V
DLV_ to DTV_ .....±10V
CHV_ or CLV_ to DUT_ .....±10V
CH_, NCH_, CL_, NCL_ to GND (open collector) ....-2.5V to +5V
CH_, NCH_, CL_, NCL_ to GND (open emitter) ..($V_{CCO\_}$ + 1.0V)
All Other Pins to GND .....(V_{EE} - 0.3V) to (V_{CC} + 0.3V)
Current Out of CH_, NCH_, CL_, NCL_ (open emitter) ....+50mA
DHV_, DLV_, DTV_, CHV_, CLV_, CPHV_, CPLV_ Current .....±10mA
TEMP Current .....-0.5mA to +20mA
DUT_ Short Circuit to -1.5V to +6.5V .....Continuous
Power Dissipation (T_A = +70°C)
MAX9967_ _CCQ (derate 167mW/°C above +70°C) 13.3W*
Storage Temperature Range .....-65°C to +150°C
Junction Temperature .....+125°C
Lead Temperature (soldering, 10s) .....+300°C

**Dissipation wattage values are based on still air with no heat sink. Actual maximum allowable power dissipation is a function of heat extraction technique and may be substantially higher.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +9.75V, V_{EE} = -5.25V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +70°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Positive Supply	V_{CC}		9.5	9.75	10.5	V
Negative Supply	V_{EE}		-6.5	-5.25	-4.5	V
Positive Supply Current (Note 2)	I_{CC}	$V_{LDH\_}$ = $V_{LDL\_}$ = 0		120	155	mA
		$V_{LDH\_}$ = $V_{LDL\_}$ = 3.5V, load enabled, driver = high impedance		220	255	
Negative Supply Current (Note 2)	I_{EE}	$V_{LDH\_}$ = $V_{LDL\_}$ = 0		-220	-265	mA
		$V_{LDH\_}$ = $V_{LDL\_}$ = 3.5V, load enabled, driver = high impedance		-320	-365	
Power Dissipation	P_D	(Notes 2, 3)		2.3	2.9	W
DUT_ CHARACTERISTICS						
Operating Voltage Range	V_{DUT}	(Note 4)	-1.5		+6.5	V
Leakage Current in High-Impedance Mode	I_{DUT}	LLEAK = 0; 0 ≤ $V_{DUT\_}$ ≤ 3V			±1.5	µA
		LLEAK = 0; $V_{DUT\_}$ = -1.5V, +6.5V			±3	
Leakage Current in Low-Leakage Mode		LLEAK = 1; 0 ≤ $V_{DUT\_}$ ≤ 3V, T_J < +90°C			±60	nA
		LLEAK = 1; $V_{DUT\_}$ = -1.5V, +6.5V; T_J < +90°C			±110	
		LLEAK = 1; 0 ≤ $V_{DUT\_}$ ≤ 3V, $V_{LDL\_}$= $V_{LDH\_}$ = 3.5V; T_J < +90°C			±80	
		LLEAK = 1; $V_{DUT\_}$ = -1.5V, +6.5V; $V_{LDL\_}$ = $V_{LDH\_}$ = 3.5V; T_J < +90°C			±160	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -5.25V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +70°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Combined Capacitance	C_{DUT}	Driver in term mode (DUT_ = DTV_)		4.0		pF
		Driver in high-impedance mode		8.0		
Low-Leakage Enable Time		(Notes 5, 6)		20		µs
Low-Leakage Disable Time		(Notes 6, 7)		20		µs
Low-Leakage Recovery		Time to return to the specified maximum leakage after a 3V, 4V/ns step at DUT_		4		µs
LEVEL PROGRAMMING INPUTS (DHV_, DLV_, DTV_, CHV_, CLV_, CPHV_, CPLV_, COM_, LDH_, LDL_)						
Input Bias Current	I_{BIAS}				±25	µA
Settling time		To 0.1% of full-scale change (Note 7)		1		µs
DIFFERENTIAL CONTROL INPUTS (DATA_, NDATA_, RCV_, NRCV_, LDEN_, NLDEN_)						
Input High Voltage	V_{IH}		-1.6		+3.5	V
Input Low Voltage	V_{IL}		-2.0		+3.1	V
Differential Input Voltage	V_{DIFF}		±0.15		±1.0	V
Input Bias Current		MAX9967_DCCQ, MAX9967_MCCQ			±25	µA
Input Termination Voltage	$V_{TDATA\_}$, $V_{TRCV\_}$, $V_{TLDEN\_}$	MAX9967_GCCQ, MAX9967_LCCQ, and MAX9967_QCCQ	-2.1		+3.5	V
Input Termination Resistor		MAX9967_GCCQ, MAX9967_LCCQ, and MAX9967_QCCQ, between signal and corresponding termination voltage input	48		52	Ω
SINGLE-ENDED CONTROL INPUTS ($\overline{CS}$, SCLK, DIN, $\overline{RST}$)						
Internal Threshold Reference	V_{THRINT}		1.05	1.25	1.45	V
Internal Reference Output Resistance	R_O			20		kΩ
External Threshold Reference	V_{THR}		0.43		1.73	V
Input High Voltage	V_{IH}		V_{THR} + 0.2		3.5	V
Input Low Voltage	V_{IL}		-0.1		V_{THR} - 0.2	V
Input Bias Current	I_B				±25	µA
SERIAL INTERFACE TIMING (Figure 6)						
SCLK Frequency	f_{SCLK}				50	MHz
SCLK Pulse-Width High	t_{CH}		8			ns
SCLK Pulse-Width Low	t_{CL}		8			ns
$\overline{CS}$ Low to SCLK High Setup	t_{CSS0}		3.5			ns
$\overline{CS}$ High to SCLK High Setup	t_{CSS1}		3.5			ns

Dual, Low-Power, 500Mbps ATE Driver/Comparator with 35mA Load

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -5.25V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +70°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SCLK High to $\overline{CS}$ High Hold	t_{CSH1}			3.5			ns
DIN to SCLK High Setup	t_{DS}			3.5			ns
DIN to SCLK High Hold	t_{DH}			3.5			ns
$\overline{CS}$ Pulse Width High	t_{CSWH}			20			ns
TEMPERATURE MONITOR (TEMP)							
Nominal Voltage		T_J = +70°C, $R_L \geq 10M\Omega$			3.43		V
Temperature Coefficient					+10		mV/°C
Output Resistance					15		kΩ
DRIVERS (Note 8)							
DC OUTPUT CHARACTERISTICS ($R_L \geq 10M\Omega$)							
DHV_, DLV_, DTV_, Output Offset Voltage	V_{OS}	At DUT_ with $V_{DHV\_}$, $V_{DTV\_}$, $V_{DLV\_}$ independently tested at +1.5V	MAX9967A			±15	mV
			MAX9967B			±100	
DHV_, DLV_, DTV_, Output Offset Temperature Coefficient					±65		µV/°C
DHV_, DLV_, DTV_, Gain	A_V	Measured with $V_{DHV\_}$, $V_{DLV\_}$, and $V_{DTV\_}$ at 0 and 4.5V	MAX9967A (Note 9)	0.999	1.00	1.001	V/V
			MAX9967B	0.96		1.001	
DHV_, DLV_, DTV_, Gain Temperature Coefficient					-35		ppm/°C
Linearity Error		V_{DUT} = 1.5V, 3V (Note 10)				±5	mV
		Full range (Notes 10, 11)				±15	
DHV_ to DLV_ Crosstalk		$V_{DLV\_}$ = 0; $V_{DHV\_}$ = 200mV, 6.5V				±2	mV
DLV_ to DHV_ Crosstalk		$V_{DHV\_}$ = 5V; $V_{DLV\_}$ = -1.5V, +4.8V				±2	mV
DTV_ to DLV_ and DHV_ Crosstalk		$V_{DHV\_}$ = 3V; $V_{DLV\_}$ = 0; $V_{DTV\_}$ = -1.5V, +6.5V				±2	mV
DHV_ to DTV_ Crosstalk		$V_{DTV\_}$ = 1.5V; $V_{DLV\_}$ = 0; $V_{DHV\_}$ = 1.6V, 3V				±3	mV
DLV_ to DTV_ Crosstalk		$V_{DTV\_}$ = 1.5V; $V_{DHV\_}$ = 3V; $V_{DLV\_}$ = 0, 1.4V				±3	mV
DHV_, DTV_, DLV_ DC Power-Supply Rejection Ratio	PSRR	(Note 12)		40			dB
Maximum DC Drive Current	$I_{DUT\_}$			±60		±120	mA
DC Output Resistance	$R_{DUT\_}$	$I_{DUT\_}$ = ±30mA (Note 13)		49	50	51	Ω
DC Output Resistance Variation	$\Delta R_{DUT\_}$	$I_{DUT\_}$ = ±1mA to ±8mA			0.5		Ω
		$I_{DUT\_}$ = ±1mA to ±40mA			1	2.5	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -5.25V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +70°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Sense Resistance	R_{SENSE}		7.50	10	13.75	kΩ
Force Resistance	R_{FORCE}		320	400	500	Ω
Force Capacitance	C_{FORCE}			2		pF
DYNAMIC OUTPUT CHARACTERISTICS (Z_L = 50Ω)						
Drive-Mode Overshoot		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 0.1V		30		mV
		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 1V		40		
		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 3V		50		
Term-Mode Overshoot		(Note 14)		0		mV
Settling Time to Within 25mV		3V step (Note 15)		10		ns
Settling Time to Within 5mV		3V step (Note 15)		20		ns
TIMING CHARACTERISTICS (Z_L = 50Ω) (Note 16)						
Prop Delay, Data to Output	t_{PDD}			2.2		ns
Prop Delay Match, t_{LH} vs. t_{HL}		$3V_{P-P}$		±50		ps
Prop Delay Match, Drivers Within Package		(Note 17)		40		ps
Prop Delay Temperature Coefficient				+3		ps/°C
Prop Delay Change vs. Pulse Width		$3V_{P-P}$, 40MHz, 2.5ns to 22.5ns pulse width, relative to 12.5ns pulse width		±60		ps
Prop Delay Change vs. Common-Mode Voltage		$V_{DHV\_}$ - $V_{DLV\_}$ = 1V, $V_{DHV\_}$ = 0 to 6V		85		ps
Prop Delay, Drive to High Impedance	t_{PDDZ}	$V_{DHV\_}$ = 1.0V, $V_{DLV\_}$ = -1.0V, $V_{DTV\_}$ = 0		3.2		ns
Prop Delay, High Impedance to Drive	t_{PDZD}	$V_{DHV\_}$ = 1.0V, $V_{DLV\_}$ = -1.0V, $V_{DTV\_}$ = 0		3.3		ns
Prop Delay, Drive to Term	t_{PDDT}	$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V		2.5		ns
Prop Delay, Term to Drive	t_{PDTD}	$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V		2.2		ns
DYNAMIC PERFORMANCE (Z_L = 50Ω)						
Rise and Fall Time	t_R, t_F	$0.2V_{P-P}$, 20% to 80%		370		ps
		$1V_{P-P}$, 10% to 90%		630		
		$3V_{P-P}$, 10% to 90%	1.0	1.3	1.5	ns
		$5V_{P-P}$, 10% to 90%		2.0		
Rise and Fall Time Match	t_R vs. t_F	$3V_{P-P}$, 10% to 90%		±0.03		ns
SC1 = 0, SC0 = 1 Slew Rate		Percent of full speed (SC0 = SC1 = 0), $3V_{P-P}$, 20% to 80%		75		%
SC1 = 1, SC0 = 0 Slew Rate		Percent of full speed (SC0 = SC1 = 0), $3V_{P-P}$, 20% to 80%		50		%
SC1 = 1, SC0 = 1 Slew Rate		Percent of full speed (SC0 = SC1 = 0), $3V_{P-P}$, 20% to 80%		25		%

Dual, Low-Power, 500Mbps ATE Driver/Comparator with 35mA Load

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -5.25V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +70°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Pulse Width (Note 18)		$0.2V_{P-P}$			650		ps
		$1V_{P-P}$			1.0		ns
		$3V_{P-P}$			2.0		
		$5V_{P-P}$			2.9		
Data Rate (Note 19)		$0.2V_{P-P}$			1700		Mbps
		$1V_{P-P}$			1000		
		$3V_{P-P}$			500		
		$5V_{P-P}$			350		
Dynamic Crosstalk		(Note 20)			10		mV_{P-P}
Rise and Fall Time, Drive to Term	t_{DTR}, t_{DTF}	$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V, 10% to 90%, Figure 1a (Note 21)			1.6		ns
Rise and Fall Time, Term to Drive	t_{TDR}, t_{TDF}	$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V, 10% to 90%, Figure 1b (Note 21)			0.7		ns
COMPARATORS (Note 8)							
DC CHARACTERISTICS							
Input Voltage Range	V_{IN}	(Note 4)		-1.5		+6.5	V
Differential Input Voltage	V_{DIFF}			±8			V
Hysteresis	V_{HYST}				0		mV
Input Offset Voltage	V_{OS}	$V_{DUT\_}$ = 1.5V	MAX9967A			±20	mV
			MAX9967B			±100	
Input Offset Voltage Temperature Coefficient					±50		µV/°C
Common-Mode Rejection Ratio (Note 22)	CMRR	$V_{DUT\_}$ = 0, 3V		47	78		dB
		$V_{DUT\_}$ = 0, 6.5V		54	78		
		$V_{DUT\_}$ = -1.5V, +6.5V		44	61		
Linearity Error (Note 10)		$V_{DUT\_}$ = 1.5V, 3V				±3	mV
		$V_{DUT\_}$ = 6.5V				±5	
		$V_{DUT\_}$ = -1.5V				±25	
V_{CC} Power-Supply Rejection Ratio (Note 12)	PSRR	$V_{DUT\_}$ = -1.5V, +6.5V		57	80		dB
V_{EE} Power-Supply Rejection Ratio (Note 12)	PSRR	$V_{DUT\_}$ = 0, 6.5V		44	64		dB
		$V_{DUT\_}$ = -1.5V		33	60		
AC CHARACTERISTICS (Note 23)							
Minimum Pulse Width (Note 24)	$t_{PW(MIN)}$	MAX9967_DCCQ, MAX9967_GCCQ, MAX9967_LCCQ, MAX9967_RCCQ			0.7		ns
		MAX9967_MCCQ, MAX9967_QCCQ			0.85		
Prop Delay	t_{PDL}				2.2		ns
Prop Delay Temperature Coefficient					+6		ps/°C

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -5.25V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +70°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Prop Delay Match, High/Low vs. Low/High					±25		ps
Prop Delay Match, Comparators Within Package		(Note 17)			35		ps
Prop Delay Dispersion vs. Common-Mode Input (Note 25)		$V_{CHV\_}$ = $V_{CLV\_}$ = 0, 6.4V			±75		ps
		$V_{CHV\_}$ = $V_{CLV\_}$ = -1.4V			±175		
Prop Delay Dispersion vs. Overdrive		100mV to 1V			220		ps
Prop Delay Dispersion vs. Pulse Width		2.5ns to 22.5ns pulse width, relative to 12.5ns pulse width			±40		ps
Prop Delay Dispersion vs. Slew Rate		0.5V/ns to 2V/ns slew rate			100		ps
Waveform Tracking 10% to 90%		$V_{DUT\_}$ = 1.0V_{P-P}, t_R = t_F = 1.0ns, 10% to 90% relative to timing at 50% point	Term mode		250		ps
			High-Z mode		500		
OPEN-COLLECTOR LOGIC OUTPUTS (CH_, NCH_, CL_, NCL_: MAX9967_DCCQ, MAX9967_GCCQ, MAX9967_LCCQ, and MAX9967_RCCQ)							
$V_{CCO\_}$ Voltage Range	$V_{VCCO\_}$			0		3.5	V
Output Low-Voltage Compliance		Set by I_{OL}, R_{TERM}, and $V_{CCO\_}$			-0.5		V
Output High Current	I_{OH}	MAX9967_DCCQ, MAX9967_GCCQ		-0.05	0	+0.10	mA
Output Low Current	I_{OL}	MAX9967_DCCQ, MAX9967_GCCQ		7.6	8	8.4	mA
Output High Voltage	V_{OH}	$I_{CH\_}$ = $I_{NCH\_}$ = $I_{CL\_}$ = $I_{NCL\_}$ = 0, MAX9967_LCCQ, MAX9967_RCCQ		$V_{CCO\_}$ - 0.05	$V_{CCO\_}$ - 0.005		V
Output Low Voltage	V_{OL}	$I_{CH\_}$ = $I_{NCH\_}$ = $I_{CL\_}$ = $I_{NCL\_}$ = 0, MAX9967_LCCQ, MAX9967_RCCQ			$V_{CCO\_}$ - 0.4		V
Output Voltage Swing		$I_{CH\_}$ = $I_{NCH\_}$ = $I_{CL\_}$ = $I_{NCL\_}$ = 0, MAX9967_LCCQ, MAX9967_RCCQ		360	390	440	mV
Output Termination Resistor	R_{TERM}	Single-ended measurement from $V_{CCO\_}$ to CH_, NCH_, CL_, NCL_, MAX9967_LCCQ, MAX9967_RCCQ		48		52	Ω
Differential Rise Time	t_R	20% to 80%	MAX9967_DCCQ, MAX9967_GCCQ, R_{TERM} = 50Ω at end of line		280		ps
			MAX9967_LCCQ, MAX9967_RCCQ				
Differential Fall Time	t_F	20% to 80%	MAX9967_DCCQ, MAX9967_GCCQ, R_{TERM} = 50Ω at end of line		280		ps
			MAX9967_LCCQ, MAX9967_RCCQ				
OPEN-EMITTER LOGIC OUTPUTS (CH_, NCH_, CL_, NCL_: MAX9967_MCCQ and MAX9967_QCCQ)							
$V_{CCO\_}$ Voltage Range	$V_{VCCO\_}$			-0.1		+3.5	V
$V_{CCO\_}$ Supply Current	$I_{VCCO\_}$	All outputs 50Ω to ($V_{VCCO\_}$ - 2V)			165		mA

Dual, Low-Power, 500Mbps ATE Driver/Comparator with 35mA Load

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -5.25V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +70°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH}	50Ω to ($V_{VCCO\_}$ - 2V)		$V_{CCO\_}$ - 1.0	$V_{CCO\_}$ - 0.85		V
Output Low Voltage	V_{OL}	50Ω to ($V_{VCCO\_}$ - 2V)			$V_{CCO\_}$ - 1.7	$V_{CCO\_}$ - 1.6	V
Output Voltage Swing		50Ω_to ($V_{VCCO\_}$ - 2V)		800	850	900	mV
Differential Rise Time	t_R	20% to 80%			370		ps
Differential Fall Time	t_F	20% to 80%			370		ps
CLAMPS							
High Clamp Input Voltage Range	$V_{CPH\_}$			-0.3		+7.5	V
Low Clamp Input Voltage Range	$V_{CPL\_}$			-2.5		+5.3	V
Clamp Offset Voltage	V_{OS}	At DUT_ with $I_{DUT\_}$ = 1mA, $V_{CPHV\_}$ = 0				±100	mV
		At DUT_ with $I_{DUT\_}$ = -1mA, $V_{CPLV\_}$ = 0				±100	
Offset Voltage Temperature Coefficient					±0.5		mV/°C
Clamp Power-Supply Rejection Ratio (Note 12)	PSRR	$I_{DUT\_}$ = 1mA, $V_{CPHV\_}$ = 0			54		dB
		$I_{DUT\_}$ = -1mA, $V_{CPLV\_}$ = 0			54		
Voltage Gain	A_V			0.96		1.00	V/V
Voltage Gain Temperature Coefficient					-100		ppm/°C
Clamp Linearity		$I_{DUT\_}$ = 1mA, $V_{CPLV\_}$ = -1.5V, $V_{CPHV\_}$ = -0.3V to +6.5V			±10		mV
		$I_{DUT\_}$ = -1mA, $V_{CPHV\_}$ = 6.5V, $V_{CPLV\_}$ = -1.5V to +5.3V			±10		
Short-Circuit Output Current	$I_{SCDUT\_}$	$V_{CPHV\_}$ = 0, $V_{CPLV\_}$ = -1.5V, $V_{DUT\_}$ = 6.5V		50		95	mA
		$V_{CPHV\_}$ = 6.5V, $V_{CPLV\_}$ = 5V, $V_{DUT\_}$ = -1.5V		-95		-50	mA
Clamp DC Impedance	R_{OUT}	$V_{CPHV\_}$ = 3V, $V_{CPLV\_}$ = 0, $I_{DUT\_}$ = ±5mA and ±15mA		50		55	Ω
ACTIVE LOAD ($V_{COM\_}$ = +1.5V, R_L > 1MΩ, driver in high-impedance mode, unless otherwise noted)							
COM_ Voltage Range	$V_{COM\_}$			-1.5		+5.7	V
Differential Voltage Range		$V_{DUT\_}$ - $V_{COM\_}$		-7.2		+8.0	V
COM_ Offset Voltage	Vos	I_{SOURCE} = I_{SINK} = 20mA	MAX9967A			±15	mV
			MAX9967B			±100	
Offset Voltage Temperature Coefficient					50		µV/°C
COM_ Voltage Gain	A_V	$V_{COM\_}$ = 0, 4.5V, I_{SOURCE} = I_{SINK} = 20mA		0.98		1.00	V/V
Voltage Gain Temperature Coefficient					±25		ppm/°C

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -5.25V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +70°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
COM_ Linearity Error		$V_{COM\_}$ = -1.5V, +5.7V; I_{SOURCE} = I_{SINK} = 20mA (Note 10)			±3	±15	mV
COM_ Output-Voltage Power-Supply Rejection Ratio	PSRR	$V_{COM\_}$ = 2.5V, I_{SOURCE} = I_{SINK} = 20mA		40			dB
Output Resistance, Sink or Source	Ro	I_{SOURCE} = I_{SINK} = 35mA; $V_{DUT\_}$ = 3V, 6.5V with $V_{COM\_}$ = -1.5V and $V_{DUT\_}$ = -1.5V, +2V with $V_{COM\_}$ = 5.7V		25			kΩ
		I_{SOURCE} = I_{SINK} = 1mA; $V_{DUT\_}$ = 3V, 6.5V with $V_{COM\_}$ = -1.5V and $V_{DUT\_}$ = -1.5V, +2V with $V_{COM\_}$ = 5.7V		500			kΩ
Output Resistance, Linear Region	Ro	$I_{DUT\_}$ = ±10mA, I_{SOURCE} = I_{SINK} = 35mA, $V_{COM\_}$ = 2.5V			6		Ω
Deadband		$V_{COM\_}$ = 2.5V, 95% I_{SOURCE} to 95% I_{SINK}			400	700	mV
SOURCE CURRENT ($V_{DUT\_}$ = 4.5V)							
Maximum Source Current		$V_{LDL\_}$ = 3.8V		36		40	mA
Source Programming Gain	A_{TC}	$V_{LDL\_}$ = 0.3V, 3V; V_{LDH} = 0.1V		9.9	10	10.1	mA/V
Source Current Offset (Combined Offset of LDL_ and GS)	I_{OS}	$V_{LDL\_}$ = 20mV	MAX9967A (Note 9)	10		50	µA
			MAX9967B	0		200	
Source Current Temperature Coefficient		I_{SOURCE} = 35mA			-6		µA/°C
Source Current Power-Supply Rejection Ratio	PSRR	I_{SOURCE} = 25mA				±70	µA/V
		I_{SOURCE} = 35mA				±84	
Source Current Linearity (Note 26)		$V_{LDL\_}$ = 100mV, 1V, 2.5V				±60	µA
		$V_{LDL\_}$ = 3.5V				±130	
SINK CURRENT ($V_{DUT\_}$ = -1.5V)							
Maximum Sink Current		$V_{LDH\_}$ = 3.8V		-40		-36	mA
Sink Programming Gain	A_{TC}	$V_{LDH\_}$ = 0.3V, 3V; $V_{LDL\_}$ = 0.1V		-10.1	-10	-9.9	mA/V
Sink Current Offset (Combined Offset of LDH_ and GS)	I_{OS}	$V_{LDH\_}$ = 20mV	MAX9967A (Note 9)	-50		-10	µA
			MAX9967B	-200		0	
Sink Current Temperature Coefficient		I_{SINK} = 35mA			+6		µA/°C
Sink Current Power-Supply Rejection Ratio	PSRR	I_{SINK} = 25mA				±70	µA /V
		I_{SINK} = 35mA				±84	

Dual, Low-Power, 500Mbps ATE Driver/Comparator with 35mA Load

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -5.25V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +70°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Sink Current Linearity (Note 26)		$V_{LDH\_}$ = 100mV, 1V, 2.5V			±60	µA
		$V_{LDH\_}$ = 3.5V			±130	
GROUND SENSE						
GS Voltage Range	V_{GS}	Verified by GS common-mode error test	±250			mV
GS Common-Mode Error		$V_{DUT\_}$ = -1.5V, V_{GS} = ±250mV, $V_{LDH\_}$ - V_{GS} = 0.1V			±25	µA
		$V_{DUT\_}$ = +4.5V, V_{GS} = ±250mV, $V_{LDL\_}$ - V_{GS} = 0.1V			±25	
GS Input Bias Current		V_{GS} = 0			±25	µA
AC CHARACTERISTICS (Z_L = 50Ω to GND)						
Enable Time (Note 27)	t_{EN}	I_{SOURCE} = 20mA, $V_{COM\_}$ = -1.5V		2.2		ns
		I_{SINK} = 20mA, $V_{COM\_}$ = +1.5V				
Disable Time (Note 27)	t_{DIS}	I_{SOURCE} = 20mA, $V_{COM\_}$ = -1.5V		1.9		ns
		I_{SINK} = 20mA, $V_{COM\_}$ = +1.5V				
Current Settling Time on Commutation		I_{SOURCE} = I_{SINK} = 1mA and 35mA (Notes 7, 28) To 10%		10		ns
		To 1.5%		50		
Spike During Enable/Disable Transition		I_{SOURCE} = I_{SINK} = 35mA, $V_{COM\_}$ = 0		100		mV

Note 1: All minimum and maximum limits are 100% production tested. Tests are performed at nominal supply voltages unless otherwise noted.

Note 2: Total for dual device at worst-case setting. $R_L \geq 10M\Omega$. The supply currents are measured with typical supply voltages.

Note 3: Does not include internal dissipation of the comparator outputs. With output loads of 50Ω to (V_{VCCO} - 2V), this adds 120mW (typ) to the total device power (MAX9967_MCCQ and MAX9967_QCCQ). For MAX9967_LCCQ, additional power dissipation is typically (32mA x V_{VCCO}).

Note 4: Externally forced voltages may exceed this range provided that the Absolute Maximum Ratings are not exceeded.

Note 5: Transition time from LLEAK being asserted to leakage current dropping below specified limits.

Note 6: Based on simulation results only.

Note 7: Transition time from LLEAK being deasserted to output returning to normal operating mode.

Note 8: With the exception of Offset and Gain/CMRR tests, reference input values are calibrated for offset and gain.

Note 9: Measured at V_{CC} = +9.75, V_{EE} = -5.25V, and T_J = +85°C.

Note 10: Relative to straight line between 0 and 4.5V.

Note 11: Specifications measured at the end points of the full range. Full ranges are -1.3V ≤ $V_{DHV\_}$ ≤ 6.5V, -1.5V ≤ $V_{DLV\_}$ ≤ 6.3V, -1.5V ≤ $V_{DTV\_}$ ≤ 6.5V.

Note 12: Change in offset voltage with power supplies independently set to their minimum and maximum values.

Note 13: Nominal target value is 50Ω. Contact factory for alternate trim selections within the 45Ω to 51Ω range.

Note 14: $V_{DTV\_}$ = +1.5V, R_S = 50Ω. External signal driven into T-line is a 0 to +3V edge with 1.2ns rise time (10% to 90%). Measurement is made using the comparator.

Note 15: Measured from the crossing point of DATA_ inputs to the settling of the driver output.

Note 16: Prop delays are measured from the crossing point of the differential input signals to the 50% point of the expected output swing. Rise time of differential inputs DATA_ and RCV_ is 250ps (10% to 90%).

Note 17: Rising edge to rising edge or falling edge to falling edge.

Note 18: Specified amplitude is programmed. At this pulse width, the output reaches at least 95% of its nominal (DC) amplitude. The pulse width is measured at DATA_.

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -5.25V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +70°C to +100°C, unless otherwise noted.) (Note 1)

Note 19: Specified amplitude is programmed. Maximum data rate is specified in transitions per second. A square wave that reaches at least 95% of its programmed amplitude may be generated at one-half this frequency.

Note 20: Crosstalk from either driver to the other. Aggressor channel is driving $3V_{P-P}$ into a 50Ω load. Victim channel is in term mode with $V_{DTV\_}$ = +1.5V.

Note 21: Indicative of switching speed from DHV_ or DLV_ to DTV_ and DTV_ to DHV_ or DLV_ when $V_{DLV\_} < V_{DTV\_} < V_{DHV\_}$. If $V_{DTV\_} < V_{DLV\_}$ or $V_{DTV\_} > V_{DHV\_}$, switching speed is degraded by approximately a factor of 3.

Note 22: Change in offset voltage over the input range.

Note 23: Unless otherwise noted, all propagation delays are measured at 40MHz, $V_{DUT\_}$ = 0 to +2V, $V_{CHV\_}$ = $V_{CLV\_}$ = +1V, slew rate = 2V/ns, Z_S = 50Ω, driver in term mode with $V_{DTV\_}$ = 0. Comparator outputs are terminated with 50Ω to GND at scope input with $V_{CCO\_}$ = 2V. Open-collector outputs are also terminated (internally or externally) with R_{TERM} = 50Ω to $V_{CCO\_}$. Measured from $V_{DUT\_}$ crossing calibrated CHV_/CLV_ threshold to crossing point of differential outputs.

Note 24: $V_{DUT\_}$ = 0 to +1V, $V_{CHV\_}$ = $V_{CLV\ \_}$ = +0.5V. At this pulse width, the output reaches at least 90% of its DC voltage swing. The pulse width is measured at the crossing points of the differential outputs.

Note 25: Relative to propagation delay at $V_{CHV\_}$ = $V_{CLV\_}$ = +1.5V. $V_{DUT\_}$ = $200mV_{P-P}$. Overdrive = 100mV.

Note 26: Relative to segmented interpolations between 20mV, 200mV, 2V, and 3V.

Note 27: Measured from the crossing point of LDEN_ inputs to the 10% point of the output voltage change.

Note 28: $V_{COM\_}$ = 1.5V, R_S = 50Ω, driving voltage = +4V to -1V transition and -1V to +4V transition. Settling time is measured from $V_{DUT\_}$ = 1.5V to I_{SINK}/I_{SOURCE} settling within specified tolerance.

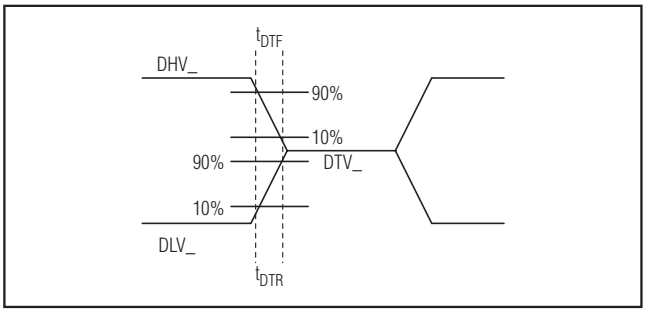


Figure 1a. Drive to Term Rise and Fall Time

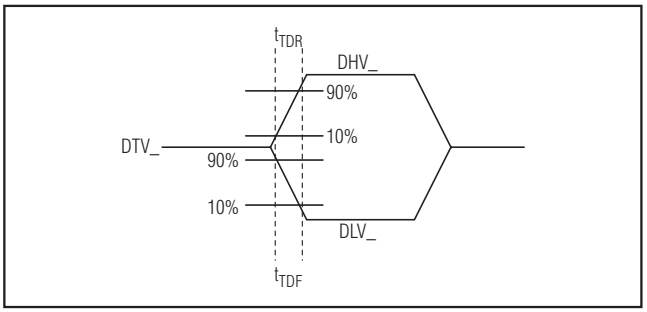
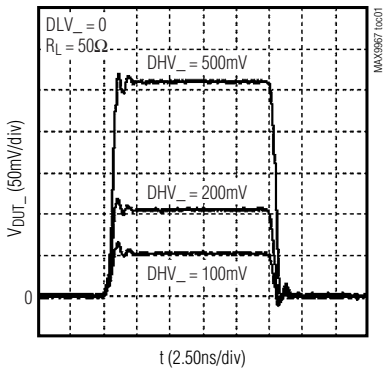


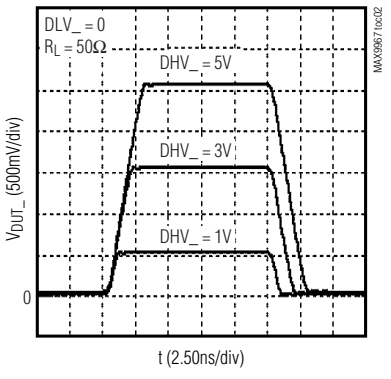
Figure 1b. Term to Drive Rise and Fall Time

Typical Operating Characteristics

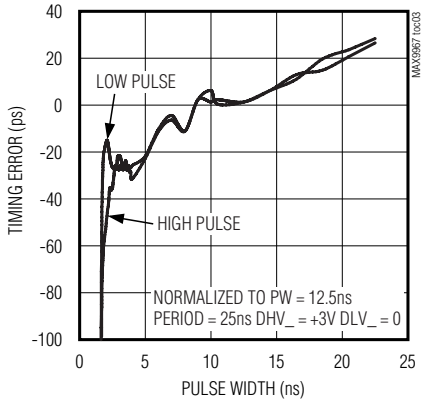
DRIVER SMALL-SIGNAL RESPONSE



DRIVER LARGE-SIGNAL RESPONSE



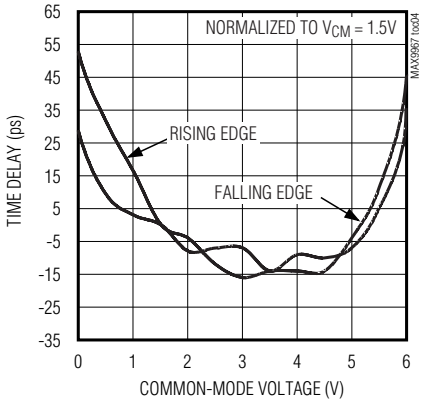
DRIVER TRAILING EDGE TIMING ERROR vs. PULSE WIDTH



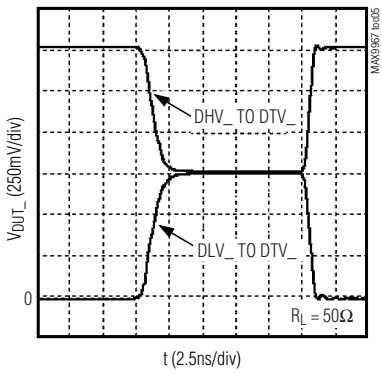
Dual, Low-Power, 500Mbps ATE Driver/Comparator with 35mA Load

Typical Operating Characteristics (continued)

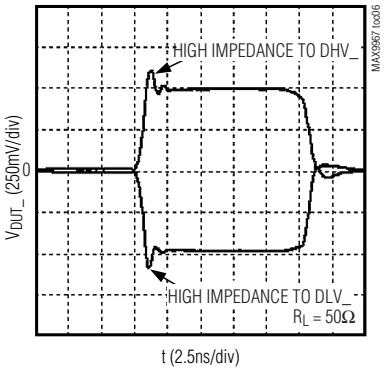
DRIVER TIME DELAY vs. COMMON-MODE VOLTAGE



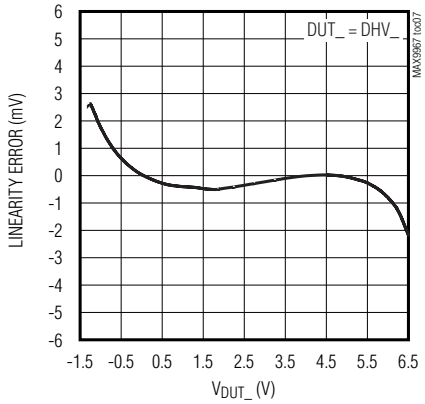
DRIVE-TO-TERM TRANSITION



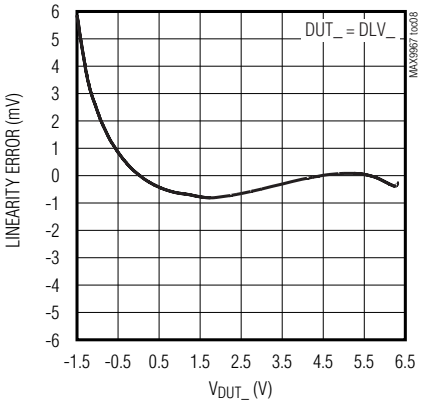
HIGH IMPEDANCE TO DRIVE TRANSITION



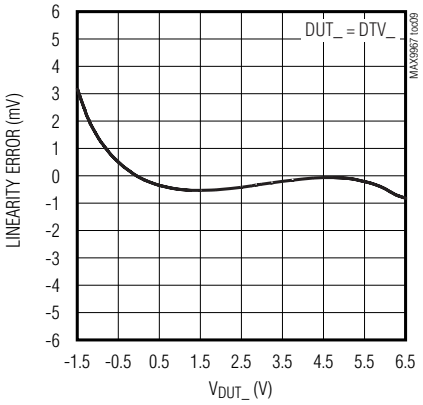
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



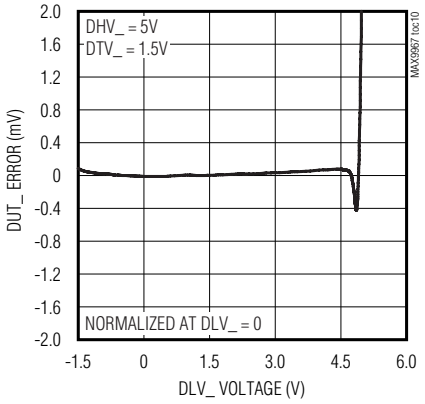
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



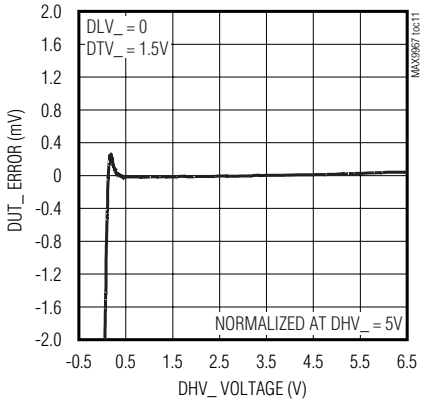
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



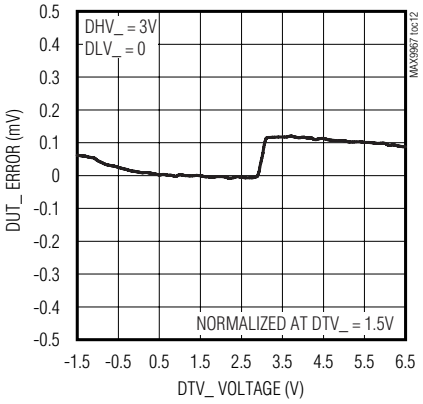
CROSSTALK TO DUT_ FROM DLV_ WITH DUT_ = DHV_



CROSSTALK TO DUT_ FROM DHV_ WITH DUT_ = DLV_



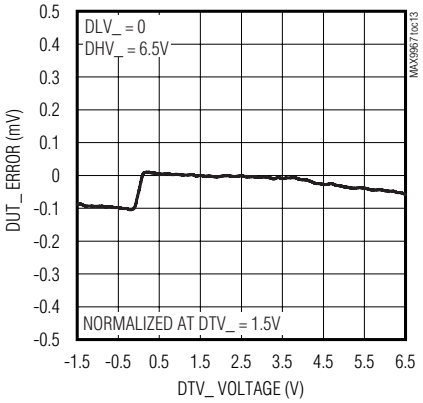
CROSSTALK TO DUT_ FROM DTV_ WITH DUT_ = DHV_



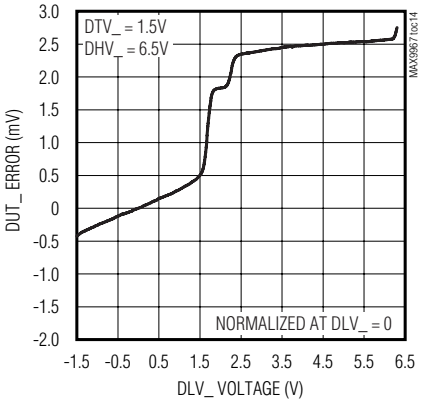
Dual, Low-Power, 500Mbps ATE Driver/Comparator with 35mA Load

Typical Operating Characteristics (continued)

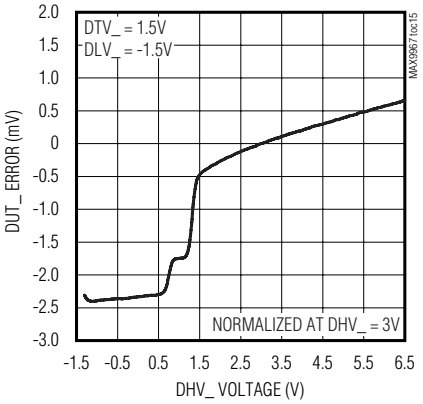
CROSSTALK TO DUT_ FROM DTV_ WITH DUT_ = DLV_



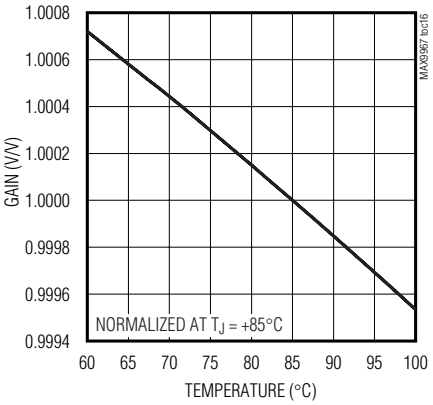
CROSSTALK TO DUT_ FROM DLV_ WITH DUT_ = DTV_



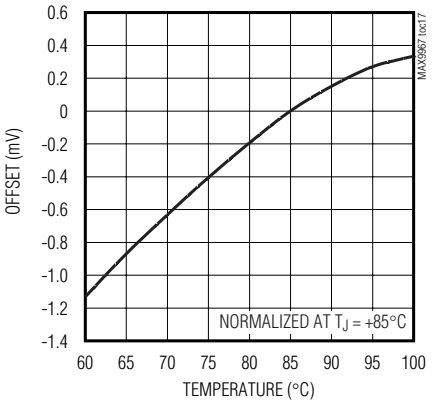
CROSSTALK TO DUT_ FROM DHV_ WITH DUT_ = DTV_



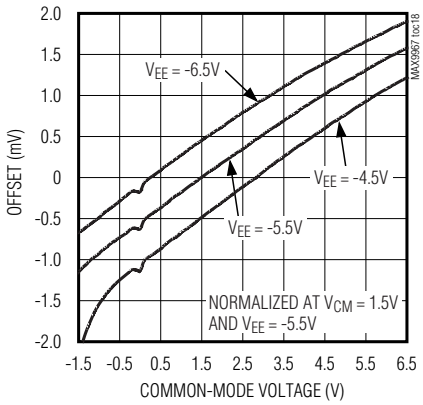
DRIVER GAIN vs. TEMPERATURE



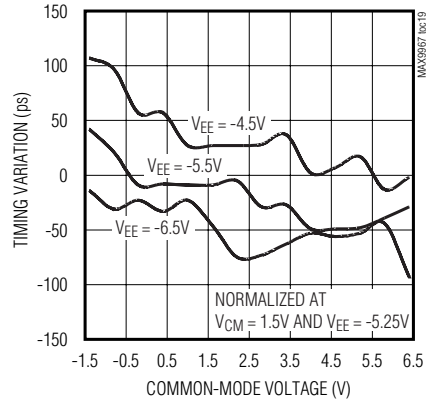
DRIVER OFFSET vs. TEMPERATURE



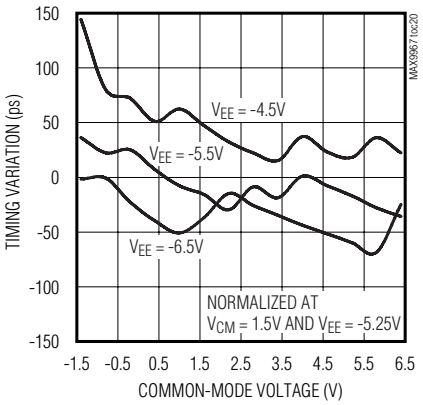
COMPARATOR OFFSET vs. COMMON-MODE VOLTAGE



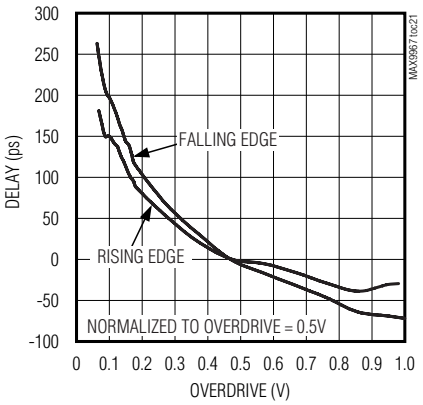
COMPARATOR RISING-EDGE TIMING VARIATION vs. COMMON-MODE VOLTAGE



COMPARATOR FALLING-EDGE TIMING VARIATION vs. COMMON-MODE VOLTAGE



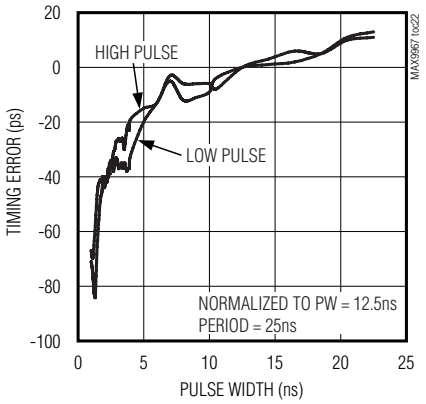
COMPARATOR TIMING VARIATION vs. OVERDRIVE



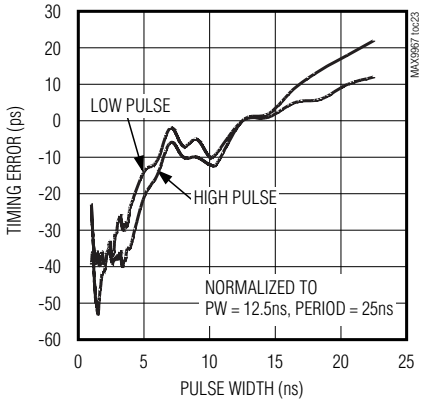
Dual, Low-Power, 500Mbps ATE Driver/Comparator with 35mA Load

Typical Operating Characteristics (continued)

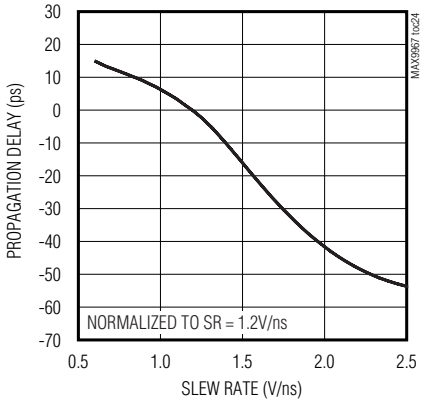
COMPARATOR TRAILING TIMING ERROR vs. PULSE WIDTH, MAX9967_LCCQ



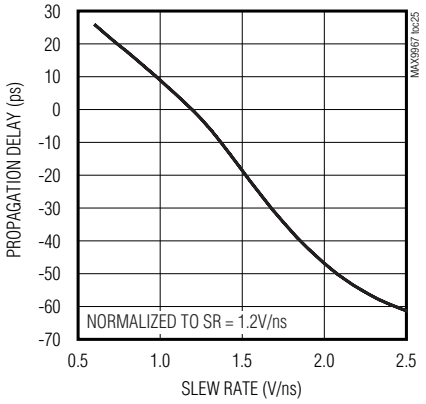
COMPARATOR TRAILING-EDGE TIMING ERROR vs. PULSE WIDTH, MAX9967_MCCQ



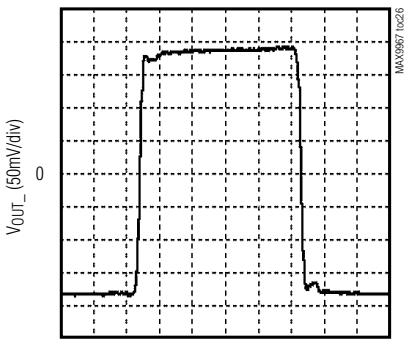
COMPARATOR TIMING VARIATION vs. INPUT SLEW RATE, DUT_ RISING



COMPARATOR TIMING VARIATION vs. INPUT SLEW RATE, DUT_ FALLING

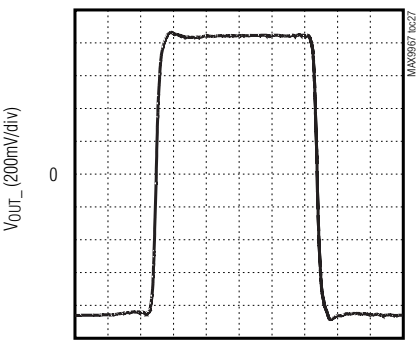


COMPARATOR DIFFERENTIAL OUTPUT RESPONSE (MAX9967_LCCQ)



$V_{DUT\_}$ = 0 TO 3V PULSE, CHV_ = CLV_ = +1.5V, EXTERNAL LOAD = 50Ω

COMPARATOR DIFFERENTIAL OUTPUT RESPONSE (MAX9967_MCCQ)

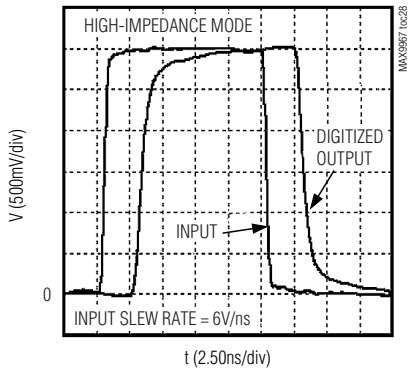


V_{DUT} = 0 TO 3V PULSE, CHV_ = CLV_ = 1.5V, EXTERNAL LOAD = 50Ω

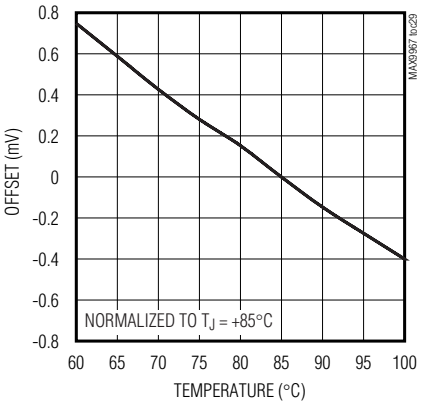
Dual, Low-Power, 500Mbps ATE Driver/Comparator with 35mA Load

Typical Operating Characteristics (continued)

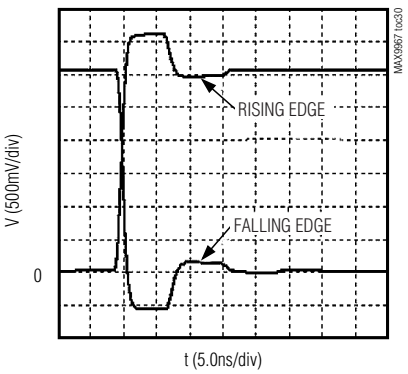
COMPARATOR RESPONSE HIGH SLEW-RATE OVERDRIVE



COMPARATOR OFFSET vs. TEMPERATURE

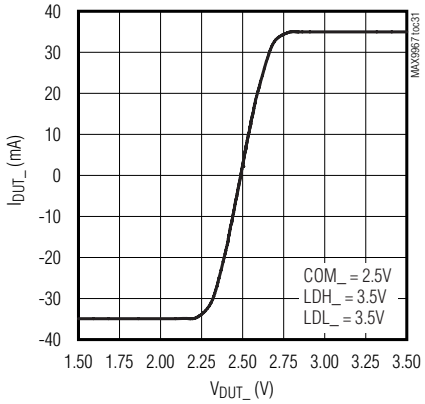


CLAMP RESPONSE

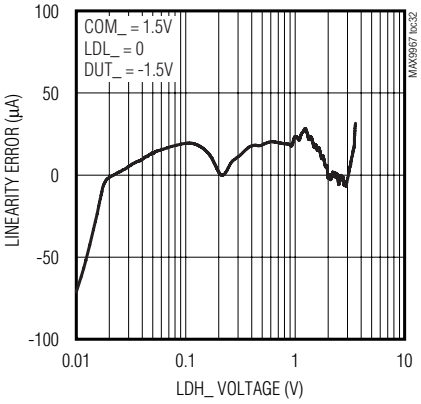


DUT_ = 0 TO 3V SQUARE WAVE
R_S = 25Ω
CPLV_ = -0.1V CPHV_ = +3.1V

ACTIVE-LOAD VOLTAGE vs. CURRENT

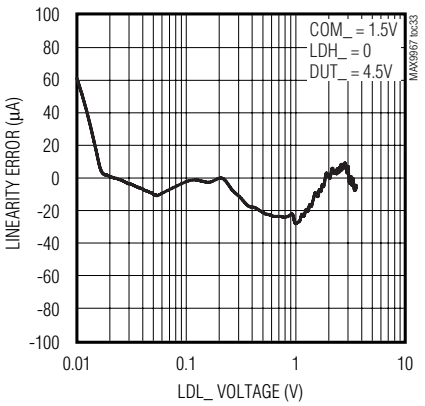


ACTIVE-LOAD LINEARITY ERROR $I_{DUT\_}$ vs. LDH_



CALIBRATION POINTS AT
LDH_ = 20mV, 200mV, 2V, 3V

ACTIVE-LOAD LINEARITY ERROR $I_{DUT\_}$ vs. LDL_

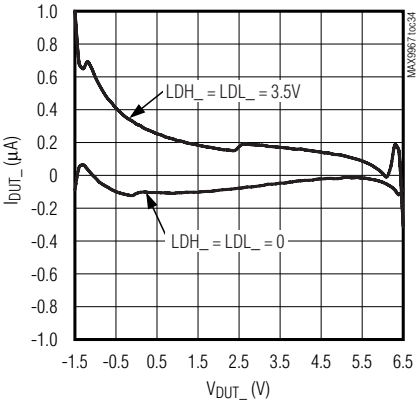


CALIBRATION POINTS AT
LDL_ = 20mV, 200mV, 2V, 3V

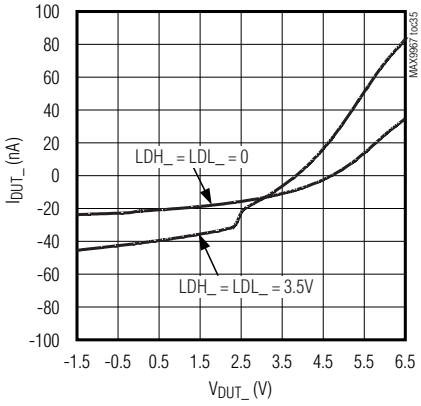
Dual, Low-Power, 500Mbps ATE Driver/Comparator with 35mA Load

Typical Operating Characteristics (continued)

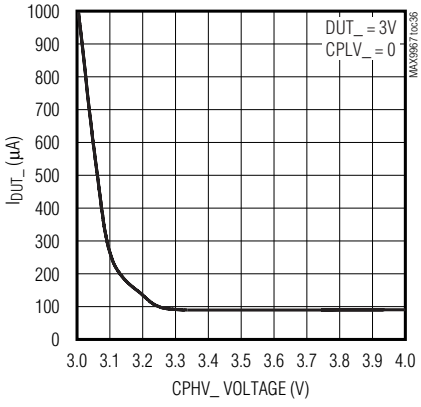
HIGH-IMPEDANCE LEAKAGE CURRENT vs. DUT_ VOLTAGE



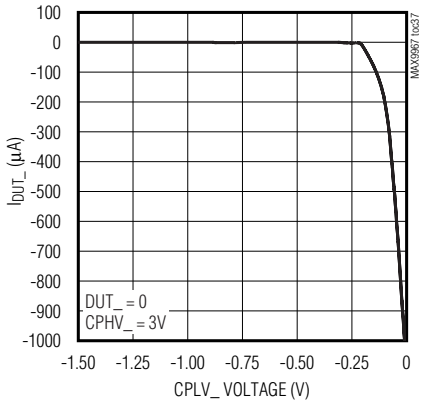
LOW-LEAKAGE CURRENT vs. DUT_ VOLTAGE



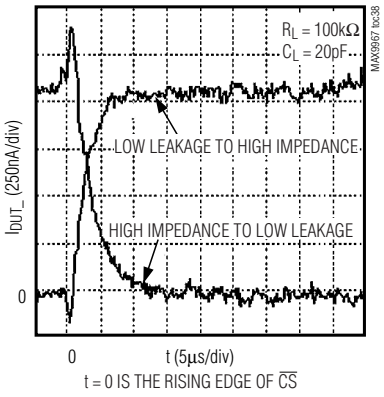
CLAMP CURRENT vs. DIFFERENCE VOLTAGE



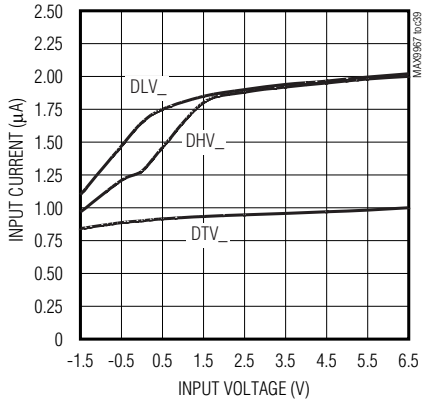
CLAMP CURRENT vs. DIFFERENCE VOLTAGE



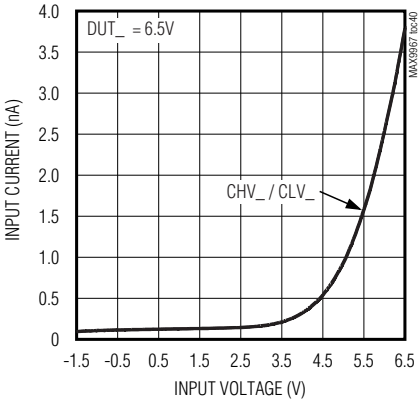
HIGH-IMPEDANCE TO LOW-LEAKAGE TRANSITION



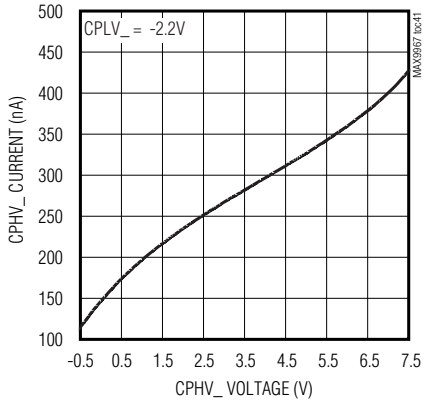
DRIVER REFERENCE CURRENT vs. DRIVER REFERENCE VOLTAGE



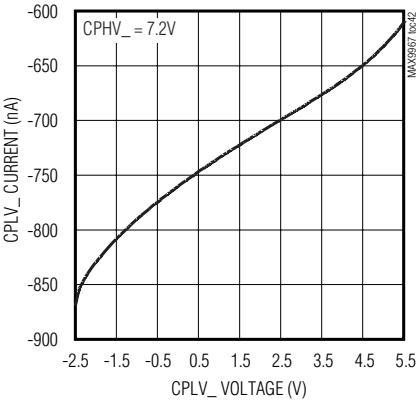
COMPARATOR REFERENCE INPUT CURRENT vs. INPUT VOLTAGE



INPUT CURRENT vs. INPUT VOLTAGE, CPHV_

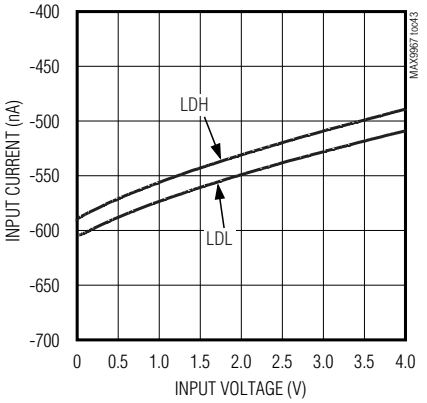


INPUT CURRENT vs. INPUT VOLTAGE, CPLV_

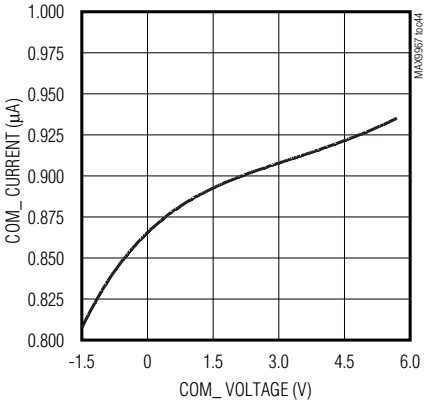


Typical Operating Characteristics (continued)

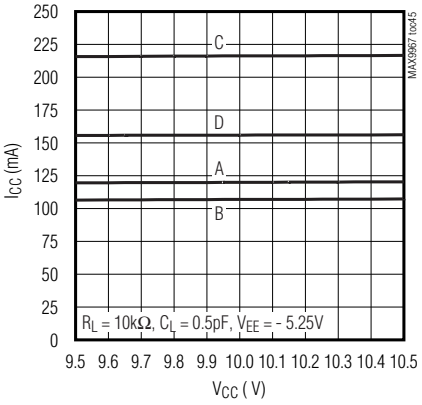
LOAD REFERENCES INPUT CURRENTS vs. INPUT VOLTAGE



INPUT CURRENTS vs. INPUT VOLTAGE, COM_



SUPPLY CURRENT, I_{CC} vs. V_{CC}



A: DUT_ = DTV_ = 1.5V, DHV_ = 3V, DLV_ = 0, CHV_ = CLV_ = 0, CPHV_ = 7.2V, CPLV_ = -2.2V, LDH_ = LDL_ = 0

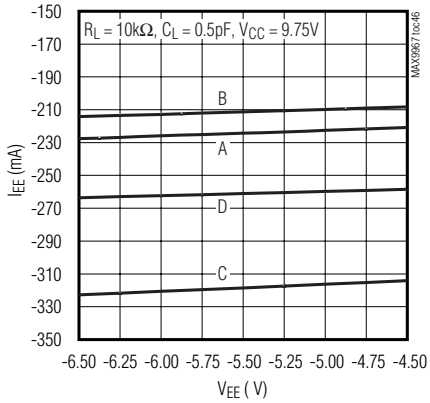
$I_{SOURCE} = I_{SINK} = 0$

B: SAME AS A EXCEPT DRIVER DISABLED HIGH-Z AND LOAD ENABLED

C: SAME AS B EXCEPT $I_{SOURCE} = I_{SINK} = 35mA$

D: SAME AS C EXCEPT LOW-LEAKAGE MODE ASSERTED

SUPPLY CURRENT, I_{EE} vs. V_{EE}



A: DUT_ = DTV_ = 1.5V, DHV_ = 3V, DLV_ = 0, CHV_ = CLV_ = 0, CPHV_ = 7.2V, CPLV_ = -2.2V, LDH_ = LDL_ = 0

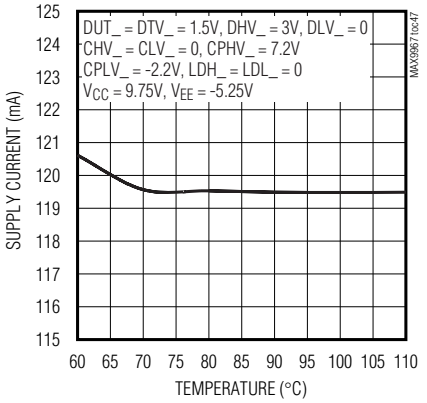
$I_{SOURCE} = I_{SINK} = 0$

B: SAME AS A EXCEPT DRIVER DISABLED HIGH-Z AND LOAD ENABLED

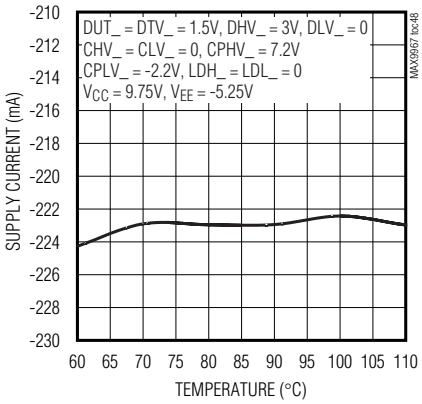
C: SAME AS B EXCEPT $I_{SOURCE} = I_{SINK} = 35mA$

D: SAME AS C EXCEPT LOW-LEAKAGE MODE ASSERTED

I_{CC} vs. TEMPERATURE



I_{EE} vs. TEMPERATURE



Dual, Low-Power, 500Mbps ATE Driver/Comparator with 35mA Load

Pin Description

PIN	NAME	FUNCTION
1	TEMP	Temperature Monitor Output
2, 9, 12, 14, 17, 24, 35, 45, 46, 60, 80, 81, 91	V_{EE}	Negative Power-Supply Input
3, 5, 10, 16, 21, 23, 25, 34, 43, 44, 82, 83, 92	GND	Ground Connection
4, 11, 15, 22, 33, 41, 42, 66, 84, 85, 93	V_{CC}	Positive Power-Supply Input
6	FORCE1	Channel 1 Force Input from External PMU
7	DUT1	Channel 1 Device-Under-Test Input/Output. Combined I/O for driver, comparator, clamp, and load.
8	SENSE1	Channel 1 Sense Output to External PMU
13	GS	Ground Sense. GS is the ground reference for LDH_ and LDL_.
18	SENSE2	Channel 2 Sense Output to External PMU
19	DUT2	Channel 2 Device-Under-Test Input/Output. Combined I/O for driver, comparator, clamp, and load.
20	FORCE2	Channel 2 Force Input from External PMU
26	CLV2	Channel 2 Low Comparator Reference Input
27	CHV2	Channel 2 High Comparator Reference Input
28	DLV2	Channel 2 Driver Low Reference Input
29	DTV2	Channel 2 Driver Termination Reference Input
30	DHV2	Channel 2 Driver High Reference Input
31	CPLV2	Channel 2 Low-Clamp Reference Input
32	CPHV2	Channel 2 High-Clamp Reference Input
36	NCH2	Channel 2 Comparator High Output. Differential output of channel 2 high comparator.
37	CH2	
38	V_{CCO2}	Channel 2 Collector Voltage Input. Voltage for channel 2 comparator output pullup resistors. For open-collector outputs, this is the pullup voltage for the internal termination resistors. For open-emitter outputs, this is the collector voltage of the output transistors. Not internally connected on open-collector versions without internal termination resistors.
39	NCL2	Channel 2 Comparator Low Output. Differential output of channel 2 low comparator.
40	CL2	
47	COM2	Channel 2 Active-Load Commutation Voltage Reference Input
48	LDL2	Channel 2 Active-Load Source Current Reference Input
49	LDH2	Channel 2 Active-Load Sink Current Reference Input
50, 76	N.C.	No Connect. Make no connection.
51	TDATA2	Channel 2 Data Termination Voltage Input. Termination voltage input for the DATA2 and NDATA2 differential inputs. Not internally connected on versions without internal termination resistors.
52	NDATA2	Channel 2 Multiplexer Control Inputs. Differential controls DATA2 and NDATA2 select driver 2's input from DHV2 or DLV2. Drive DATA2 above NDATA2 to select DHV2. Drive NDATA2 above DATA2 to select DLV2.
53	DATA2	

Pin Description (continued)

PIN	NAME	FUNCTION
54	TRCV2	Channel 2 RCV Termination Voltage Input. Termination voltage input for the RCV2 and NRCV2 differential inputs. Not internally connected on versions without internal termination resistors.
55	NRCV2	Channel 2 Multiplexer Control Inputs. Differential controls RCV2 and NRCV2 place channel 2 into receive mode. Drive RCV2 above NRCV2 to place channel 2 into receive mode. Drive NRCV2 above RCV2 to place channel 2 into drive mode.
56	RCV2	
57	TLDEN2	Channel 2 Load Enable Termination Voltage Input. Termination voltage input for the LDEN2 and NLDEN2 differential inputs. Not internally connected on versions without internal termination resistors.
58	NLDEN2	Channel 2 Multiplexer Control Inputs. Differential controls LDEN2 and NLDEN2 enable/disable the active load. Drive LDEN2 above NLDEN2 to enable the channel 2 active load. Drive NLDEN2 above LDEN2 to disable the channel 2 active load.
59	LDEN2	
61	$\overline{RST}$	Reset Input. Asynchronous reset input for the serial register. $\overline{RST}$ is active low and asserts low-leakage mode. At power-up, hold $\overline{RST}$ low until V_{CC} and V_{EE} have stabilized.
62	$\overline{CS}$	Chip-Select Input. Serial port activation input. $\overline{CS}$ is active low.
63	THR	Single-Ended Logic Threshold. Leave THR unconnected to set the threshold to +1.25V or force THR to a desired threshold voltage.
64	SCLK	Serial-Clock Input. Clock for serial port.
65	DIN	Data Input. Serial port data input.
67	LDEN1	Channel 1 Multiplexer Control Inputs. Differential controls LDEN1 and NLDEN1 enable/disable the active load. Drive LDEN1 above NLDEN1 to enable the channel 1 active load. Drive NLDEN1 above LDEN1 to disable the channel 1 active load.
68	NLDEN1	
69	TLDEN1	Channel 1 Load Enable Termination Voltage Input. Termination voltage input for the LDEN1 and NLDEN1 differential inputs. Not internally connected on versions without internal termination resistors.
70	RCV1	Channel 1 Multiplexer Control Inputs. Differential controls RCV1 and NRCV1 place channel 1 into receive mode. Drive RCV1 above NRCV1 to place channel 1 into receive mode. Drive NRCV1 above RCV1 to place channel 1 into drive mode.
71	NRCV1	
72	TRCV1	Channel 1 RCV Termination Voltage Input. Termination voltage input for the RCV1 and NRCV1 differential inputs. Not internally connected on versions without internal termination resistors.
73	DATA1	Channel 1 Multiplexer Control Inputs. Differential controls DATA1 and NDATA1 select driver 1's input from DHV1 or DLV1. Drive DATA1 above NDATA1 to select DHV1. Drive NDATA1 above DATA1 to select DLV1.
74	NDATA1	
75	TDATA1	Channel 1 Data Termination Voltage Input. Termination voltage input for the DATA1 and NDATA1 differential inputs. Not internally connected on versions without internal termination resistors.
77	LDH1	Channel 1 Active-Load Sink Current Reference Input
78	LDL1	Channel 1 Active-Load Source Current Reference Input
79	COM1	Channel 1 Active Load Commutation Voltage Reference Input
86	CL1	Channel 1 Low Comparator Output. Differential output of channel 1 low comparator.
87	NCL1	

Dual, Low-Power, 500Mbps ATE Driver/Comparator with 35mA Load

Pin Description (continued)

PIN	NAME	FUNCTION
88	V_{CCO1}	Channel 1 Collector Voltage Input. Voltage for channel 1 comparator output pullup resistors. For open-collector outputs, this is the pullup voltage for the internal termination resistors. For open-emitter outputs, this is the collector voltage of the output transistors. Not internally connected on open-collector versions without internal termination resistors.
89	CH1	Channel 1 High Comparator High Output. Differential output of channel 1 high-side comparator.
90	NCH1	
94	CPHV1	Channel 1 High-Clamp Reference Input
95	CPLV1	Channel 1 Low-Clamp Reference Input
96	DHV1	Channel 1 Driver High Reference Input
97	DTV1	Channel 1 Driver Termination Reference Input
98	DLV1	Channel 1 Driver Low Reference Input
99	CHV1	Channel 1 High-Comparator Reference Input
100	CLV1	Channel 1 Low-Comparator Reference Input

Detailed Description

The MAX9967 dual, low-power, high-speed, pin electronics DCL IC includes, for each channel, a three-level pin driver, a dual comparator, variable clamps, and an active load. The driver features a -1.5V to +6.5V operating range and high-speed operation, includes high-impedance and active-termination (3rd-level drive) modes, and is highly linear even at low voltage swings. The dual comparator provides low dispersion (timing variation) over a wide variety of input conditions. The clamps provide damping of high-speed DUT_ waveforms when the device is configured as a high-impedance receiver. The programmable load supplies up to 35mA of source and sink current. The load facilitates contact/continuity testing, at-speed parametric testing of IOH and IOL, and pullup of high output-impedance devices.

The MAX9967A provides tight matching of gain and offset for the drivers and offset for the comparators and active load, allowing reference levels to be shared across multiple channels in cost-sensitive systems. Use the MAX9967B for system designs that incorporate independent reference levels for each channel.

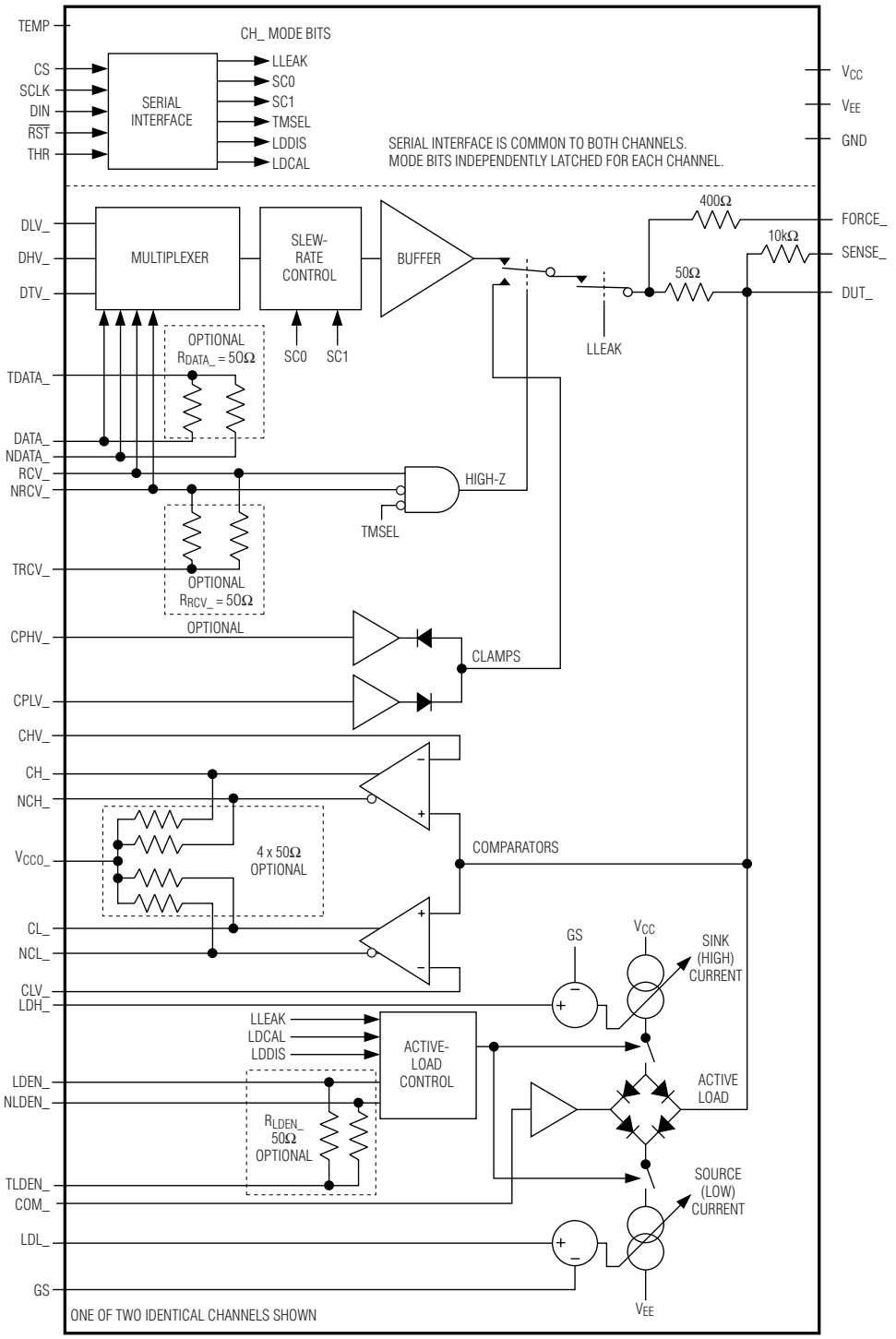
Optional internal resistors at the high-speed inputs provide compatibility with ECL, LVPECL, LVDS, and GTL interfaces. Connect the termination voltage inputs (TDATA_, TRCV_, TLDEN_) to the appropriate voltage for terminating ECL, LVPECL, GTL, or other logic. Leave the inputs unconnected for 100Ω differential LVDS termination. In addition, ECL/LVPECL or flexible open-collector outputs with optional internal pullup resistors are available for the comparators. These features significantly reduce the discrete component count on the circuit board.

A 3-wire, low-voltage, CMOS-compatible serial interface programs the low-leakage, load-disable, slew-rate, and tri-state/terminate operational configurations of the MAX9967.

Output Driver

The driver input is a high-speed multiplexer that selects one of three voltage inputs: DHV_, DLV_, or DTV_. This switching is controlled by high-speed inputs DATA_ and RCV_ and mode control bit TMSEL (Table 1). A slew-rate circuit controls the slew rate of the buffer input. Select one of four possible slew rates according to Table 2. The speed of the internal multiplexer sets the100% driver slew rate (see the Driver Large-Signal Response graph in the *Typical Operating Characteristics*).

Functional Diagram



Dual, Low-Power, 500Mbps ATE Driver/Comparator with 35mA Load

DUT_ can be toggled at high speed between the buffer output and high-impedance mode, or it can be placed into low-leakage mode (Figure 2, Table 1). In high-impedance mode, the clamps are connected. High-speed input RCV_ and mode control bits TMSEL and LLEAK control the switching. In high-impedance mode, the bias current at DUT_ is less than 1.5µA over the 0 to 3V range, while the node maintains its ability to track high-speed signals. In low-leakage mode, the bias current at DUT_ is further reduced to less than 50nA, and signal tracking slows. See the *Low-Leakage Mode, LLEAK* section for more details.

The nominal driver output resistance is 50Ω. Contact the factory for different resistance values within the 45Ω to 51Ω range.

Clamps

Configure the voltage clamps (high and low) to limit the voltage at DUT_ and to suppress reflections when the channel is configured as a high-impedance receiver. The clamps behave as diodes connected to the outputs of high-current buffers. Internal circuitry compensates for the diode drop at 1mA clamp current. Set the clamp voltages using the external connections CPHV_ and CPLV_. The clamps are enabled only when the driver is in the high-impedance mode (Figure 2). For transient suppression, set the clamp voltages to approximately the minimum and maximum expected DUT_ voltage range. The optimal clamp voltages are application specific and must be empirically determined. If clamping is not desired, set the clamp voltages at least 0.7V outside the expected DUT_ voltage range; overvoltage protection remains active without loading DUT_.

Comparators

The MAX9967 provides two independent high-speed comparators for each channel. Each comparator has one input connected internally to DUT_ and the other input connected to either CHV_ or CLV_ (see the *Functional Diagram*). Comparator outputs are a logical result of the input conditions, as indicated in Table 3.

Three configurations are available for the comparator differential outputs to ease interfacing with a wide variety of logic families. An open-collector configuration switches an 8mA current source between the two outputs. This configuration is available with and without internal termination resistors connected to $V_{CCO\_}$ (Figure 3). For open-collector versions without internal termination, leave $V_{CCO\_}$ unconnected and add the required external resistors. These resistors are typically 50Ω to the pullup voltage at the receiving end of the output trace. Alternate configurations may be used, provided that the *Absolute Maximum Ratings* are not exceeded. For open-collector versions with internal termination, connect $V_{CCO\_}$ to the desired V_{OH} voltage.

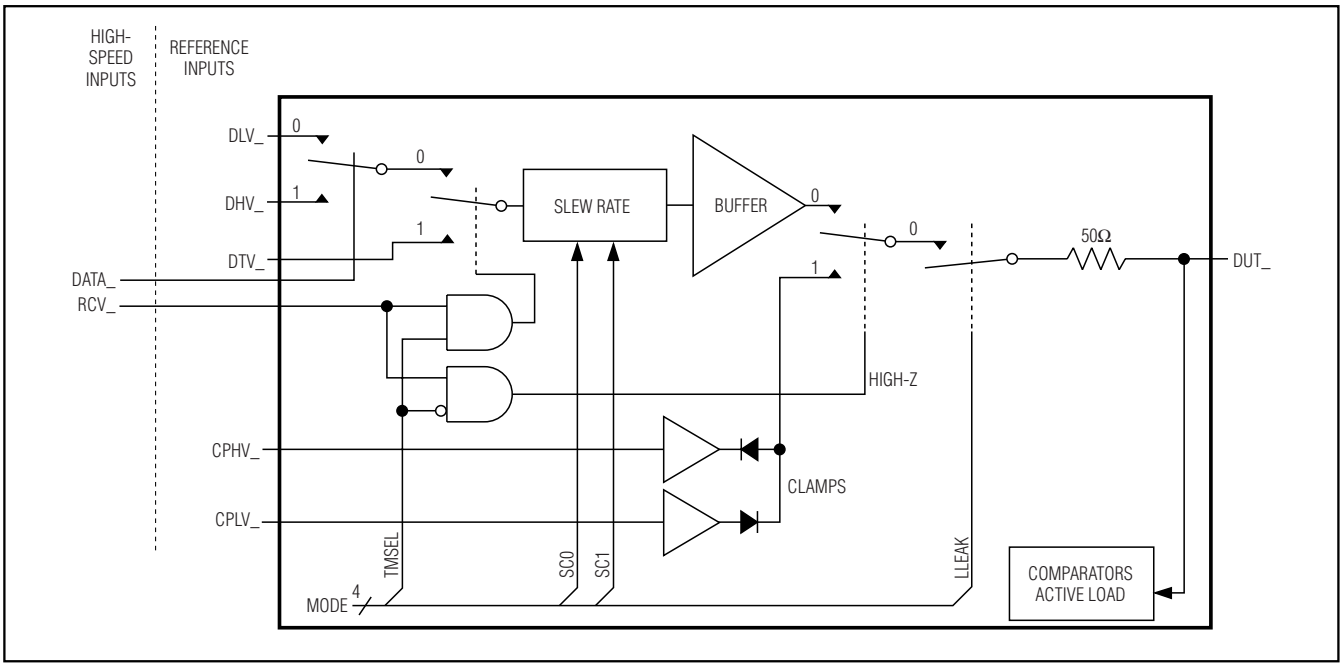


Figure 2. Simplified Driver Channel

Table 1. Driver Logic

EXTERNAL CONNECTIONS		INTERNAL CONTROL REGISTER		DRIVER OUTPUT
DATA_	RCV_	TMSEL	LLEAK	
1	0	X	0	Drive to DHV_
0	0	X	0	Drive to DLV_
X	1	1	0	Drive to DTV_ (term mode)
X	1	0	0	High-impedance (high-z) mode
X	X	X	1	Low-leakage mode

Table 2. Slew-Rate Logic

SC1	SC0	DRIVER SLEW RATE (%)
0	0	100
0	1	75
1	0	50
1	1	25

Each output provides a nominal 400mV$_{P-P}$ swing and 50Ω source termination.

An open-emitter configuration is also available (Figure 4). Connect an external collector voltage to $V_{CCO\_}$ and add external pulldown resistors. These resistors are typically 50Ω to $V_{CCO\_}$ - 2V at the receiving end of the output trace. Alternate configurations may be used provided that the *Absolute Maximum Ratings* are not exceeded.

Active Load

The active load consists of linearly programmable source and sink current sources, a commutation buffer, and a diode bridge (see *Functional Diagram*). Analog reference inputs LDH_ and LDL_ program the sink and source currents, respectively, within the 0 to 35mA range. Analog reference input COM_ sets the commutation buffer output voltage. The source and sink naming convention is referenced to the device under test. Current out of the MAX9967 constitutes sink current and current into the MAX9967 constitutes source current.

The programmed source (low) current loads the device under test when $V_{DUT\_} > V_{COM\_}$. The programmed sink (high) current loads the device under test when $V_{DUT\_} < V_{COM\_}$.

The GS input allows a single level-setting DAC, such as the MAX5631 or MAX5734, to program the MAX9967's active load, driver, comparator, and clamps. Although all of the DAC levels are typically offset by V_{GS}, the operation of the MAX9967's ground-sense input nullifies this offset with respect to the active-load currents. Connect GS to the ground reference used by the DAC. ($V_{LDL\_}$ - V_{GS}) sets the source current by +10mA/V. ($V_{LDH\_}$ - V_{GS}) sets the sink current by -10mA/V.

The high-speed differential input LDEN_ and 3 bits of the control word (LDCAL, LDDIS, and LLEAK) control the load (Table 4). When the load is enabled, the internal source and sink current sources connect to the diode bridge. When the load is disabled, the internal current sources shunt to ground and the top and bottom of the bridge float (see the *Functional Diagram*). LLEAK places the load in low-leakage mode. LLEAK overrides LDEN_, LDDIS, and LDCAL. See the *Low-Leakage Mode, LLEAK* section for more detailed information.

LDDIS and LDCAL

In some tester configurations, the load enable is driven with the complement of the driver high-impedance signal (RCV_), so disabling the driver enables the load and vice versa. The LDDIS and LDCAL signals disable and enable the load independently of the state of LDEN_. This allows the load and driver to be simultaneously enabled and disabled for diagnostic purposes (Table 4).

Low-Leakage Mode, LLEAK

Asserting LLEAK through the serial port or with $\overline{RST}$ places the MAX9967 into a very low-leakage state (see the *Electrical Characteristics*). The comparators function at full speed, but the driver, clamps, and active load are disabled. This mode is convenient for making IDDQ and PMU measurements without the need for an output disconnect relay. LLEAK is programmed independently for each channel.

When DUT_ is driven with a high-speed signal while LLEAK is asserted, the leakage current momentarily increases beyond the limits specified for normal operation. The low-leakage recovery specification in the *Electrical Characteristics* table indicates device behavior under this condition.

Table 3. Comparator Logic

DUT_ > CHV_	DUT_ > CLV_	CH_	CL_
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

Dual, Low-Power, 500Mbps ATE Driver/Comparator with 35mA Load

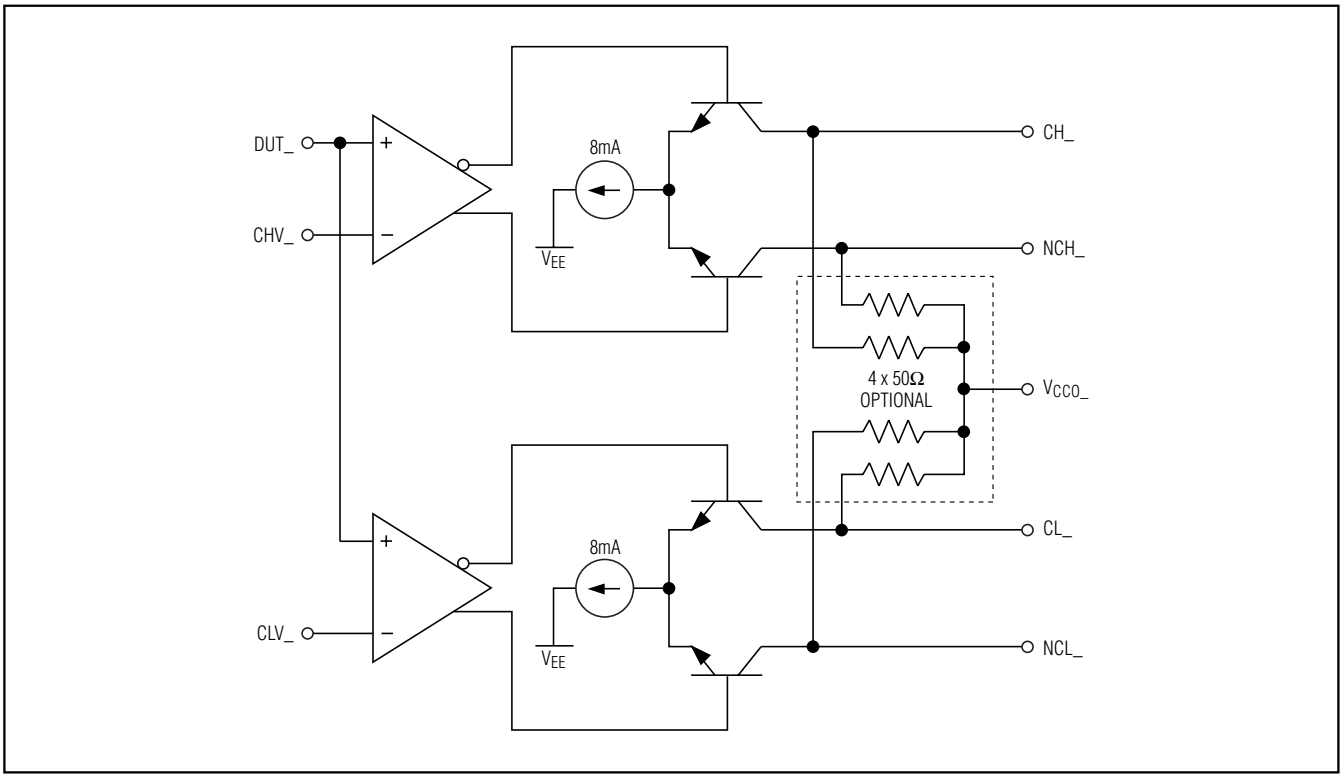


Figure 3. Open-Collector Comparator Outputs

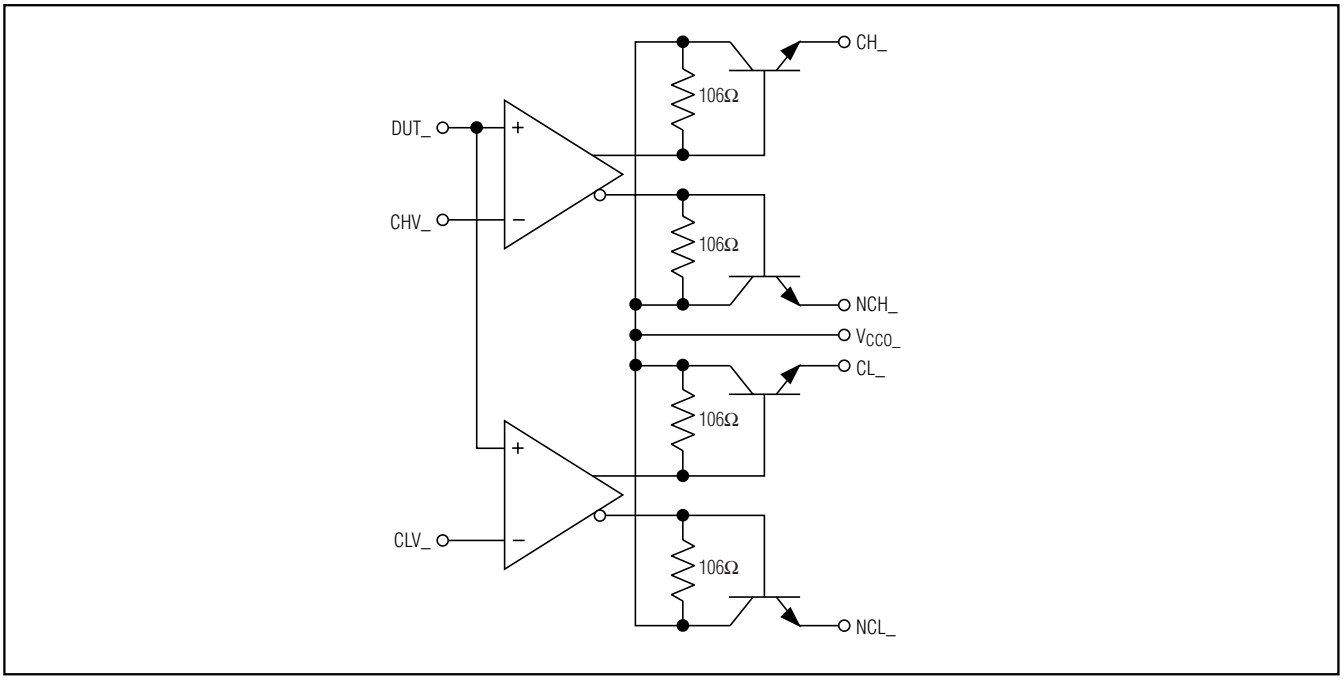


Figure 4. Open-Emitter Comparator Outputs

Table 4. Active Load Programming

EXTERNAL CONNECTIONS	INTERNAL CONTROL REGISTER			MODE
LDEN_	LDCAL	LDDIS	LLEAK	
0	0	0	0	Normal operating mode, load disabled
1	0	0	0	Normal operating mode, load enabled
X	1	0	0	Load enabled for diagnostics
X	X	1	0	Load disabled
X	X	X	1	Low-leakage mode

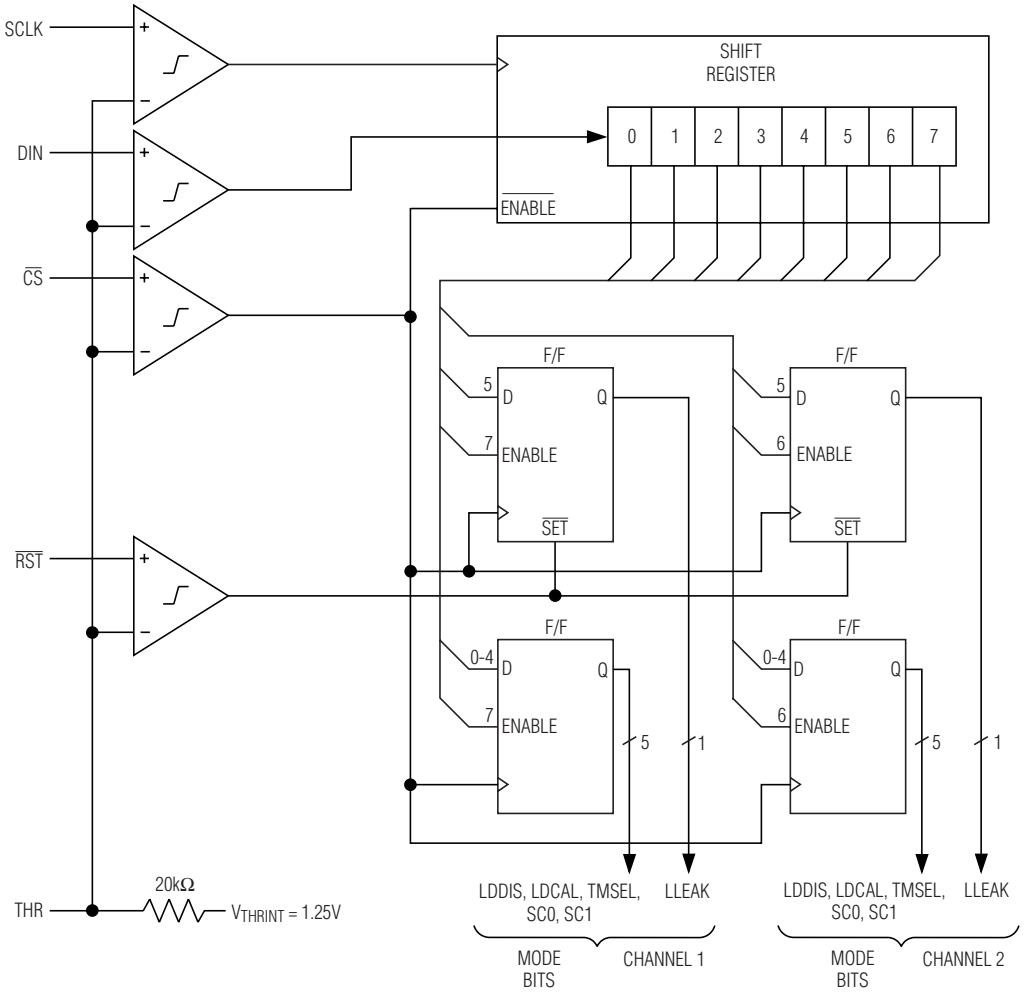


Figure 5. Serial Interface

Dual, Low-Power, 500Mbps ATE Driver/Comparator with 35mA Load

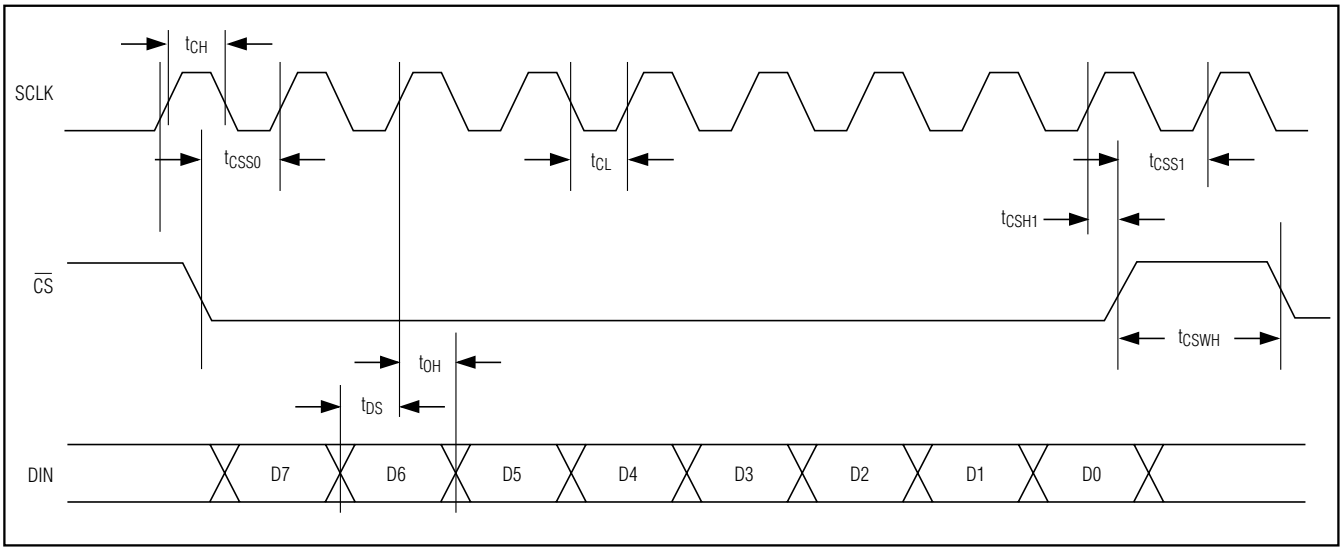


Figure 6. Serial-Interface Timing

Serial Interface and Device Control

A CMOS-compatible serial interface controls the MAX9967 modes (Figure 5). Control data flow into an 8-bit shift register (MSB first) and are latched when $\overline{CS}$ is taken high, as shown in Figure 6. Latches contain 6 control bits for each channel of the dual pin driver. Data from the shift register are loaded to either or both of the latches as determined by bits D6 and D7, and indicated in Figure 5 and Table 5. The control bits, in conjunction with external inputs DATA_ and RCV_, manage the features of each channel, as shown in Tables 1 and 2. $\overline{RST}$ sets LLEAK = 1 for both channels, forcing them into low-leakage mode. All other bits are unaffected. At power-up, hold $\overline{RST}$ low until V_{CC} and V_{EE} have stabilized.

Analog control input THR sets the threshold for the input logic, allowing operation with CMOS logic as low as 0.9V. Leaving THR unconnected results in a nominal threshold of 1.25V from an internal reference, providing compatibility with 2.5 to 3.3V logic.

Table 5. Shift-Register Functions

BIT	NAME	DESCRIPTION
D7	CH1	Channel 1 Write Enable. Set to 1 to update the control byte for channel 1. Set to 0 to make no changes to channel 1.
D6	CH2	Channel 2 Write Enable. Set to 1 to update the control byte for channel 2. Set to 0 to make no changes to channel 2.
D5	LLEAK	Low-Leakage Select. Set to 1 to put driver, load, and clamps into low-leakage mode. Comparators remain active in low-leakage mode. Set to 0 for normal operation.
D4	TMSEL	Driver Termination Select. Set to 1 to force the driver output to the DTV_ voltage when RCV_ = 1 (term). Set to 0 to place the driver into high-impedance mode when RCV_ = 1 (high-Z). See Table 1.
D3	SC1	Driver Slew-Rate Select. SC1 and SC0 set the driver slew rate. See Table 2.
D2	SC0	
D1	LDDIS	Load Disable. Set LDDIS to 1 to disable the load. Set to 0 for normal operation. See Table 4.
D0	LDCAL	Load Calibrate. Overrides LDEN to enable load. Set LDCAL to 1 to enable load. Set LDCAL to 0 for normal operation. See Table 4.

Temperature Monitor

The MAX9967 supplies a temperature output signal, TEMP, that asserts a nominal output voltage of 3.43V at a die temperature of +70°C (343K). The output voltage increases proportionately with temperature.

Heat Removal

Under normal circumstances, the MAX9967 requires heat removal through the exposed pad by use of an external heat sink. The exposed pad is electrically at V_{EE} potential, and must be either connected to V_{EE} or isolated.

Power dissipation is highly dependent upon the application. The *Electrical Characteristics Table* indicates power dissipation under the condition that the source and sink currents are programmed to 0mA. Maximum dissipation occurs when the source and sink currents are both at 35mA, the $V_{DUT\_}$ is at an extreme of the voltage range (-1.5V or +6.5V), and the diode bridge is fully commutated. Under these conditions, the additional power dissipated (per channel) is:

If the DUT is sourcing current, $\Delta P_D = (V_{DUT\_} - V_{EE}) \times I_{SOURCE} + (V_{CC} - V_{EE}) \times I_{SINK}$.

If the DUT is sinking current, $\Delta P_D = (V_{CC} - V_{DUT\_}) \times I_{SINK} + (V_{CC} - V_{EE}) \times I_{SOURCE}$.

The DUT sources the programmed (low) current when $V_{DUT\_} > V_{COM\_}$. The path of the current is from the DUT through the outside of the diode bridge and the source (low) current source to V_{EE}. The programmed sink current flows from V_{CC} through the sink (high) current source, the inside of the diode bridge, and the commutation buffer to V_{EE}.

The DUT sinks the programmed (high) current when $V_{DUT\_} < V_{COM\_}$. The path of the current is from V_{CC} through the sink (high) current source and the outside of the diode bridge to the DUT. The programmed source current flows from V_{CC} through the commutation buffer, the inside of the diode bridge, and the source (low) current source to V_{EE}.

Theta J-C of the exposed-pad package is very low, approximately 3°C/W to 4°C/W. Die temperature is thus highly dependent upon the heat-removal techniques used in the application.

Maximum total power dissipation occurs under the following conditions:

- V_{CC} = +10.5V
- V_{EE} = -6.5V
- $I_{SOURCE} = I_{SINK}$ = 35mA for both channels
- Load enabled
- $V_{DUT\_}$ = +6.5V
- $V_{COM\_}$ < +5.5V

Under these extreme conditions, the total power dissipation is approximately 6W. If the die temperature cannot be maintained at an acceptable level under these conditions, use software clamping to limit the load output currents to lower values and/or reduce the supply voltages.

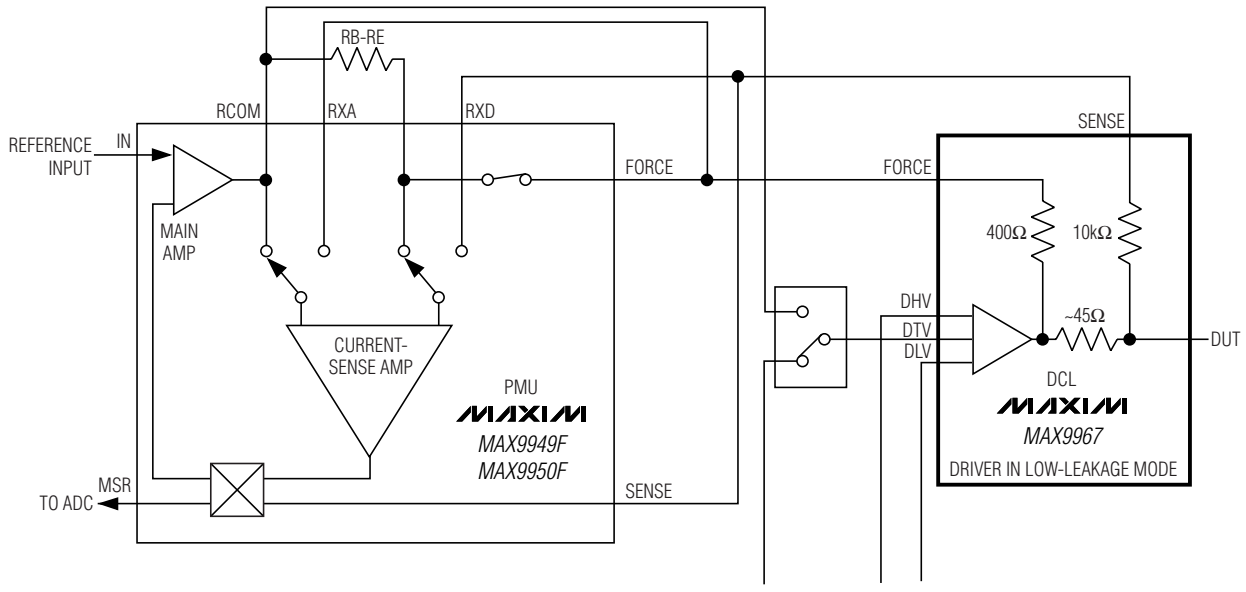
Chip Information

TRANSISTOR COUNT: 5656

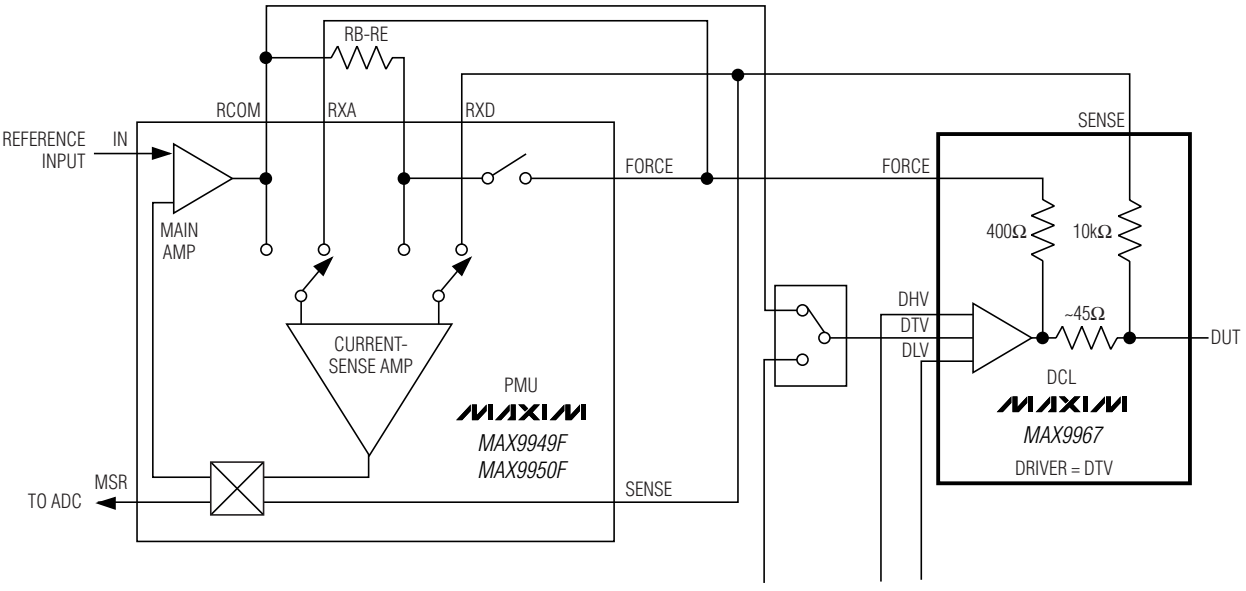
PROCESS: Bipolar

Dual, Low-Power, 500Mbps ATE Driver/Comparator with 35mA Load

Typical Application Circuits (Simplified)



INTERFACING TO PMU WITHOUT EXTERNAL RELAYS. PMU SOURCING 2mA OR LESS.



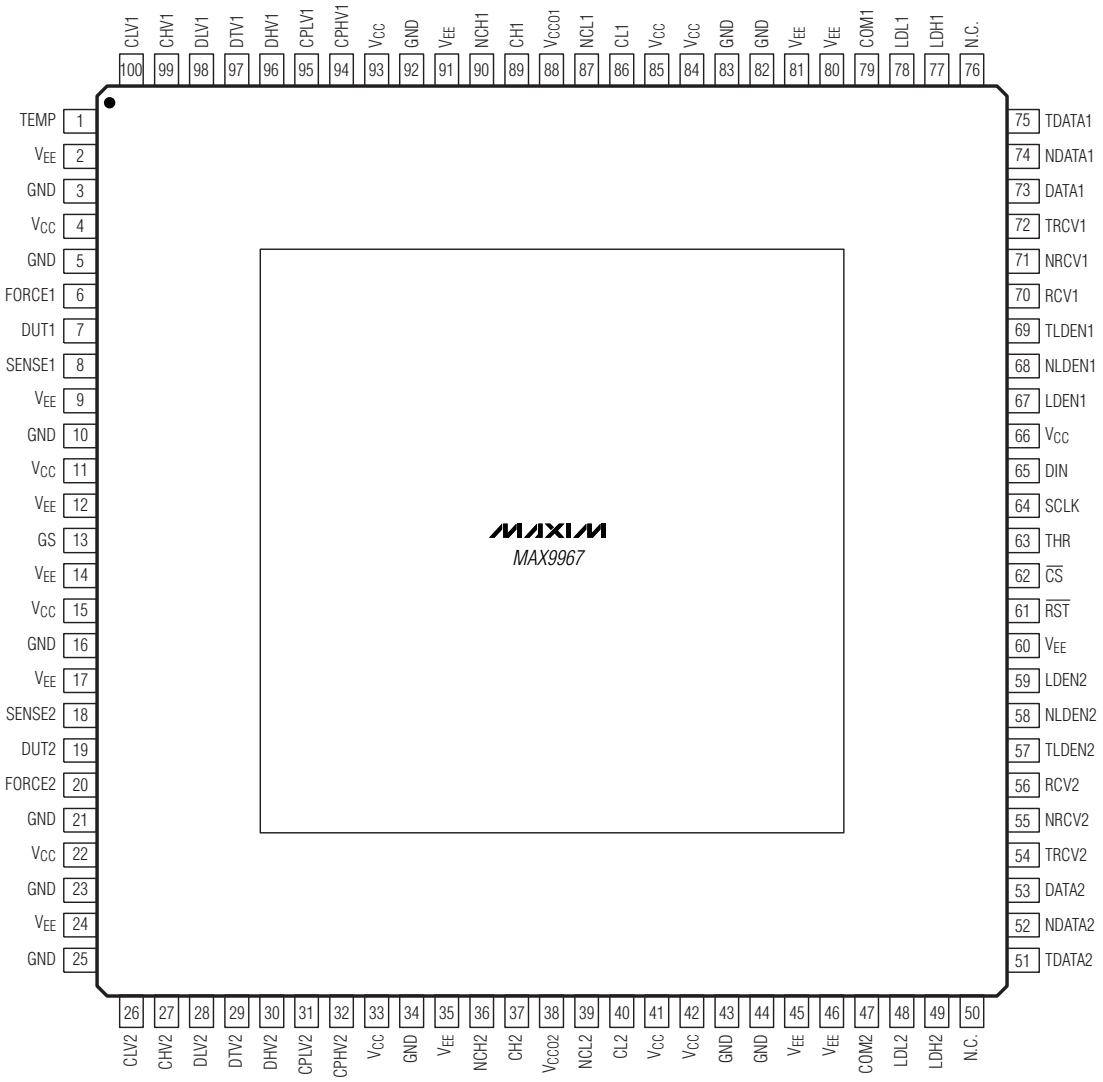
INTERFACING TO PMU WITHOUT EXTERNAL RELAYS. DCL SOURCING UP TO 60mA.

Selector Guide

PART	ACCURACY GRADE	COMPARATOR OUTPUT TYPE	COMPARATOR OUTPUT TERMINATION	HIGH-SPEED DIGITAL INPUT TERMINATION			HEAT EXTRACTION
				RCV_	DATA_	LDEN_	
MAX9967ADCCQ	A	Open collector	None	None	None	None	Top
MAX9967AGCCQ	A	Open collector	None	100	100	100	Top
MAX9967ALCCQ	A	Open collector	50Ω to $V_{CCO\_}$	100	100	100	Top
MAX9967AMCCQ	A	Open emitter	ECL/LVPECL	None	None	None	Top
MAX9967AQCCQ	A	Open emitter	ECL/LVPECL	100	100	100	Top
MAX967ARCCQ	A	Open collector	50Ω to $V_{CCO\_}$	None	100	100	Top
MAX9967BDCCQ	B	Open collector	None	None	None	None	Top
MAX9967BGCCQ	B	Open collector	None	100	100	100	Top
MAX9967BLCCQ	B	Open collector	50Ω to $V_{CCO\_}$	100	100	100	Top
MAX9967BMCCQ	B	Open emitter	ECL/LVPECL	None	None	None	Top
MAX9967BQCCQ	B	Open emitter	ECL/LVPECL	100	100	100	Top
MAX9967BRCCQ	B	Open collector	50Ω to $V_{CCO\_}$	None	100	100	Top

Dual, Low-Power, 500Mbps ATE Driver/Comparator with 35mA Load

Pin Configuration



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