4-CHANNEL ESD PROTECTION ARRAY WITH 1.5-pF IO CAPACITANCE

Check for Samples: TPD4E001-Q1

FEATURES

- **Qualified for Automotive Applications**
- **AEC-Q100 Qualified With the Following Results:**
  - **Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range**
  - **Device HBM ESD Classification Level H3B**
  - **HBM Level 15 kV**
  - **Device CDM ESD Classification Level C4B**
- **4-Channel ESD Clamp Array to Enhance System-Level ESD Protection**
- **Exceeds IEC61000-4-2 (Level 4) ESD Protection Requirements**
  - **±8-kV IEC 61000-4-2 Contact Discharge**
  - **±15-kV IEC 61000-4-2 Air-Gap Discharge**
- **5.5-A Peak Pulse Current (8/20-µs Pulse)**
- **Low 1.5-pF Input Capacitance**
- **Low 10-nA (Max) Leakage Current**
- **0.9-V to 5.5-V Supply-Voltage Range**

APPLICATIONS

- **Automotive Infotainment**
- **USB 2.0**
- **Ethernet**
- **Precision Analog Interface**
- **SVGA Connections**

DESCRIPTION

The TPD4E001-Q1 is a low-capacitance ESD-protection diode array designed to protect sensitive electronics connected to communication lines. Each channel consists of a pair of diodes that steer ESD pulses to V_{CC} or GND. The TPD4E001-Q1 protects against ESD pulses up to ±8-kV contact discharge and ±15-kV air-gap discharge, as specified in IEC 61000-4-2. This device has a 1.5-pF IO capacitance per channel, making it ideal for use in high-speed data IO interfaces. The low leakage current (10 nA maximum) ensures minimum power consumption for the system.

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	DBV (SOT-23)	Reel of 3000	TPD4E001QDBVRQ1	AAXQ

(1) For the most-current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

DBV PACKAGE
(TOP VIEW)

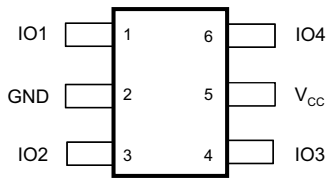
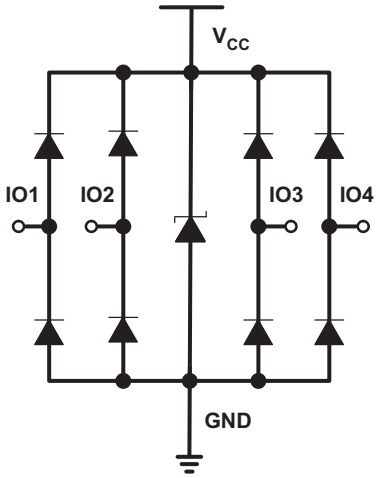


Figure 1. FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

DBV NO.	NAME	FUNCTION
1, 3, 4, 6	IOx	ESD-protected channel
2	GND	Ground
5	V_{CC}	Power-supply input. Bypass V_{CC} to GND with a 0.1-µF ceramic capacitor.

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}			–0.3	7	V
$V_{I/O}$	IO voltage tolerance		–0.3	V_{CC} + 0.3	V
T_{stg}	Storage temperature range		–65	150	°C
T_J	Junction temperature			150	°C
ESD	Electrostatic discharge	Human-body model, HBM, ESD classification level H3B		15	kV
		Charged-device model, CDM, ESD Classification Level C4B		750	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC[1]		TPD4E001-Q1 DBV 6 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance[2]	202.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance[3]	146.2	°C/W
θ_{JB}	Junction-to-board thermal resistance[4]	47.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter[5]	37.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter[6]	46.7	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[7]	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

Electrical Characteristics

V_{CC} = 5 V ± 10%, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[1]	MAX	UNIT
V_{CC}	Supply voltage			0.9		5.5	V
I_{CC}	Supply current				1	200	nA
V_F	Diode forward voltage	I_F = 10 mA		0.65		0.95	V
V_{BR}	Breakdown voltage	I_{BR} = 10 mA		11			V
V_{CLAMP}	Clamping voltage	Surge strike[2] on IO pin, GND pin grounded, V_{CC} = 5.5 V, I_{PP} = 5.5 A	Positive transients		16		V
V_{RWM}	Reverse standoff voltage	IO pin to GND pin				5.5	V
$I_{i/o}$	Channel leakage current	$V_{i/o}$ = GND to V_{CC}				±10	nA
$C_{i/o}$	Channel input capacitance	V_{CC} = 5 V, bias of V_{CC}/2			1.5		pF

(1) Typical values are at V_{CC} = 5 V and T_A = 25°C.
(2) Non-repetitive current pulse 8/20 µs exponentially decaying waveform according to IEC 61000-4-5.

ESD Protection

PARAMETER	TYP	UNIT
HBM	±15	kV
IEC 61000-4-2 contact discharge	±8	kV
IEC 61000-4-2 air-gap discharge	±15	kV
Peak pulse current, I_{PP} (Tp = 8/20 µs) [1]	5.5	A
Peak pulse power, P_{PP} (Tp = 8/20 µs) [1]	100	W

(1) Non-repetitive current pulse 8/20 µs exponentially decaying waveform according to IEC 61000-4-5.

TYPICAL OPERATING CHARACTERISTICS

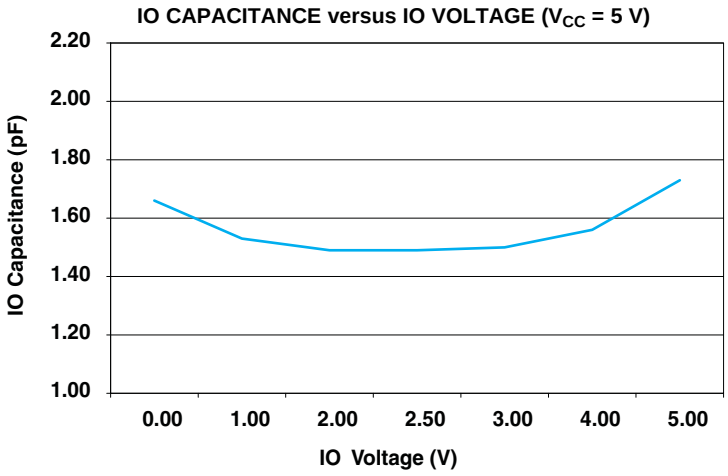


Figure 2.

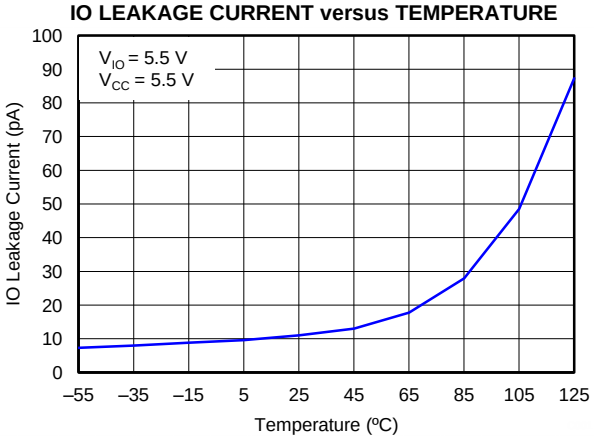


Figure 3.

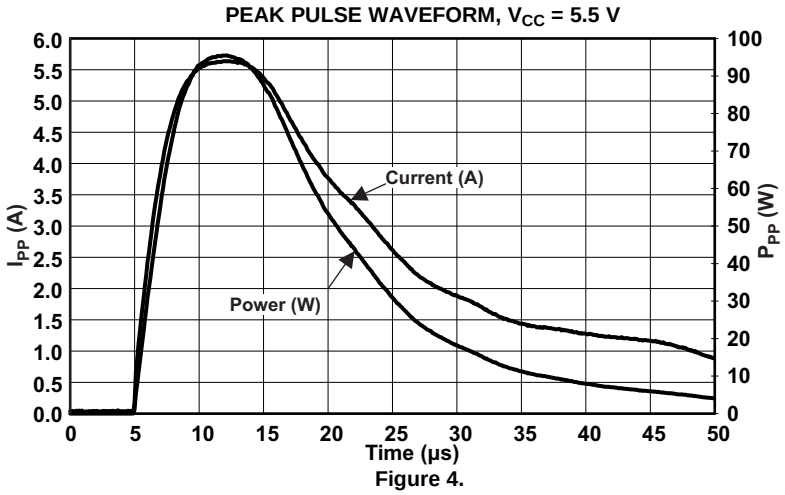
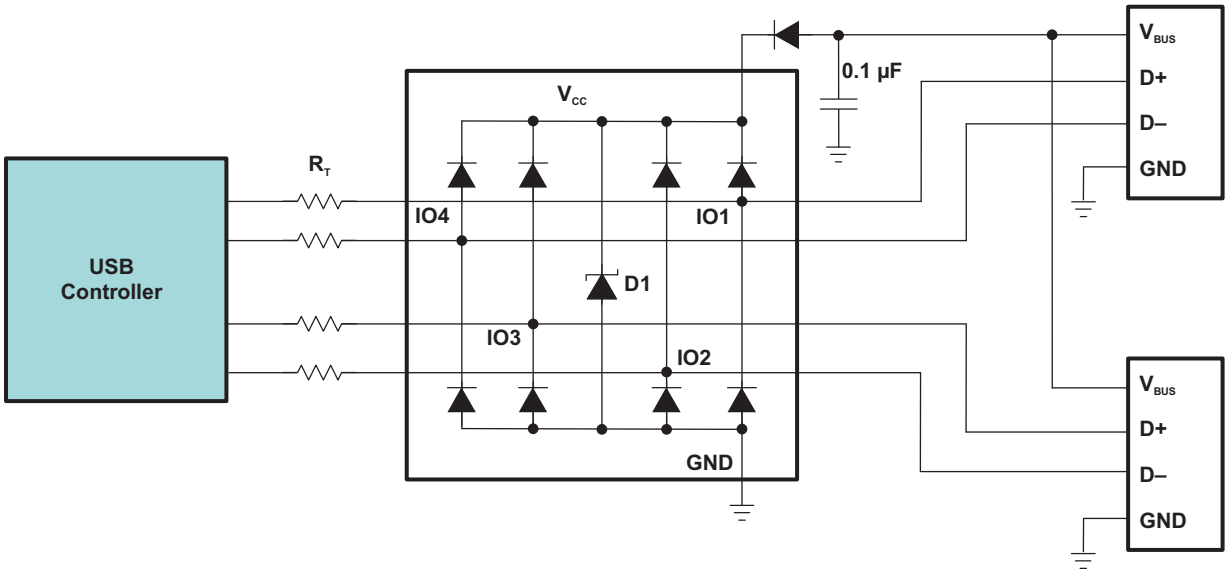


Figure 4.

APPLICATION INFORMATION



Detailed Description

When placed near the connector, the TPD4E001-Q1 ESD solution offers little or no signal distortion during normal operation due to low IO capacitance and ultralow leakage-current specifications. The TPD4E001-Q1 ensures that the core circuitry is protected and the system is functioning properly in the event of an ESD strike. For proper operation, observe the following layout and design guidelines:

1. Place the TPD4E001-Q1 solution close to the connector. This allows the TPD4E001-Q1 to take away the energy associated with ESD strike before it reaches the internal circuitry of the system board.
2. Place a 0.1-µF capacitor very close to the V_{CC} pin. This limits any momentary voltage surge at the IO pin during the ESD strike event.
3. Ensure that there is enough metallization for the V_{CC} and GND loop. During normal operation, the TPD4E001-Q1 consumes nA leakage current. But during the ESD event, V_{CC} and GND may see 15 A to 30 A of current, depending on the ESD level. Sufficient current path enables safe discharge of all the energy associated with the ESD strike.
4. Leave the unused IO pins floating.
5. One can connect the V_{CC} pin in two different ways:
   (a) If the V_{CC} pin connects to the system power supply, the TPD4E001-Q1 works as a transient suppressor for any signal swing above V_{CC} + V_F. TI recommends a 0.1-µF capacitor on the device V_{CC} pin for ESD bypass.
   (b) If the V_{CC} pin does not connect to the system power supply, the TPD4E001-Q1 can tolerate higher signal swing in the range up to 10 V. Note that TI still recommends a 0.1-µF capacitor at the V_{CC} pin for ESD bypass.

REVISION HISTORY

Changes from Revision B (February 2012) to Revision C **Page**

- Changed maximum I_{CC} supply current in Electrical Characteristics 3

Changes from Revision A (April 2013) to Revision B **Page**

- Made changes to FEATURES and APPLICATIONS 1
- Revised text in DESCRIPTION section 1
- Made change in the Elecrical Characteristics 3
- Added notes to ESD Protection table 3
- Revised Figure 3 graph 4
- Revised APPLICATION INFORMATION schematic 5

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD4E001QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AAXQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

OTHER QUALIFIED VERSIONS OF TPD4E001-Q1 :

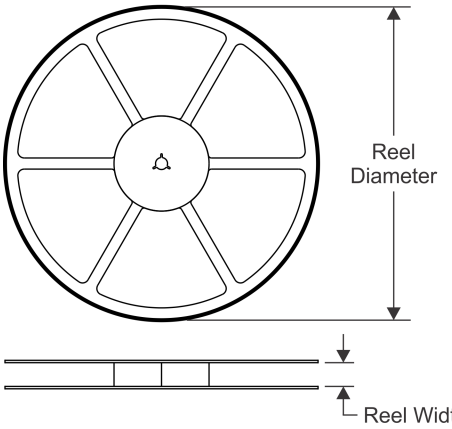
- Catalog: TPD4E001

NOTE: Qualified Version Definitions:

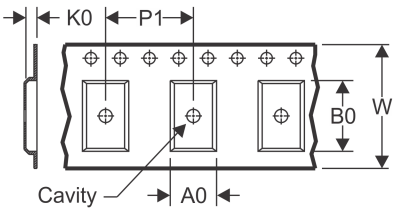
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

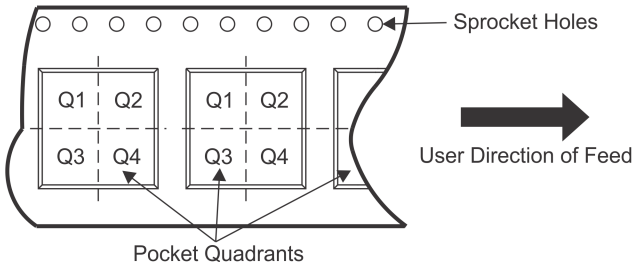


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

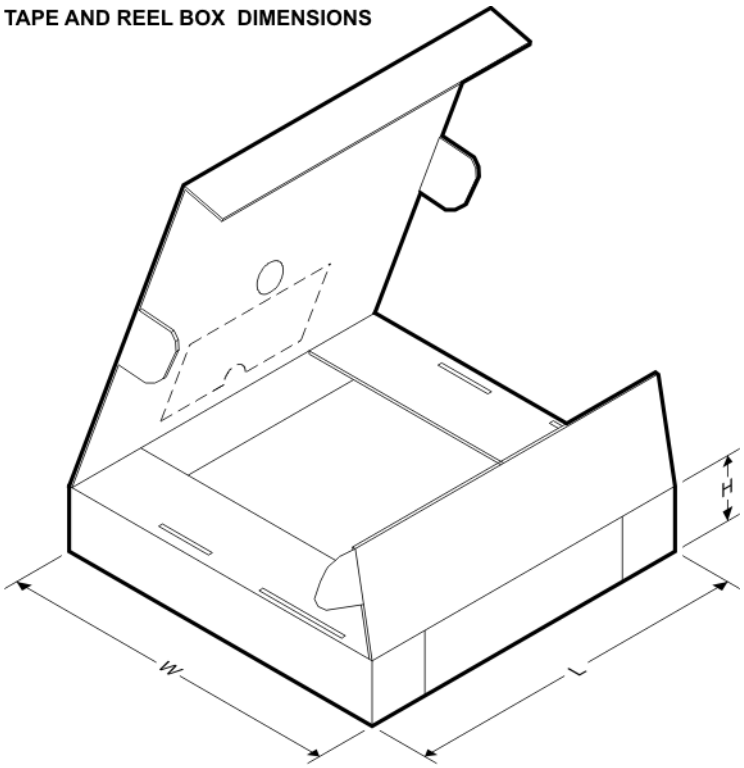
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4E001QDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

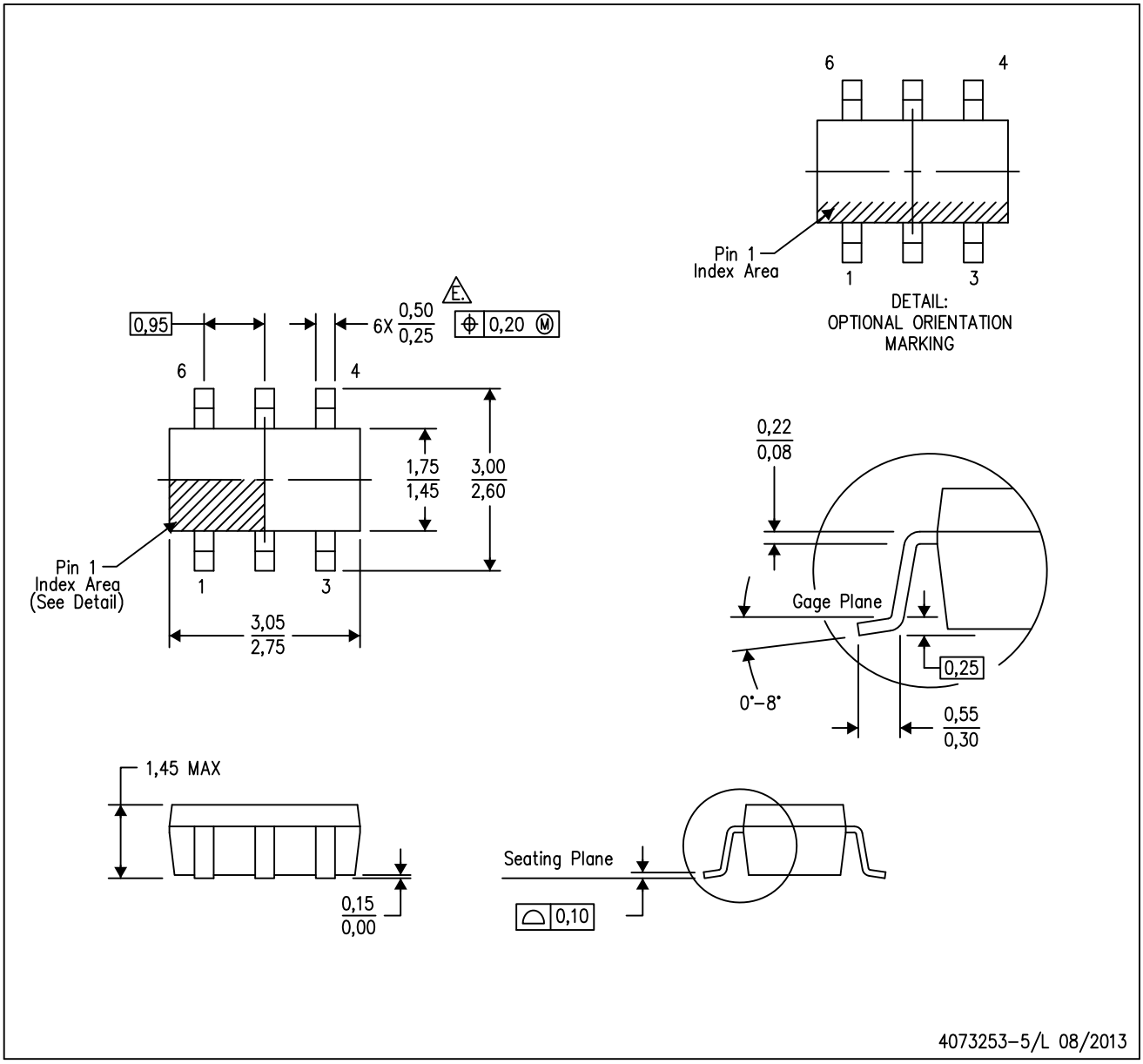
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

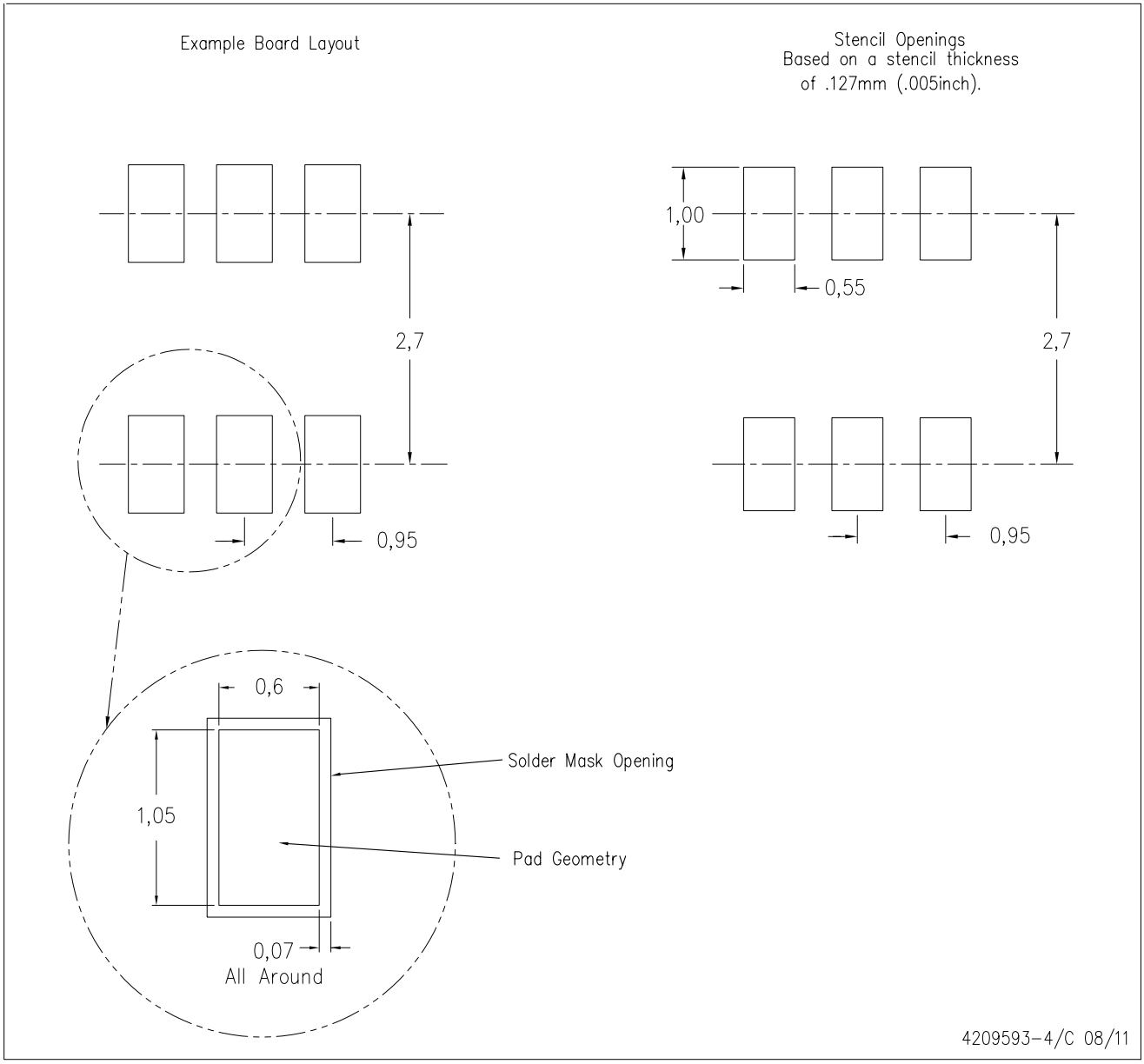
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4E001QDBVRQ1	SOT-23	DBV	6	3000	180.0	180.0	18.0

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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