High-Performance, Eco-mode™, Single Synchronous Step-Down Controller with PMBus™

Check for Samples: TPS53819A

FEATURES

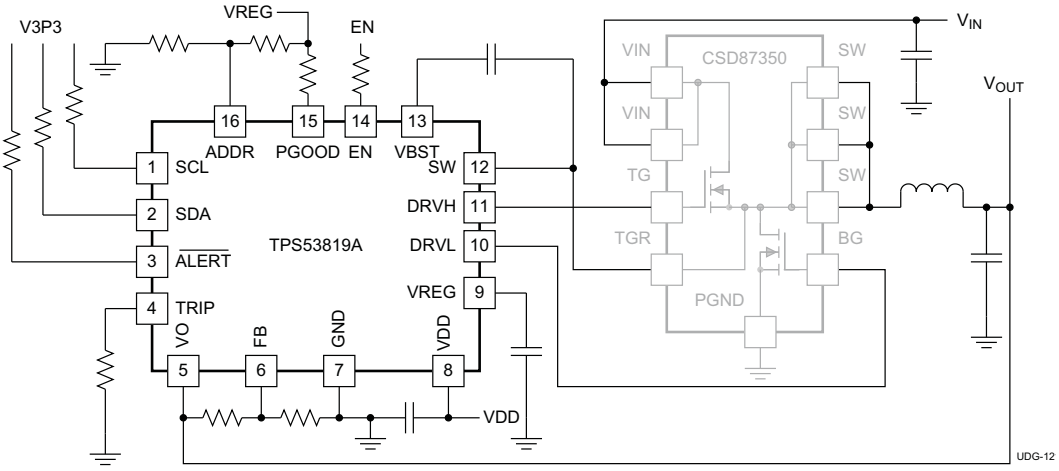
- **Conversion Input Voltage Range: 3 V to 28 V**
- **VDD Input Voltage Range: 4.5 V to 28 V**
- **Output Voltage Range: 0.6 V to 5.5 V**
- **Supports All Ceramic Output Capacitors**
- **Reference Voltage: 600 mV ±0.5% Tolerance**
- **±9% Voltage Adjustment via PMBus™**
- **Built-in 5-V LDO**
- **D-CAP2™ Mode with 100-ns Load Step Response**
- **Auto-Skip Eco-mode™ for Light-Load Efficiency**
- **Adaptive On-Time Control Architecture With Eight Selectable Frequencies via PMBus**
- **Supports Voltage Margining via PMBus**
- **Programmable Soft-Start Time via PMBus**
- **Programmable Power-On Delay via PMBus**
- **Programmable VDD UVLO Level via PMBus**
- **Fault Report via PMBus**
- **Pre-Charged Start-Up Capability**
- **Built-In Output Discharge**
- **Power Good Output With Programmable Delay**
- **Internal Overvoltage, Undervoltage, and Overcurrent Limit Protections**
- **Thermal Shutdown (Non-Latch)**
- **3 mm × 3 mm 16-pin QFN Package**

APPLICATIONS

- **Point-of-Load Systems**
  - **Storage Computers**
  - **Server Computers**
  - **Multi-Function Printers**
  - **Embedded Computing**

DESCRIPTION

TPS53819A is a small-sized, single buck controller with adaptive on-time D-CAP2 mode control and PMBus. The device is suitable for low output voltage and high current, system power rail, or similar point-of-load (POL) power supply in digital consumer products. Small package with minimal pin-count saves space on the PCB, while the programmability and fault report via PMBus simplify the power supply design. The skip-mode at light-load condition combined with strong gate drivers and low-side FET $R_{DS(on)}$ current sensing can support low-loss and high efficiency operation, over a broad load range. The conversion input voltage, which is the high-side FET drain voltage, ranges from 3 V to 28 V. The supply voltage (VDD) for TPS53819A is from 4.5 V to 28 V. The output voltage ranges from 0.6 V to 5.5 V. The TPS53819A is available in a 16-pin, QFN package and is specified from –40°C to 85°C.



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Eco-mode, D-CAP2 are trademarks of Texas Instruments.
PMBus is a trademark of SMIF, Inc.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)(2)

T_A	PACKAGE	ORDERABLE DEVICE	PINS	OUTPUT SUPPLY	MINIMUM ORDER QUANTITY	ECO PLAN
–40°C to 85°C	Plastic QFN (RGT)	TPS53819ARGTR	16	Tape-and-Reel	3000	Green (RoHS and no Pb/Br)
		TPS53819ARGTT		Mini-reel	250	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the TI website at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			VALUE		UNIT
			MIN	MAX	
Input voltage range(2)	VBST		–0.3	38	V
	VBST(3)		–0.3	6	
	EN		–0.3	7.7	
	VO, FB, SCL, SDA, ADDR		–0.3	6	
	VDD		–0.3	30	
	SW	DC	–3	32	
		Pulse < 30% of the repetitive period	–5	32	
Output voltage range(2)	DRVH	DC	–3	38	V
		Pulse < 30% of the repetitive period	–5	38	
	DRVH(3), DRVL		–0.3	6	
	$\overline{\text{ALERT}}$, VREG, TRIP		–0.3	6	
	PGOOD		–0.3	7.7	
Electrostatic discharge	Human body model (HBM) QSS 009-105 (JESD22-A114A)			2000	V
	Charged device model (CDM) QSS 009-147 (JESD22-C101B.01)			500	
Junction temperature range, T_J				150	°C
Storage temperature range, T_{stg}			–55	150	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.
(3) Voltage values are with respect to the SW terminal.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS53819A RGT 16 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	51.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	85.4	
θ_{JB}	Junction-to-board thermal resistance(4)	20.1	
ψ_{JT}	Junction-to-top characterization parameter(5)	1.3	
ψ_{JB}	Junction-to-board characterization parameter(6)	19.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	6.0	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
Input voltage range	VBST		–0.1		35.5	V
	VBST(1)		–0.1		5.5	
	EN		–0.1		6.5	
	VO, FB, SCL, SDA, ADDR		–0.1		5.5	
	VDD		4.5		28	
	SW	DC	–3		30	V
		Pulse < 30% of the repetitive period	–4.5		30	
Output voltage range	DRVH	DC	–3		35.5	V
		Pulse < 30% of the repetitive period	–4.5		35.5	
	DRVH(1), DRVL		–0.1		5.5	
	$\overline{\text{ALERT}}$, VREG		–0.1		5.5	
	PGOOD		–0.1		6.5	
T_A	Operating free-air temperature		–40		85	°C

(1) Voltage values are with respect to the SW terminal.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, V_{VREG}= 5 V, V_{EN}= 5 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{VDD}	VDD bias current	T_A = 25°C, no load, power conversion enabled (no switching)		920		µA
$I_{VDDSTBY}$	VDD standby current	T_A = 25°C, no load, power conversion disabled		610		µA
INTERNAL REFERENCE AND FEEDBACK REGULATION VOLTAGE						
V_{FB}	Feedback regulation voltage	FB w/r/t GND, CCM condition		600		mV
V_{FBTOL}	Feedback voltage tolerance	FB w/r/t GND, 0°C ≤ T_J ≤ 85°C	597	600	603	mV
$V_{DACTOL1}$	DAC voltage tolerance 1	FB w/r/t GND, 0°C ≤ T_A ≤ 85°C, all settings with VOUT_ADJUSTMENT only	–4.8		4.8	mV
$V_{DACTOL2}$	DAC voltage tolerance 2	FB w/r/t GND, 0°C ≤ T_A ≤ 85°C, all settings with VOUT_MARGIN only	–4.8		4.8	mV
$V_{DACTOL3}$	DAC voltage tolerance 3	FB w/r/t GND, 0°C ≤ T_A ≤ 85°C, with VOUT_ADJUSTMENT=0Dh and VOUT_MARGIN=70h for +5%	–4.8		4.8	mV
$V_{DACTOL4}$	DAC voltage tolerance 4	FB w/r/t GND, 0°C ≤ T_A ≤ 85°C, with VOUT_ADJUSTMENT=13h and VOUT_MARGIN=07h for -5%	–4.8		4.8	mV
V_{IOS_LPCMP}	Loop comparator input offset voltage	V_{REF} to V_{FB}, T_A = 25°C	–2.5		2.5	mV
I_{FB}	FB pin input current	V_{FB} = 600 mV	–1		1	µA
OUTPUT VOLTAGE						
I_{VODIS}	VO discharge current	V_{VO} = 0.5 V, power conversion disabled	10	12		mA
FREQUENCY CONTROL						
f_{SW}	VO switching frequency	V_{IN} = 12 V, V_{VO} = 3.3 V, FS <2:0> =000		275		kHz
		V_{IN} = 12 V, V_{VO} = 3.3 V, FS <2:0> =001		325		
		V_{IN} = 12 V, V_{VO} = 3.3 V, FS <2:0> =010		425		
		V_{IN} = 12 V, V_{VO} = 3.3 V, FS <2:0> =011		525		
		V_{IN} = 12 V, V_{VO} = 3.3 V, FS <2:0> =100		625		
		V_{IN} = 12 V, V_{VO} = 3.3 V, FS <2:0> =101		750		
		V_{IN} = 12 V, V_{VO} = 3.3 V, FS <2:0> =110		850		
		V_{IN} = 12 V, V_{VO} = 3.3 V, FS <2:0> =111		1000		
$t_{ON(min)}$	Minimum on-time(1)	DRVH rising to falling		60		ns
$t_{OFF(min)}$	Minimum off-time	DRVH falling to rising		320		ns
DRIVER						
R_{DRVH}	DRVH resistance	Source, I_{DRVH} = 50 mA		1.6		Ω
		Sink, I_{DRVH} = 50 mA		0.6		
R_{DRVL}	DRVL resistance	Source, I_{DRVL} = 50 mA		0.9		
		Sink, I_{DRVL} = 50 mA		0.5		
t_{DEAD}	Dead time	DRVH-off to DRVL-on		10		ns
		DRVL-off to DRVH-on		20		
INTERNAL BOOT STRAP SWITCH						
V_F	Forward voltage	$V_{VREG-VBST}$, T_A = 25°C, I_F = 10 mA		0.1	0.2	V
I_{VBST}	VBST leakage current	T_A = 25°C, V_{VBST} = 33 V, V_{SW} = 28 V		0.01	1.5	µA
ENABLE LOGIC THRESHOLD						
V_L	EN low-level voltage				0.5	V
V_H	EN high-level voltage		1.8			V
V_{HYST}	EN hysteresis voltage			0.22		V
I_{LEAK}	EN input leakage current		-1	0	1	µA

(1) Specified by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, V_{VREG}= 5 V, V_{EN}= 5 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
SOFT START						
t_{SS}	Soft-start time	SST<1:0>=00		1.0		ms
		SST<1:0>=01		2.0		
		SST<1:0>=10		4.0		
		SST<1:0>=11		8.0		
POWER-ON DELAY						
t_{PODLY}	Power-on delay time	Delay from enable to switching POD<2:0>=000		356		µs
		Delay from enable to switching POD<2:0>=001		612		µs
		Delay from enable to switching POD<2:0>=010		1.124		ms
		Delay from enable to switching POD<2:0>=011		2.148		ms
		Delay from enable to switching POD<2:0>=100		4.196		ms
		Delay from enable to switching POD<2:0>=101		8.292		ms
		Delay from enable to switching POD<2:0>=110		16.48		ms
		Delay from enable to switching POD<2:0>=111		32.86		ms
POWER GOOD COMPARATOR						
V_{PGTH}	Powergood threshold	PGOOD in from higher	105%	108%	111%	
		PGOOD in from lower	89%	92%	95%	
		PGOOD out to higher	113%	116%	119%	
		PGOOD out to lower	81%	84%	87%	
t_{PGDLY}	PGOOD delay time	Delay for PGOOD going in PGD<2:0>=000	165	256	320	µs
		Delay for PGOOD going in PGD<2:0>=001	409	512	614	µs
		Delay for PGOOD going in PGD<2:0>=010	0.819	1.024	1.228	ms
		Delay for PGOOD going in PGD<2:0>=011	1.638	2.048	2.458	ms
		Delay for PGOOD going in PGD<2:0>=100	3.276	4.096	4.915	ms
		Delay for PGOOD going in PGD<2:0>=101	6.553	8.192	9.83	ms
		Delay for PGOOD going in PGD<2:0>=110	13.104	16.38	19.656	ms
		Delay for PGOOD going in PGD<2:0>=111	105	131	157	ms
		Delay for PGOOD coming out			2	µs
I_{PG}	PGOOD sink current	V_{PGOOD} = 0.5 V		6.9		mA
I_{PGLK}	PGOOD leakage current	V_{PGOOD} = 5.0 V	-1	0	1	µA

ELECTRICAL CHARACTERISTICS (continued)

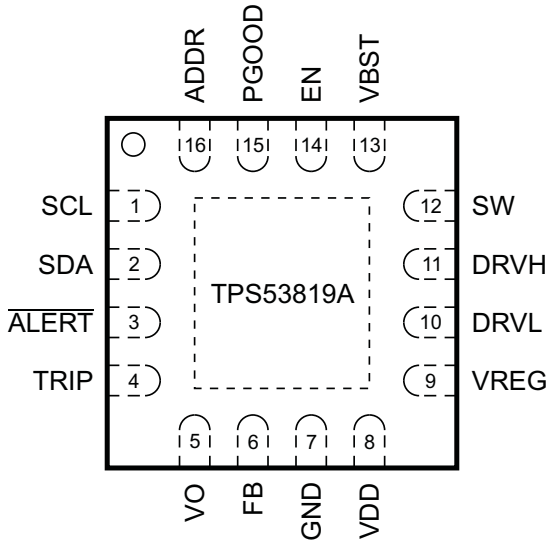
over operating free-air temperature range, V_{VREG}= 5 V, V_{EN}= 5 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
CURRENT DETECTION						
I_{TRIP}	TRIP source current	T_A = 25°C, V_{TRIP} = 0.4 V, $R_{DS(on)}$ sensing	9	10	11	µA
TC_{ITRIP}	TRIP source current temperature coefficient(2)	$R_{DS(on)}$ sensing		4700		ppm/°C
V_{TRIP}	TRIP voltage range	$R_{DS(on)}$ sensing	0.2		3	V
V_{OCLP}	Positive current limit threshold	V_{TRIP} = 3.0 V, $R_{DS(on)}$ sensing	360	375	390	mV
		V_{TRIP} = 1.6 V, $R_{DS(on)}$ sensing	190	200	210	
		V_{TRIP} = 0.2 V, $R_{DS(on)}$ sensing	20	25	30	
V_{OCLN}	Negative current limit threshold	V_{TRIP} = 3.0 V, $R_{DS(on)}$ sensing	–390	–375	–360	mV
		V_{TRIP} = 1.6 V, $R_{DS(on)}$ sensing	–212	–200	–188	
		V_{TRIP} = 0.2 V, $R_{DS(on)}$ sensing	–30	–25	–20	
V_{ZC}	Zero cross detection offset			0		mV
PROTECTIONS						
$V_{VREGUVLO}$	VREG UVLO threshold voltage	Wake-up		3.32		V
		Shutdown		3.11		
V_{OVP}	OVP threshold voltage	OVP detect voltage	117%	120%	123%	
t_{OVPDLY}	OVP propagation delay time	With 100-mV overdrive		430		ns
V_{UVP}	UVP threshold voltage	UVP detect voltage	65%	68%	71%	
t_{UVPDLY}	UVP delay time	UVP filter delay		1		ms
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold	Shutdown temperature		140		°C
		Hysteresis		40		
LDO VOLTAGE						
V_{REG}	LDO output voltage	V_{IN} = 12 V, I_{LOAD} = 10 mA	4.5	5	5.5	V
V_{DOVREG}	LDO low droop drop-out voltage	V_{IN} = 4.5 V, I_{LOAD} = 30 mA, T_A = 25°C			365	mV
$I_{LDO(max)}$	LDO overcurrent limit(2)	V_{IN} = 12 V, T_A = 25°C		152		mA
VDD UVLO VOLTAGE						
VDD_{UVLO}	VDD UVLO voltage	VDDINUVLO<2:0>=0xx		10.2		V
		VDDINUVLO<2:0>=101	4.1	4.25	4.4	
		VDDINUVLO<2:0>=110		6.0		
		VDDINUVLO<2:0>=111		8.1		
$VDD_{HY-UVLO}$	VDD UVLO hysteresis voltage	0°C ≤ T_J ≤ 85°C		0.2		V
PMBus SCL and SDA INPUT BUFFER LOGIC THRESHOLDS						
$V_{IL-PMBUS}$	SCL and SDA low-level input voltage(2)	0°C ≤ T_J ≤ 85°C			0.8	V
$V_{IH-PMBUS}$	SCL and SDA high-level input voltage(2)	0°C ≤ T_J ≤ 85°C	2.1			V
$V_{HY-PMBUS}$	SCL and SDA hysteresis voltage(2)	0°C ≤ T_J ≤ 85°C		240		mV
PMBus SDA and $\overline{\text{ALERT}}$ OUTPUT PULLDOWN						
$V_{OL1-PMBUS}$	SDA and $\overline{\text{ALERT}}$ low-level output voltage(2)	$V_{DDPMBus}$ = 5.5 V, R_{PULLUP} = 1.1 kΩ, 0°C ≤ T_J ≤ 85°C			0.4	V
$V_{OL2-PMBUS}$	SDA and $\overline{\text{ALERT}}$ low-level output voltage(2)	$V_{DDPMBus}$ = 3.6 V, R_{PULLUP} = 0.7 kΩ, 0°C ≤ T_J ≤ 85°C			0.4	V

(2) Specified by design. Not production tested.

DEVICE INFORMATION

RGT PACKAGE
16 PINS
(TOP VIEW)

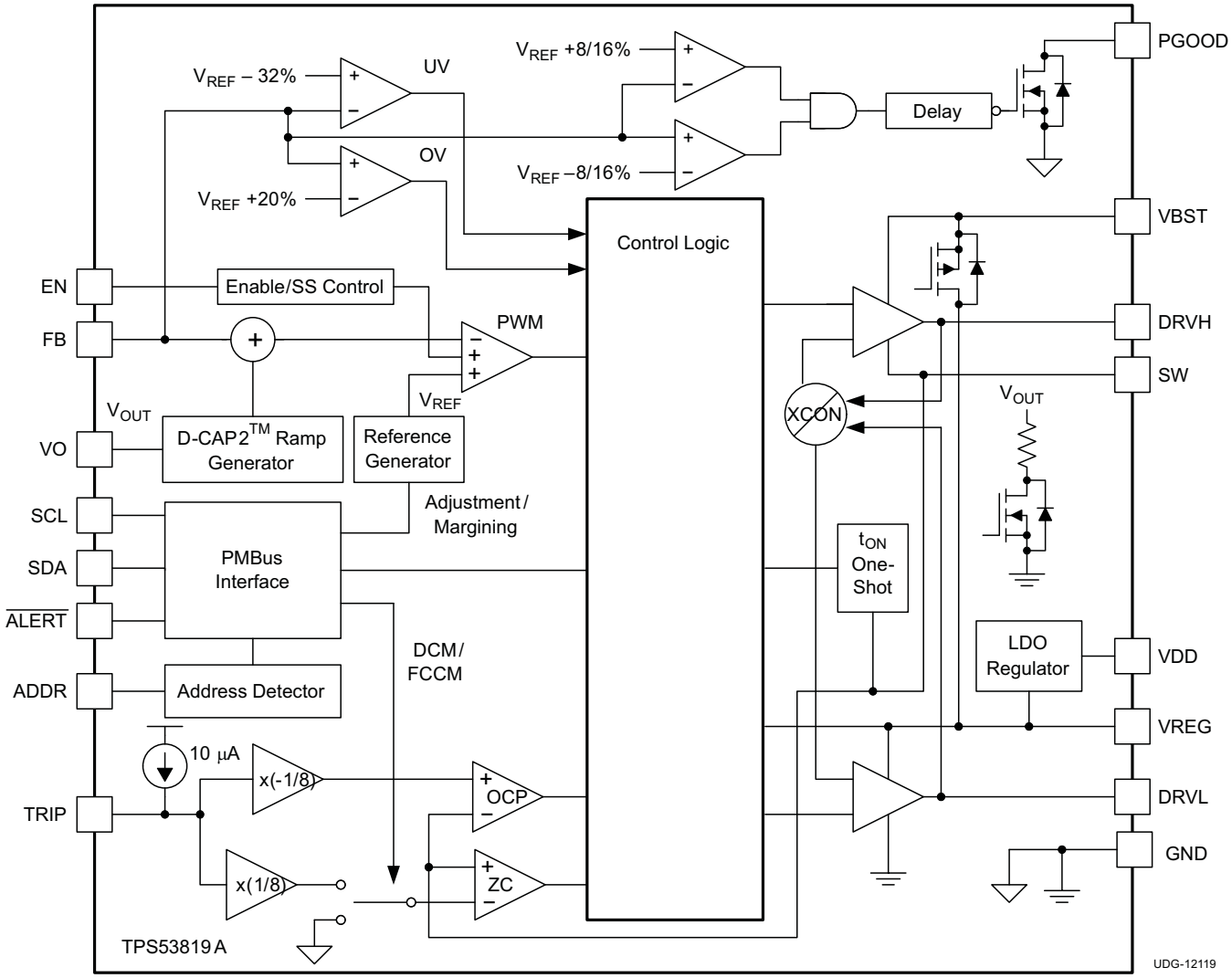


PIN FUNCTIONS (PMBus version)

NAME	NO.	I/O/P (1)	DESCRIPTION
ADDR	16	I	PMBus address configuration. Connect this pin to a resistor divider between VREG and GND to program different address settings. (See Table 2 for details.)
$\overline{\text{ALERT}}$	3	O	Open-drain alert output for the PMBus interface.
DRVH	11	O	High-side MOSFET floating driver output that is referenced to SW node. The gate drive voltage is defined by the voltage across bootstrap capacitor between VBST and SW.
DRVL	10	O	Synchronous MOSFET driver output that is referenced to GND. The gate drive voltage is defined by VREG voltage.
EN	14	I	Enable pin that can turn on the DC/DC switching converter. EN pin works in conjunction with the CP bit in PMBus ON_OFF_CONFIG register.
FB	6	I	Output voltage feedback input. Connect this pin to a resistor divider between output voltage and GND.
GND	7	G	Ground pin.
PGOOD	15	O	Open drain power good status signal. Provides start-up delay time after FB voltage falls within specified limits. After FB voltage goes out of specified limits, PGOOD goes low within 2 µs.
SCL	1	I	Clock input for the PMBus interface.
SDA	2	I/O	Data I/O for the PMBus interface.
SW	12	P	Output switching terminal of power converter. Connect this pin to the output inductor.
TRIP	4	I/O	OCL detection threshold setting pin. A 10-µA current with a T_C of 4700ppm/°C is sourced out of the TRIP pin and is used to set the OCL trip voltage as follows: $V_{OCL} = V_{TRIP}/8$ ($V_{TRIP} \le 3$ V, $V_{OCL} \le 375$ mV)
VBST	13	P	Supply rail for high-side gate driver (boost terminal). Connect bootstrap capacitor from this pin to SW node. Internally connected to VREG via bootstrap PMOS switch.
VDD	8	P	Controller power supply input.
VO	5	I	Output voltage.
VREG	9	P	5-V low-drop-out (LDO) output. Supplies the internal analog and driver circuitry.

(1) I=Input, O=Output, P=Power, G=Ground

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

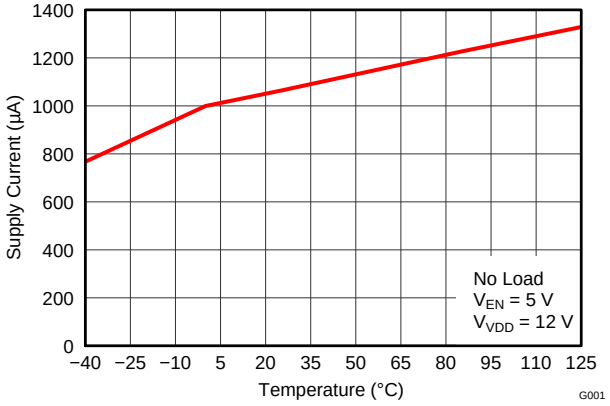


Figure 1. VDD Supply Current vs Temperature

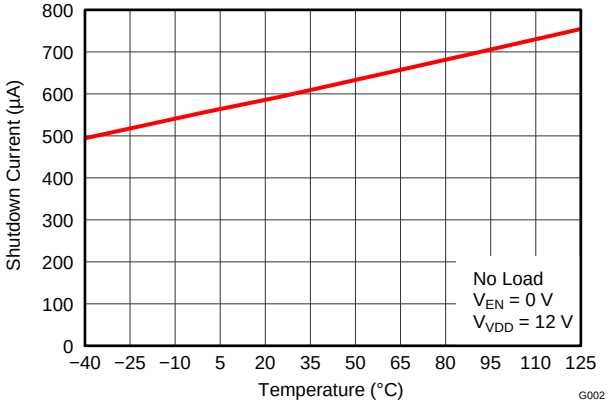


Figure 2. VDD Shutdown Current vs Temperature

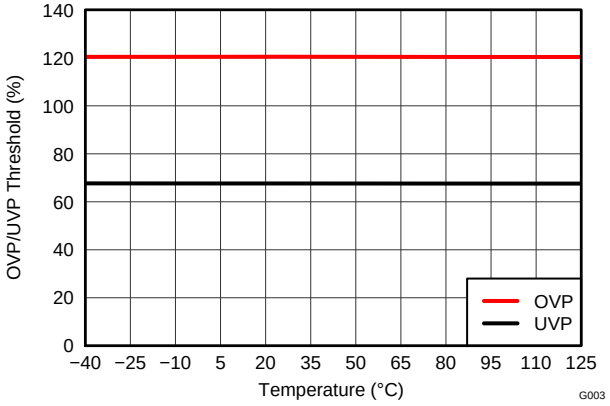


Figure 3. OVP/UVP Thresholds vs Temperature

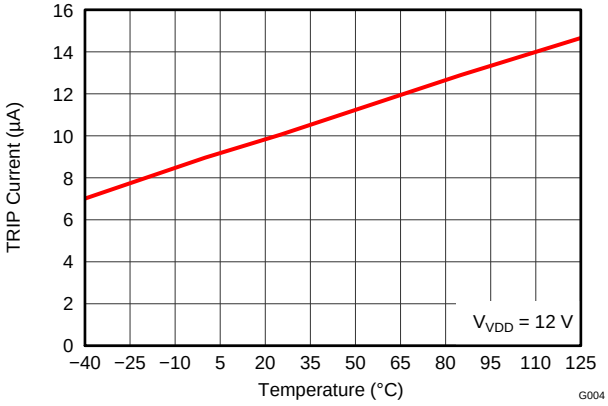


Figure 4. TRIP Pin Current vs Temperature

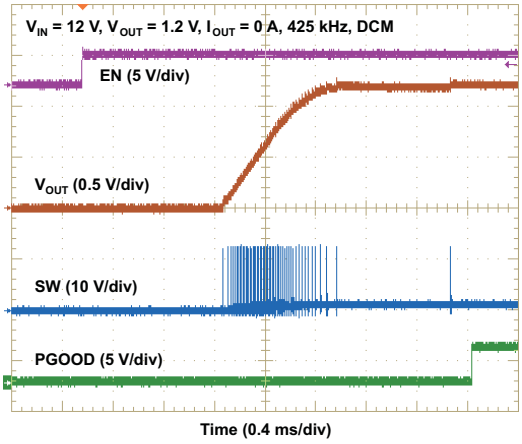


Figure 5. No-Load Start-Up Waveforms with DCM

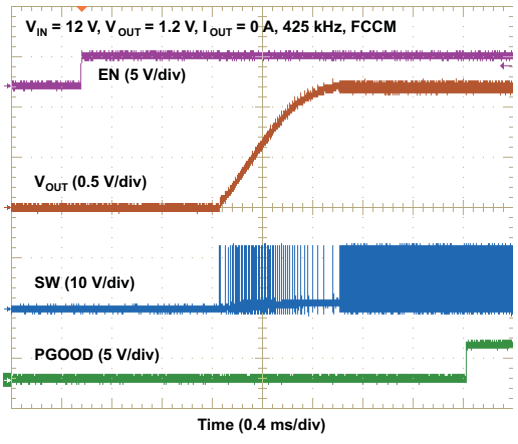


Figure 6. No-Load Start-Up Waveforms with FCCM

TYPICAL CHARACTERISTICS (continued)

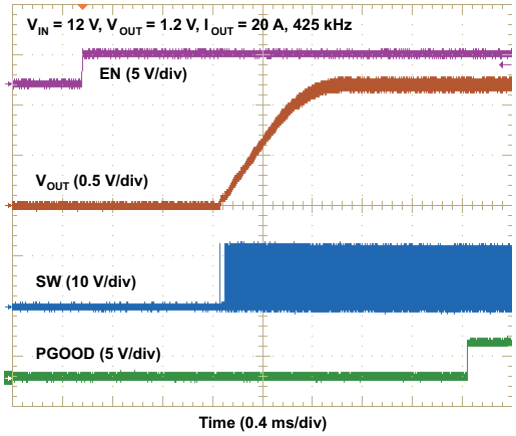


Figure 7. Full-Load Start-Up Waveforms

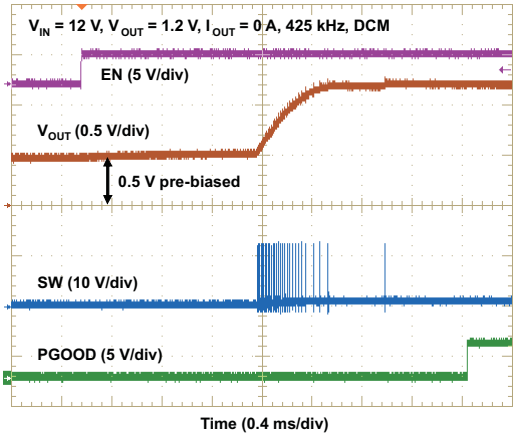


Figure 8. Pre-Bias Start-Up Waveforms with DCM

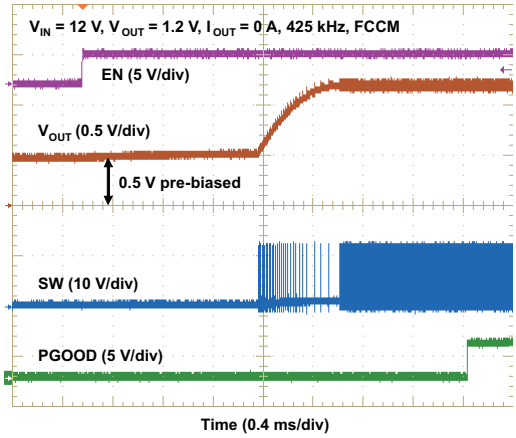


Figure 9. Pre-Bias Start-Up Waveforms with FCCM

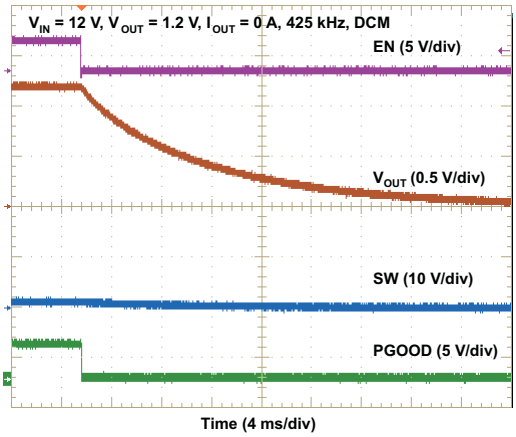


Figure 10. No-Load Shutdown Waveforms with DCM

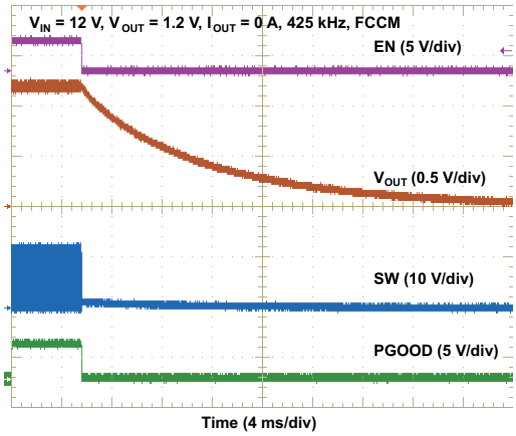


Figure 11. No-Load Shutdown Waveforms with FCCM

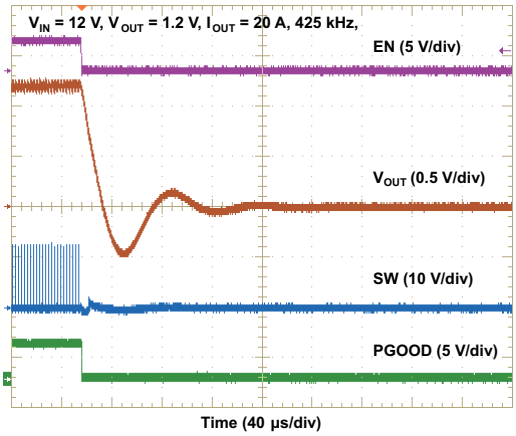


Figure 12. Full-Load Shutdown Waveforms

TYPICAL CHARACTERISTICS (continued)

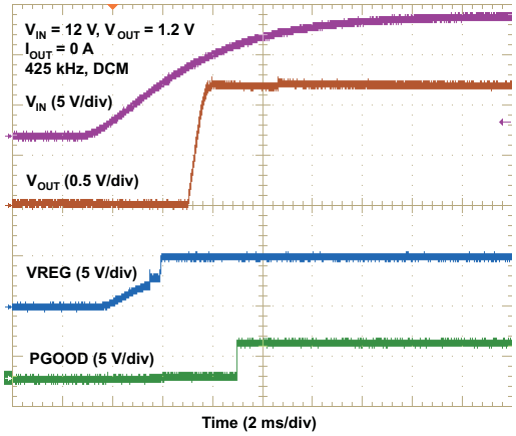


Figure 13. No-Load UVLO Start-Up Waveforms

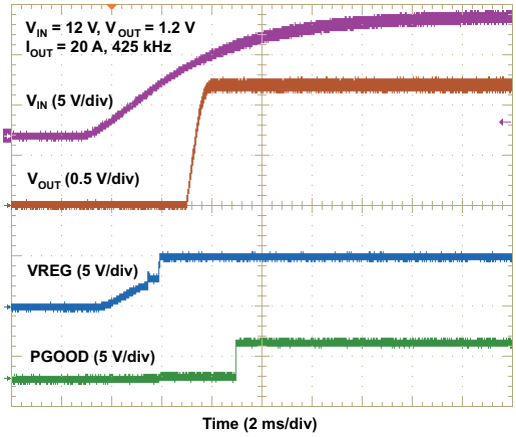


Figure 14. Full-Load UVLO Start-Up Waveforms

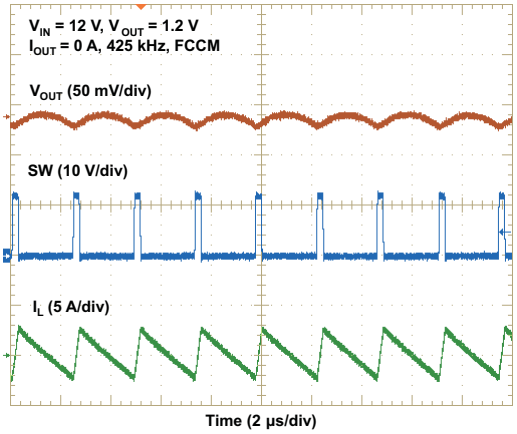


Figure 15. 1.2-V Output Ripple with FCCM

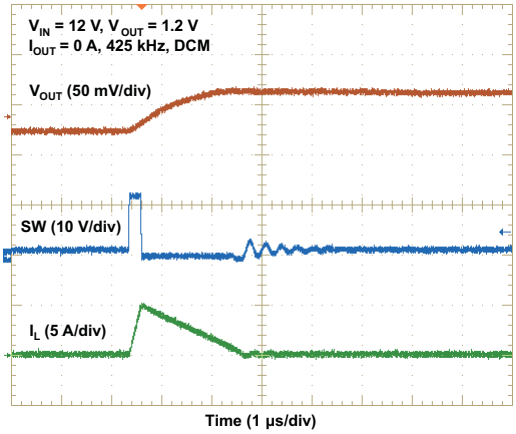


Figure 16. 1.2-V Output Ripple with DCM

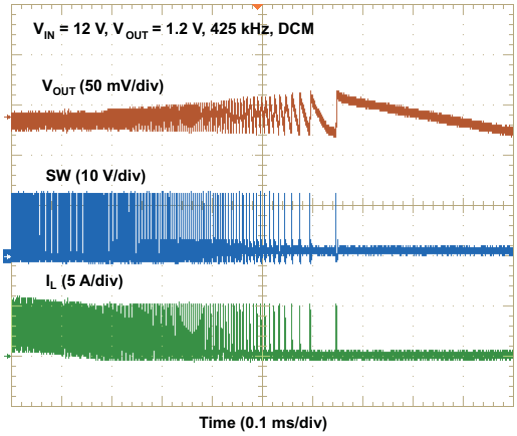


Figure 17. CCM to DCM Transitions

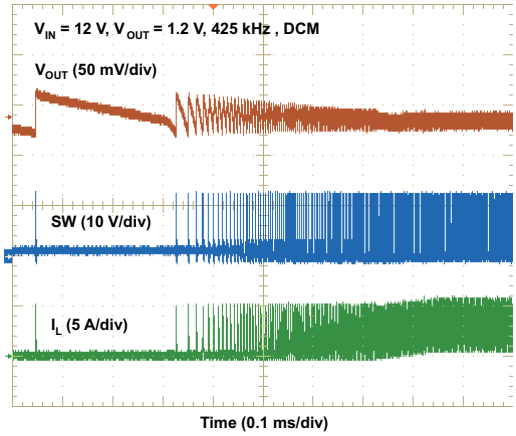


Figure 18. DCM to CCM Transitions

TYPICAL CHARACTERISTICS (continued)

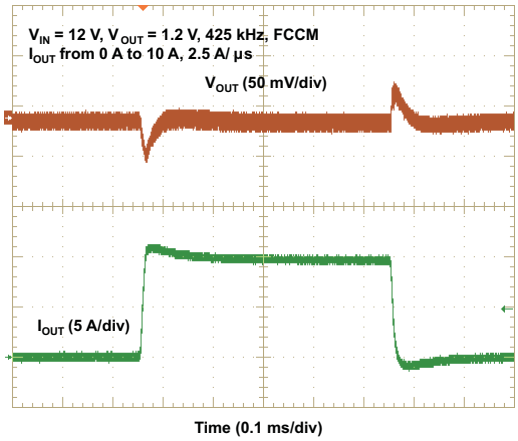


Figure 19. FCCM Load Transients

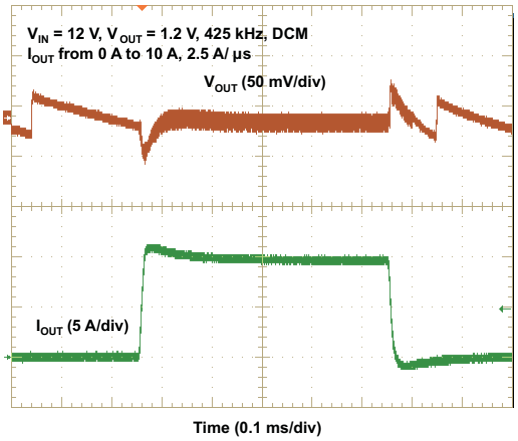


Figure 20. DCM Load Transients

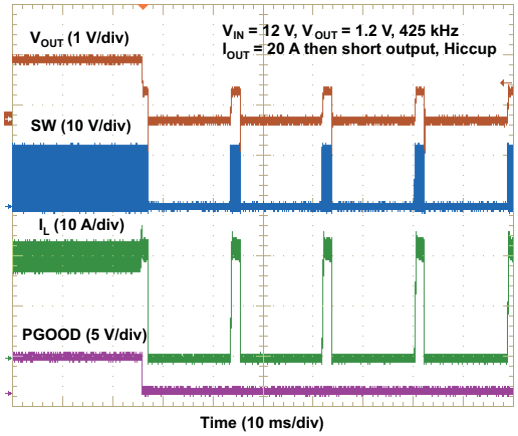


Figure 21. Output Short Circuit Protection with Hiccup

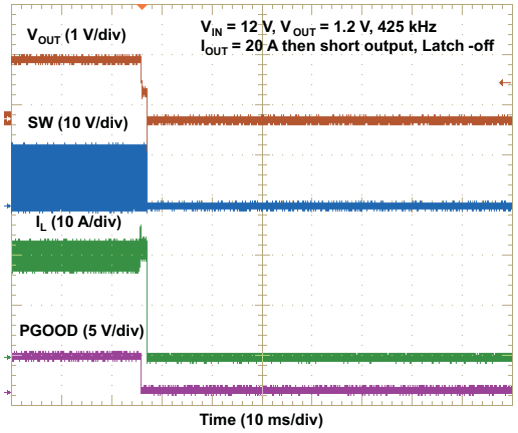


Figure 22. Output Short Circuit Protection with Latch-off

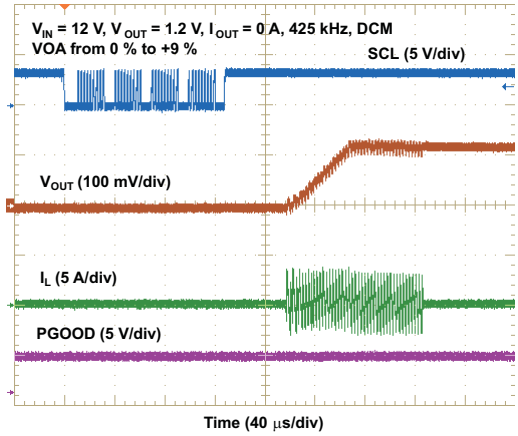


Figure 23. No-Load V_{OUT} Adjustment Waveforms

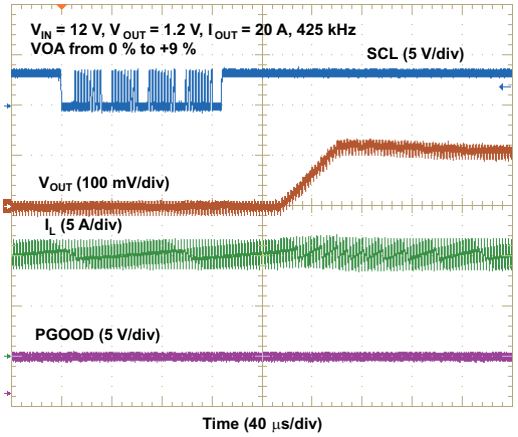


Figure 24. Full-Load V_{OUT} Adjustment Waveforms

TYPICAL CHARACTERISTICS (continued)

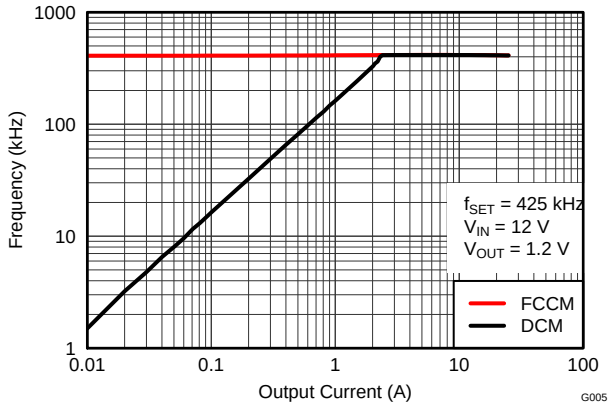


Figure 25. Switching Frequency vs. Output Current

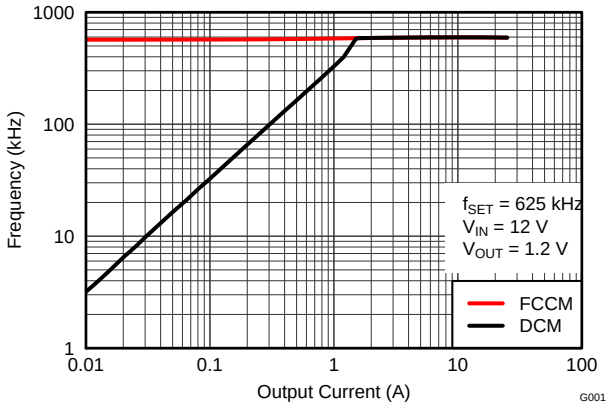


Figure 26. Switching Frequency vs. Output Current

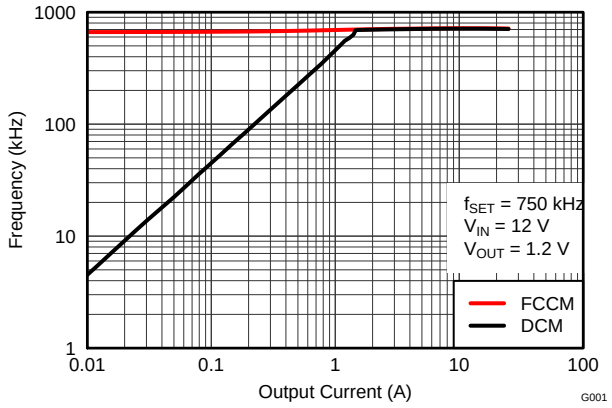


Figure 27. Switching Frequency vs. Output Current

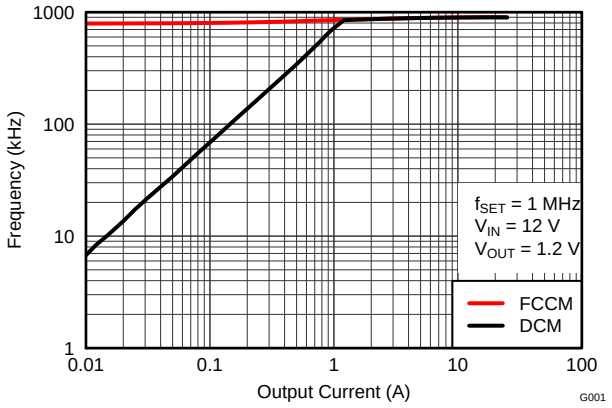


Figure 28. Switching Frequency vs. Output Current

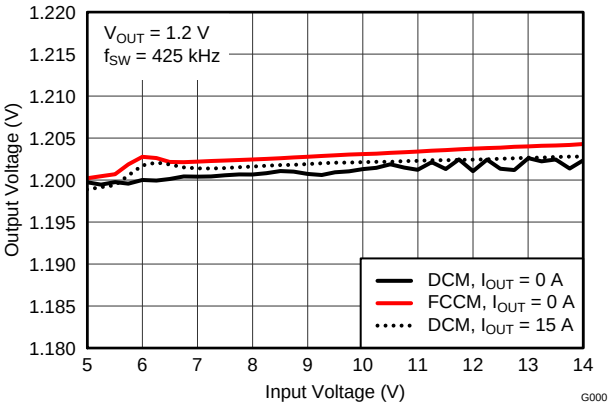


Figure 29. Output Voltage vs. Input Voltage

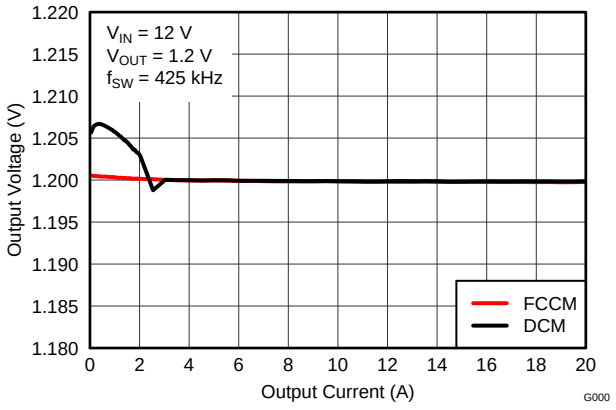


Figure 30. Output Voltage vs. Output Current

TYPICAL CHARACTERISTICS (continued)

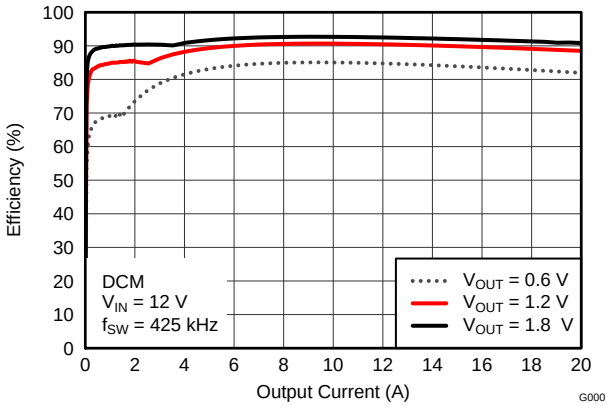


Figure 31. Efficiency vs. Output Current

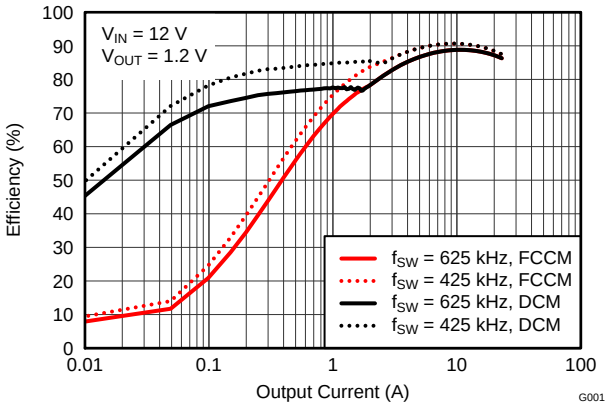


Figure 32. Efficiency vs. Output Current

GENERAL DESCRIPTION

Introduction

The TPS53819A is a high-efficiency, single-channel, synchronous buck regulator controller that uses the PMBus protocol. It is suitable for low output voltage, point-of-load applications in computing and similar digital consumer applications. The device features proprietary D-CAP2 mode control combined with adaptive on-time architecture. This combination is ideal for building modern low duty-ratio and ultra-fast load step response DC-DC converters. The output voltage ranges from 0.6 V to 5.5 V. The conversion input voltage range is from 3 V to 28 V. The D-CAP2 mode uses emulated current information to control the loop modulation. One advantage of this control scheme is that it does not require an external phase compensation network, which makes it easy to use. It also allows for a low external component count. The switching frequency is selectable from eight preset values through the PMBus interface. Adaptive on-time control tracks the preset switching frequency over a wide range of input and output voltages while increasing the switching frequency as needed during load step transient.

Enable and Soft-Start

When the EN pin voltage rises above the enable threshold voltage and/or ON_OFF bit is set via PMBus according to the setting in OPERATION command, the controller enters a start-up sequence. After a programmed power-on-delay duration from 0.35 ms to 32.86 ms, the internal DAC starts ramping up the reference voltage from 0 V to a target voltage (typically 0.6 V) with the programmed soft-start time from 1 ms to 8 ms. The device maintains a smooth and constant output voltage ramp-up during start-up regardless of load current.

Adaptive On-Time Control

The TPS53819A does not have a dedicated oscillator. The device operates with a pseudo-constant frequency by feed-forwarding the input and output voltages into the on-time one-shot timer. The adaptive on-time control adjusts the on-time to be inversely proportional to the input voltage and proportional to the output voltage ($t_{ON} \propto V_{OUT}/V_{IN}$). This makes the switching frequency fairly constant in steady state conditions over a wide input voltage range. The switching frequency is selectable from 275 kHz to 1 MHz via PMBus (FREQUENCY_CONFIG).

Light-Load Condition in Auto-Skip Operation (Eco-mode)

If the discontinuous conduction mode (DCM) is selected via PMBus (MODE_SOFT_START_CONFIG), TPS53819A automatically reduces the switching frequency at light-load conditions to maintain high efficiency. Specifically, as the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to the point that its ripple valley current touches zero level, which is the boundary between continuous conduction mode (CCM) and discontinuous conduction mode (DCM). The synchronous MOSFET is turned OFF when this zero inductor current is detected. As the load current further decreases, the converter runs into DCM.

NOTE

The zero current must be detected for at least 16 switching cycles to switch from CCM to DCM.

The on-time remains almost the same as continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the reference voltage level. The transition point to the light-load operation $I_{OUT(LL)}$ (i.e., the threshold between continuous and discontinuous conduction mode) is calculated in Equation 1.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (1)$$

where

- f_{SW} is the PWM switching frequency

Switching frequency versus output current in the light-load condition is a function of L, V_{IN} and V_{OUT}, but it decreases almost proportionally to the output current when below the $I_{OUT(LL)}$ given in Equation 1. For example, it is 65 kHz at $I_{O(LL)}/5$ if the frequency setting is 325 kHz.

Zero Crossing Detection

The TPS53819A uses a low offset comparator to detect SW node zero crossing event in order to optimize turn-off timing of low-side MOSFET.

Forced Continuous Conduction Mode

When the forced continuous conduction mode (FCCM) is selected via PMBus (MODE_SOFT_START_CONFIG), the controller maintains continuous conduction mode even in light-load condition. In FCCM mode, switching frequency maintains a constant level over the entire load range which is suitable for applications that need tight control of the switching frequency at a cost of lower efficiency. During the soft-start time, the controller maintains discontinuous conduction mode, and then switches to continuous conduction mode if FCCM is selected after the soft-start operation is completed.

Output Discharge Control

When the EN pin voltage falls below the enable threshold voltage and/or ON_OFF bit is reset via PMBus according to the setting in OPERATION command, the TPS53819A discharges output capacitor using internal MOSFET connected between the VOUT pin and the GND pin while the high-side and low-side MOSFETs are maintained in the OFF state. The typical discharge resistance is 40 Ω.

Low-Side Driver

The low-side driver is designed to drive high-current, low-$R_{DS(on)}$, N-channel MOSFET(s). The drive capability is represented by the internal resistance, which is 0.9 Ω for VREG to DRVL and 0.5 Ω for DRVL to GND. A dead-time period to prevent shoot through is internally generated between high-side MOSFET OFF to low-side MOSFET ON, and low-side MOSFET OFF to high-side MOSFET ON. The 5-V, VREG supply voltage delivers the bias voltage. A bypass capacitor connected between the VREG and GND pins supplies the instantaneous drive current. Equation 2 shows the average low-side gate drive current.

$$I_{GL} = C_{GL} \times V_{VDRV} \times f_{SW} \quad (2)$$

High-Side Driver

The high-side driver drives high current, low $R_{DS(on)}$, N-channel MOSFET(s). When configured as a floating driver, the VREG pin supply delivers the bias voltage. Equation 3 shows the average high-side gate current.

$$I_{GH} = C_{GH} \times V_{VDRV} \times f_{SW} \quad (3)$$

The flying capacitor between the VBST and SW pins supplies the instantaneous drive current. The internal resistance, which is 1.6 Ω for VBST to DRVH and 0.6 Ω for DRVH to SW represents the drive capability. Equation 4 calculates the driver power dissipation required for the TPS53819A

$$P_{DRV} = \left(I_{GL} + I_{GH}\right) \times V_{VDRV} \quad (4)$$

Power Good

The TPS53819A indicates the switcher output is within the target range when the power-good output is high. The power-good function activates after the soft-start operation has finished. If the output voltage comes within ±8% of the target value, internal comparators detect power-good state and the power-good signal becomes high after a programmed delay time between 0.25 ms and 131 ms. If the output voltage goes outside of ±16% of the target value, the power-good signal becomes low after a 2-µs internal delay. The power-good output is an open drain output and must be pulled up externally.

Current Sense and Overcurrent Protection

TPS53819A has cycle-by-cycle overcurrent limiting control. The inductor current is monitored during the OFF state and the controller maintains the OFF state during the period when inductor current is larger than the overcurrent trip level. In order to provide both good accuracy and cost effective solution, TPS53819A supports temperature compensated MOSFET on-resistance ($R_{DS(on)}$) sensing. The TRIP pin should be connected to GND through the trip voltage setting resistor, R_{TRIP}. The TRIP terminal sources I_{TRIP} current, which is 10 µA typically at room temperature, and the trip level is set to the OCL trip voltage V_{TRIP} as shown in Equation 5. Note that the V_{TRIP} is limited up to approximately 3 V internally.

$$V_{TRIP}\left(mV\right) = R_{TRIP}\left(k\Omega\right) \times I_{TRIP}\left(\mu A\right) \tag{5}$$

The inductor current is monitored by the voltage between GND pin and SW pin so that SW pin should be properly connected to the drain terminal of the low-side MOSFET. The TRIP current has a 4700-ppm/°C temperature slope to compensate the temperature dependency of the on-resistance. The device uses the GND pin as the positive current sensing node. As the comparison occurs during the OFF state, V_{TRIP} sets the valley level of the inductor current. Thus, the average load current at the overcurrent threshold, I_{OCP}, is calculated as shown in Equation 6.

$$I_{OCP} = \frac{V_{TRIP}}{\left(8 \times R_{DS(on)}\right)} + \frac{I_{IND(ripple)}}{2} = \frac{V_{TRIP}}{\left(8 \times R_{DS(on)}\right)} + \frac{1}{2 \times L \times f_{SW}} \times \frac{\left(V_{IN} - V_{OUT}\right) \times V_{OUT}}{V_{IN}} \tag{6}$$

In an overcurrent condition, the load current exceeds the inductor current delivered to the output capacitor, thus the output voltage tends to fall. Eventually, it crosses the undervoltage protection threshold and the device shuts down. If hiccup mode is selected, then after a hiccup delay time (8.96 ms + 7× programmed soft-start time), the controller restarts. If the overcurrent condition remains, the procedure is repeated and the device enters hiccup mode. During the CCM, the negative current limit (NCL) protects the external FET from carrying too much current. The OCLN detect threshold is set at the same absolute value as positive current limit (OCLP) but with negative polarity. Note that the threshold still represents the valley value of the inductor current. When an OCLP or OCLN event occurs, the corresponding fault signals (IOUT_OC and IOUT) of the STATUS_WORD register is latched to indicate the faults and can be read via PMBus.

Overvoltage and Undervoltage Protection

TPS53819A monitors a resistor divided feedback voltage to detect overvoltage and undervoltage conditions. When the feedback voltage becomes lower than 68% of the target voltage, the undervoltage protection (UVP) comparator output goes high and an internal UVP delay time counter begins counting. After 1 ms, the device turns OFF both high-side and low-side MOSFETs drivers. If the hiccup mode is selected, then the controller restarts after a hiccup delay time (8.96 ms + 7 × programmed soft-start time). This function is enabled after the soft-start operation is completed. When the feedback voltage becomes higher than 120% of the target voltage, the overvoltage protection (OVP) comparator output goes high and the circuit latches OFF the high-side MOSFET driver and latches ON the low-side MOSFET driver. If the sensed inductor current reaches the negative current limit, then the low-side MOSFET driver is turned OFF, and high-side MOSFET driver is turned ON with an appropriate on-time to limit the inductor current while the output voltage discharges.

Out-of-Bound Protection

TPS53819A has an out-of-bound (OOB) overvoltage protection that tries to protect the output load at a much lower overvoltage threshold of 8% above the target voltage. OOB protection does not trigger an overvoltage fault, so the device is not latched off after an OOB event. OOB protection is intended as an early no-fault overvoltage protection mechanism, in addition to the official overvoltage protection as described in the Overvoltage and Undervoltage Protection section.

UVLO Protection

The TPS53819A has VDD undervoltage lockout protection (UVLO). When the VDD voltage is lower than the programmed UVLO threshold voltage, the switch mode power supply shuts OFF. This is a non-latch protection, but if VDD UVLO occurs when the switcher is enabled by either EN pin or ON_OFF bit via PMBus, the corresponding fault signals (VIN_UV and INPUT) of the STATUS_WORD register latch off to indicate the fault condition, and can be read via PMBus.

Thermal Shutdown

The TPS53819A has an over-temperature protection feature. If the temperature exceeds the threshold value (typically 140°C), the device is shut OFF. This is a non-latch protection, but when the temperature exceeds the threshold value, the corresponding fault signal (TEMP) of the STATUS_WORD register latches off to indicate the fault condition, and can be read via PMBus.

D-CAP2™ Mode

From small-signal loop analysis, a buck converter using D-CAP2™ mode control architecture can be simplified as shown in Figure 33 .

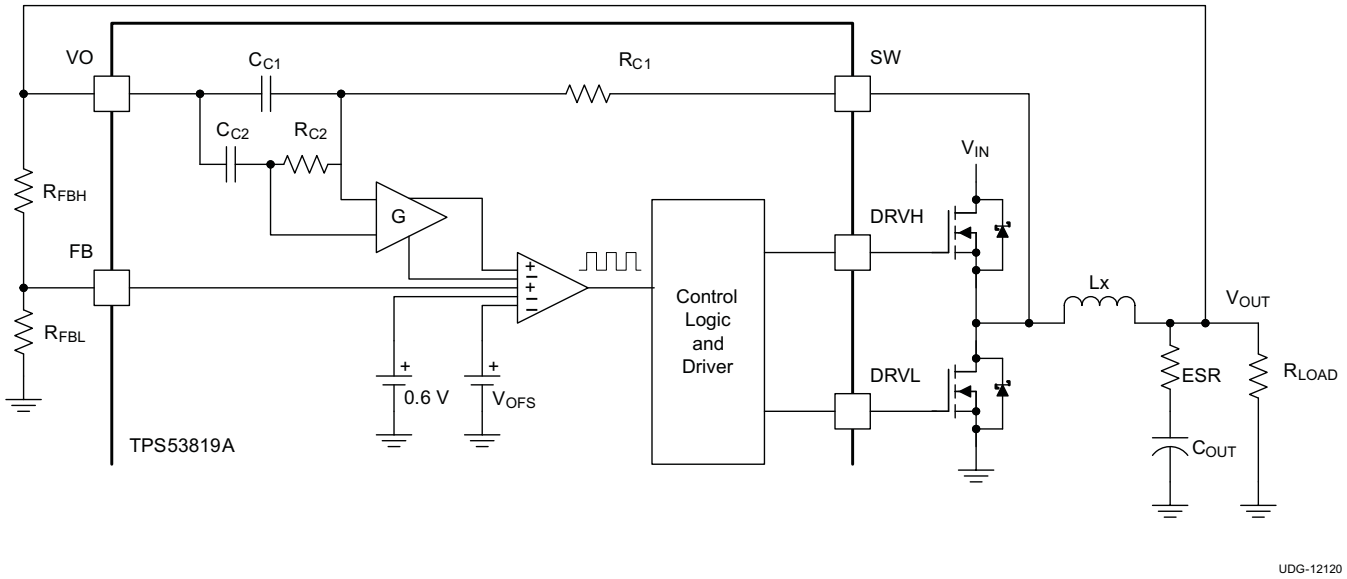


Figure 33. Simplified Modulator Using D-CAP2™ Control Architecture

The D-CAP2 control architecture in TPS53819A includes an internal ripple generation network enabling the use of very low-ESR output capacitor(s) such as multi-layer ceramic capacitors (MLCC). No external current sensing networks or compensators are required with D-CAP2 control architecture in order to simplify the power supply design. The role of the internal ripple generation network is to emulate the ripple component of the inductor current information and then combine it with the voltage feedback signal. V_{OFS} is the internal offset to compensate the offset caused by the internal ripple, and the typical V_{OFS} value is 4 mV. The 0-dB frequency of the D-CAP2 architecture can be approximated as shown in Equation 7.

$$f_0 = \frac{R_{C1} \times C_{C1} \times 0.6 \times (0.67 + D)}{2\pi \times G \times L_X \times C_{OUT} \times V_{OUT}} \quad (7)$$

where

- G is gain of the amplifier which amplifies the ripple current information generated by the network
- D is the duty ratio

The typical G value is 0.25. The $R_{C1}C_{C1}$ time constant value varies according to the selected switching frequency as shown in Table 1.

Table 1. Switching Frequency Selection

SWITCHING FREQUENCY (kHz)	$R_{C1}C_{C1}$ TIME CONSTANT (µs)
275	75
325	
425	62
525	
625	48
750	
850	36
1000	

In order to secure enough phase margin, consider that f_0 should be lower than 1/3 of the switching frequency, but is also higher than 5 times the f_{C2} as shown in Equation 8.

$$5 \times f_{C2} \le f_0 \le \frac{f_{SW}}{3}$$

where

- f_{C2} is determined by the internal network of R_{C2} and C_{C2} (1.4 kHz typ) (8)

This example describes a DC-DC converter with an input voltage range of 12-V and an output voltage of 1.2-V. If the switching frequency is 525 kHz and the inductor is given as 0.44uH, then C_{OUT} should be larger than 197 µF, and also be smaller than 4.9 mF based on the design requirements. The characteristics of the capacitors should be also taken into considerations. For MLCC, use X5R or better dielectric and take into account derating of the capacitance by both DC bias and AC bias. When derating by DC bias and AC bias are 80% and 50%, respectively, the effective derating is 40% because 0.8 x 0.5 = 0.4. The capacitance of specialty polymer capacitors may change depending on the operating frequency. Consult capacitor manufacturers for specific characteristics.

PMBus GENERAL SPECIFICATIONS

The PMBus General Descriptions

The TPS53819A has seven internal custom user-accessible 8-bit registers. The PMBus interface has been designed for program flexibility, supporting a direct format for write operation. Read operations are supported for both combined format and stop separated format. While there is no auto increment/decrement capability in the The TPS53819A PMBus logic, a tight software loop can be designed to randomly access the next register, regardless of which register was accessed first. The START and STOP commands frame the data packet and the REPEAT START condition is allowed when necessary.

The device can operate in either standard mode (100 kb/s) or fast mode (400 kb/s).

PMBus Slave Address Selection

The seven-bit slave address is $001A_3A_2A_1A_0x$, where $A_3A_2A_1A_0$ is set by the ADDR pin on the device. Bit 0 is the data direction bit, i.e., $001A_3A_2A_1A_00$ is used for write operation and $001A_3A_2A_1A_01$ is used for read operation.

PMBus Address Selection

The TPS53819A allows up to 16 different chip addresses for PMBus communication, with the first three bits fixed as 001. The address selection process is defined by the resistor divider ratio from VREG pin to ADDR pin, and the address detection circuit starts to work only after VDD input supply has risen above its UVLO threshold. The table below lists the divider ratio and some example resistor values. The 1% tolerance resistors with typical temperature coefficient of ±100ppm/°C are recommended. Higher performance resistors can be used if tighter noise margin is required for more reliable address detection, as shown in Table 2.

Table 2. PMBus Address Selection Settings

PMBus ADDRESS	RESISTOR DIVIDER RATIO	HIGH-SIDE RESISTOR (kΩ)	LOW-SIDE RESISTOR (kΩ)
0011111	> 0.557	1	300
0011110	0.509	160	165
0011101	0.461	180	154
0011100	0.416	200	143
0011011	0.375	200	120
0011010	0.334	220	110
0011001	0.297	249	105
0011000	0.263	249	88.7
0010111	0.229	240	71.5
0010110	0.195	249	60.4
0010101	0.160	249	47.5
0010100	0.126	249	36.0
0010011	0.096	255	27.0
0010010	0.068	255	18.7
0010001	0.041	270	11.5
0010000	< 0.013	300	1

Supported Formats

The supported formats are described in this section.

Direct Format: Write

The simplest format for a PMBus write is direct format. After the start condition [S], the slave chip address is sent, followed by an eighth bit indicating a write. The TPS53819A then acknowledges that it is being addressed, and the master responds with an 8-bit register address byte. The slave acknowledges and the master sends the appropriate 8-bit data byte. Again the slave acknowledges and the master terminates the transfer with the stop condition [P].

Combined Format: Read

After the start condition [S], the slave chip address is sent, followed by an eighth bit indicating a write. The TPS53819A then acknowledges that it is being addressed, and the master responds with an 8-bit register address byte. The slave acknowledges and the master sends the repeated start condition [Sr]. Again the slave chip address is sent, followed by an eighth bit indicating a read. The slave responds with an acknowledge followed by previously addressed 8 bit data byte. The master then sends a non-acknowledge (NACK) and finally terminates the transfer with the stop condition [P].

Stop-Separated Reads

Stop-separated read features are also available. This format allows a master to initialize the register address pointer for a read and return to that slave at a later time to read the data. In this format the slave chip address followed by a write bit are sent after a start [S] condition. The TPS53819A then acknowledges it is being addressed, and the master responds with the 8-bit register address byte. The master then sends a stop or restart condition and may then address another slave. After performing other tasks, the master can send a start or restart condition to the device with a read command. The device acknowledges this request and returns the data from the register location that had been set up previously.

Supported PMBus Commands

The TPS53819A supports the PMBus commands shown in Table 1 only. Not all features of each PMBus command are supported. The CLEAR_FAULTS, STORE_DEFAULT_ALL and RESTORE_DEFAULT_ALL commands have no data bytes. The non-volatile memory (NVM) cells inside the TPS53819A can permanently store some registers.

Table 3. Supported PMBus Commands

COMMAND	NOTES
OPERATION	Turn on or turn off switching converter only
ON_OFF_CONFIG	ON/OFF configuration
CLEAR_FAULTS	Clear all latched status flags
WRITE_PROTECT	Control writing to the PMBus device
STORE_DEFAULT_ALL	Store contents of user-accessible registers to non-volatile memory cells
RESTORE_DEFAULT_ALL	Copy contents of non-volatile memory cells to user-accessible registers
STATUS_WORD	PMBus read-only status and flag bits
CUSTOM_REG	MFR_SPECIFIC_00 (Custom Register 0): Custom register
DELAY_CONTROL	MFR_SPECIFIC_01 (Custom Register 1): Power on and power good delay times
MODE_SOFT_START_CONFIG	MFR_SPECIFIC_02 (Custom Register 2): Mode and soft-start time
FREQUENCY_CONFIG	MFR_SPECIFIC_03 (Custom Register 3): Switching frequency control
VOUT_ADJUSTMENT	MFR_SPECIFIC_04 (Custom Register 4): Output voltage adjustment control
VOUT_MARGIN	MFR_SPECIFIC_05 (Custom Register 5): Output voltage margin levels
UVLO_THRESHOLD	MFR_SPECIFIC_06 (Custom Register 6): Turn-on input voltage UVLO threshold

Unsupported PMBus Commands

Do not send any unsupported commands to the TPS53819A. Even though the device receives an unsupported commands, it can acknowledge the unsupported commands and any related data bytes by properly sending the ACK bits. However, the device ignores the unsupported commands and any related data bytes, which means they do not affect the device operation in any way. Although the TPS53819A may acknowledge but ignore unsupported commands and data bytes, it can however, set the CML bit in the STATUS_BYTE register and then pull down the $\overline{\text{ALERT}}$ pin to notify the host. For this reason, unsupported commands and data bytes should not be sent to TPS53819A.

OPERATION [01h] (R/W Byte)

The TPS53819A supports only the functions of the OPERATION command shown in Table 4.

Table 4. OPERATION Command Supported Functions

COMMAND	DEFINITION	DESCRIPTION	NVM
OPERATION<7>	ON_OFF	0: turn off switching converter 1: turn on switching converter	—
OPERATION<6>	—	not supported and don't care	—
OPERATION<5:2>	OPMARGIN<3:0>	00xx: turn off output voltage margin function 0101: turn on output voltage margin low and ignore fault 0110: turn on output voltage margin low and act on fault 1001: turn on output voltage margin high and ignore fault 1010: turn on output voltage margin high and act on fault	—
OPERATION<1>	—	not supported and don't care	—
OPERATION<0>	—	not supported and don't care	—

ON_OFF_CONFIG [02h] (R/W Byte)

The TPS53819A supports only the functions of the ON_OFF_CONFIG command shown in Table 5.

Table 5. ON_OFF_CONFIG Command Supported Functions

COMMAND	DEFINITION	DESCRIPTION	NVM
ON_OFF_CONFIG<7>	—	not supported and don't care	—
ON_OFF_CONFIG<6>	—	not supported and don't care	—
ON_OFF_CONFIG<5>	—	not supported and don't care	—
ON_OFF_CONFIG<4>	PU	not supported and always set to 1	—
ON_OFF_CONFIG<3>	CMD	0: ignore ON_OFF bit (OPERATION<7>)(1) 1: act on ON_OFF bit (OPERATION<7>)	Yes
ON_OFF_CONFIG<2>	CP	0: ignore EN pin 1: act on EN pin(1)	Yes
ON_OFF_CONFIG<1>	PL	not supported and always set to 1	—
ON_OFF_CONFIG<0>	SP	not supported and always set to 1	—

(1) TI default.

Conditions required to enable the switcher:

- If CMD is cleared and CP is set, then the switcher can be enabled only by the EN pin.
- If CMD is set and CP is cleared, then the switcher can be enabled only by the ON_OFF bit (OPERATION<7>) via PMBus.
- If both CMD and CP are set, then the switcher can be enabled only when both the ON_OFF bit (OPERATION<7>) and the EN pin are commanding to enable the device.
- If both CMD and CP are cleared, then the switcher is automatically enabled after the ADDR detection sequence completes, regardless of EN pin and ON_OFF bit polarities.

WRITE_PROTECT [10h] (R/W Byte)

The WRITE PROTECT command is used to control writing to the PMBus device. The intent of this command is to provide protection against accidental changes. This command has one data byte as described in Table 6.

Table 6. WRITE_PROTECT Command Supported Functions

COMMAND	DEFINITION	DESCRIPTION		NVM
WRITE_PROTECT<7:0>	WP<7:0>	10000000:	Disable all writes, except the WRITE_PROTECT command.	—
		01000000:	Disable all writes, except the WRITE_PROTECT and OPERATION commands.	—
		00100000:	Disable all writes, except the WRITE_PROTECT, OPERATION, and ON_OFF_CONFIG commands.	—
		00000000:	Enable writes to all commands.	—
		Others:	Fault data	—

CLEAR_FAULTS [03h] (Send Byte)

The CLEAR_FAULTS command is used to clear any fault bits in the STATUS_WORD and STATUS_BYTE registers that have been set. This command clears all bits in all status registers. Simultaneously, the TPS53819A releases its ALERT signal output if the device is asserting the ALERT signal. If the fault condition is still present when the bit is cleared, the fault bits shall immediately be set again, and the ALERT signal should also be re-asserted.

The CLEAR_FAULTS does not cause a unit that has latched off for a fault condition to restart. Units that have been shut down for a fault condition can be restarted with one of the following conditions.

- The output is commanded through the EN pin and/or ON_OFF bit based on the ON_OFF_CONFIG setting to turn off and then to turn back on.
- VDD power is cycled for TPS53819A

The CLEAR_FAULT command is used to clear the fault bits in the STATUS_WORD and STATUS_BYTE commands, and to release the ALERT pin. It is recommended not to send CLEAR_FAULT command when there is no fault to cause the ALERT pin to pull down.

STORE_DEFAULT_ALL [11h] (Send Byte)

The STORE_DEFAULT_ALL command instructs TPS53819A to copy the entire contents of the operating memory to the corresponding locations in the NVM. The updated contents in the non-volitile memory (NVM)s become the new default values. The STORE_DEFAULT_ALL command can be used while the device is operating. However, the device may be unresponsive during the copy operation with unpredictable results. (see *PMBus Power System Management Protocol Specificaiton*, Part II - Command Language, Revision, 1.2, 6 Sept. 2010. www.powerSIG.org). It is recommended not to exceed 1000 write/erase cycles for non-volatile memory (NVM).

RESTORE_DEFAULT_ALL [12h] (Send Byte)

The RESTORE_DEFAULT_ALL command instructs TPS53819A to copy the entire contents of the NVMs to the corresponding locations in the operating memory. The values in the operating memory are overwritten by the value retrieved from the NVM. It is permitted to use the RESTORE_DEFAULT_ALL command while the device is operating. However, the device may be unresponsive during the copy operation with unpredictable results.

STATUS_WORD [79h] (Read Word)

The TPS53819A does not support all functions of the STATUS_WORD command. A list of supported functions appears in Table 7. A status bit reflects the current state of the converter. Status bit becomes high when the specified condition has occurred and goes low when the specified condition has disappeared. A flag bit is a latched bit that becomes high when the specified condition has occurred and does not go back low when the specified condition has disappeared. STATUS_BYTE command is a subset of the STATUS_WORD command, or more specifically the lower byte of the STATUS_WORD.

Table 7. STATUS_WORD Command Supported Functions

COMMAND	DEFINITION	DESCRIPTION
Low Byte: STATUS_BYTE [78h]		
Low STATUS_WORD<7>	BUSY	not supported and always set to 0
Low STATUS_WORD<6>	OFF	0: raw status indicating device is providing power to output voltage 1: raw status indicating device is not providing power to output voltage
Low STATUS_WORD<5>	VOUT_OV	0: latched flag indicating no output voltage overvoltage fault has occurred 1: latched flag indicating an output voltage overvoltage fault has occurred
Low STATUS_WORD<4>	IOUT_OC	0: latched flag indicating no output current overcurrent fault has occurred 1: latched flag indicating an output current overcurrent fault has occurred
Low STATUS_WORD<3>	VIN_UV	0: latched flag indicating input voltage is above the UVLO turn-on threshold 1: latched flag indicating input voltage is below the UVLO turn-on threshold
Low STATUS_WORD<2>	TEMP	0: latched flag indicating no OT fault has occurred 1: latched flag indicating an OT fault has occurred
Low STATUS_WORD<1>	CML	0: latched flag indicating no communication, memory or logic fault has occurred 1: latched flag indicating a communication, memory or logic fault has occurred
Low STATUS_WORD<0>	OTHER	not supported and always set to 0
High Byte		
High STATUS_WORD<7>	VOUT	0: latched flag indicating no output voltage fault or warning has occurred 1: latched flag indicating a output voltage fault or warning has occurred
High STATUS_WORD<6>	IOUT	0: latched flag indicating no output current fault or warning has occurred 1: latched flag indicating an output current fault or warning has occurred
High STATUS_WORD<5>	INPUT	0: latched flag indicating no input voltage fault or warning has occurred 1: latched flag indicating a input voltage fault or warning has occurred
High STATUS_WORD<4>	MFR	not supported and always set to 0
High STATUS_WORD<3>	$\overline{\text{PGOOD}}$	0: raw status indicating PGOOD pin is at logic high 1: raw status indicating PGOOD pin is at logic low
High STATUS_WORD<2>	FANS	not supported and always set to 0
High STATUS_WORD<1>	OTHER	not supported and always set to 0
High STATUS_WORD<0>	UNKNOWN	not supported and always set to 0

The latched flags of faults can be removed or corrected only until **one** of the following conditions occurs:

- The device receives a CLEAR_FAULTS command.
- The output is commanded through the EN pin and/or ON_OFF bit based on the ON_OFF_CONFIG setting to turn off and then to turn back on
- VDD power is cycled for TPS53819A

If the fault condition remains present when the bit is cleared, the fault bits are immediately set again, and the $\overline{\text{ALERT}}$ signal is re-asserted.

TPS53819A supports the $\overline{\text{ALERT}}$ pin to notify the host of fault conditions. Therefore, the best practice for monitoring the fault conditions from the host is to treat the $\overline{\text{ALERT}}$ pin as an interrupt source for triggering the corresponding interrupt service routine. It is recommended not to keep polling the STATUS_WORD or STATUS_BYTE registers from the host to reduce the firmware overhead of the host.

CUSTOM_REG (MFR_SPECIFIC_00) [D0h] (R/W Byte)

Custom register 0 provides the flexibility for users to store any desired non-volatile information. For example, users can program this register to track versions of implementation or other soft identification information. The details of each setting are listed in Table 8.

Table 8. CUSTOM_REG (MFR_SPECIFIC_00) Settings

COMMAND	DEFINITION	DESCRIPTION	NVM
CUSTOM_REG<7>	—	not supported and don't care	—
CUSTOM_REG<6>	—	not supported and don't care	—
CUSTOM_REG<5:0>	CUSTOMWORD <5:0>	00000:(1) can be used to store any desired non-volatile information.	Yes

(1) TI Default

DELAY_CONTROL (MFR_SPECIFIC_01) [D1h] (R/W Byte)

Custom register 1 provides software control over key timing parameters of the controller: Power-on delay (POD) time and power-good delay (PGD) time. The details of each setting are listed in Table 9.

Table 9. DELAY_CONTROL (MFR_SPECIFIC_01) Settings

COMMAND	DEFINITION	DESCRIPTION	NVM
DELAY_CONTROL<7>	—	not supported and don't care	—
DELAY_CONTROL<6>	—	not supported and don't care	—
DELAY_CONTROL<5:3>	PGD<2:0>	000: 256 µs 001: 512 µs 010: 1.024 ms(1) 011: 2.048 ms 100: 4.096 ms 101: 8.192 ms 110: 16.384 ms 111: 131.072 ms	Yes
DELAY_CONTROL<2:0>	POD<2:0>	000: 356 µs 001: 612 µs 010: 1.124 ms(1) 011: 2.148 ms 100: 4.196 ms 101: 8.292 ms 110: 16.484 ms 111: 32.868 ms	Yes

(1) TI Default

MODE_SOFT_START_CONFIG (MFR_SPECIFIC_02) [D2h] (R/W Byte)

Custom register 2 provides software control over mode selection and soft-start time (t_{SS}). The details of each setting are listed in Table 10.

Table 10. MODE_SOFT_START_CONFIG (MFR_SPECIFIC_02) Settings

COMMAND	DEFINITION	DESCRIPTION	NVM
MODE_SOFT_START_CONFIG<7>	—	not supported and don't care	—
MODE_SOFT_START_CONFIG<6>	—	not supported and don't care	—
MODE_SOFT_START_CONFIG<5>	—	not supported and don't care	—
MODE_SOFT_START_CONFIG<4>	—	not supported and don't care	—
MODE_SOFT_START_CONFIG<3:2>	SST<1:0>	00: 1 ms(1) 01: 2 ms 10: 4 ms 11: 8 ms	Yes
MODE_SOFT_START_CONFIG<1>	HICLOFF	0: hiccup after UV(1) Hiccup interval is (8.96 ms + soft-start time × 7) 1: latch-off after UV	Yes
MODE_SOFT_START_CONFIG<0>	CM	0: DCM(1) 1: FCCM	Yes

(1) TI Default

Figure 34 shows the soft-start timing diagram of TPS53819A with the programmable power-on delay time (t_{POD}), soft-start time (t_{SST}), and PGOOD delay time (t_{PGD}). During the soft-start time, the controller remains in discontinuous conduction mode (DCM), and then switches to forced continuous conduction mode (FCCM) at the end of soft-start if CM bit (MODE_SOFT_START_CONFIG<0>) is set.

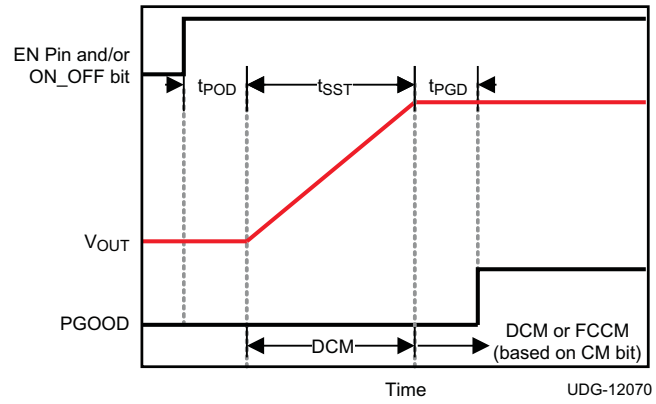


Figure 34. Programmable Soft-Start Timing

FREQUENCY_CONFIG (MFR_SPECIFIC_03) [D3h] (R/W Byte)

Custom register 3 provides software control over frequency setting (FS). The details of FS setting are listed in Table 11.

Table 11. FREQUENCY_CONFIG (MFR_SPECIFIC_03) Settings

COMMAND	DEFINITION	DESCRIPTION	NVM
FREQUENCY_CONFIG<7>	—	not supported and don't care	—
FREQUENCY_CONFIG<6>	—	not supported and don't care	—
FREQUENCY_CONFIG<5>	—	not supported and don't care	—
FREQUENCY_CONFIG<4>	—	not supported and don't care	—
FREQUENCY_CONFIG<3>	—	not supported and don't care	—
FREQUENCY_CONFIG<2:0>	FS<2:0>	000: 275 kHz 001: 325 kHz 010: 425 kHz (1) 011: 525 kHz 100: 625 kHz 101: 750 kHz 110: 850 kHz 111: 1 MHz	Yes

(1) TI default.

VOUT_ADJUSTMENT (MFR_SPECIFIC_04) [D4h] (R/W Byte)

Custom register 4 provides ouput voltage adjustment (VOA) in ±0.75% steps, with a total range of ±9%. When fine adjustment is used together with the margin setting, the change in the output voltage is determined by the multiplication of the two settings.

Table 12. VOUT_ADJUSTMENT (MFR_SPECIFIC_04) Settings

COMMAND	DEFINITION	DESCRIPTION	NVM
VOUT_ADJUSTMENT<7>	—	not supported and don't care	—
VOUT_ADJUSTMENT<6>	—	not supported and don't care	—
VOUT_ADJUSTMENT<5>	—	not supported and don't care	—
VOUT_ADJUSTMENT<4:0>	VOA<4:0>	111xx: +9.00% 11011: +8.25% 11010: +7.50% 11001: +6.75% 11000: +6.00% 10111: +5.25% 10110: +4.50% 10101: +3.75% 10100: +3.00% 10011: +2.25% 10010: +1.50% 10001: +0.75% 10000: +0%(1) 01111: –0% 01110: –0.75% 01101: –1.50% 01100: –2.25% 01011: –3.00% 01010: –3.75% 01001: –4.50% 01000: –5.25% 00111: –6.00% 00110: –6.75% 00101: –7.50% 00100: –8.25% 000xx: –9.00%	Yes

(1) TI default.

Output Voltage Fine Adjustment Soft Slew Rate

To prevent sudden buildup of voltage across inductor, output voltage fine adjustment setting cannot change output voltage instantaneously. The internal reference voltage must slew slowly to its final target, and SST<1:0> is used to provide further programmability. The details of output voltage fine adjustment slew rate are shown in Table 13.

Table 13. Output Voltage Fine Adjustment Soft Slew Rate Settings

COMMAND	DEFINITION	DESCRIPTION	NVM
MODE_SOFT_START_CONFIG<3:2>	SST<1:0>	00: 1 step per 4 µs(1) 01: 1 step per 8 µs 10: 1 step per 16 µs 11: 1 step per 32 µs	Yes

(1) TI default.

VOUT_MARGIN (MFR_SPECIFIC_05) [D5h] (R/W Byte)

Custom register 5 provides output voltage margin high (VOMH) and output voltage margin low (VOML) settings. This register works in conjunction with PMBus OPERATION command to raise or lower the output voltage by a specified amount. This register settings described in Table 14 are also used together with the fine adjustment setting described in Table 12. For example, setting fine adjustment to +9% and margin to +12% changes the output by +22.08%, whereas setting fine adjustment to –9% and margin to –9% change the output by –17.19%

Table 14. VOUT_MARGIN (MFR_SPECIFIC_05) Settings

COMMAND	DEFINITION	DESCRIPTION	NVM
VOUT_MARGIN<7:4>	VOMH<3:0>	11xx: +12.0% 1011: +10.9% 1010: +9.9% 1001: +8.8% 1000: +7.7% 0111: +6.7% 0110: +5.7% 0101: +4.7%(1) 0100: +3.7% 0011: +2.8% 0010: +1.8% 0001: +0.9% 0000: +0%	Yes
VOUT_MARGIN<3:0>	VOML<3:0>	0000: –0% 0001: –1.1% 0010: –2.1% 0011: –3.2% 0100: –4.2% 0101: –5.2% (1) 0110: –6.2% 0111: –7.1% 1000: –8.1% 1001: –9.0% 1010: –9.9% 1011: –10.7% 11xx: –11.6%	Yes

(1) TI default.

Output Voltage Margin Adjustment Soft-Slew Rate

Similar to the output voltage fine adjustment, margin adjustment also cannot change output voltage instantaneously. The soft-slew rate of margin adjustment is also programmed by SST<1:0>. The details are listed in Table 15.

Table 15. Output Voltage Margin Adjustment Soft-Slew Rate Settings

COMMAND	DEFINITION	DESCRIPTION	NVM
MODE_SOFT_START_CONFIG<3:2>	SST<1:0>	00: 1 step per 4 µs(1) 01: 1 step per 8 µs 10: 1 step per 16 µs 11: 1 step per 32 µs	Yes

(1) TI default.

Figure 35 shows the timing diagram of the output voltage adjustment via PMBus. After receiving the write command of VOUT_ADJUSTMENT (MFR_SPECIFIC_04), the output voltage starts to be adjusted after t_P delay time (about 50 µs). The time duration t_{DAC} for each DAC step change can be controlled by SST bits (MODE_SOFT_START_CONFIG<3:2:> from 4 µs to 32 µs.

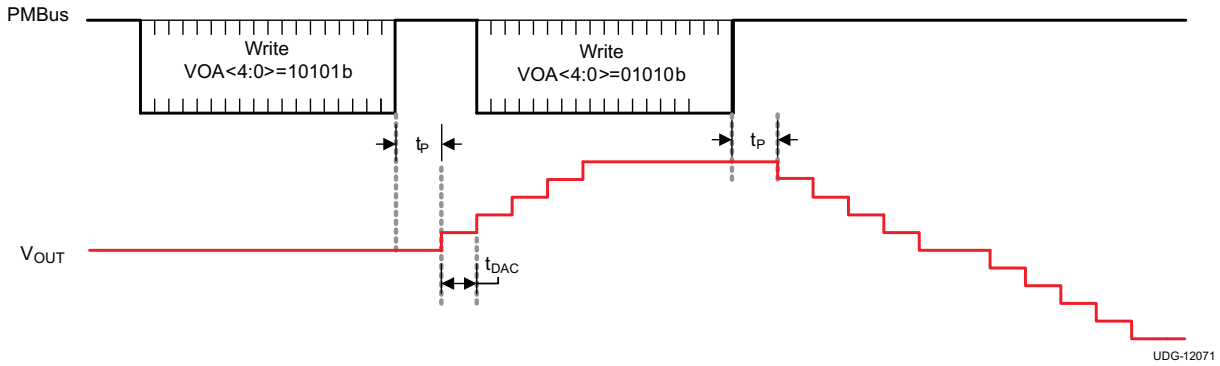


Figure 35. Output Voltage Adjustment via PMBus

The margining function is enabled by setting the OPERATION command, and the margining level is determined by the VOUT_MARGIN (MFR_SPECIFIC_05) command. Figure 36 and Figure 37 illustrate the timing diagrams of the output voltage margining via PMBus. Figure 36 shows setting the margining level first, and then enabling margining by writing OPERATION command. After the OPERATION margin high command enables the margin high setting (VOMH<3:0>), the output voltage starts to be adjusted after t_P delay time (about 50 µs). The time duration t_{DAC} for each DAC step change can be controlled by SST bits (MODE_SOFT_START_CONFIG<3:2>) from 4 µs to 32 µs.

As shown in Figure 37, the margining function is enabled first by a write command of OPERATION. The output voltage starts to be adjusted toward the default margin high level after t_P delay. Since the margining function has been enabled, the output voltage can be adjusted again by sending a different margin high level with a write command of VOUT_MARGIN. The time duration t_{DAC} for each DAC step change can be also controlled by SST bits (MODE_SOFT_START_CONFIG<3:2>) from 4 µs to 32 µs.

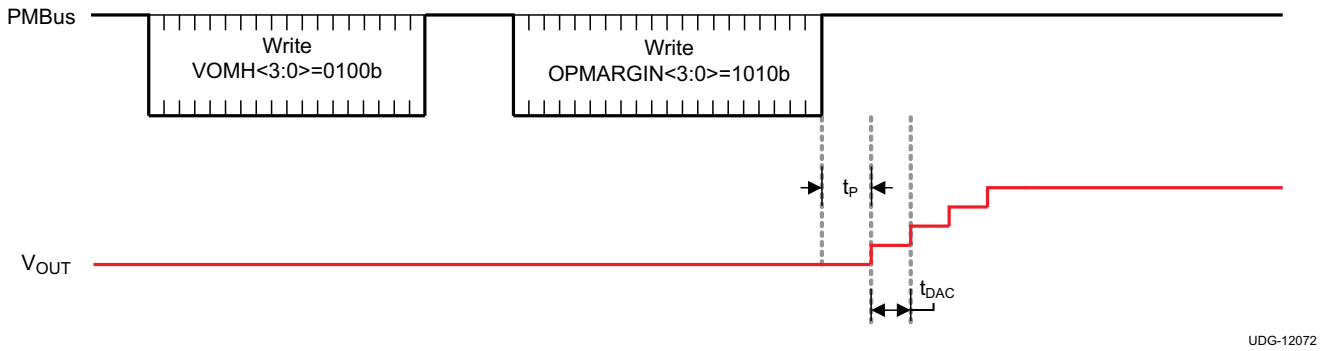


Figure 36. Setting the Margining Level First

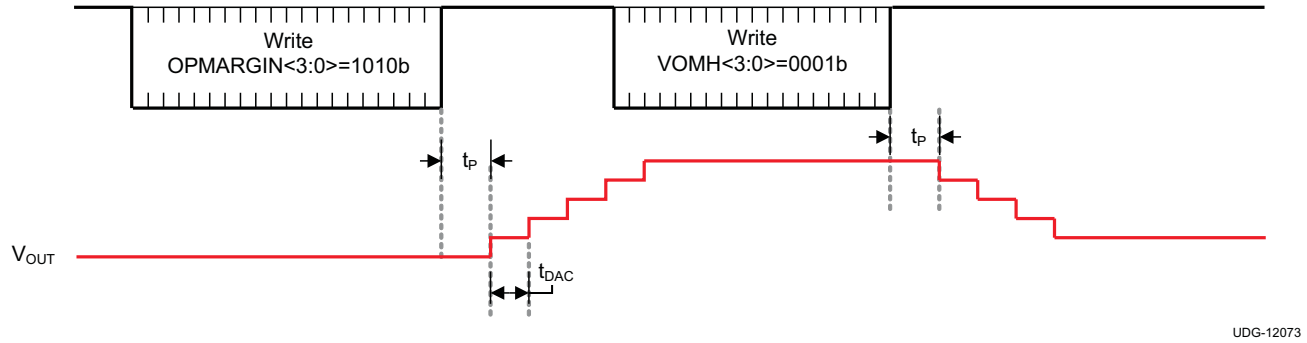


Figure 37. Enabling Margining First

UVLO_THRESHOLD (MFR_SPECIFIC_06) [D6h]

Custom register 6 provides some limited programmability of input supply UVLO threshold, as described in Table 16. The default turn-on UVLO threshold is 4.25 V.

Table 16. UVLO_THRESHOLD (MFR_SPECIFIC_06) Settings

COMMAND	DEFINITION	DESCRIPTION	NVM
UVLO_THRESHOLD<7>	—	not supported and don't care	—
UVLO_THRESHOLD<6>	—	not supported and don't care	—
UVLO_THRESHOLD<5>	—	not supported and don't care	—
UVLO_THRESHOLD<4>	—	not supported and don't care	—
UVLO_THRESHOLD<3>	—	not supported and don't care	—
UVLO_THRESHOLD<2:0>	VDDINUVLO<2:0>	0xx: 10.2 V 100: not supported and should not be used 101: 4.25 V(1) 110: 6.0 V 111: 8.1 V	Yes

(1) TI default.

DESIGN EXAMPLE

Design Example Application

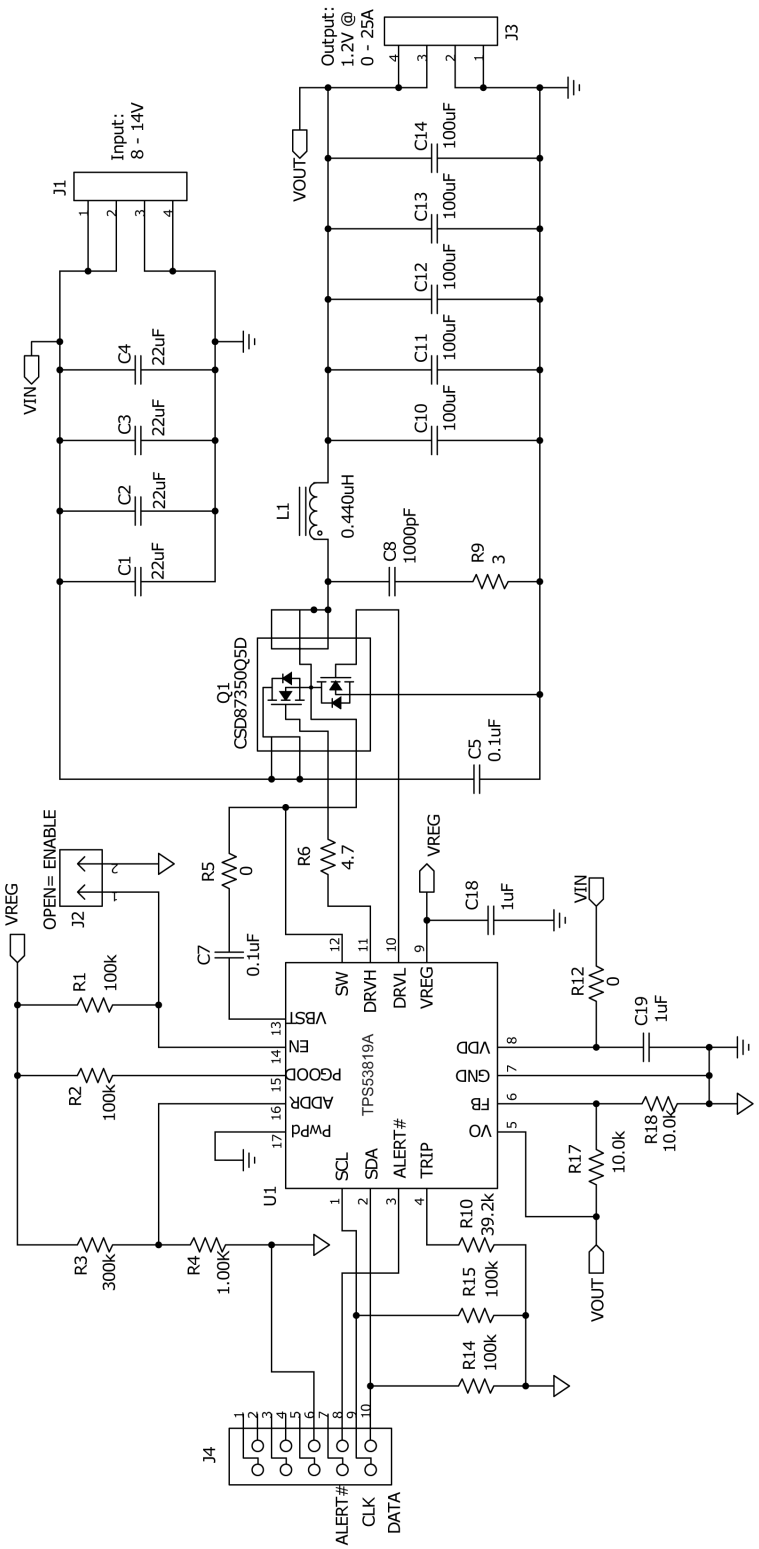


Figure 38. TPS53819A Design Example Application Schematic

Table 17. Design Example Specifications

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V_{VIN}	Input voltage range		8	12	14	V
$V_{VIN(ripple)}$	Input voltage ripple				240	mV_{PP}
V_{OUT}	Output voltage			1.2		V
V_{RIPPLE}	Output voltage ripple				12	mV_{PP}
I_{OUT}	Output load current		0		20	A
I_{OCL}	Output overcurrent			25		A
f_{SW}	Switching frequency			425		kHz

External Component Selection

Selecting external components is a simple process using D-CAP2™ Mode

1. Switching Frequency

The switching frequency must first be decided on and is set using the PMBus. When deciding on a frequency a tradeoff between component size and efficiency must be made. A lower frequency reduces the switching losses in the MOSFETs improving efficiency but a larger inductance and/or output capacitance is required for low output voltage ripple. This example uses the TI default PMBus setting, 425 kHz.

2. Inductor (L1)

Determined the inducatance to yield a ripple current ($I_{IND(ripple)}$) of approximately ¼ to ½ of maximum output current. Larger ripple current increases output ripple voltage, improves the signal-to-noise ratio and helps stable operation. Maximum current ripple occurs with the maximum input voltage. Equation 9 calculates the recommended inductance. After choosing the inductance, use Equation 10 to calculate the ripple.

$$L = \frac{1}{I_{IND(ripple)} \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} = \frac{3}{I_{OUT(max)} \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \quad (9)$$

$$I_{IND(ripple)} = \frac{1}{L \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \quad (10)$$

The inductor requires a low DCR to achieve good efficiency. The inductor also requires enough margin above the peak inductor current before saturation. The peak inductor current can be estimated in Equation 11.

$$I_{IND(peak)} = I_{OCL} + I_{IND(ripple)} \quad (11)$$

Using Equation 9 the recommended inductance for the example is 0.329 µH. An inductor supplied by Pulse Electronics (PA0513.441NLT) is selected with an inductance of 0.440 µH at 0 A and 0.363 µH at its 30 A rated current. The saturation current is 35 A and the DCR is 0.32 mΩ. Using Equation 10 with the selected inductance and maximum input voltage, the current ripple is estimated to be 6.23 A. Equation 11 calculates the peak current to be 31.3 A, well below the saturation current of the inductor. The output current threshold when the supply operates in DCM or CCM can also be estimated as half the estimated current ripple. With the maximum 14 V input in this design the output current threshold is 3.12 A. With lower input voltages, ripple decreases and so does the threshold.

3. Output Capacitor(s) (C10, C11, C12, C13, C14)

Determine the output capacitance to meet the load transient, ripple requirements, and to meet small-signal stability as shown in Equation 12.

$$5 \times f_{C2} \le \frac{R_{C1} \times C_{C1} \times 0.6 \times (0.67 + D)}{2\pi \times G \times L \times C_{OUT} \times V_{OUT}} \le \frac{f_{SW}}{3}$$

where

- G =0.25
- $R_{C1} \times C_{C1}$ time constant can be referred to Table 1
- D is the duty cycle (12)

Based on Equation 12, the value of C_{OUT} to ensure small signal stability can be calculated using Equation 13 and Equation 14. These equations assume MLCC are used and the ESR effects are negligible. If a high ESR output capacitor is used, the effects may reduce the minimum and maximum capacitance. In the design example using Table 1 for 425-kHz switching frequency, the time constant is 62 µs. The recommended minimum capacitance for a design with an 8-V minimum input voltage is 260 µF. The recommended maximum capacitance for design with a 14-V maximum input voltage is 4842 µF.

$$C_{OUT} \le \frac{R_{C1} \times C_{C1} \times 0.6 \times \left(0.67 + \frac{V_{OUT}}{V_{IN(max)}}\right)}{2\pi \times G \times L \times 5 \times f_{C2} \times V_{OUT}} \quad (13)$$

$$C_{OUT} \ge \frac{R_{C1} \times C_{C1} \times 0.6 \times \left(0.67 + \frac{V_{OUT}}{V_{IN(min)}}\right)}{2\pi \times G \times L \times \frac{f_{SW}}{3} \times V_{OUT}} \quad (14)$$

Select a larger output capacitance to decrease the output voltage change that occurs during a load transient and the output voltage ripple.

The minimum output capacitance to meet an output voltage ripple requirement can be calculated with Equation 15. In the example the minimum output capacitance for 12 mV_{PP} ripple is 162 µF. If non ceramic capacitors are used Equation 16 calculates the maximum equivalent series resistance (ESR) of the output capacitor to meet the ripple requirement. Equation 17 calculates the required RMS current rating for the output capacitor. In this example with 12-V nominal input voltage it is 1.77 A. Finally the output capacitor must be rated for the output voltage.

$$C_{OUT} \ge \frac{I_{IND(ripple)}}{8 \times V_{RIPPLE} \times f_{SW}} \quad (15)$$

$$ESR \le \frac{V_{RIPPLE} - \left(\frac{I_{IND(ripple)}}{8 \times C_{OUT} \times f_{SW}}\right)}{I_{IND(ripple)}} \quad (16)$$

$$I_{COUT(RMS)} = \frac{I_{IND(ripple)}}{\sqrt{12}} \quad (17)$$

This example uses five 1210, 100 µF, 6.3 V, X5R ceramic capacitors with 2 mΩ of ESR. From the data sheet the estimated DC derating of 95% and AC derating of 70% for a total of 66.5% at room temperature. The total output capacitance is approximately 332.5 µF.

4. Input Capacitor(s) (C1, C2, C3, C4, C5)

Choose an input capacitance that reduces the input voltage ripple. Equation 18 calculates the minimum input capacitance. In the example design to limit the input ripple to 240 mV, assuming all ceramic and ignoring ESR ripple, the minimum input capacitance is 27.8 µF. The input capacitor must also be rated for the input RMS current calculated in Equation 19. For this design example this current is 8.95 A with the minimum 8-V input voltage. Also, the input capacitors must be rated for the maximum input voltage.

$$C_{IN} \geq \frac{\Delta I_L}{8 \times V_{INRIPPLE} \times f_{SW}} \quad (18)$$

$$I_{CIN(RMS)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN(min)}} \times \frac{\left(V_{IN(min)} - V_{OUT}\right)}{V_{IN(min)}}} \quad (19)$$

This example uses four 1206, 22 µF, 16 V, X5R ceramic capacitors with 3 mΩ of ESR. An additional 0.1-µF capacitor is placed close to the drain of the high-side MOSFET and the source of the low-side MOSFET.

5. MOSFET (Q1, Q2)

The TPS53819A uses two external N-channel MOSFETs. The V_{DS} rating should be greater than the maximum input voltage and include some tolerance for ringing on the switching node. It must also be rated for the DC current. The high-side MOSFET conducts the input current and the low-side MOSFET conducts the output current. The gate drive voltage is set by the VREG voltage of 5 V typical. The gate capacitance should be reduced to minimize the current required to turn on the MOSFETs and switching losses. However it is recommended the low-side MOSFET have a higher gate capacitance to avoid unintentional shoot-through caused by the high dv/dt on the switching node during the high-side turn-on. A reduction in current also reduces power dissipation in TPS53819A. Choose a low $R_{DS(on)}$ to reduce conduction losses especially for the low-side MOSFET because it conducts the output current.

This design uses the CSD87350Q5D, 30-V, 40-A, NexFET power block with integrated low-side and high-side MOSFETs. This is optimized for applications with a 5 V gate drive. The typical gate to source capacitance of the high-side and low-side MOSFETs is 1341 pF and 2900 pF respectively. Using Equation 2 and Equation 3 the average drive currents are 2.7 mA and 5.9 mA. With Equation 4 the power dissipated in the driver is estimated to 42.4 mW. The $R_{DS(on)}$ of the high-side and low-side MOSFETs with a 5 V gate drive voltage is 5 mΩ and 2.2 mΩ respectively.

A small, 4.7-Ω resistance from R6, is added in series between DRVH and the gate of the high-side MOSFET. This slows down the turn-on time of the high-side MOSFET dv/dt and reduces rising edge ringing on the switching node to help prevent shoot-through. This value should be kept small and if it is too large it may lead to too large of a delay time in the turn-on time of the high-side switch.

6. VREG Bypass Capacitor (C18)

A ceramic capacitor with a recommended value between 0.47-µF and 2.2-µF is required on the VREG pin for proper operation. The example uses a 1-µF capacitor. Choose one rated for the VREG 5.5-V maximum voltage in order to supply the instantaneous drive current of the low-side MOSFET.

7. VDD Bypass Capacitor (C19)

A 1-µF capacitor should be placed at the VDD pin rated for the maximum input voltage. If power stage switching noise is causing faults, a small resistor (R12) can be added between VDD and all the input capacitors (C1-C5). This creates an R-C filter and reduces any switching noise in the device input.

8. VBST Capacitor (C7)

The bootstrap capacitor is required to generate the high-side gate drive bias voltage and provide the instantaneous drive current for DRVH. A 0.1-µF ceramic capacitor is recommended to limit the ripple voltage.

R5 (0-Ω) resistance, is added in series with the bootstrap capacitor. This resistor can be used to slow down the turn on time of the high-side MOSFET dv/dt and reduces rising edge ringing on the SW node to help prevent shoot-through. Keep the value small because a higher value may increase the the turn-on delay time of the high-side switch.

9. Snubber (C8 and R9)

Fast-switching edges and parasitic inductance and capacitance cause voltage ringing on the SW node . If the ringing results in excessive voltage on the SW node or erratic operation an R-C snubber can be used to reduce ringing on the SW node and ensure proper operation in all operating conditions.

10. Feedback Resistance, R_{FBH} and R_{FBL} (R17 and R18)

The values of the voltage-divider resistors, R_{FBH} and R_{FBL} determine the output voltage as shown in Figure 38. R_{FBH} is connected between the FB pin and the output, and R_{FBL} is connected between the FB pin and GND. The recommended R_{FBH} value is between 10 kΩ and 20 kΩ. Determine R_{FBL} using Equation 20.

$$R_{FBL} = \frac{R_{FBH}}{\left[\frac{V_{OUT} - \frac{1}{2}\times\left(I_{IND(ripple)}\times\left(ESR + \frac{1}{8\times C_{OUT}\times f_{SW}}\right)\right)}{0.6 - \left(\frac{1}{2}\times\left(I_{IND(ripple)}\times\frac{L}{4\times R_{C1}\times C_{C1}}\right) - V_{OFS}\right)}\right] - 1}$$

where

- V_{OFS} is the internal offset voltage (4 mV)
- ESR is the from the output capacitors

(20)

In this example R17 has a value of 10-kΩ. R18 is calculated to be 9.91 kΩ. The nearest standard value of 10 kΩ is used for R18.

11. Overcurrent limit (OCL) setting resistance (R10)

Combining Equation 7 and Equation 8, Equation 21 calculates R_{TRIP}.

$$R_{TRIP} = \frac{8\times\left(I_{OCL} - \left(\frac{(V_{IN} - V_{OUT})}{(2\times L_X)}\right)\times\frac{V_{OUT}}{(f_{SW}\times V_{IN})}\right)\times R_{DS(on)}}{I_{TRIP}} \quad (21)$$

In this example for a 25-A current limit, R_{TRIP} is calculated as 38.5 kΩ and is rounded up to the nearest standard value of 39.2 kΩ.

12. PMBus address of the device (R3 and R4)

The PMBus address is selected using a resistive divider as shown in Table 2. In this example the address is set to 0010000 with a 300-kΩ resistor (R3) and a 1.00-kΩ (R4).

13. PGOOD pull-up resistor (R2)

A pull-up resistor is required because the PGOOD pin is an open-drain output. Use a value between 10 kΩ to 100 kΩ. The recommended max 100 kΩ resistor is used.

14. SCL AND SDA pull-down resistors (R14 and R15)

If there is no PMBus (I^2C) needed in the system, pull these two pins down to ground. If a PMBus interface is always present, then these resistors are not needed. This example design uses 100-kΩ of resistance to pull these pins down to ground, allowing it to operate with or without a PMBus interface.

15. PMBus pull-up resistors

Due to the limited drive strength of pulldown MOSFETs on SDA and $\overline{\text{ALERT}}$ pins, the external PMBus pull-up resistors must be kept within certain ranges. For example, if the external PMBus supply is 3.3 V, then use a pull-up resistance of 1-kΩ. If the external PMBus supply is 5 V, then use a pull-up resistance of 1.5 kΩ.

Layout Considerations

Note these design considerations before starting a layout work using TPS53819A

- Inductor, V_{IN} capacitor(s), V_{OUT} capacitor(s) and MOSFETs are the power components and should be placed on one side of the PCB (solder side). Other small signal components can be placed on another side (component side). At least one inner plane should be inserted, connected to ground, in order to shield and isolate the small signal traces from noisy power lines.
- Place all sensitive analog traces and components such as FB, VO, TRIP, PGOOD, and EN away from high-voltage switching nodes such as SW, DRVL, DRVH or VBST to avoid coupling. Use internal layer(s) as ground plane(s) and shield feedback trace from power traces and components.
- Keep PMBus interfacing signals away from the sensitive analog traces.
- The DC/DC converter has several high-current loops. Minimize the area of these loops in order to suppress switching noise.
  - The path from the V_{IN} capacitor(s) through the high and low-side MOSFETs and back to the capacitor(s) through ground, is the most important loop area to minimize. Connect the negative node of the V_{IN} capacitor(s) and the source of the low-side MOSFET at ground as close as possible.
  - The second important loop is the path from the low-side MOSFET through inductor and V_{OUT} capacitor(s), and back to source of the low-side MOSFET through ground. Connect source of the low-side MOSFET and negative node of V_{OUT} capacitor(s) at ground as close as possible.
  - The third important loop is that of the gate driving system for the low-side MOSFET. To turn on the low-side MOSFET, high current flows from the VDRV capacitor through the gate driver and the low-side MOSFET, and back to negative node of the capacitor through ground. To turn off the low-side MOSFET, high current flows from gate of the low-side MOSFET through the gate driver and PGND of the device, and back to source of the low-side MOSFET through ground. Connect the negative node of the VREG capacitor, source of the low-side MOSFET and PGND of the device at ground as close as possible.
- A separate AGND from the high-current loop PGND should be used for the return of the sensitive analog circuitry. The two grounds should connect at a single point as close to the GND pin as possible.
- Minimize the current loop from the VDD and VREG pins through their respective capacitors to the GND pin.
- Because the TPS53819A controls the output voltage referring to voltage across V_{OUT} capacitor, the top-side resistor of the voltage divider should be connected to the positive node of the V_{OUT} capacitor. In a same manner both bottom side resistor and GND of the device should be connected to the negative node of V_{OUT} capacitor. The trace from these resistors to the VFB pin should be short and thin. Place on the component side and avoid via(s) between these resistors and the device.
- Connect the overcurrent setting resistor from the TRIP pin to ground and make the connections as close as possible to the device. Avoid coupling a high-voltage switching node to the trace from the TRIP pin to R_{TRIP} and from R_{TRIP} to ground .
- Connections from gate drivers to the respective gate of the high-side or the low-side MOSFET should be as short as possible to reduce stray inductance. Use 0.65 mm (25 mils) or wider trace and via(s) of at least 0.5 mm (20 mils) diameter along this trace.
- The PCB trace defined as switch node, which connects to source of high-side MOSFET, drain of low-side MOSFET and high-voltage side of the inductor, should be as short and wide as possible.
- Follow any layout considerations for the MOSFET provided by the MOSFET manufacturer.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS53819ARGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	3819A	Samples
TPS53819ARGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	3819A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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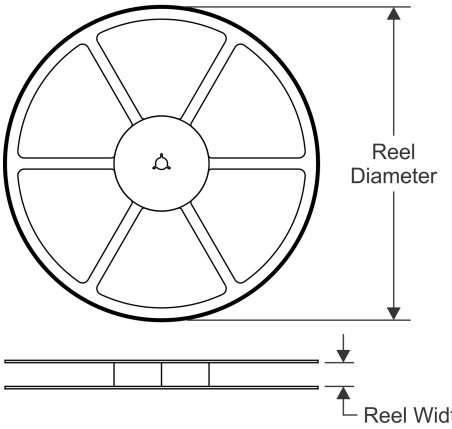
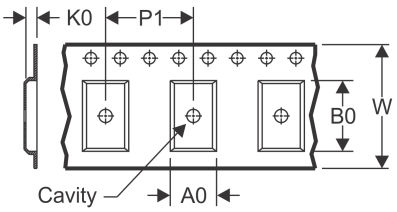
TAPE AND REEL INFORMATION

REEL DIMENSIONS

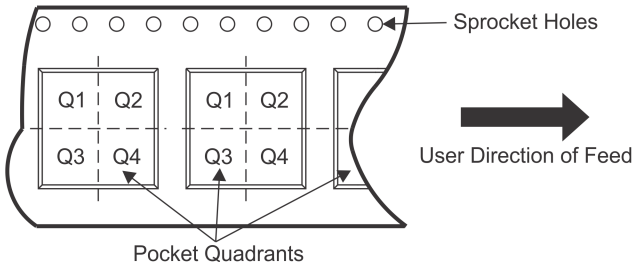


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

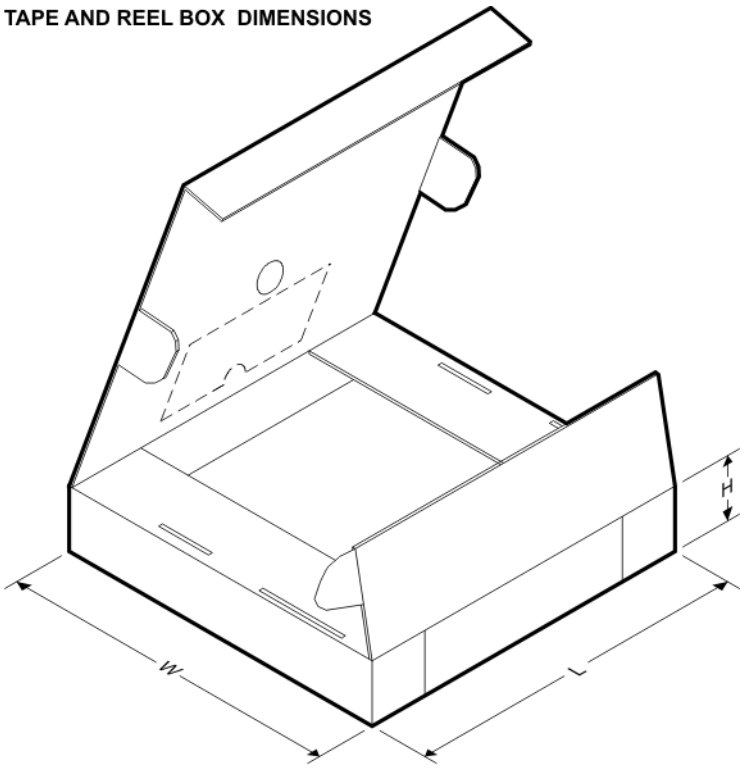
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53819ARGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS53819ARGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS53819ARGTT	QFN	RGT	16	250	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2

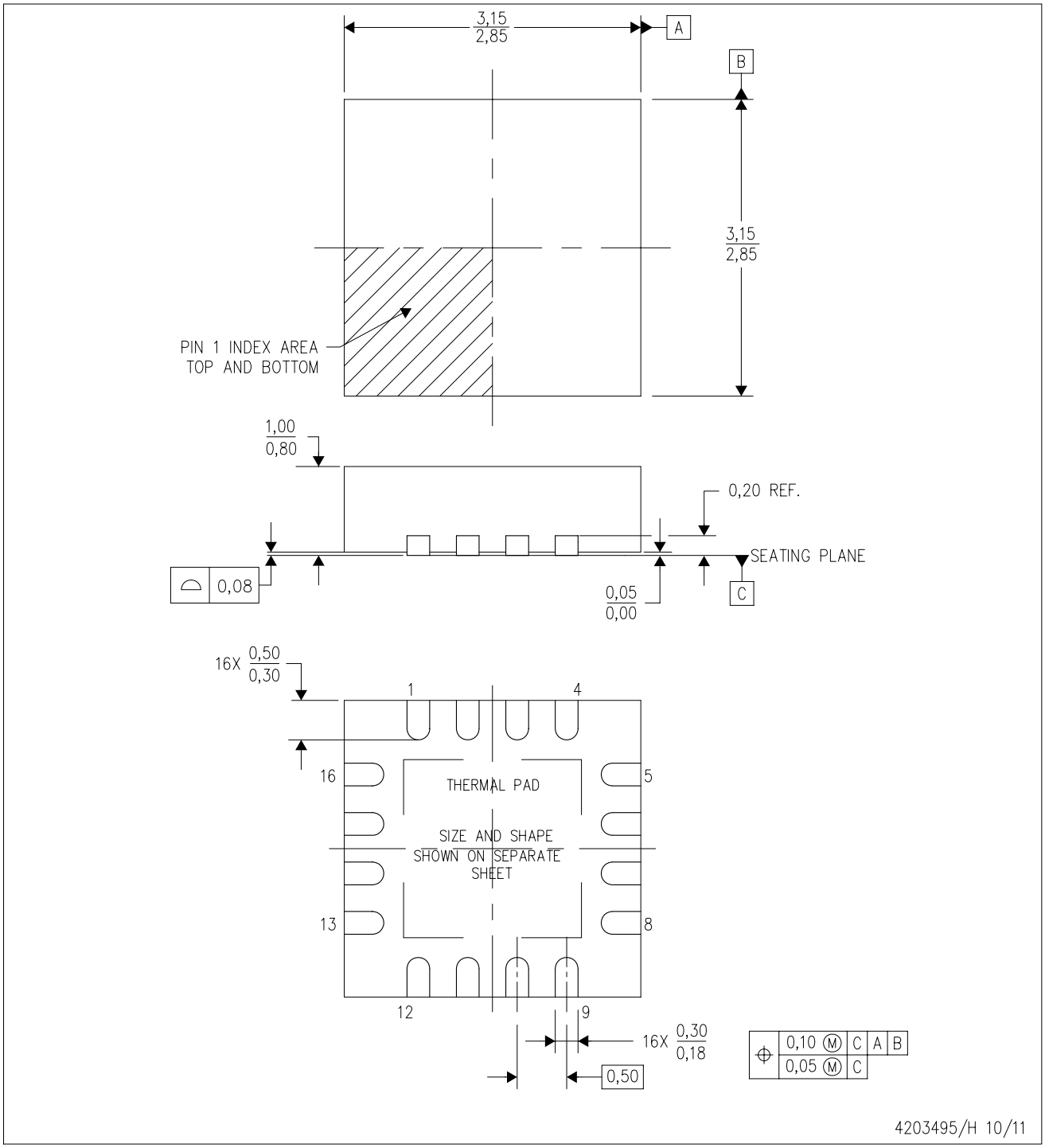
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53819ARGTR	QFN	RGT	16	3000	367.0	367.0	35.0
TPS53819ARGTR	QFN	RGT	16	3000	338.0	355.0	50.0
TPS53819ARGTT	QFN	RGT	16	250	338.0	355.0	50.0

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

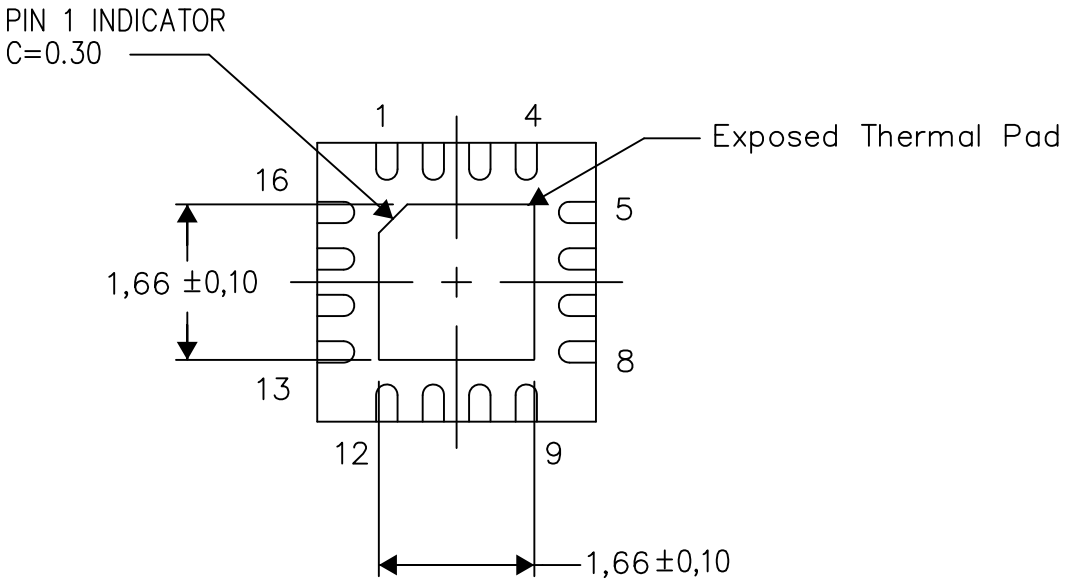
RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206349–10/W 10/14

NOTE: All linear dimensions are in millimeters

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