

# TLV431A, TLV431B, TLV431C, SCV431B, NCV431

## Low Voltage Precision Adjustable Shunt Regulator

The TLV431A, B and C series are precision low voltage shunt regulators that are programmable over a wide voltage range of 1.24 V to 16 V. The TLV431A series features a guaranteed reference accuracy of  $\pm 1.0\%$  at 25°C and  $\pm 2.0\%$  over the entire industrial temperature range of -40°C to 85°C. The TLV431B series features higher reference accuracy of  $\pm 0.5\%$  and  $\pm 1.0\%$  respectively. For the TLV431C series, the accuracy is even higher. It is  $\pm 0.2\%$  and  $\pm 1.0\%$  respectively. These devices exhibit a sharp low current turn-on characteristic with a low dynamic impedance of 0.20  $\Omega$  over an operating current range of 100  $\mu\text{A}$  to 20 mA. This combination of features makes this series an excellent replacement for zener diodes in numerous applications circuits that require a precise reference voltage. When combined with an optocoupler, the TLV431A/B/C can be used as an error amplifier for controlling the feedback loop in isolated low output voltage (3.0 V to 3.3 V) switching power supplies. These devices are available in economical TO-92-3 and micro size TSOP-5 and SOT-23-3 packages.

### Features

- Programmable Output Voltage Range of 1.24 V to 16 V
- Voltage Reference Tolerance  $\pm 1.0\%$  for A Series,  $\pm 0.5\%$  for B Series and  $\pm 0.2\%$  for C Series
- Sharp Low Current Turn-On Characteristic
- Low Dynamic Output Impedance of 0.20  $\Omega$  from 100  $\mu\text{A}$  to 20 mA
- Wide Operating Current Range of 50  $\mu\text{A}$  to 20 mA
- Micro Miniature TSOP-5, SOT-23-3 and TO-92-3 Packages
- These are Pb-Free and Halide-Free Devices
- SCV and NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

### Applications

- Low Output Voltage (3.0 V to 3.3 V) Switching Power Supply Error Amplifier
- Adjustable Voltage or Current Linear and Switching Power Supplies
- Voltage Monitoring
- Current Source and Sink Circuits
- Analog and Digital Circuits Requiring Precision References
- Low Voltage Zener Diode Replacements

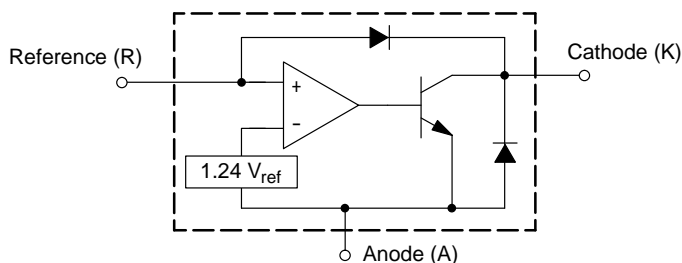
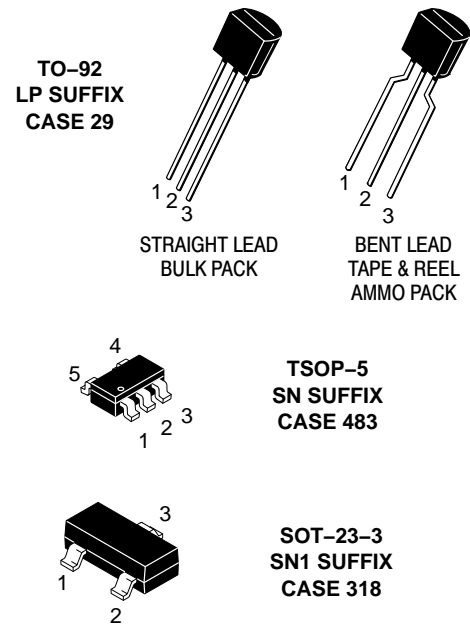


Figure 1. Representative Block Diagram



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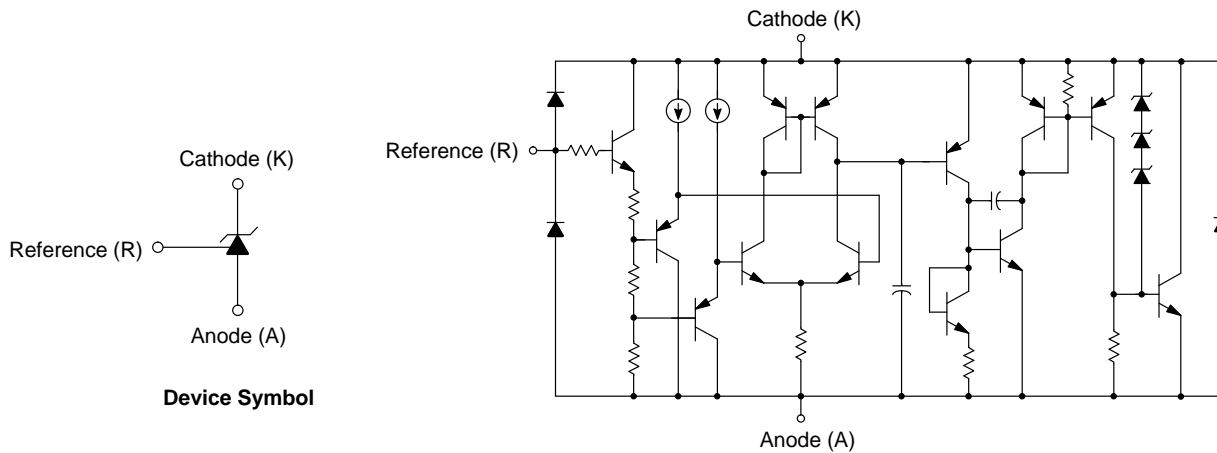
### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.

### DEVICE MARKING INFORMATION AND PIN CONNECTIONS

See general marking information in the device marking section on page 13 of this data sheet.

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The device contains 13 active transistors.

**Figure 2. Representative Device Symbol and Schematic Diagram**

## MAXIMUM RATINGS (Full operating ambient temperature range applies, unless otherwise noted)

Rating	Symbol	Value	Unit
Cathode to Anode Voltage	$V_{KA}$	18	V
Cathode Current Range, Continuous	$I_K$	-20 to 25	mA
Reference Input Current Range, Continuous	$I_{ref}$	-0.05 to 10	mA
Thermal Characteristics			$^{\circ}C/W$
LP Suffix Package, TO-92-3 Package			
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	178	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	83	
SN Suffix Package, TSOP-5 Package			
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	226	
SN1 Suffix Package, SOT-23-3 Package			
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	491	
Operating Junction Temperature	$T_J$	150	$^{\circ}C$
Operating Ambient Temperature Range	$T_A$	TLV431x -40 to 85 NCV431, SCV431B -40 to 125	$^{\circ}C$
Storage Temperature Range	$T_{stg}$	-65 to 150	$^{\circ}C$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

NOTE: This device series contains ESD protection and exceeds the following tests:

Human Body Model 2000 V per JEDEC JESD22-A114F, Machine Model Method 200 V per JEDEC JESD22-A115C, Charged Device Method 500 V per JEDEC JESD22-C101E. This device contains latch-up protection and exceeds  $\pm 100$  mA per JEDEC standard JESD78.

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

## RECOMMENDED OPERATING CONDITIONS

Condition	Symbol	Min	Max	Unit
Cathode to Anode Voltage	$V_{KA}$	$V_{ref}$	16	V
Cathode Current	$I_K$	0.1	20	mA

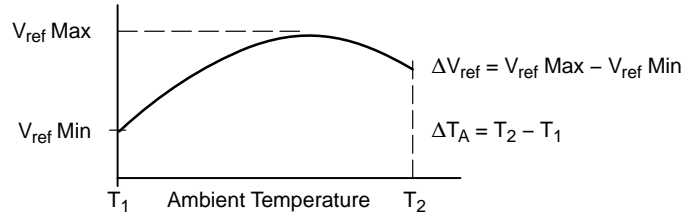
Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

# TLV431A, TLV431B, TLV431C, SCV431B, NCV431

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	TLV431A			TLV431B			Unit
		Min	Typ	Max	Min	Typ	Max	
Reference Voltage (Figure 3) (V <sub>KA</sub> = V <sub>ref</sub> , I <sub>K</sub> = 10 mA, T <sub>A</sub> = 25°C) (T <sub>A</sub> = T <sub>low</sub> to T <sub>high</sub> , Note 1)	V <sub>ref</sub>	1.228 1.215	1.240 –	1.252 1.265	1.234 1.228	1.240 –	1.246 1.252	V
Reference Input Voltage Deviation Over Temperature (Figure 3) (V <sub>KA</sub> = V <sub>ref</sub> , I <sub>K</sub> = 10 mA, T <sub>A</sub> = T <sub>low</sub> to T <sub>high</sub> , Notes 1, 2, 3)	ΔV <sub>ref</sub>	–	7.2	20	–	7.2	20	mV
Ration of Reference Input Voltage Change to Cathode Voltage Change (Figure 4) (V <sub>KA</sub> = V <sub>ref</sub> to 16 V, I <sub>K</sub> = 10 mA)	$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	–	–0.6	–1.5	–	–0.6	–1.5	$\frac{mV}{V}$
Reference Terminal Current (Figure 4) (I <sub>K</sub> = 10 mA, R1 = 10 kΩ, R2 = open)	I <sub>ref</sub>	–	0.15	0.3	–	0.15	0.3	μA
Reference Input Current Deviation Over Temperature (Figure 4) (I <sub>K</sub> = 10 mA, R1 = 10 kΩ, R2 = open, Notes 1, 2, 3)	ΔI <sub>ref</sub>	–	0.04	0.08	–	0.04	0.08	μA
Minimum Cathode Current for Regulation (Figure 3)	I <sub>K(min)</sub>	–	30	80	–	30	80	μA
Off-State Cathode Current (Figure 5) (V <sub>KA</sub> = 6.0 V, V <sub>ref</sub> = 0) (V <sub>KA</sub> = 16 V, V <sub>ref</sub> = 0)	I <sub>K(off)</sub>	– –	0.01 0.012	0.04 0.05	– –	0.01 0.012	0.04 0.05	μA
Dynamic Impedance (Figure 3) (V <sub>KA</sub> = V <sub>ref</sub> , I <sub>K</sub> = 0.1 mA to 20 mA, f ≤ 1.0 kHz, Note 4)	Z <sub>KA</sub>	–	0.25	0.4	–	0.25	0.4	Ω

1. Ambient temperature range: T<sub>low</sub> = –40°C, T<sub>high</sub> = 85°C.
2. Guaranteed but not tested.
3. The deviation parameters ΔV<sub>ref</sub> and ΔI<sub>ref</sub> are defined as the difference between the maximum value and minimum value obtained over the full operating ambient temperature range that applied.



The average temperature coefficient of the reference input voltage, αV<sub>ref</sub> is defined as:

$$\alpha V_{ref} \left( \frac{\text{ppm}}{^{\circ}\text{C}} \right) = \frac{\left( \frac{\Delta V_{ref}}{V_{ref} (T_A = 25^{\circ}\text{C})} \times 10^6 \right)}{\Delta T_A}$$

αV<sub>ref</sub> can be positive or negative depending on whether V<sub>ref</sub> Min or V<sub>ref</sub> Max occurs at the lower ambient temperature, refer to Figure 8.

Example: ΔV<sub>ref</sub> = 7.2 mV and the slope is positive,

$$V_{ref} @ 25^{\circ}\text{C} = 1.241 \text{ V}$$

$$\Delta T_A = 125^{\circ}\text{C}$$

$$\alpha V_{ref} \left( \frac{\text{ppm}}{^{\circ}\text{C}} \right) = \frac{0.0072 \times 10^6}{1.241 \times 125} = 46 \text{ ppm}/^{\circ}\text{C}$$

4. The dynamic impedance Z<sub>KA</sub> is defined as:

$$|Z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_K}$$

When the device is operating with two external resistors, R1 and R2, (refer to Figure 4) the total dynamic impedance of the circuit is given by:

$$|Z_{KA}'| = |Z_{KA}| \times \left( 1 + \frac{R1}{R2} \right)$$

# TLV431A, TLV431B, TLV431C, SCV431B, NCV431

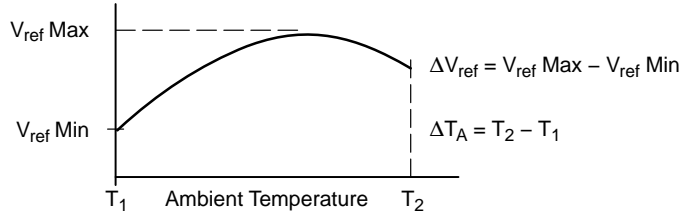
## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	TLV431C			Unit
		Min	Typ	Max	
Reference Voltage (Figure 3) (V <sub>KA</sub> = V <sub>ref</sub> , I <sub>K</sub> = 10 mA, T <sub>A</sub> = 25°C) (T <sub>A</sub> = T <sub>low</sub> to T <sub>high</sub> , Note 5)	V <sub>ref</sub>	1.237 1.228	1.240 –	1.243 1.252	V
Reference Input Voltage Deviation Over Temperature (Figure 3) (V <sub>KA</sub> = V <sub>ref</sub> , I <sub>K</sub> = 10 mA, T <sub>A</sub> = T <sub>low</sub> to T <sub>high</sub> , Notes 5, 6, 7)	ΔV <sub>ref</sub>	–	7.2	2.0	mV
Ration of Reference Input Voltage Change to Cathode Voltage Change (Figure 4) (V <sub>KA</sub> = V <sub>ref</sub> to 16 V, I <sub>K</sub> = 10 mA)	$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	–	–0.6	–1.5	$\frac{mV}{V}$
Reference Terminal Current (Figure 4) (I <sub>K</sub> = 10 mA, R1 = 10 kΩ, R2 = open)	I <sub>ref</sub>	–	0.15	0.3	μA
Reference Input Current Deviation Over Temperature (Figure 4) (I <sub>K</sub> = 10 mA, R1 = 10 kΩ, R2 = open, Notes 5, 6, 7)	ΔI <sub>ref</sub>	–	0.04	0.08	μA
Minimum Cathode Current for Regulation (Figure 3)	I <sub>K(min)</sub>	–	30	80	μA
Off-State Cathode Current (Figure 5) (V <sub>KA</sub> = 6.0 V, V <sub>ref</sub> = 0) (V <sub>KA</sub> = 16 V, V <sub>ref</sub> = 0)	I <sub>K(off)</sub>	– –	0.01 0.012	0.04 0.05	μA
Dynamic Impedance (Figure 3) (V <sub>KA</sub> = V <sub>ref</sub> , I <sub>K</sub> = 0.1 mA to 20 mA, f ≤ 1.0 kHz, Note 8)	Z <sub>KA</sub>	–	0.25	0.4	Ω

5. Ambient temperature range: T<sub>low</sub> = –40°C, T<sub>high</sub> = 85°C.

6. Guaranteed but not tested.

7. The deviation parameters ΔV<sub>ref</sub> and ΔI<sub>ref</sub> are defined as the difference between the maximum value and minimum value obtained over the full operating ambient temperature range that applied.



The average temperature coefficient of the reference input voltage, αV<sub>ref</sub> is defined as:

$$\alpha V_{ref} \left( \frac{\text{ppm}}{^{\circ}\text{C}} \right) = \frac{\left( \frac{\Delta V_{ref}}{V_{ref} (T_A = 25^{\circ}\text{C})} \times 10^6 \right)}{\Delta T_A}$$

αV<sub>ref</sub> can be positive or negative depending on whether V<sub>ref</sub> Min or V<sub>ref</sub> Max occurs at the lower ambient temperature, refer to Figure 8.

Example: ΔV<sub>ref</sub> = 7.2 mV and the slope is positive,

$$V_{ref} @ 25^{\circ}\text{C} = 1.241 \text{ V}$$

$$\Delta T_A = 125^{\circ}\text{C}$$

$$\alpha V_{ref} \left( \frac{\text{ppm}}{^{\circ}\text{C}} \right) = \frac{0.0072 \times 10^6}{1.241 \times 125} = 46 \text{ ppm}/^{\circ}\text{C}$$

8. The dynamic impedance Z<sub>KA</sub> is defined as:

$$|Z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_K}$$

When the device is operating with two external resistors, R1 and R2, (refer to Figure 4) the total dynamic impedance of the circuit is given by:

$$|Z_{KA}'| = |Z_{KA}| \times \left( 1 + \frac{R1}{R2} \right)$$

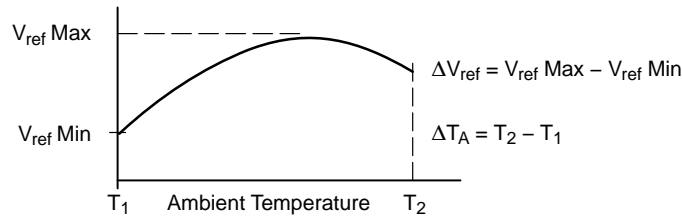
# TLV431A, TLV431B, TLV431C, SCV431B, NCV431

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	NCV431A			Unit
		Min	Typ	Max	
Reference Voltage (Figure 3) (V <sub>KA</sub> = V <sub>ref</sub> , I <sub>K</sub> = 10 mA, T <sub>A</sub> = 25°C) (T <sub>A</sub> = -40°C to 85°C) (T <sub>A</sub> = -40°C to 125°C)	V <sub>ref</sub>	1.228 1.215 1.211	1.240 – –	1.252 1.265 1.265	V
Reference Input Voltage Deviation Over Temperature (Figure 3) (V <sub>KA</sub> = V <sub>ref</sub> , I <sub>K</sub> = 10 mA, T <sub>A</sub> = -40°C to 85°C, Notes 9, 10) (V <sub>KA</sub> = V <sub>ref</sub> , I <sub>K</sub> = 10 mA, T <sub>A</sub> = -40°C to 125°C, Notes 9, 10)	ΔV <sub>ref</sub>	– –	7.2 7.2	20 24	mV
Ration of Reference Input Voltage Change to Cathode Voltage Change (Figure 4) (V <sub>KA</sub> = V <sub>ref</sub> to 16 V, I <sub>K</sub> = 10 mA)	$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	–	-0.6	-1.5	$\frac{mV}{V}$
Reference Terminal Current (Figure 4) (I <sub>K</sub> = 10 mA, R1 = 10 kΩ, R2 = open)	I <sub>ref</sub>	–	0.15	0.3	μA
Reference Input Current Deviation Over Temperature (Figure 4) (I <sub>K</sub> = 10 mA, R1 = 10 kΩ, R2 = open, T <sub>A</sub> = -40°C to 85°C, Notes 9, 10) (I <sub>K</sub> = 10 mA, R1 = 10 kΩ, R2 = open, T <sub>A</sub> = -40°C to 125°C, Notes 9, 10)	ΔI <sub>ref</sub>	– –	0.04 –	0.08 0.10	μA
Minimum Cathode Current for Regulation (Figure 3)	I <sub>K(min)</sub>	–	30	80	μA
Off-State Cathode Current (Figure 5) (V <sub>KA</sub> = 6.0 V, V <sub>ref</sub> = 0) (V <sub>KA</sub> = 16 V, V <sub>ref</sub> = 0)	I <sub>K(off)</sub>	– –	0.01 0.012	0.04 0.05	μA
Dynamic Impedance (Figure 3) (V <sub>KA</sub> = V <sub>ref</sub> , I <sub>K</sub> = 0.1 mA to 20 mA, f ≤ 1.0 kHz, Note 11)	Z <sub>KA</sub>	–	0.25	0.4	Ω

9. Guaranteed but not tested.

10. The deviation parameters ΔV<sub>ref</sub> and ΔI<sub>ref</sub> are defined as the difference between the maximum value and minimum value obtained over the full operating ambient temperature range that applied.



The average temperature coefficient of the reference input voltage, αV<sub>ref</sub> is defined as:

$$\alpha V_{ref} \left( \frac{\text{ppm}}{^{\circ}\text{C}} \right) = \frac{\left( \frac{\Delta V_{ref}}{V_{ref} (T_A = 25^{\circ}\text{C})} \times 10^6 \right)}{\Delta T_A}$$

αV<sub>ref</sub> can be positive or negative depending on whether V<sub>ref</sub> Min or V<sub>ref</sub> Max occurs at the lower ambient temperature, refer to Figure 8.

Example: ΔV<sub>ref</sub> = 7.2 mV and the slope is positive,

$$V_{ref} @ 25^{\circ}\text{C} = 1.241 \text{ V}$$

$$\Delta T_A = 125^{\circ}\text{C}$$

$$\alpha V_{ref} \left( \frac{\text{ppm}}{^{\circ}\text{C}} \right) = \frac{0.0072 \times 10^6}{1.241 \times 125} = 46 \text{ ppm}/^{\circ}\text{C}$$

11. The dynamic impedance Z<sub>KA</sub> is defined as:

$$|Z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_K}$$

When the device is operating with two external resistors, R1 and R2, (refer to Figure 4) the total dynamic impedance of the circuit is given by:

$$|Z_{KA}'| = |Z_{KA}| \times \left( 1 + \frac{R1}{R2} \right)$$

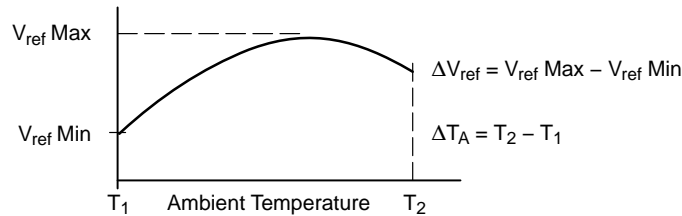
# TLV431A, TLV431B, TLV431C, SCV431B, NCV431

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	SCV431B, NCV431B			Unit
		Min	Typ	Max	
Reference Voltage (Figure 3) (V <sub>KA</sub> = V <sub>ref</sub> , I <sub>K</sub> = 10 mA, T <sub>A</sub> = 25°C) (T <sub>A</sub> = -40°C to 85°C) (T <sub>A</sub> = -40°C to 125°C)	V <sub>ref</sub>	1.234 1.228 1.224	1.240 – –	1.246 1.252 1.252	V
Reference Input Voltage Deviation Over Temperature (Figure 3) (V <sub>KA</sub> = V <sub>ref</sub> , I <sub>K</sub> = 10 mA, T <sub>A</sub> = -40°C to 85°C, Notes 9, 10) (V <sub>KA</sub> = V <sub>ref</sub> , I <sub>K</sub> = 10 mA, T <sub>A</sub> = -40°C to 125°C, Notes 9, 10)	ΔV <sub>ref</sub>	– –	7.2 7.2	20 24	mV
Ration of Reference Input Voltage Change to Cathode Voltage Change (Figure 4) (V <sub>KA</sub> = V <sub>ref</sub> to 16 V, I <sub>K</sub> = 10 mA)	$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	–	-0.6	-1.5	$\frac{mV}{V}$
Reference Terminal Current (Figure 4) (I <sub>K</sub> = 10 mA, R1 = 10 kΩ, R2 = open)	I <sub>ref</sub>	–	0.15	0.3	μA
Reference Input Current Deviation Over Temperature (Figure 4) (I <sub>K</sub> = 10 mA, R1 = 10 kΩ, R2 = open, T <sub>A</sub> = -40°C to 85°C, Notes 12, 13) (I <sub>K</sub> = 10 mA, R1 = 10 kΩ, R2 = open, T <sub>A</sub> = -40°C to 125°C, Notes 12, 13)	ΔI <sub>ref</sub>	– –	0.04 –	0.08 0.10	μA
Minimum Cathode Current for Regulation (Figure 3)	I <sub>K(min)</sub>	–	30	80	μA
Off-State Cathode Current (Figure 5) (V <sub>KA</sub> = 6.0 V, V <sub>ref</sub> = 0) (V <sub>KA</sub> = 16 V, V <sub>ref</sub> = 0)	I <sub>K(off)</sub>	– –	0.01 0.012	0.04 0.05	μA
Dynamic Impedance (Figure 3) (V <sub>KA</sub> = V <sub>ref</sub> , I <sub>K</sub> = 0.1 mA to 20 mA, f ≤ 1.0 kHz, Note 14)	Z <sub>KA</sub>	–	0.25	0.4	Ω

12. Guaranteed but not tested.

13. The deviation parameters ΔV<sub>ref</sub> and ΔI<sub>ref</sub> are defined as the difference between the maximum value and minimum value obtained over the full operating ambient temperature range that applied.



The average temperature coefficient of the reference input voltage, αV<sub>ref</sub> is defined as:

$$\alpha V_{ref} \left( \frac{\text{ppm}}{^{\circ}\text{C}} \right) = \frac{\left( \frac{\Delta V_{ref}}{V_{ref} (T_A = 25^{\circ}\text{C})} \times 10^6 \right)}{\Delta T_A}$$

αV<sub>ref</sub> can be positive or negative depending on whether V<sub>ref</sub> Min or V<sub>ref</sub> Max occurs at the lower ambient temperature, refer to Figure 8.

Example: ΔV<sub>ref</sub> = 7.2 mV and the slope is positive,

$$V_{ref} @ 25^{\circ}\text{C} = 1.241 \text{ V}$$

$$\Delta T_A = 125^{\circ}\text{C}$$

$$\alpha V_{ref} \left( \frac{\text{ppm}}{^{\circ}\text{C}} \right) = \frac{0.0072 \times 10^6}{1.241 \times 125} = 46 \text{ ppm}/^{\circ}\text{C}$$

14. The dynamic impedance Z<sub>KA</sub> is defined as:

$$|Z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_K}$$

When the device is operating with two external resistors, R1 and R2, (refer to Figure 4) the total dynamic impedance of the circuit is given by:

$$|Z_{KA}'| = |Z_{KA}| \times \left( 1 + \frac{R1}{R2} \right)$$

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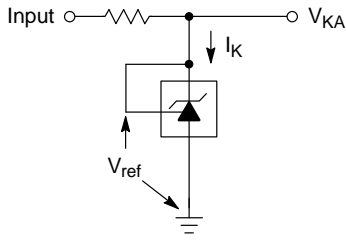


Figure 3. Test Circuit for  $V_{KA} = V_{ref}$

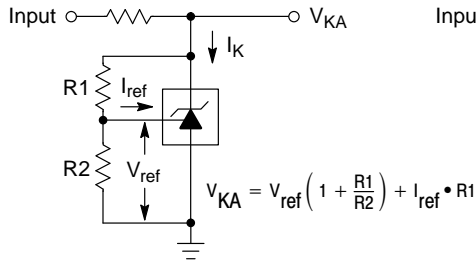


Figure 4. Test Circuit for  $V_{KA} > V_{ref}$

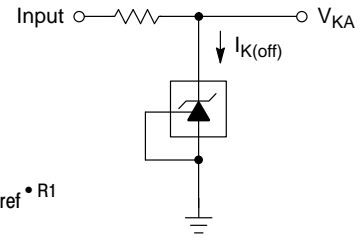


Figure 5. Test Circuit for  $I_{K(off)}$

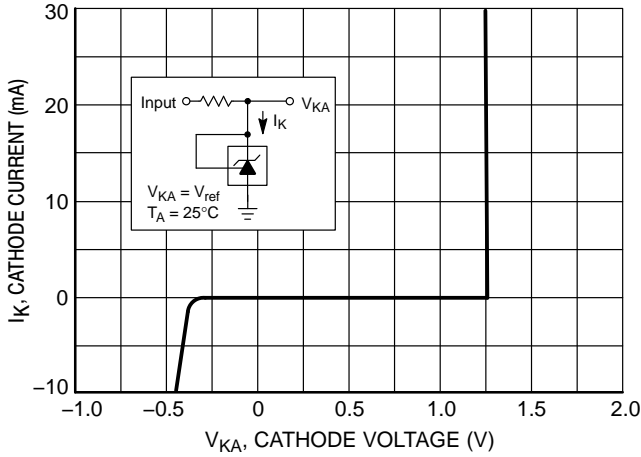


Figure 6. Cathode Current vs. Cathode Voltage

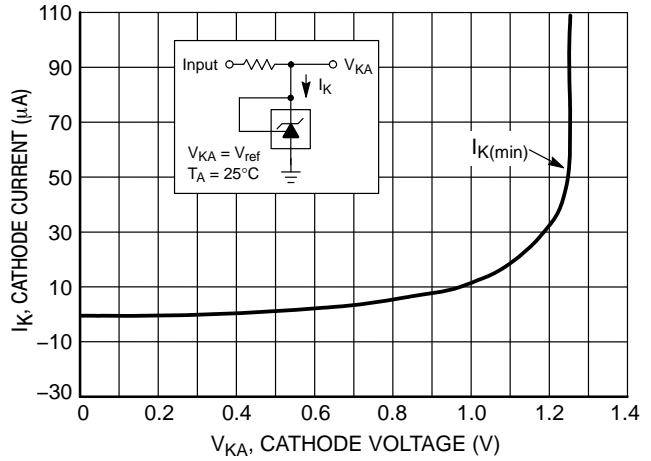


Figure 7. Cathode Current vs. Cathode Voltage

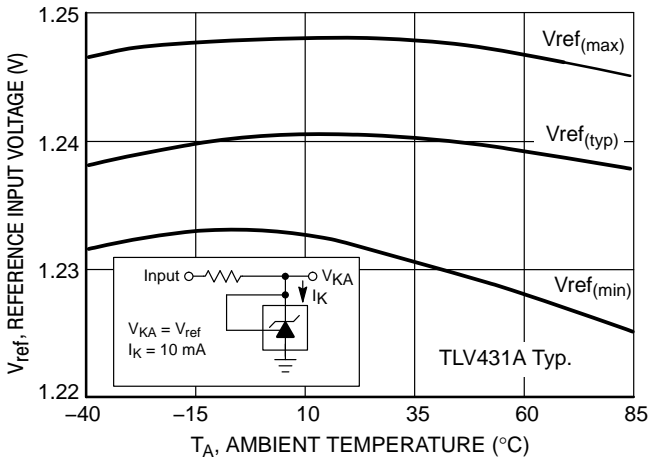


Figure 8. Reference Input Voltage versus Ambient Temperature

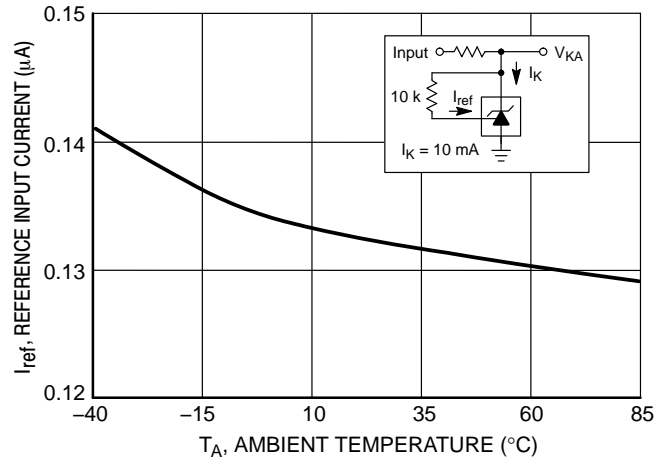


Figure 9. Reference Input Current versus Ambient Temperature

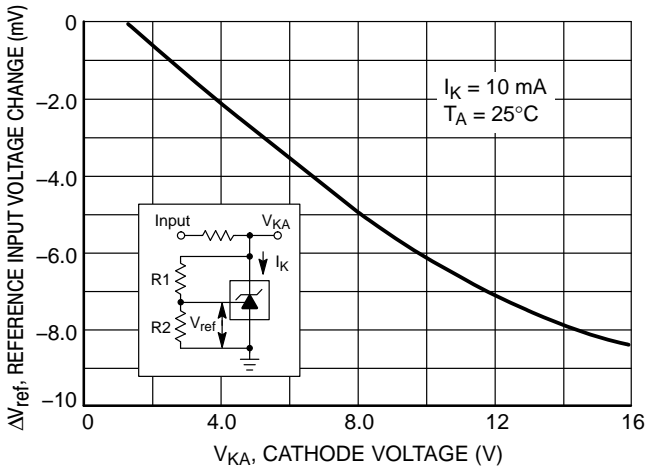


Figure 10. Reference Input Voltage Change versus Cathode Voltage

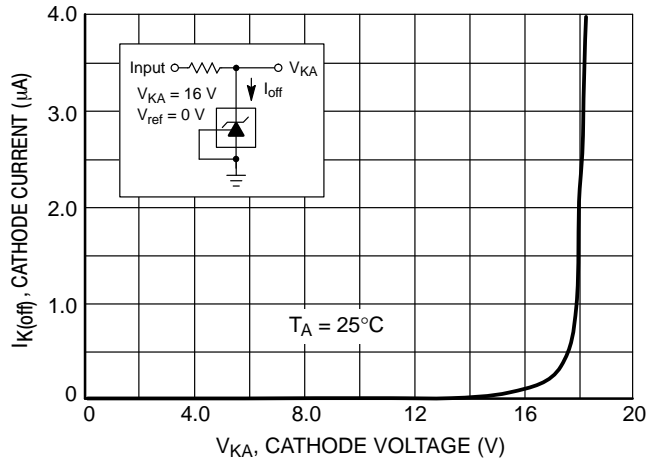


Figure 11. Off-State Cathode Current versus Cathode Voltage

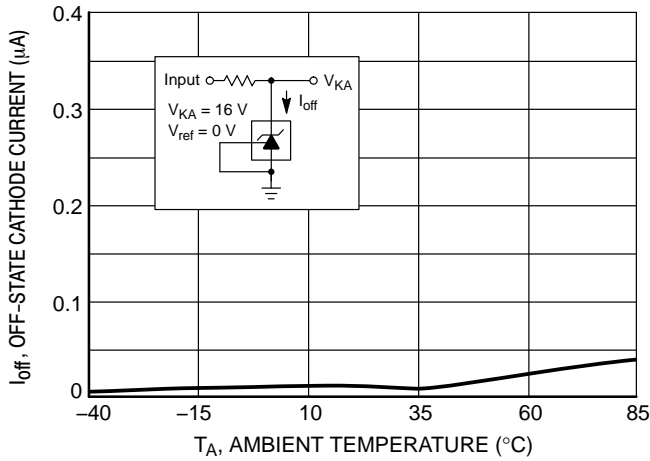


Figure 12. Off-State Cathode Current versus Ambient Temperature

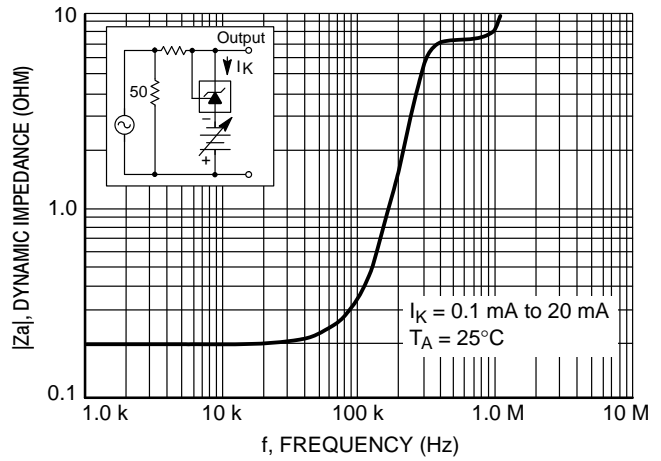


Figure 13. Dynamic Impedance versus Frequency

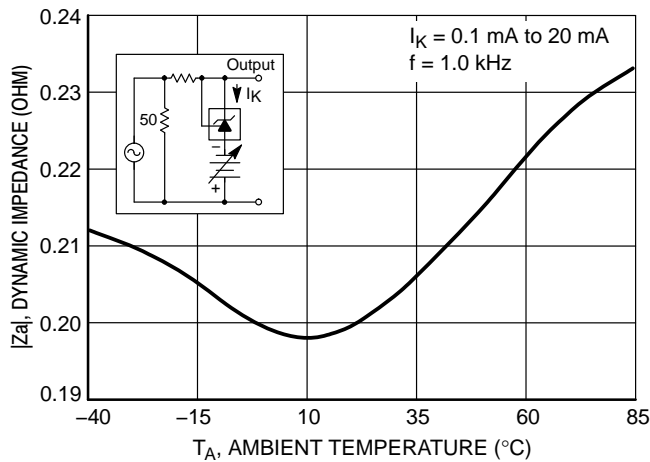


Figure 14. Dynamic Impedance versus Ambient Temperature

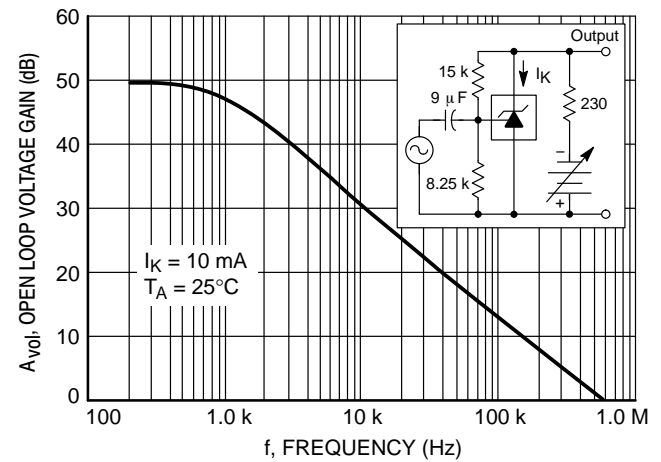


Figure 15. Open-Loop Voltage Gain versus Frequency



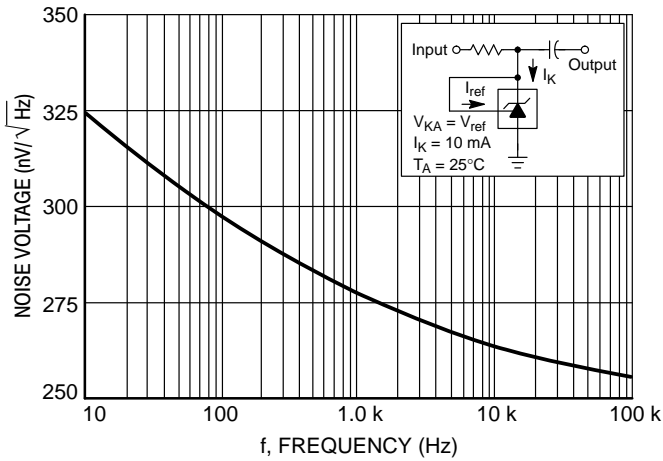


Figure 16. Spectral Noise Density

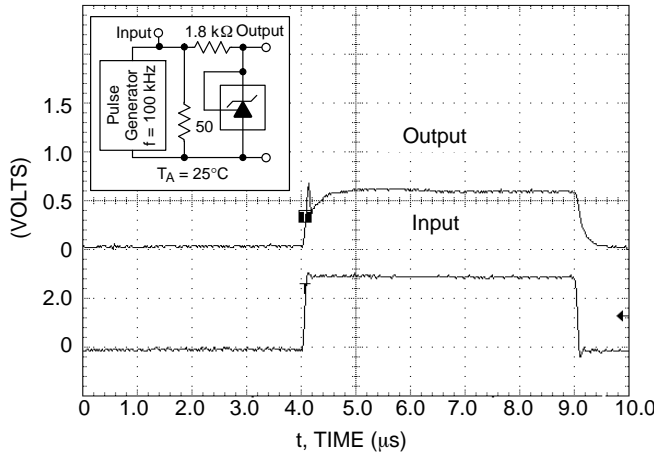


Figure 17. Pulse Response

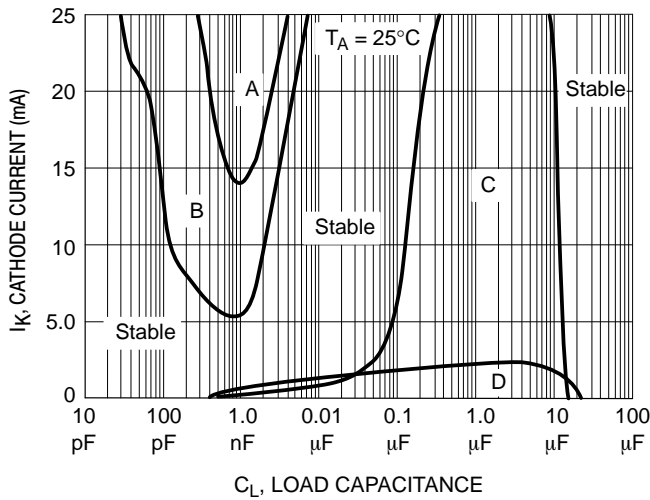
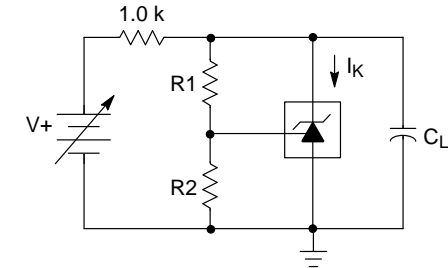


Figure 18. Stability Boundary Conditions



Unstable Regions	V <sub>KA</sub> (V)	R1 (kΩ)	R2 (kΩ)
A, C	V <sub>ref</sub>	0	∞
B, D	5.0	30.4	10

Figure 19. Test Circuit for Figure 18

### Stability

Figures 18 and 19 show the stability boundaries and circuit configurations for the worst case conditions with the load capacitance mounted as close as possible to the device. The required load capacitance for stable operation can vary depending on the operating temperature and capacitor

equivalent series resistance (ESR). Ceramic or tantalum surface mount capacitors are recommended for both temperature and ESR. The application circuit stability should be verified over the anticipated operating current and temperature ranges.

TYPICAL APPLICATIONS

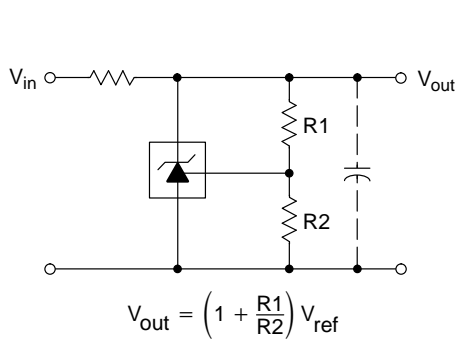


Figure 20. Shunt Regulator

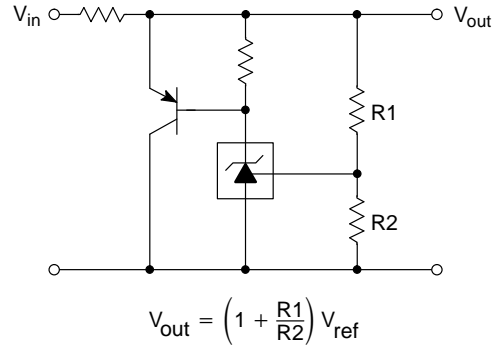


Figure 21. High Current Shunt Regulator

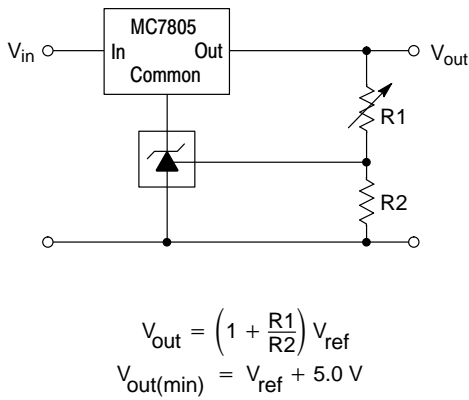


Figure 22. Output Control for a Three Terminal Fixed Regulator

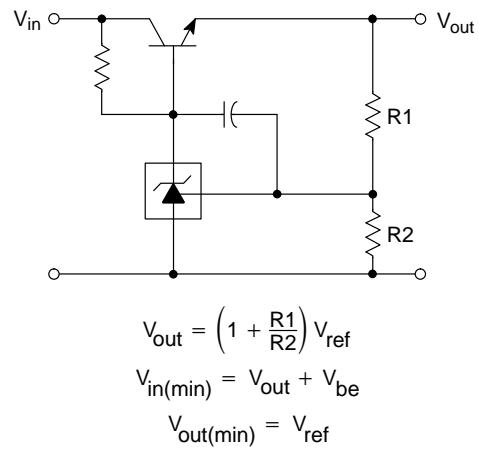


Figure 23. Series Pass Regulator

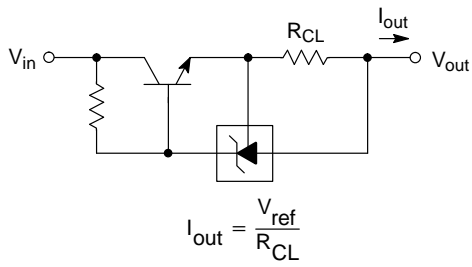


Figure 24. Constant Current Source

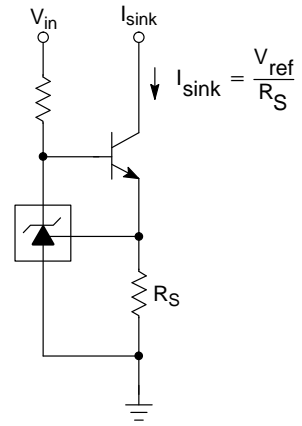


Figure 25. Constant Current Sink

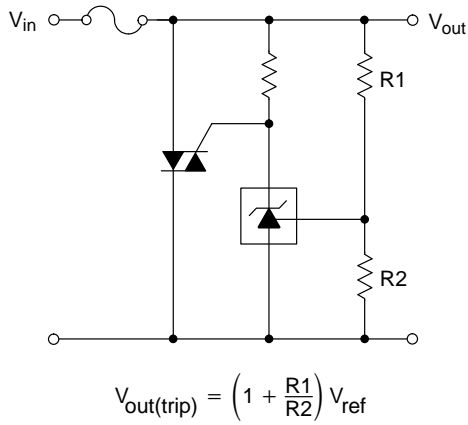


Figure 26. TRIAC Crowbar

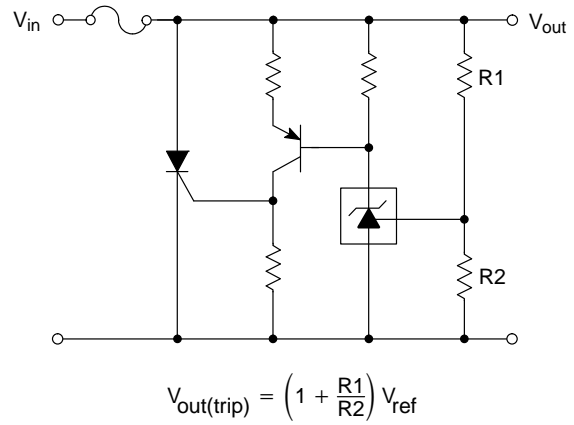
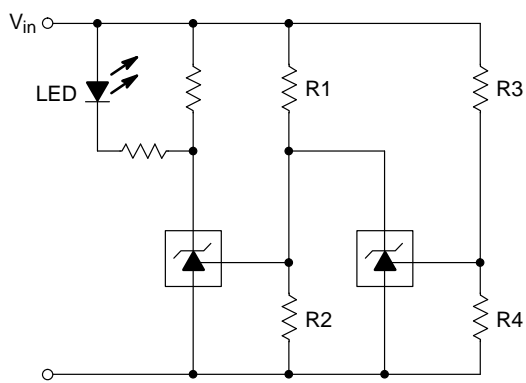


Figure 27. SCR Crowbar

# TLV431A, TLV431B, TLV431C, SCV431B, NCV431

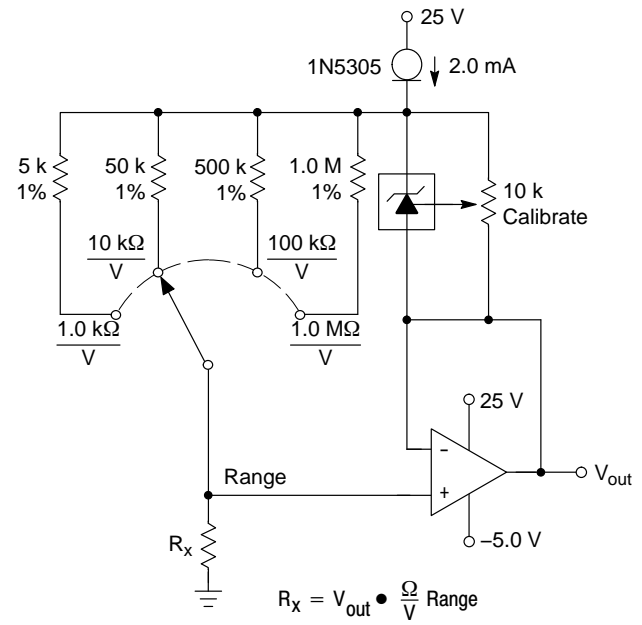


L.E.D. indicator is 'ON' when  $V_{in}$  is between the upper and lower limits,

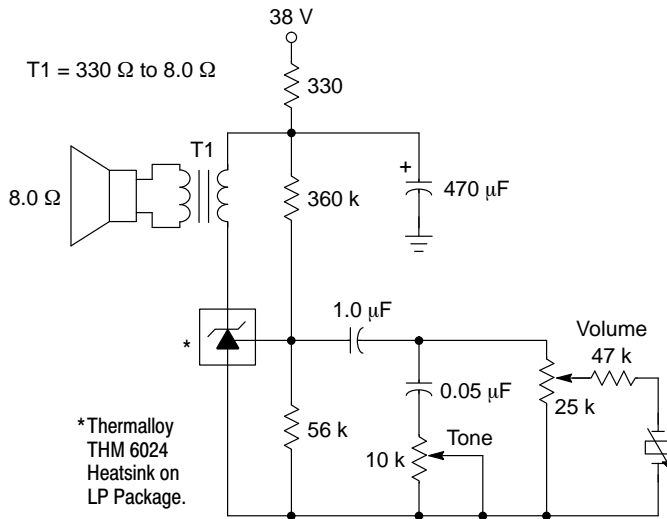
$$\text{Lower limit} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

$$\text{Upper limit} = \left(1 + \frac{R3}{R4}\right) V_{ref}$$

**Figure 28. Voltage Monitor**



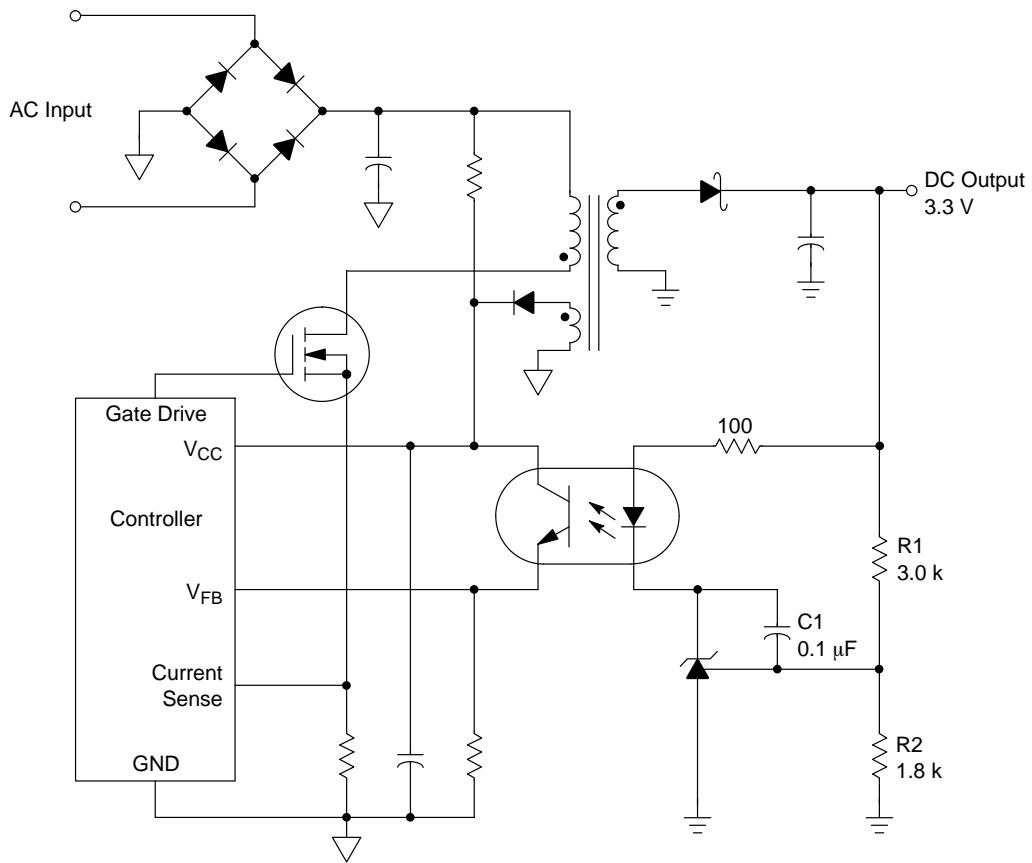
**Figure 29. Linear Ohmmeter**



\*Thermalloy THM 6024 Heatsink on LP Package.

**Figure 30. Simple 400 mW Phono Amplifier**

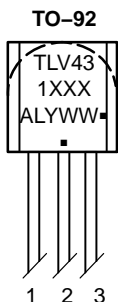
# TLV431A, TLV431B, TLV431C, SCV431B, NCV431



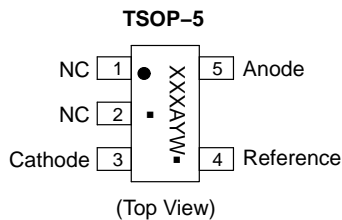
**Figure 31. Isolated Output Line Powered Switching Power Supply**

The above circuit shows the TLV431A/B/C as a compensated amplifier controlling the feedback loop of an isolated output line powered switching regulator. The output voltage is programmed to 3.3 V by the resistors values selected for R1 and R2. The minimum output voltage that can be programmed with this circuit is 2.64 V, and is limited by the sum of the reference voltage (1.24 V) and the forward drop of the optocoupler light emitting diode (1.4 V). Capacitor C1 provides loop compensation.

## PIN CONNECTIONS AND DEVICE MARKING

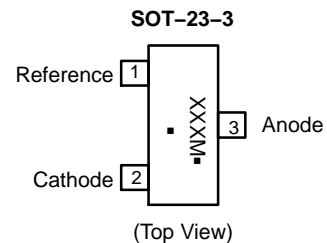


1. Reference
2. Anode
3. Cathode



(Top View)

- XXX = Specific Device Code
  - A = Assembly Location
  - Y = Year
  - L = Wafer Lot
  - WW, W = Work Week
  - = Pb-Free Package
- (Note: Microdot may be in either location)



(Top View)

- XXX = Specific Device Code
  - M = Date Code
  - = Pb-Free Package
- (Note: Microdot may be in either location)

## TLV431A, TLV431B, TLV431C, SCV431B, NCV431

### ORDERING INFORMATION

Device	Device Code	Package	Shipping†
TLV431ALPG	ALP	TO-92-3 (Pb-Free)	6000 / Box
TLV431ALPRAG	ALP	TO-92-3 (Pb-Free)	2000 / Tape & Reel
TLV431ALPREG	ALP	TO-92-3 (Pb-Free)	2000 / Tape & Reel
TLV431ALPRMG	ALP	TO-92-3 (Pb-Free)	2000 / Ammo Pack
TLV431ALPRPG	ALP	TO-92-3 (Pb-Free)	2000 / Ammo Pack
TLV431ASNT1G	RAA	TSOP-5 (Pb-Free, Halide-Free)	3000 / Tape & Reel
TLV431ASN1T1G	RAF	SOT-23-3 (Pb-Free, Halide-Free)	3000 / Tape & Reel
TLV431BLPG	BLP	TO-92-3 (Pb-Free)	6000 / Box
TLV431BLPRAG	BLP	TO-92-3 (Pb-Free)	2000 / Tape & Reel
TLV431BLPREG	BLP	TO-92-3 (Pb-Free)	2000 / Tape & Reel
TLV431BLPRMG	BLP	TO-92-3 (Pb-Free)	2000 / Ammo Pack
TLV431BLPRPG	BLP	TO-92-3 (Pb-Free)	2000 / Ammo Pack
TLV431BSNT1G	RAH	TSOP-5 (Pb-Free, Halide-Free)	3000 / Tape & Reel
TLV431BSN1T1G	RAG	SOT-23-3 (Pb-Free, Halide-Free)	3000 / Tape & Reel
TLV431CSN1T1G	AAN	SOT-23-3 (Pb-Free, Halide-Free)	3000 / Tape & Reel
SCV431BSN1T1G*	RAC	SOT-23-3 (Pb-Free, Halide-Free)	3000 / Tape & Reel
NCV431ASNT1G*	ACH	TSOP-5 (Pb-Free, Halide-Free)	3000 / Tape & Reel
NCV431BSNT1G*	AD6	TSOP-5 (Pb-Free, Halide-Free)	3000 / Tape & Reel

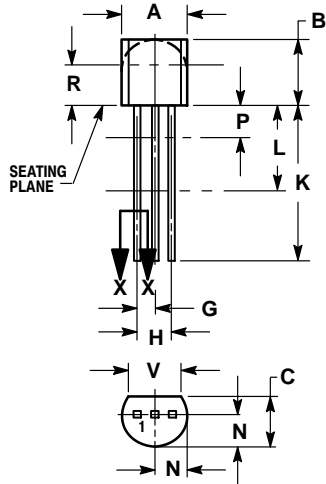
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*SCV, NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

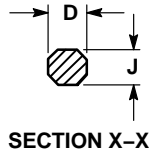
# TLV431A, TLV431B, TLV431C, SCV431B, NCV431

## PACKAGE DIMENSIONS

TO-92 (TO-226)  
LP SUFFIX  
CASE 29-11  
ISSUE AM



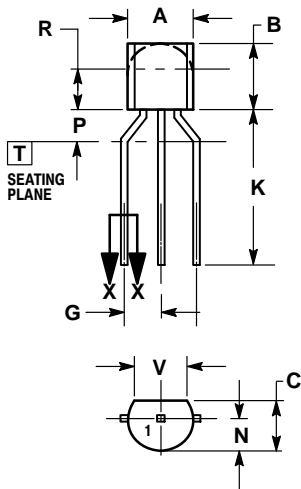
STRAIGHT LEAD  
BULK PACK



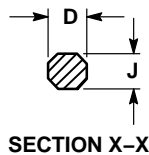
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.115	---	2.93	---
V	0.135	---	3.43	---



BENT LEAD  
TAPE & REEL  
AMMO PACK



NOTES:

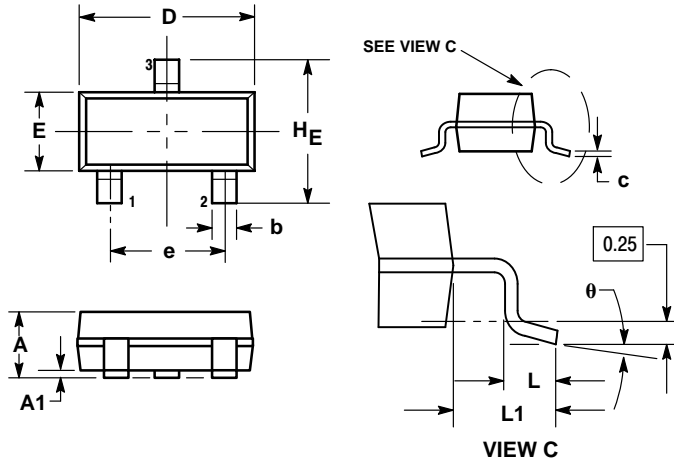
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	MILLIMETERS	
	MIN	MAX
A	4.45	5.20
B	4.32	5.33
C	3.18	4.19
D	0.40	0.54
G	2.40	2.80
J	0.39	0.50
K	12.70	---
N	2.04	2.66
P	1.50	4.00
R	2.93	---
V	3.43	---

# TLV431A, TLV431B, TLV431C, SCV431B, NCV431

## PACKAGE DIMENSIONS

SOT-23-3  
SN1 SUFFIX  
CASE 318-08  
ISSUE AP

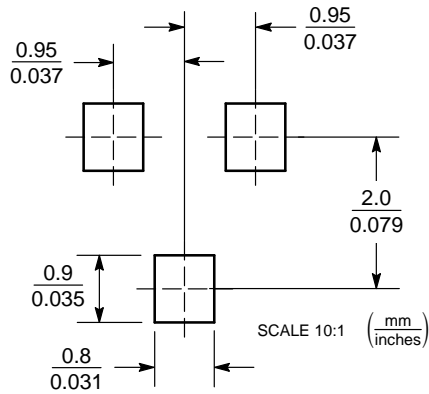


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
HE	2.10	2.40	2.64	0.083	0.094	0.104
θ	0°	---	10°	0°	---	10°

### SOLDERING FOOTPRINT

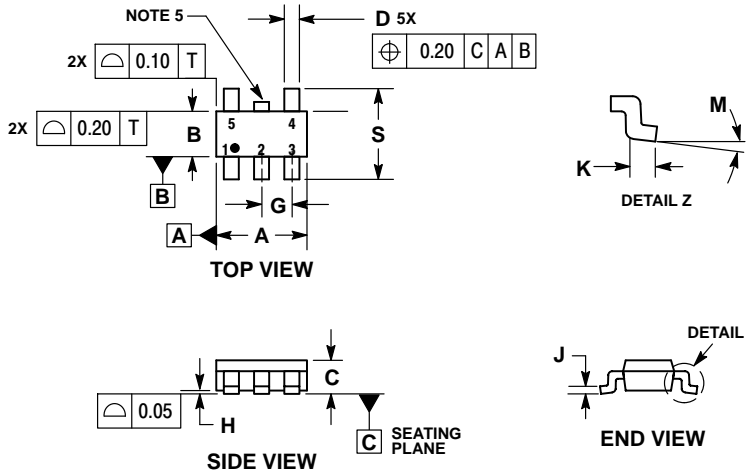




# TLV431A, TLV431B, TLV431C, SCV431B, NCV431

## PACKAGE DIMENSIONS

TSOP-5  
SN SUFFIX  
CASE 483-02  
ISSUE K

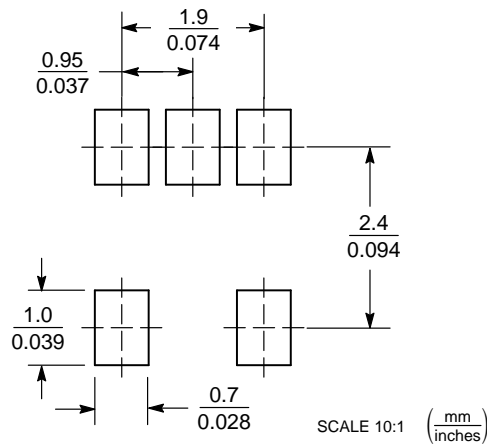


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

DIM	MILLIMETERS	
	MIN	MAX
A	3.00 BSC	
B	1.50 BSC	
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0° 10°	
S	2.50	3.00

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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