

IRFL024ZPbF

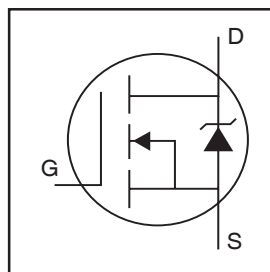
HEXFET® Power MOSFET

Features

- Advanced Process Technology
- Ultra Low On-Resistance
- 150°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to T_{jmax}
- Lead-Free

Description

This HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 150°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in a wide variety of applications.



$V_{DSS} = 55V$
$R_{DS(on)} = 57.5m\Omega$
$I_D = 5.1A$



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited) ⑦	5.1	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ⑦	4.1	
I_{DM}	Pulsed Drain Current ①	41	
$P_D @ T_A = 25^\circ C$	Power Dissipation ⑦	2.8	W
$P_D @ T_A = 25^\circ C$	Power Dissipation ⑧	1.0	
	Linear Derating Factor ⑦	0.02	
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ②	13	mJ
E_{AS} (Tested)	Single Pulse Avalanche Energy Tested Value ③	32	
I_{AR}	Avalanche Current ①	See Fig.12a, 12b, 15, 16	A
E_{AR}	Repetitive Avalanche Energy ⑤		mJ
T_J	Operating Junction and	-55 to + 150	$^\circ C$
T_{STG}	Storage Temperature Range		

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient (PCB mount, steady state) ⑦	—	45	$^\circ C/W$
$R_{\theta JA}$	Junction-to-Ambient (PCB mount, steady state) ⑧	—	120	

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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.053	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	46.2	57.5	m Ω	$V_{GS} = 10V, I_D = 3.1A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
gfs	Forward Transconductance	6.2	—	—	S	$V_{DS} = 25V, I_D = 3.1A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 55V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 55V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{GS} = -20V$
Q_g	Total Gate Charge	—	9.1	14	nC	$I_D = 3.1A$
Q_{gs}	Gate-to-Source Charge	—	1.9	—		$V_{DS} = 44V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	3.9	—		$V_{GS} = 10V$ ③
$t_{d(on)}$	Turn-On Delay Time	—	7.8	—	ns	$V_{DD} = 28V$
t_r	Rise Time	—	21	—		$I_D = 3.1A$
$t_{d(off)}$	Turn-Off Delay Time	—	30	—		$R_G = 53\Omega$
t_f	Fall Time	—	23	—		$V_{GS} = 10V$ ③
C_{iss}	Input Capacitance	—	340	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	68	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	39	—		$f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	210	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	55	—		$V_{GS} = 0V, V_{DS} = 44V, f = 1.0\text{MHz}$
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	93	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 44V$ ④

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	5.1	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	41		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 3.1A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	15	23	ns	$T_J = 25^\circ\text{C}, I_F = 3.1A, V_{DD} = 28V$
Q_{rr}	Reverse Recovery Charge	—	9.8	15	nC	$di/dt = 100A/\mu s$ ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 2.8\text{mH}$
 $R_G = 25\Omega, I_{AS} = 3.1A, V_{GS} = 10V$.
Part not recommended for use above this value.
- ③ Pulse width $\leq 1.0\text{ms}$; duty cycle $\leq 2\%$.
- ④ $C_{oss \text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

- ⑤ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑥ This value determined from sample failure population. 100% tested to this value in production.
- ⑦ When mounted on 1 inch square copper board.
- ⑧ When mounted on FR-4 board using minimum recommended footprint.

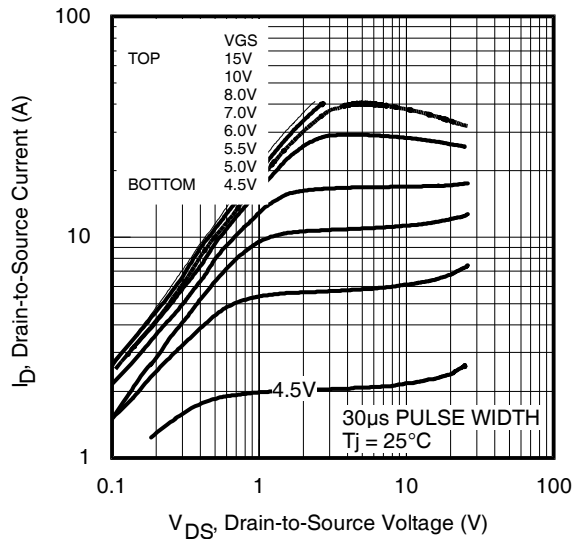


Fig 1. Typical Output Characteristics

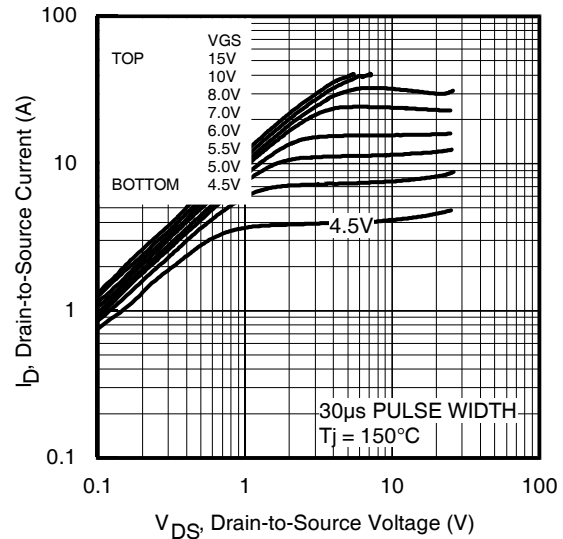


Fig 2. Typical Output Characteristics

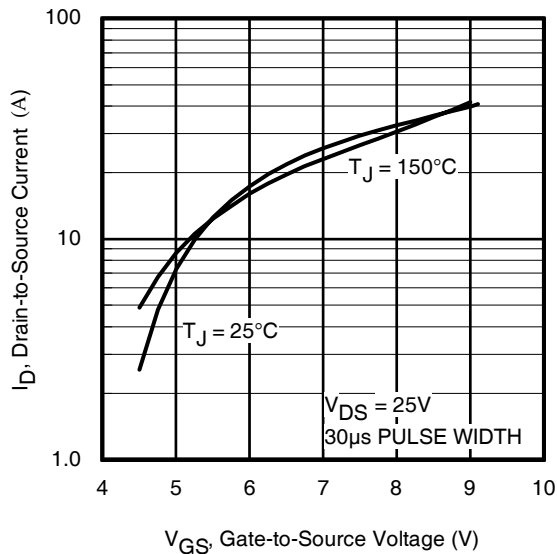


Fig 3. Typical Transfer Characteristics

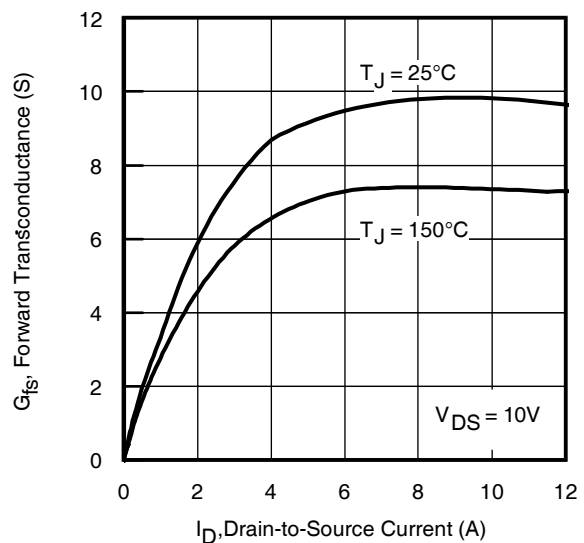
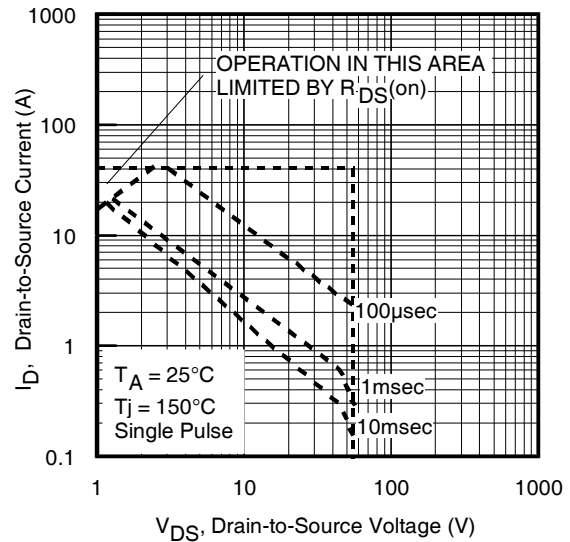
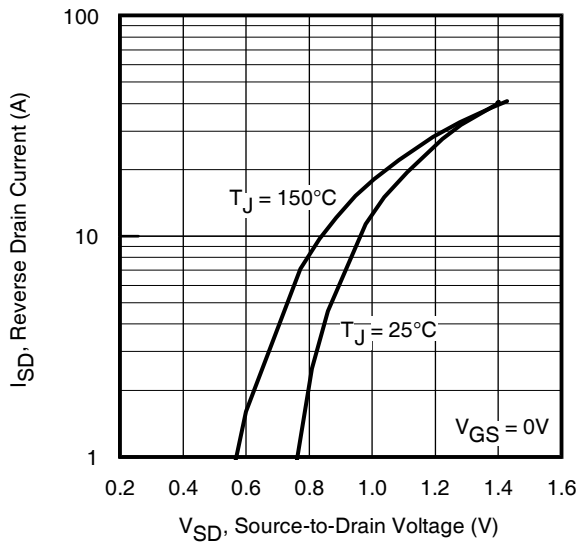
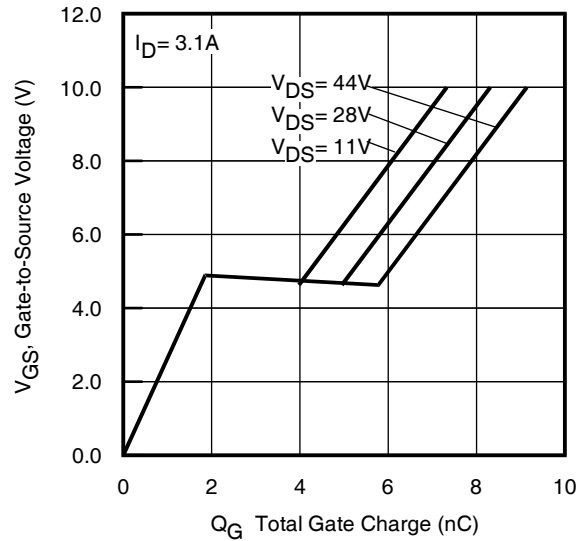
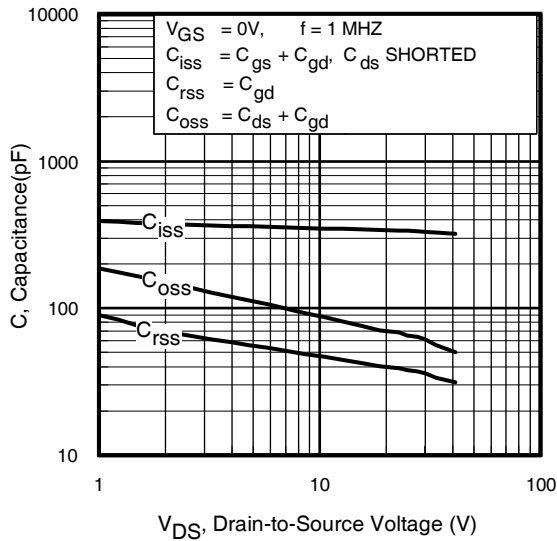


Fig 4. Typical Forward Transconductance vs. Drain Current



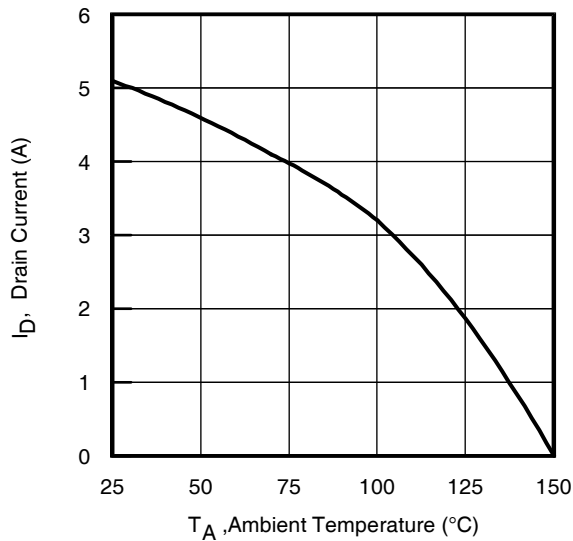


Fig 9. Maximum Drain Current vs. Ambient Temperature

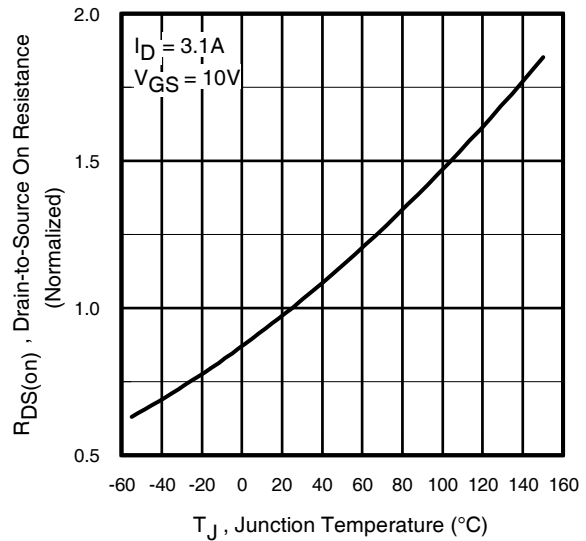


Fig 10. Normalized On-Resistance vs. Temperature

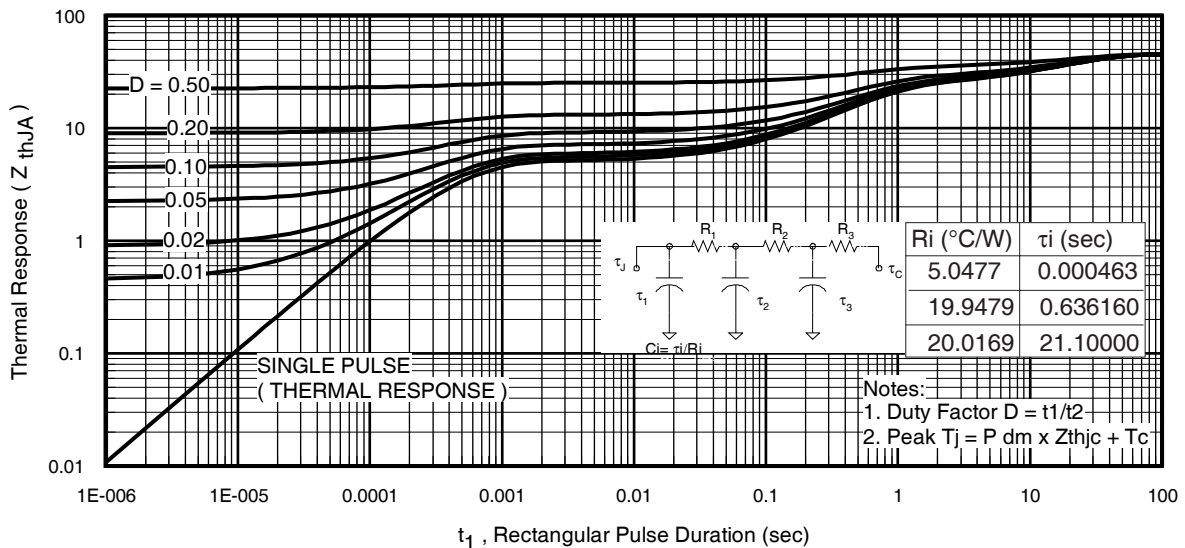


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

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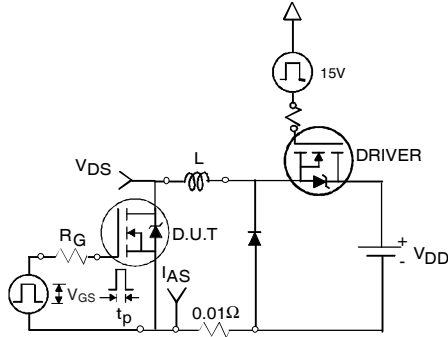


Fig 12a. Unclamped Inductive Test Circuit

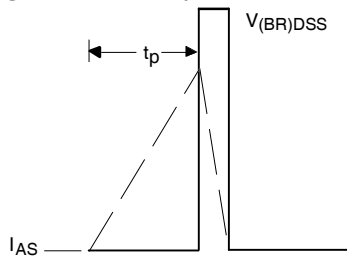


Fig 12b. Unclamped Inductive Waveforms

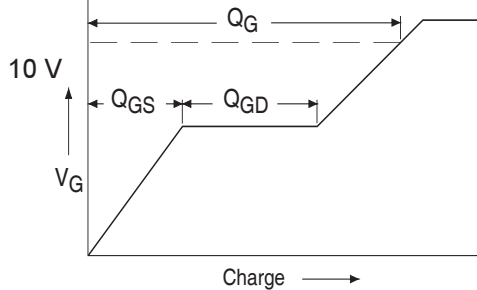


Fig 13a. Basic Gate Charge Waveform

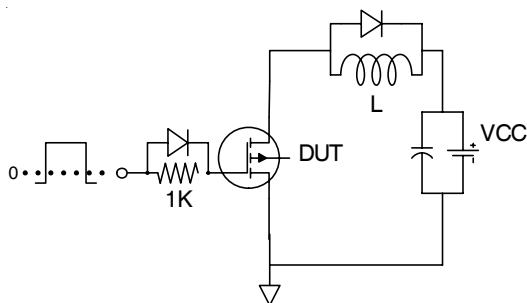


Fig 13b. Gate Charge Test Circuit

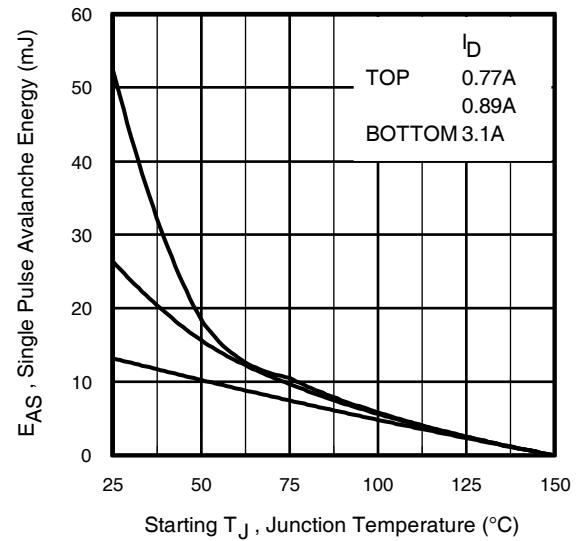


Fig 12c. Maximum Avalanche Energy vs. Drain Current

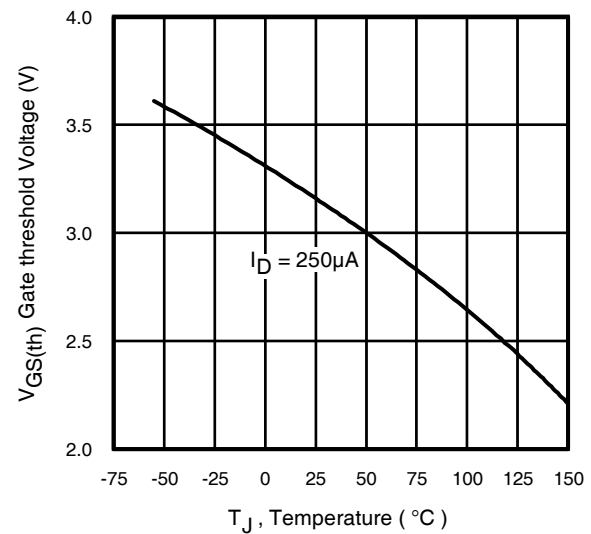


Fig 14. Threshold Voltage vs. Temperature

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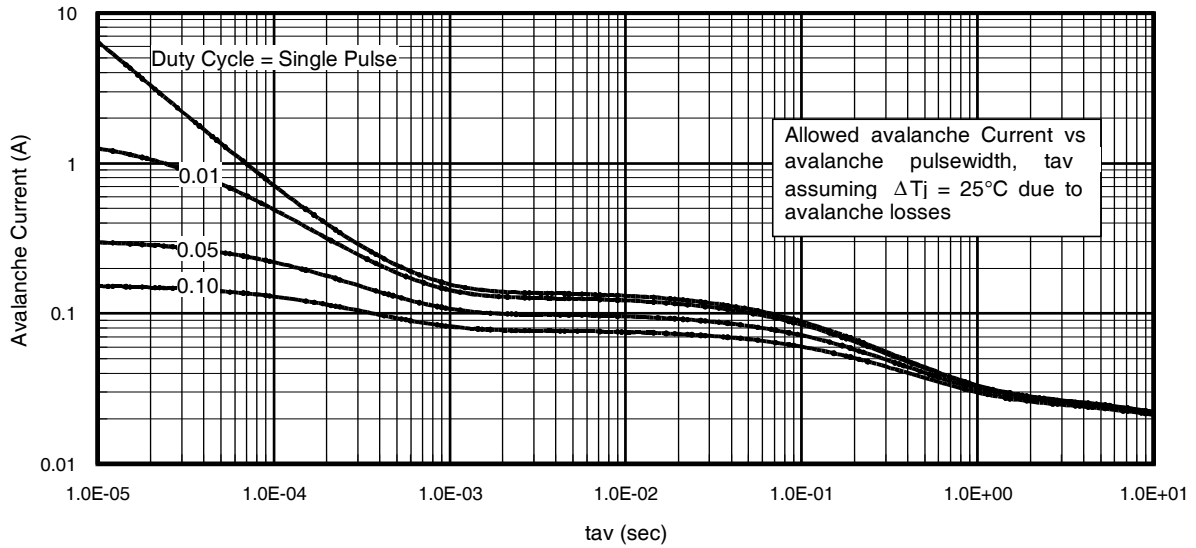


Fig 15. Typical Avalanche Current vs. Pulsewidth

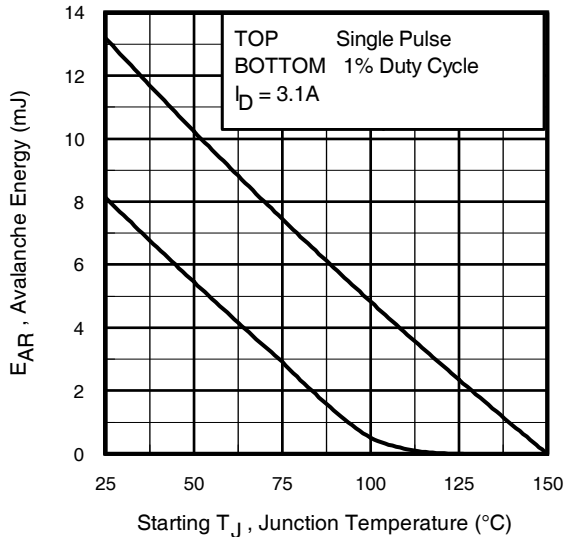


Fig 16. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

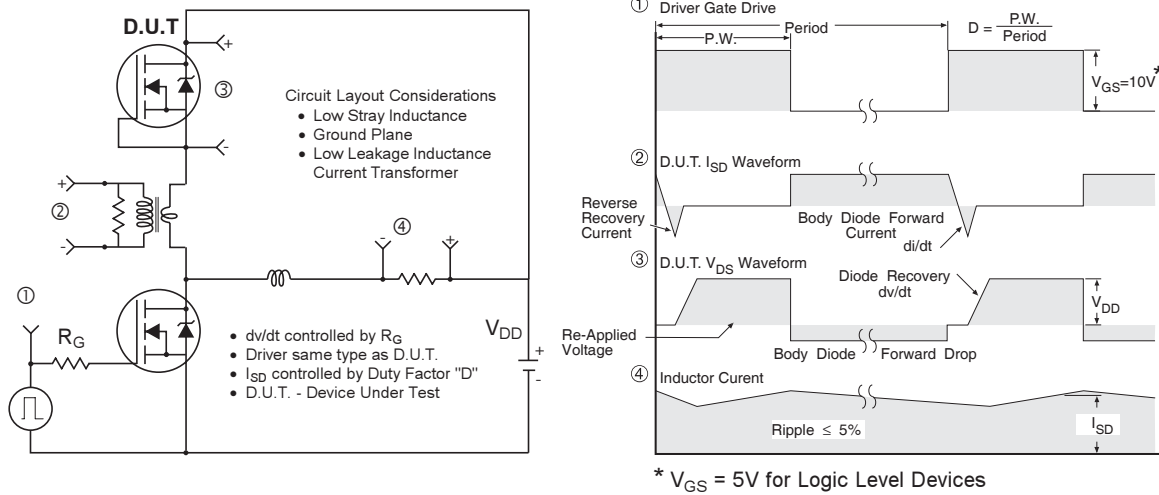


Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

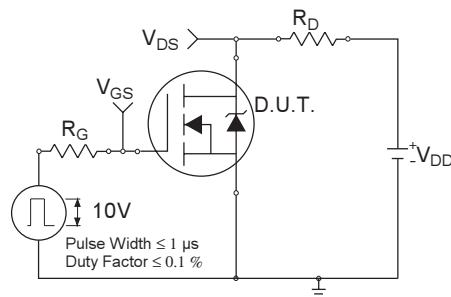


Fig 18a. Switching Time Test Circuit

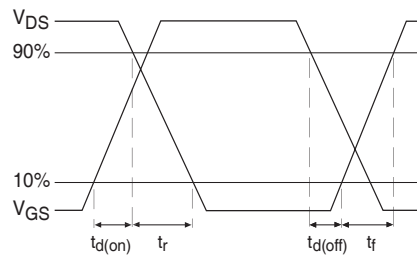
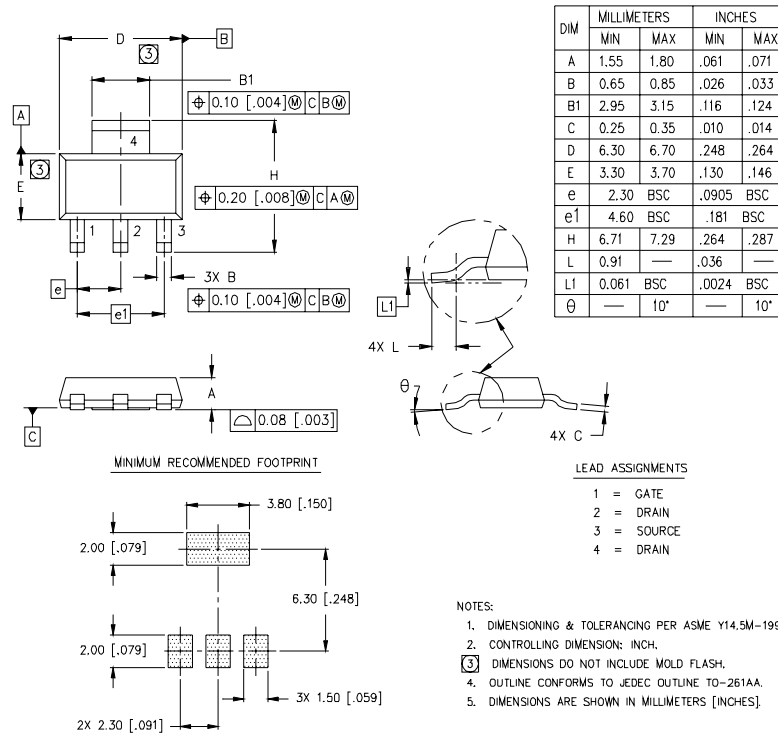


Fig 18b. Switching Time Waveforms

SOT-223 (TO-261AA) Package Outline

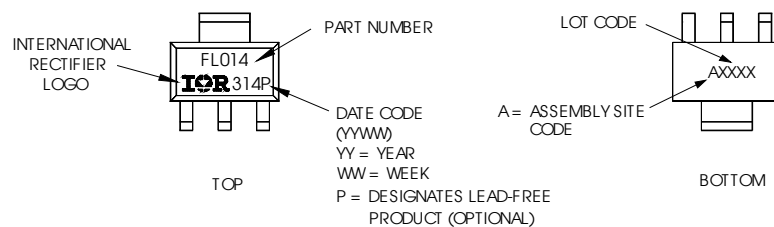
Dimensions are shown in millimeters (inches)



SOT-223 (TO-261AA) Part Marking Information

HEXFET PRODUCT MARKING

EXAMPLE: THIS IS AN IRFL014



Notes:

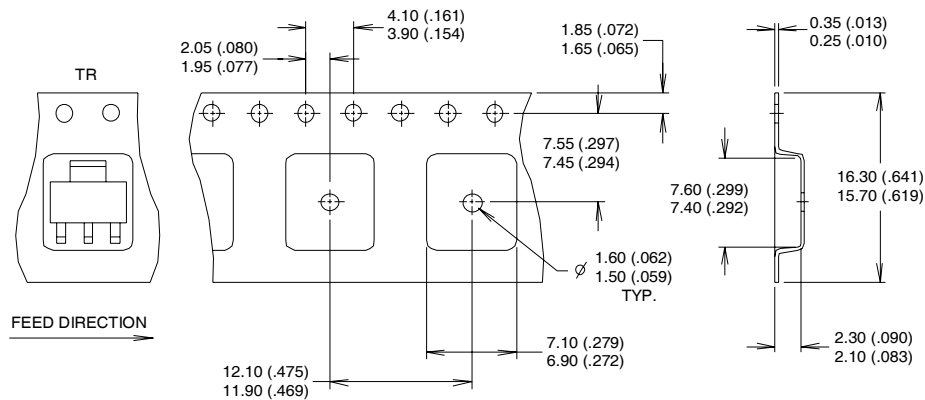
1. For an Automotive Qualified version of this part please see <http://www.irf.com/product-info/auto/>
2. For the most current drawing please refer to IR website at <http://www.irf.com/package/>

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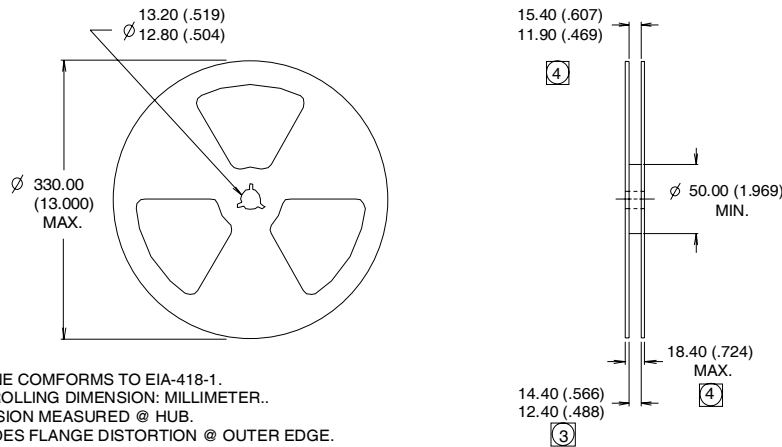
SOT-223 (TO-261AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONTROLLING DIMENSION: MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.
3. EACH Ø330.00 (13.00) REEL CONTAINS 2,500 DEVICES.



NOTES :

1. OUTLINE CONFORMS TO EIA-418-1.
2. CONTROLLING DIMENSION: MILLIMETER..
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Data and specifications subject to change without notice.
This product has been designed for the Industrial market.
Qualification Standards can be found on IR's Web site.

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