

SK8603140L

Silicon N-channel MOS FET

For Load-switching / For DC-DC Converter

■ Features

- Low Drain-source On-state Resistance : $R_{DS(on)}$ typ = $1.8 \text{ m}\Omega$ ($V_{GS} = 4.5 \text{ V}$)
- Halogen-free / RoHS compliant
(EU RoHS / UL-94 V-0 / MSL : Level 1 compliant)

■ Marking Symbol : 14

■ Packaging

Embossed type (Thermo-compression sealing) : 3 000 pcs / reel (standard)

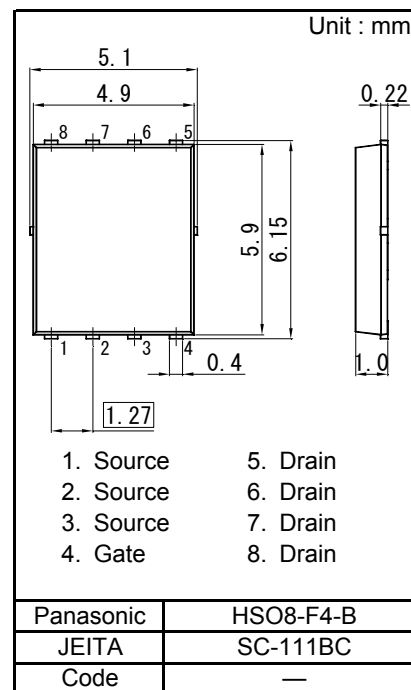
■ Absolute Maximum Ratings $T_a = 25 \text{ }^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Drain to Source Voltage	V_{DS}	30	V
Gate to Source Voltage	V_{GS}	± 20	
Drain Current	I_D	$T_a = 25 \text{ }^\circ\text{C}, t = 10 \text{ s}^{*1}$	A
		$T_a = 25 \text{ }^\circ\text{C}, \text{DC}^{*1}$	
		$T_c = 25 \text{ }^\circ\text{C}$	
		Pulsed, $T_{ch} < 150 \text{ }^\circ\text{C}^{*2}$	
Total Power Dissipation	PD	$T_a = 25 \text{ }^\circ\text{C}, \text{DC}^{*1}$	W
		$T_c = 25 \text{ }^\circ\text{C}$	
Thermal Resistance	Channel to Ambient	$R_{th(ch-a)}$	$^\circ\text{C} / \text{W}$
	Channel to Case	$R_{th(ch-c)}$	
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Operating ambient temperature	T_{opr}	-40 to +85	
Storage Temperature Range	T_{stg}	-55 to +150	
Avalanche Current (Single pulse) ^{*3}	IAR	23	A
Avalanche Energy (Single pulse) ^{*3}	EAR	61	mJ

Note *1 Device mounted on a glass-epoxy board in Figure 1

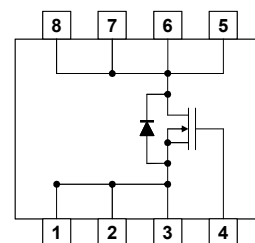
*2 Pulse test: Ensure that the channel temperature does not exceed $150 \text{ }^\circ\text{C}$

*3 $V_{DD} = 24 \text{ V}$, $V_{GS} = 10 \text{ to } 0 \text{ V}$, $L = 0.1 \text{ mH}$, $T_{ch} = 25 \text{ }^\circ\text{C}$ (initial)



- | | |
|-----------|----------|
| 1. Source | 5. Drain |
| 2. Source | 6. Drain |
| 3. Source | 7. Drain |
| 4. Gate | 8. Drain |

Internal Connection



Pin Name

- | | |
|-----------|----------|
| 1. Source | 5. Drain |
| 2. Source | 6. Drain |
| 3. Source | 7. Drain |
| 4. Gate | 8. Drain |

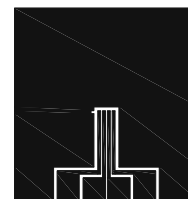


Figure 1 FR4 Glass-Epoxy Board
25.4 mm × 25.4 mm × 0.8 mm

■ Electrical Characteristics Ta = 25 °C ± 3 °C

Static Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source Breakdown Voltage	VDSS	ID = 1 mA, VGS = 0 V	30			V
Zero Gate Voltage Drain Current	IDSS	VDS = 30 V, VGS = 0 V			10	μA
Gate-source Leakage Current	IGSS	VGS = ±16 V, VDS = 0 V			±10	μA
Gate-source Threshold Voltage	Vth	ID = 5.85 mA, VDS = 10 V	1.3		3	V
Drain-source On-state Resistance	RDS(on)1	ID = 23 A, VGS = 10 V		1.6	2.2	mΩ
	RDS(on)2	ID = 23 A, VGS = 4.5 V		1.8	2.5	

Dynamic Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Capacitance	Ciss	VDS = 10 V, VGS = 0 V f = 1 MHz		4 900	6 860	pF
Output Capacitance	Coss			570	798	
Reverse Transfer Capacitance	Crss			410	656	
Turn-on Delay Time ^{*1}	td(on)	VDD = 15 V, VGS = 0 to 10 V		18		ns
Rise Time ^{*1}	tr	ID = 23 A		14		
Turn-off Delay Time ^{*1}	td(off)	VDD = 15 V, VGS = 10 to 0 V		75		ns
Fall Time ^{*1}	tf	ID = 23 A		11		
Total Gate Charge	Qg	VDD = 15 V, VGS = 0 to 4.5 V ID = 23 A		37		nC
Gate to Source Charge	Qgs			12		
Gate to Drain Charge	Qgd			14		
Gate resistance	rg	f = 5 MHz		1.2	3	Ω

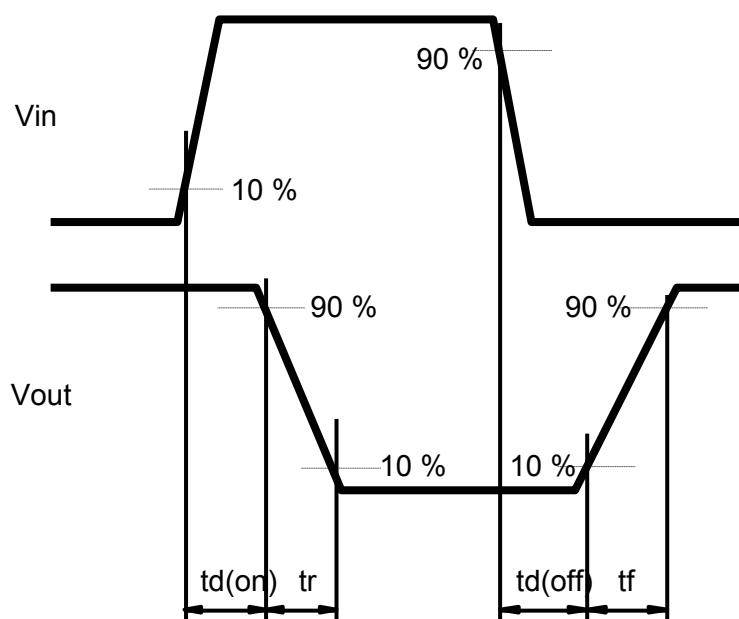
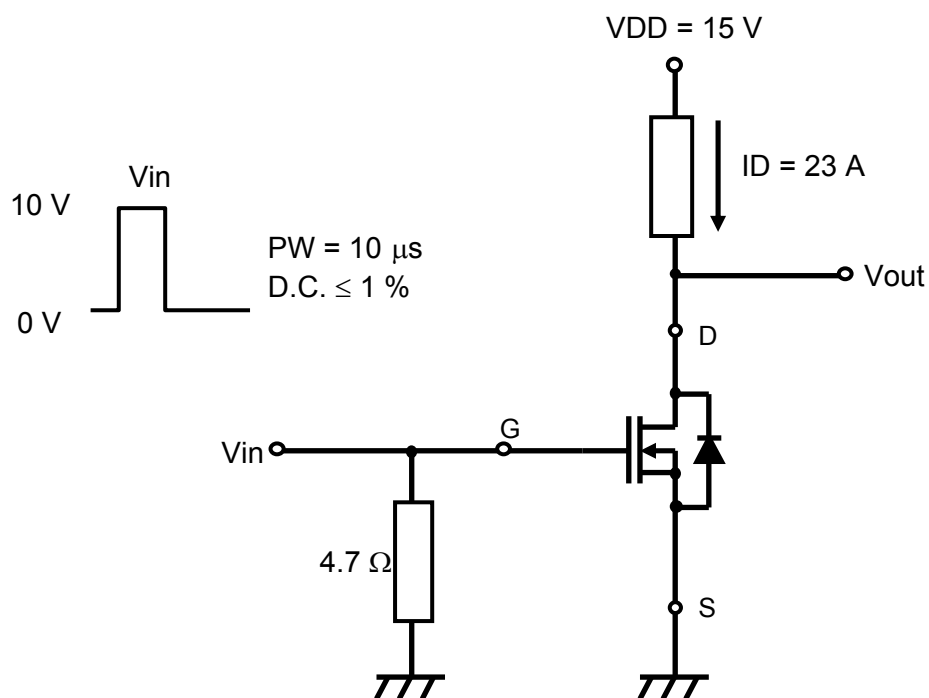
Body Diode Characteristic

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Diode Forward Voltage	VSD	IS = 23 A, VGS = 0 V		0.8	1.2	V

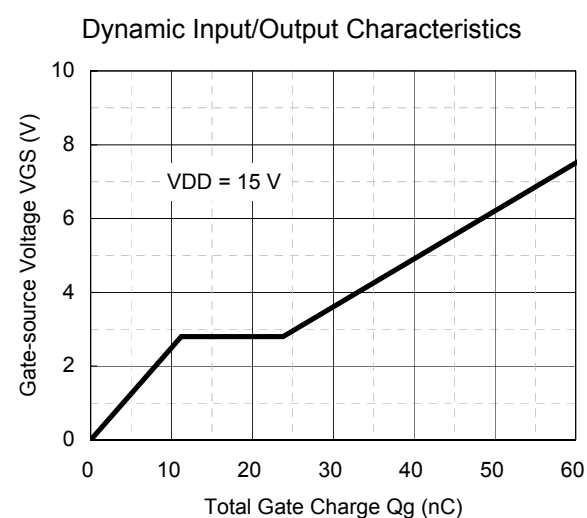
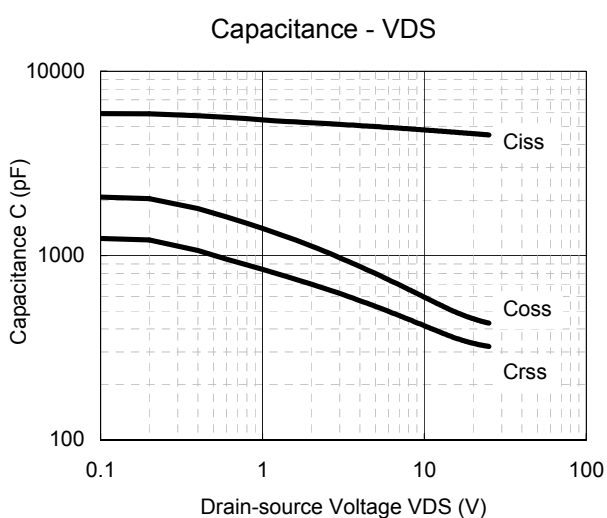
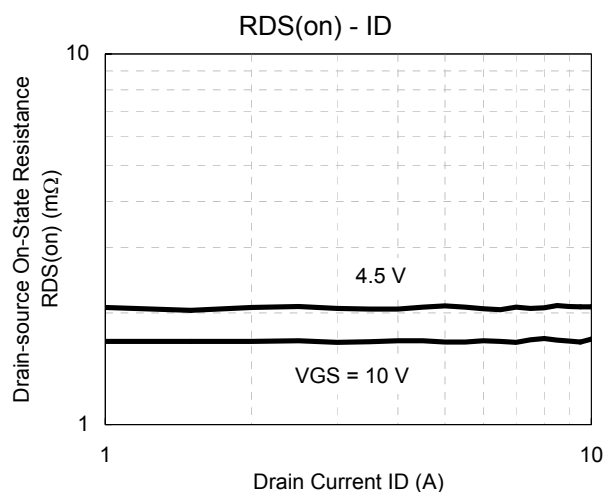
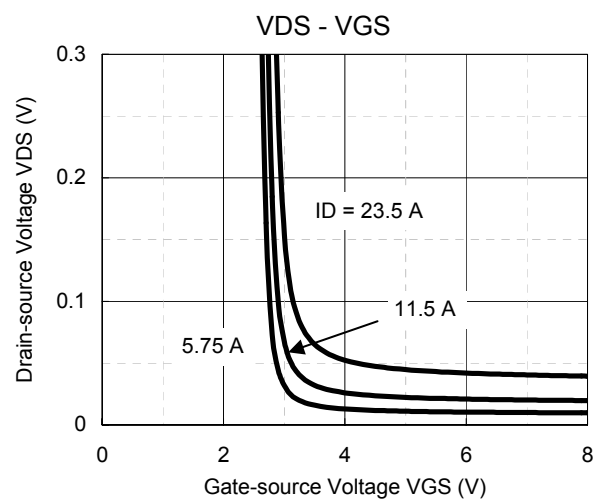
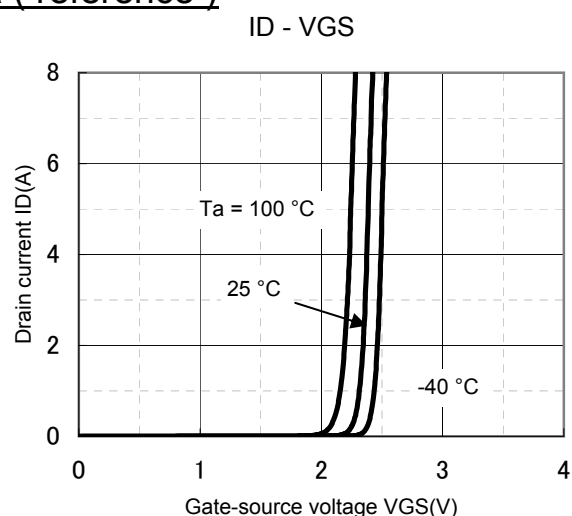
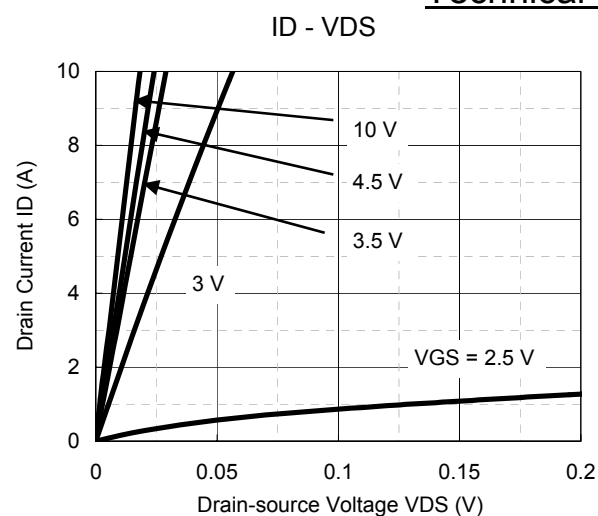
Note : 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

2. ^{*1} Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time

*1 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time

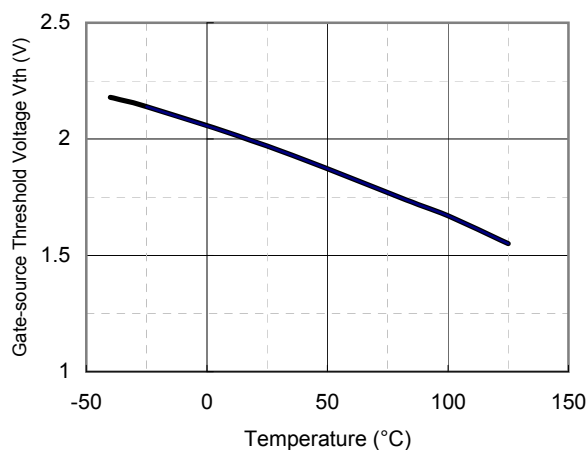


Technical Data (reference)

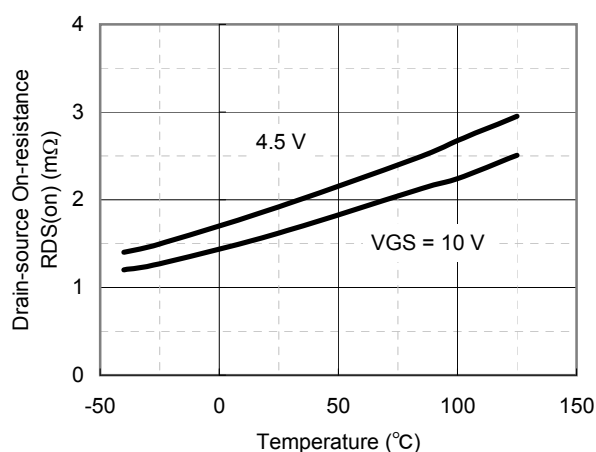


Technical Data (reference)

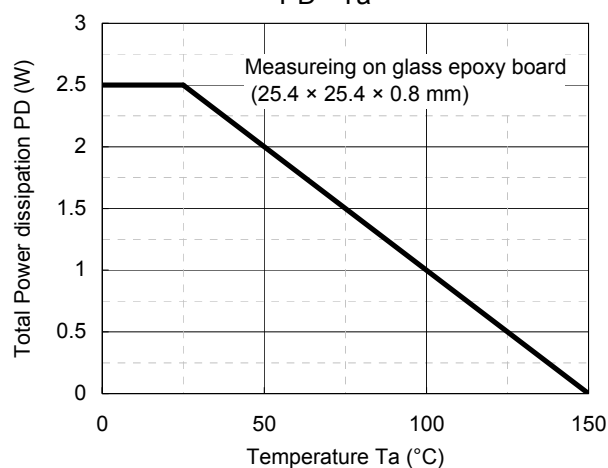
V_{th} - T_a



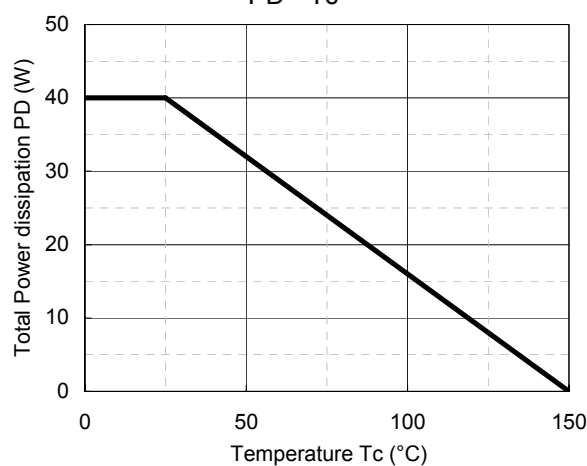
R_{DS(on)} - T_a



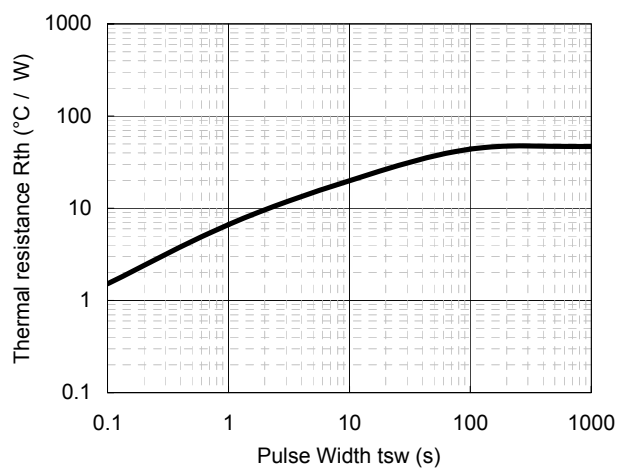
PD - T_a



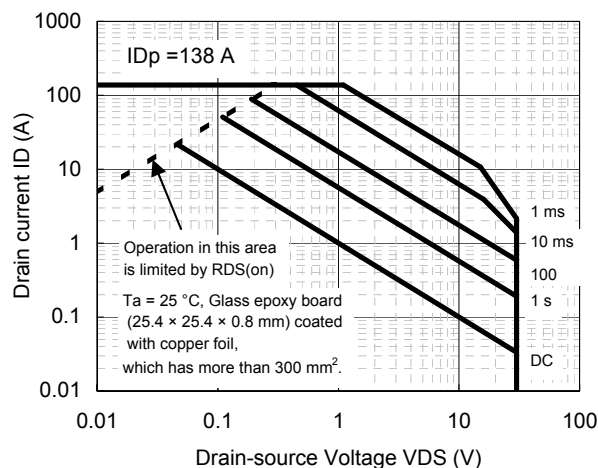
PD - T_c



R_{th} - t_{sw}



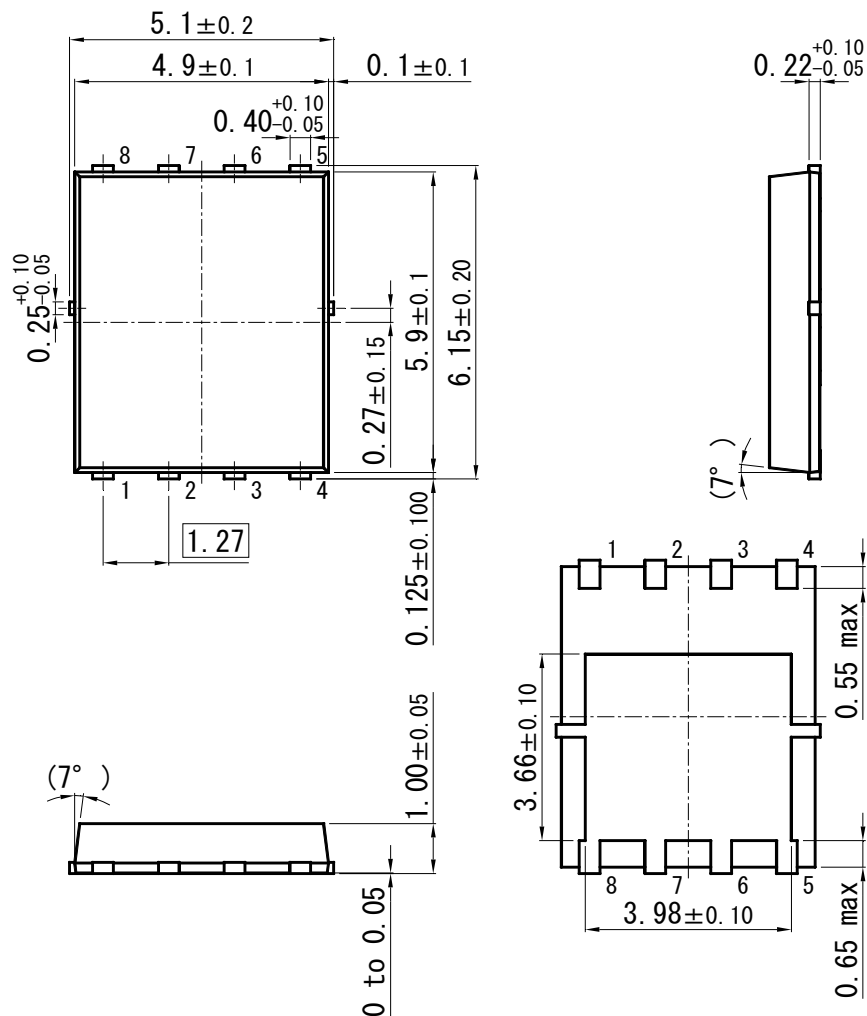
Safe Operating Area



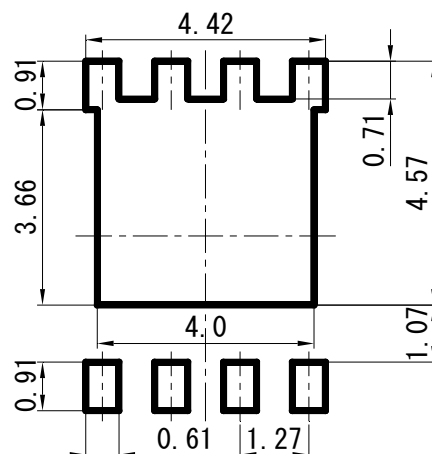
Panasonic

MOS FET
SK8603140L

HSO8-F4-B



■ Land Pattern (Reference) (Unit : mm)



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