2.4-GHz RF FRONT END

Check for Samples: CC2595

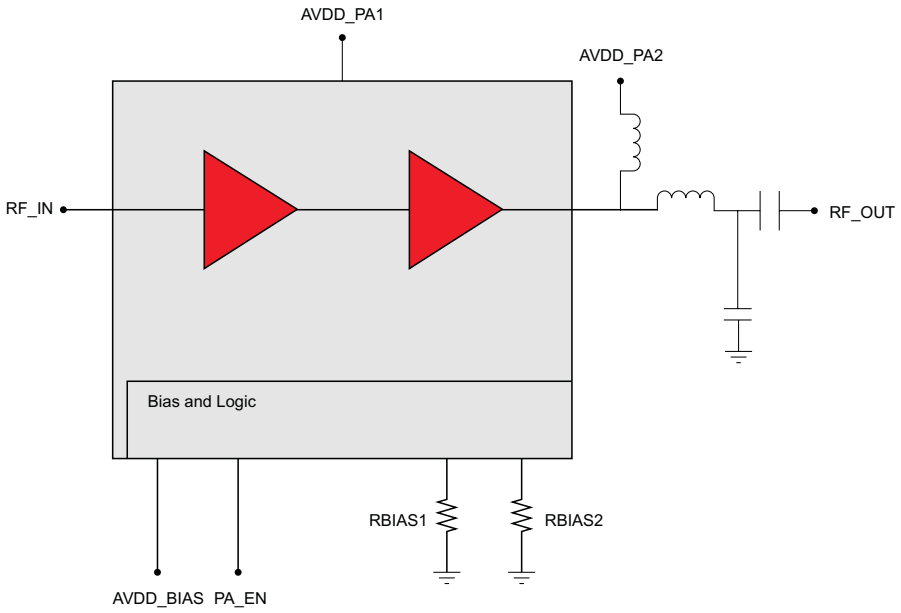
FEATURES

- **Low Cost and Small Package**
- **Very Few External Components**
- **2.0-V to 3.6-V Operation**
- **Less Than 1-µA Current Consumption in Power Down Mode**
- **Low Transmit Current Consumption**
- **98 mA at 3 V for +20.7 dBm Out (PAE = 40%)**
- **RoHS Compliant 3- x 3-mm QFN-16 Package**

DESCRIPTION

CC2595 is a PA solution that extends the range of any Zigbee or Bluetooth transceiver. It is a cost-effective and high performance RF front end for low-power and low-voltage wireless applications in the 2.4-GHz band. Its single-ended RF input and output make it compatible with any manufacturer's transceiver if appropriate external parts are used. When a transmit/receive (T/R) switch and a balun are used, it can interface with existing and future CC24XX and CC25XX transceiver products. CC2595 extends the link budget by providing a power amplifier for improved output power. It is highly effective for high (+20 dBm) output power making it suitable for battery-operated systems. CC2595 contains PA and RF-matching for simple design of high performance wireless applications. It is packaged in a 3- x 3-mm, 16-lead QFN package with exposed paddle.

FUNCTIONAL BLOCK DIAGRAM



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN ASSIGNMENTS

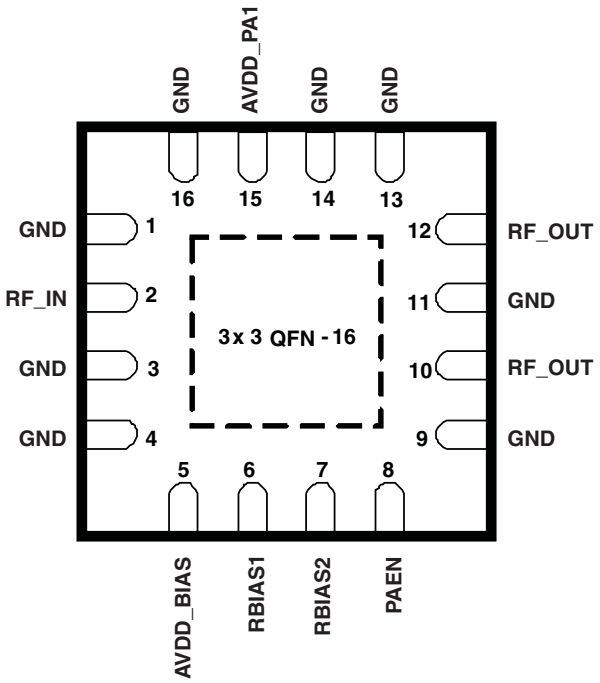


Figure 1. CC2595 Pinout

Table 1. Pin Descriptions for CC2595

PIN NO.	PIN NAME	TYPE	DESCRIPTION
1	GND	GND	
2	RF_IN	RF in/out	RF single-ended input
3	GND	GND	
4	GND	GND	
5	AVDD_BIAS	Power	Supply voltage, analog and logic
6	RBIAS1	Analog	Bias set resistor, stage 1
7	RBIAS2	Analog	Bias set resistor, stage 2
8	PAEN	Digital in	Chip enable: high = PA on
9	GND	GND	
10	RF_OUT	RF in/out	RF single-ended output (1 of 2)
11	GND	GND	
12	RF_OUT	RF in/out	RF single-ended output (2 of 2)
13	GND	GND	
14	GND	GND	
15	AVDD_PA1	Power	Supply voltage, PA stage 1
16	GND	GND	

Table 2. ORDERING INFORMATION(1)

T_A	PACKAGE(2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40ºC to 85ºC	RGT (QFN)	CC2595RGTR	C2595

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

				VALUE	UNIT
	Supply voltage range			-0.3 to 3.6	V
	Voltage on any digital pin			-0.3 to V_{DD} + 0.3, max 3.6	V
	RF input power RF_IN			+10	dBm
T_{STG}	Storage temperature range			–50 to 150	°C
T_J	Junction temperature			150	°C
	ESD	RF pins	HBM (Human Body Model)	1500	V
		Excluding RF pins		2000	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
	Operating supply voltage	2		3.6	V
T_A	Operating free air temperature range	–40		85	°C

ELECTRICAL CHARACTERISTICS

T_J = 25°C, V_{DD} = 3 V (unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current consumption	No input signal		30		mA
Power down current	EN = LOW			1	µA
High input level (control pin)		1.3		V_{DD}	V
Low input level (control pin)				0.3	V
Power down → Transmit	Time from EN goes HIGH to settled in TX			1	µs

RF CHARACTERISTICS

T_J = 25°C, V_{DD} = 3 V (unless otherwise specified)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
f	Frequency range of operation			2400		2483.5	MHz
P_{OUT}	Output power		Pin = 0 dBm	+20	+20.7		dBm
PAE	Power added efficiency		Pin = 0 dBm		40		%
P_{OUTHI}	Output power (high)		V_{DD} = 3.3 V, Pin = +3 dBm	+22	+22.5		dBm
PAE_{HI}	Power added efficiency (high)		V_{DD} = 3.3 V, Pin = +3 dBm		45		%
P_{1dB}	Output 1-dB compression point				+17		dBm
IRL	Input return loss			10	15		dB
ORL	Output return loss			8	10		dB
	Output power variation over frequency		2400 MHz to 2483.5 MHz		0.5		dB
	Output power variation over supply voltage		2 V to 3.6 V		4		dB
	Output power variation over temperature		-40°C to 85°C		1		dB
	Harmonics	2nd harmonic	The harmonics can be further reduced by using an external LC filter and antenna.	Compliant with international regulatory standards			
		3rd harmonic		Compliant with international regulatory standards			
K	Stability			Unconditionally stable			
	Load mismatch		No damage at 10:1 VSWR condition; all phases				

TYPICAL CHARACTERISTICS

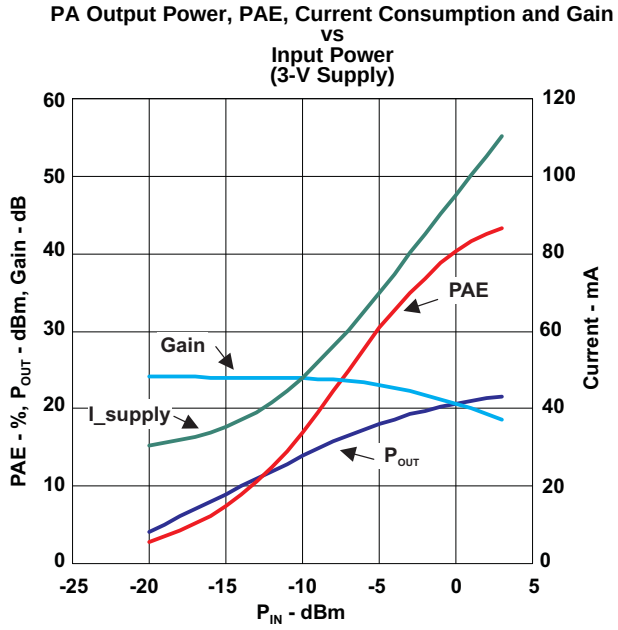


Figure 2.

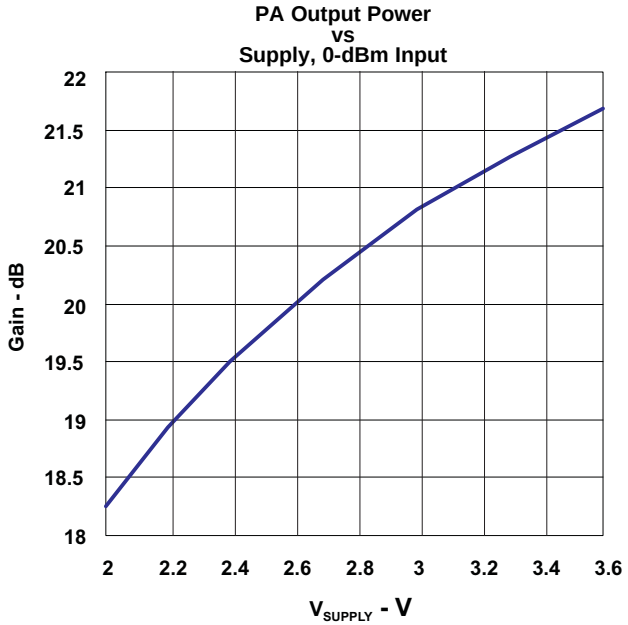


Figure 3.

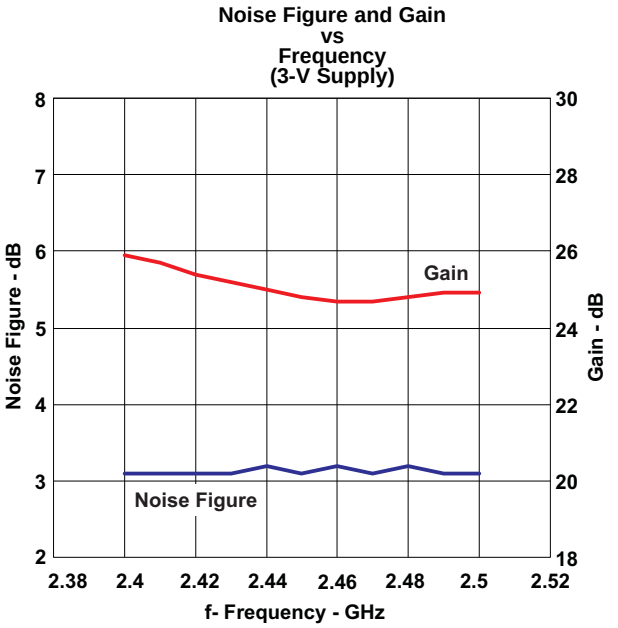


Figure 4.

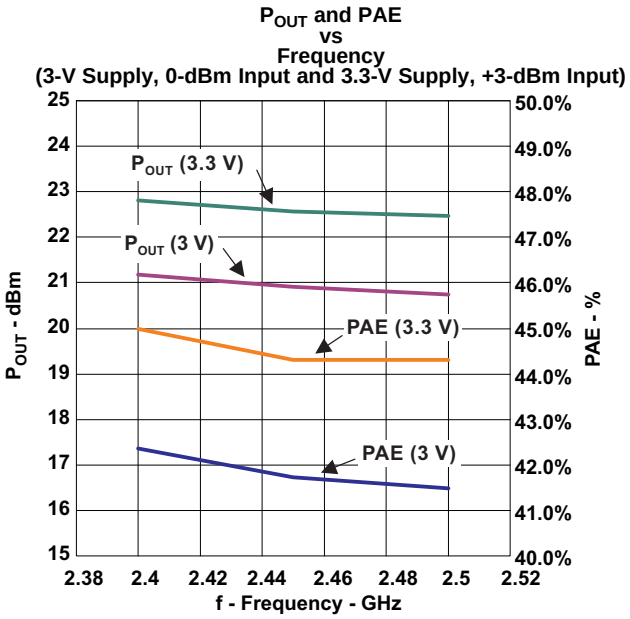


Figure 5.

TYPICAL CHARACTERISTICS (continued)

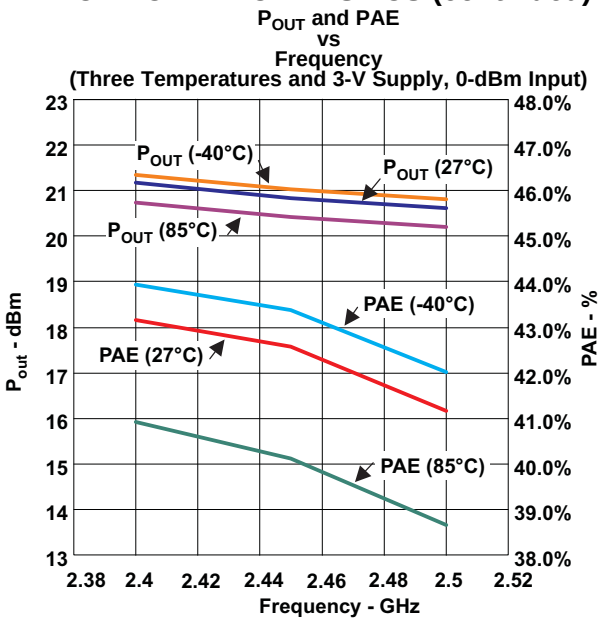


Figure 6.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CC2595RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	C2595	Samples
CC2595RGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	C2595	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

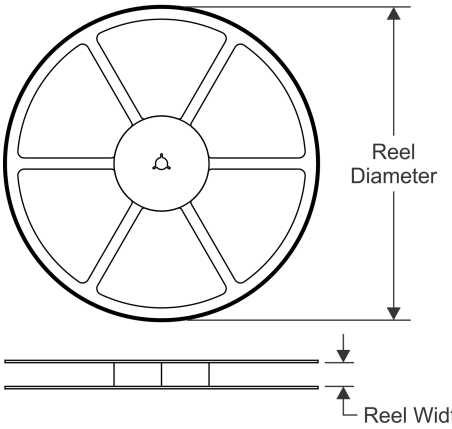
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

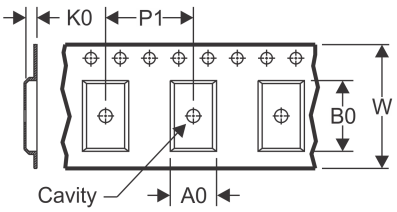
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

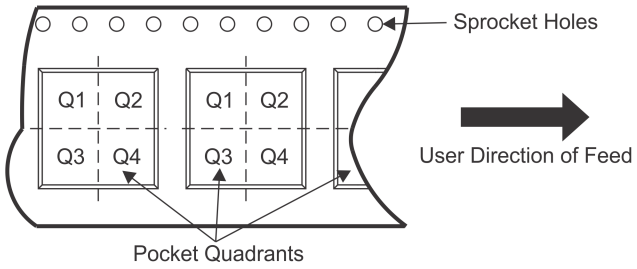


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

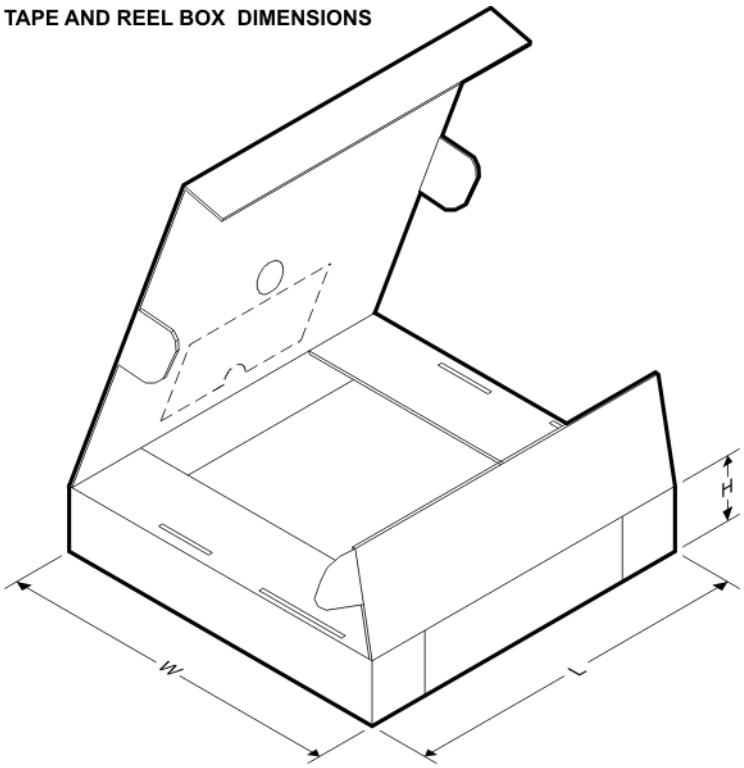
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CC2595RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
CC2595RGTT	QFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

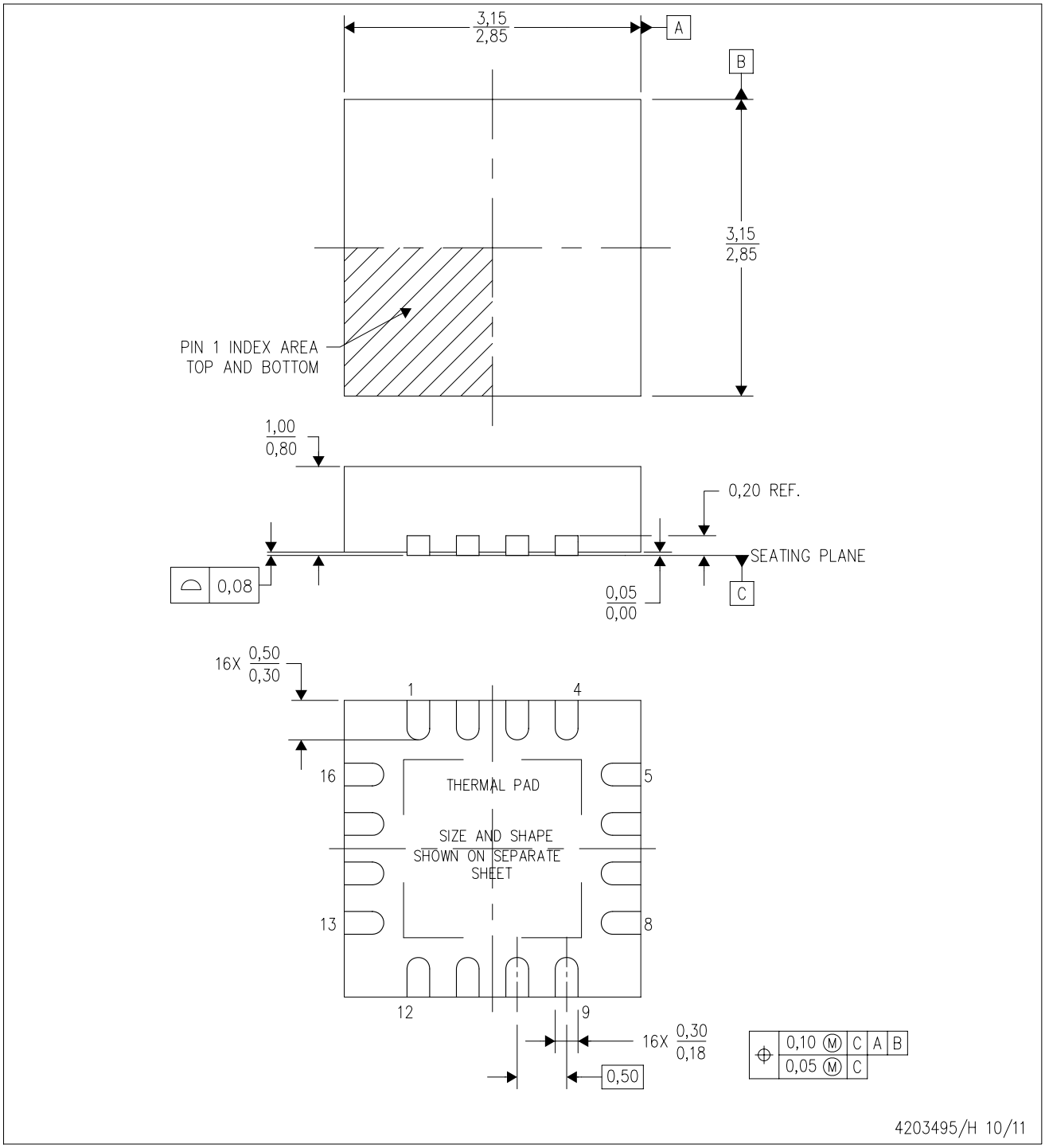
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CC2595RGTR	QFN	RGT	16	3000	338.1	338.1	20.6
CC2595RGTT	QFN	RGT	16	250	210.0	185.0	35.0

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

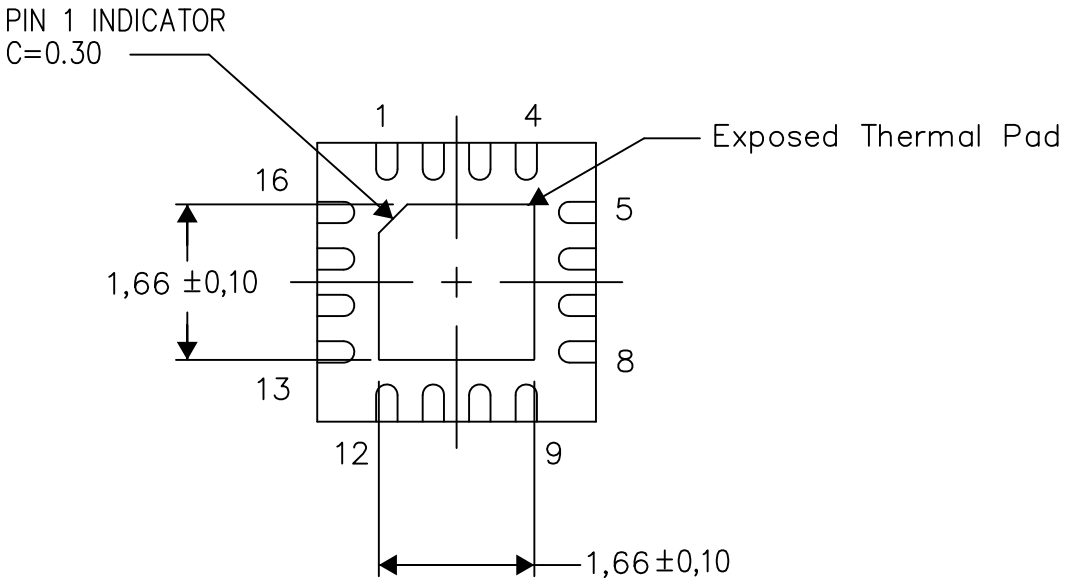
RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206349–10/W 10/14

NOTE: All linear dimensions are in millimeters

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