Data Sheet | October 7, 2008 | FN6288.5

Single-Phase Buck PWM Controller with Integrated High Speed MOSFET Driver and Pre-Biased Load Capability

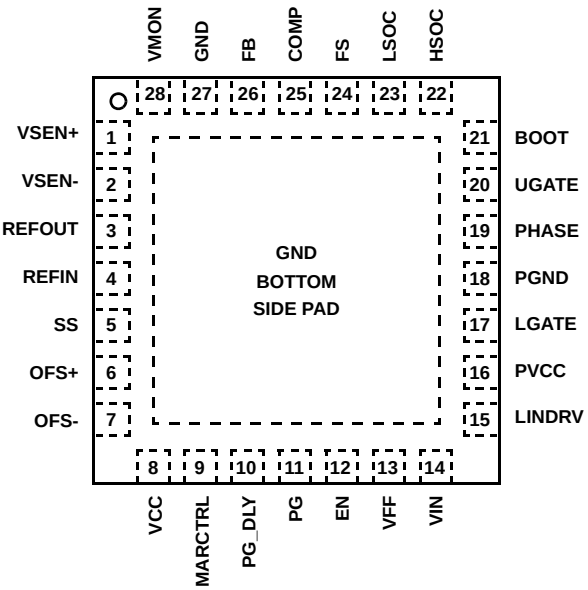
The ISL6540A is an improved version of the ISL6540 single-phase voltage-mode PWM controller with input voltage feed-forward compensation to maintain a constant loop gain for optimal transient response, especially for applications with a wide input voltage range. Its integrated high speed synchronous rectified MOSFET drivers and other sophisticated features provide complete control and protection for a DC/DC converter with minimum external components, resulting in minimum cost and less engineering design efforts.

The output voltage of the converter can be precisely regulated with an internal reference voltage of 0.591V, and has an improved system tolerance of ±0.68% over commercial temperature and line load variations. An external voltage can be used in place of the internal reference for voltage tracking/DDR applications.

The ISL6540A has an internal linear regulator or external linear regulator drive options for applications with only a single supply rail. The internal oscillator is adjustable from 250kHz to 2MHz. The integrated voltage margining, programmable pre-biased soft-start, differential remote sensing amplifier, and programmable input voltage POR features enhance the ISL6540A value.

Pinout

ISL6540A
(28 LD 5x5 QFN)
TOP VIEW



Features

- VIN and Power Rail Operation from +3.3V to +20V
- Fast Transient Response - 0 to 100% Duty Cycle
  - 15MHz Bandwidth Error Amplifier with 6V/µs Slew Rate
  - Voltage-Mode PWM Leading and Trailing-Edge Modulation Control
  - Input Voltage Feedforward Compensation
- 2.9V to 5.5V High Speed 2A/4A MOSFET Gate Drivers
  - Tri-state for Power Stage Shutdown
- Internal Linear Regulator (LR) - 5.5V Bias from VIN
- External LR Drive for Optimal Thermal Performance
- Voltage Margining with Independently Adjustable Upper and Lower Settings for System Stress Testing and Over Clocking
- Reference Voltage I/O for DDR/Tracking Applications
- Improved 0.591V Internal Reference with Buffered Output
  - ±0.68%/±1.0% Over Commercial/Industrial Range
- Source and Sink Overcurrent Protections
  - Low-and High-Side MOSFET $r_{DS(ON)}$ Sensing
- Overvoltage and Undervoltage Protections
- Small Converter Size - QFN package
- Oscillator Programmable from 250kHz to 2MHz
- Differential Remote Voltage Sensing with Unity Gain
- Programmable Soft-Start with Pre-Biased Load Capability
- Power-Good Indication with Programmable Delay
- EN Input with Voltage Monitoring Capability
- Pb-Free (RoHS Compliant)

Applications

- Power Supply for some Microprocessors and GPUs
- Wide and Narrow Input Voltage Range Buck Regulators
- Point of Load Applications
- Low-Voltage and High Current Distributed Power Supplies

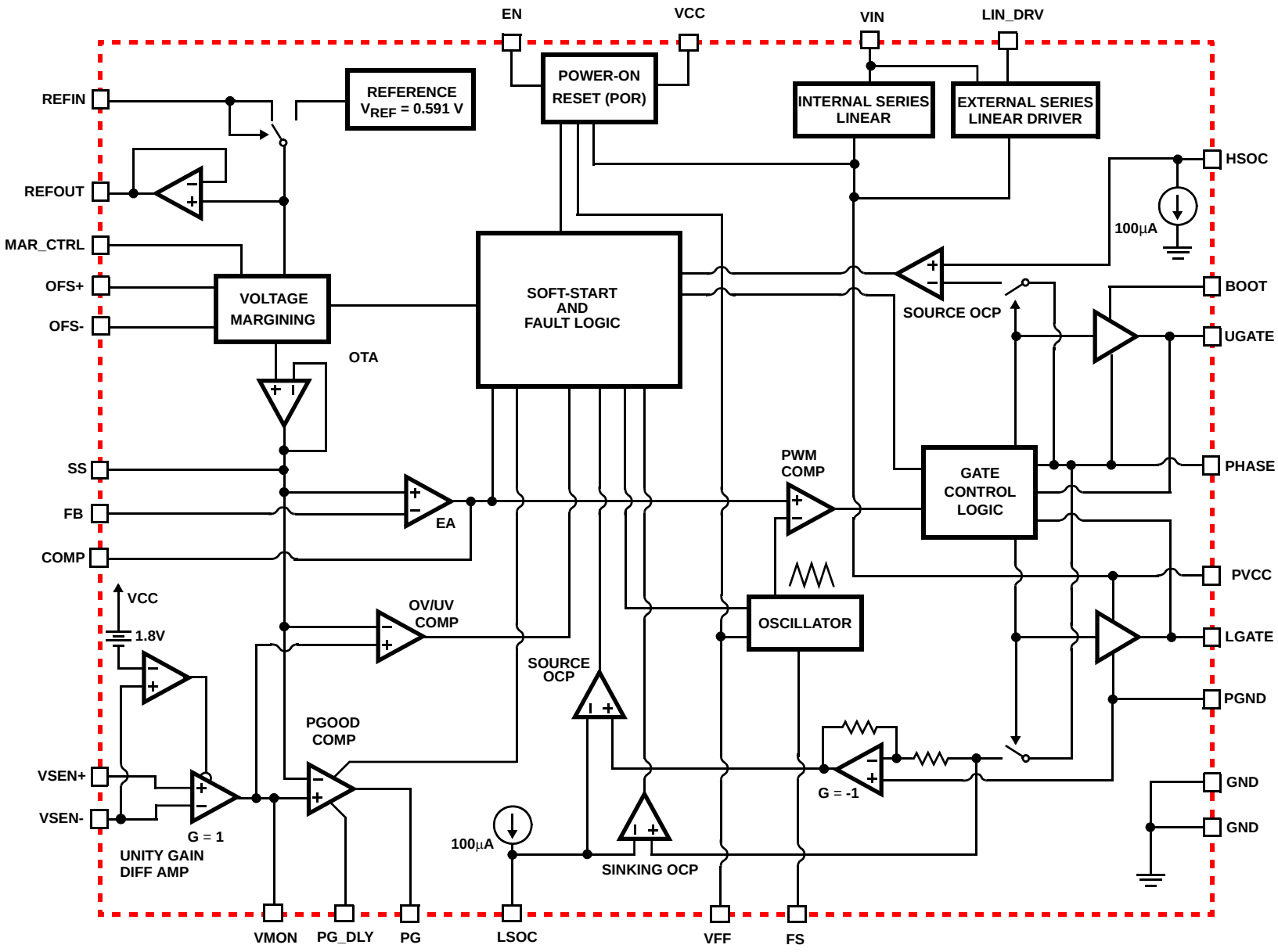
Ordering Information

PART NUMBER* (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL6540ACRZ*	ISL6540 ACRZ	0 to +70	28 Ld 5x5 QFN	L28.5x5
ISL6540AIRZ*	ISL6540 AIRZ	-40 to +85	28 Ld 5x5 QFN	L28.5x5
ISL6540AIRZA*	ISL6540 AIRZ	-40 to +85	28 Ld 5x5 QFN	L28.5x5

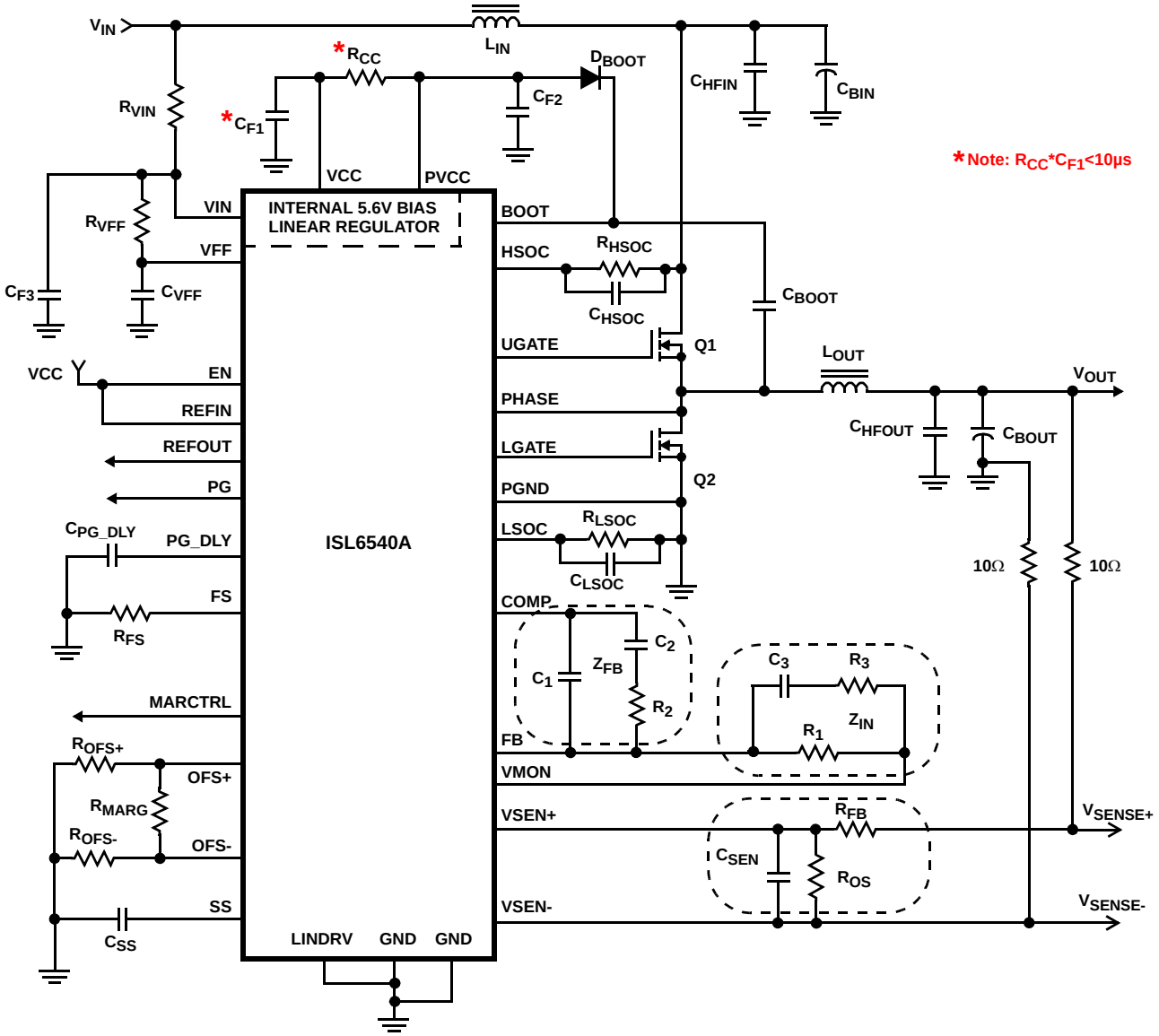
*Add “-T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

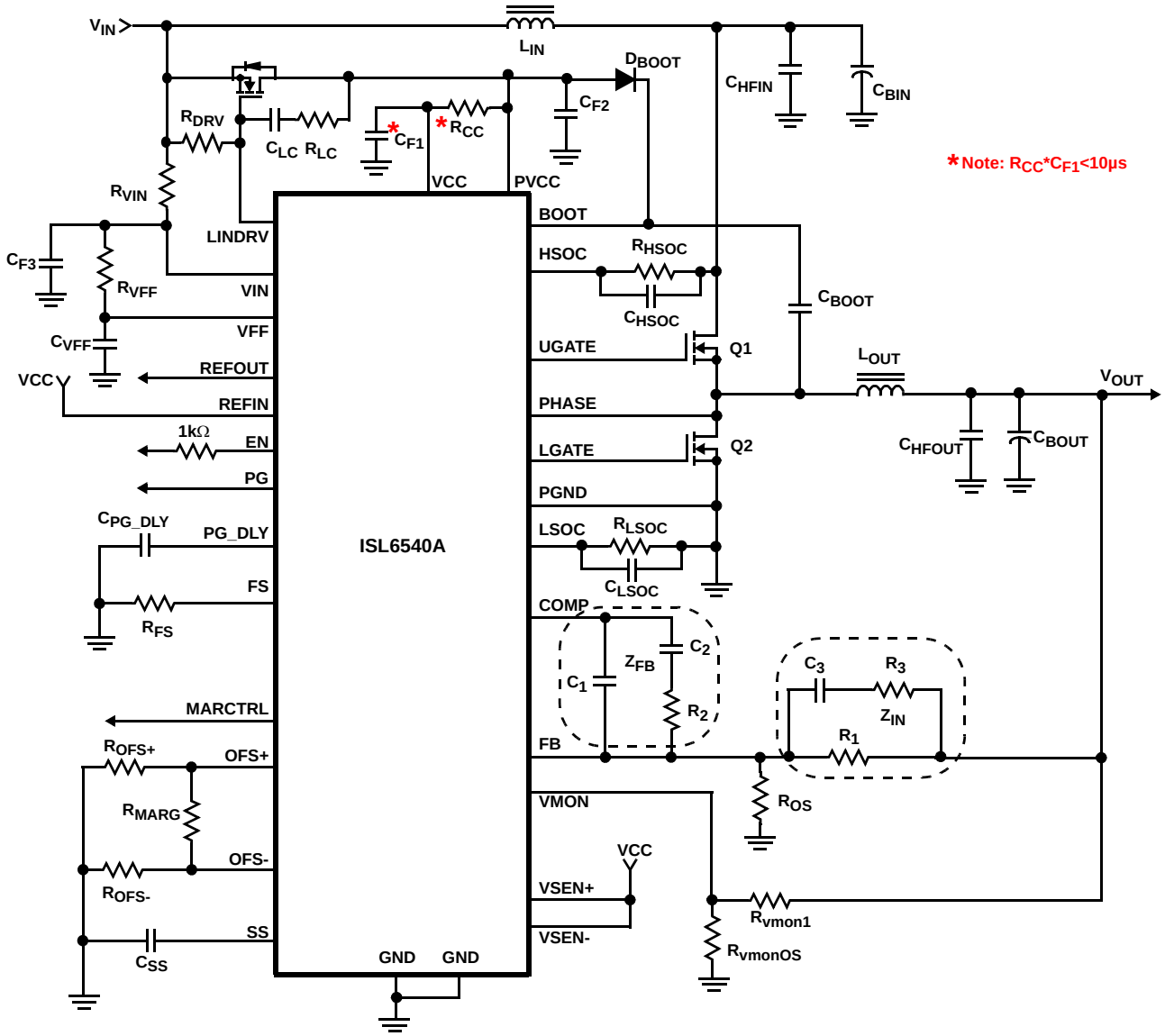
Block Diagram



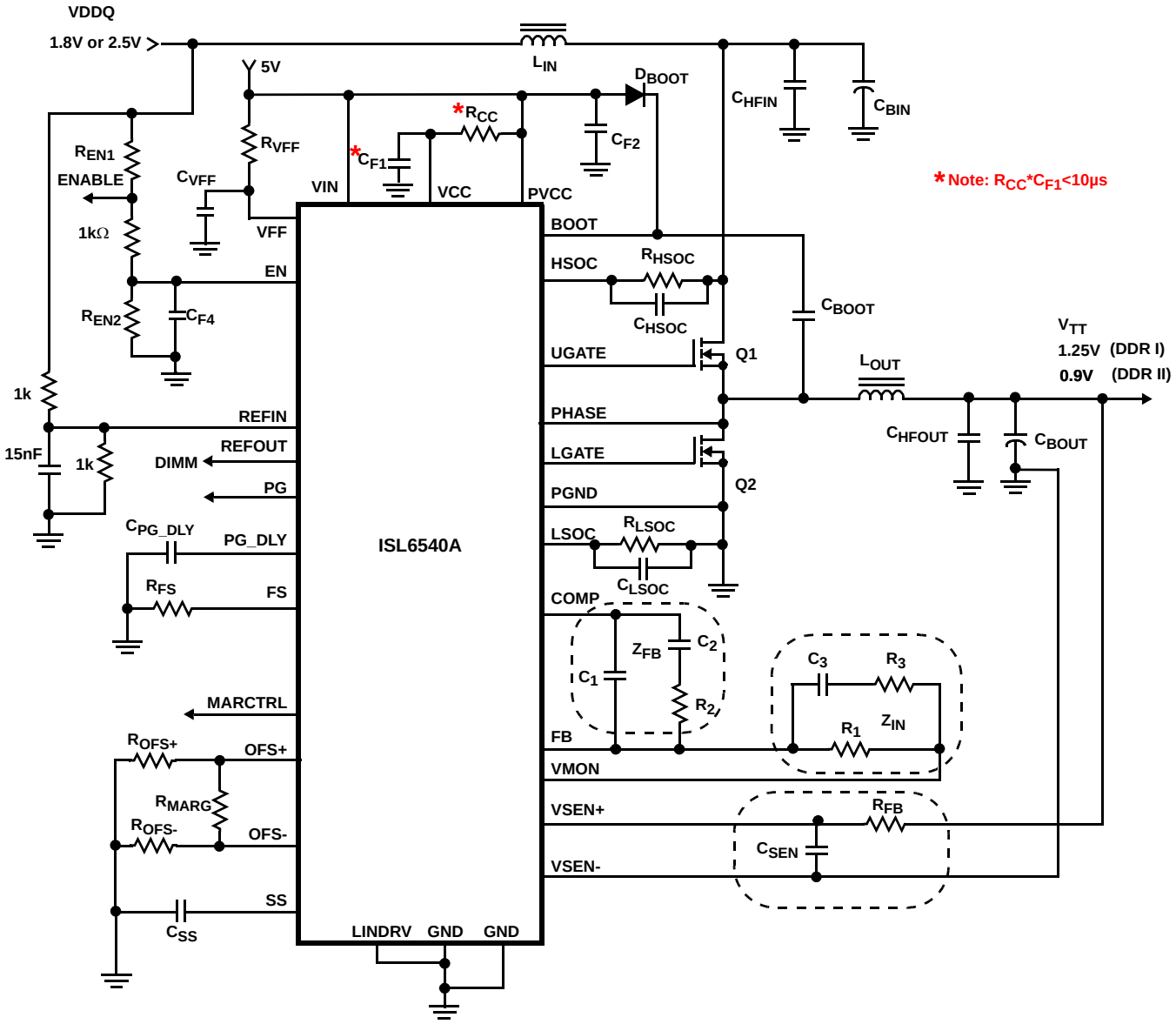
Typical Application I (Internal Linear Regulator with Remote Sense)



Typical Application II (External Linear Regulator without Remote Sense)



Typical Application III (Dual Data Rate I or II)



Absolute Maximum Ratings

Input Voltage, VIN, VFF, HSOC . . . . . -0.3V to +22.0V
Driver Bias Voltage, PVCC . . . . . -0.3V to +6.5V
Signal Bias Voltage, VCC . . . . . -0.3V to +6.5V
BOOT Voltage, V_{BOOT} . . . . . -0.3 to +36V
BOOT to PHASE Voltage (V_{BOOT}-V_{PHASE}) . . . . . -0.3V to 7V (DC)
. . . . . -0.3V to 9V (<10ns)
PHASE Voltage, V_{PHASE} . . . . . V_{BOOT} - 7V to V_{BOOT} + 0.3V
. . . . . V_{BOOT} - 9V (<10ns) to V_{BOOT} + 0.3V
UGATE Voltage . . . . . V_{PHASE} - 0.3V (DC) to V_{BOOT}
V_{PHASE} - 5V (<20ns Pulse Width, 10µJ) to V_{BOOT}
LGATE Voltage . . . . . GND - 0.3V (DC) to VCC + 0.3V
GND - 2.5V (<20ns Pulse Width, 5µJ) to VCC + 0.3V
Other Input or Output Voltages . . . . . -0.3V to VCC +0.3V

Thermal Information

Thermal Resistance (Notes 1, 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package	32	5

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Input Voltage, VIN, VFF . . . . . 3.3V to 20V ±10%
Driver Bias Voltage, PVCC . . . . . 2.9V to 5.5V
Signal Bias Voltage, VCC . . . . . 2.9V to 5.5V
Boot to Phase Voltage (Overcharged), V_{BOOT} - V_{PHASE} . . . . . <6V
Ambient Temperature Range . . . . . -40°C to +85°C
Junction Temperature Range . . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features.
2. θ_{JC}, "case temperature" location is at the center of the package underside exposed pad. See Tech Brief TB379 for details.
3. Limits should be considered typical and are not production tested.

Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Noted. Parts are 100% tested at +25°C. Temperature limits established by characterization and are not production tested.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY CURRENTS						
I_{VCC}	Nominal VCC Supply Current	VIN = VCC = PVCC = 5V, Fs = 600kHz, UGATE and LGATE Open	-	8	13	mA
I_{PVCC}	Nominal PVCC Supply Current	VIN = VCC = PVCC = 5V; Fs = 600kHz, UGATE and LGATE Open	-	3	4	mA
I_{VIN}	Nominal VIN Supply Current	VIN = VCC = PVCC = 5V; Fs = 600kHz, UGATE and LGATE Open	-	0.5	1	mA
I_{VCC_S}	Shutdown VCC Supply Current	EN = 0V, VCC = PVCC = VIN = 5V	-	3	4	mA
I_{PVCC_S}	Shutdown PVCC Supply Current	EN = 0V, VCC = PVCC = VIN = 5V	-	1	2	mA
I_{VIN_S}	Shutdown VIN Supply Current	EN = 0V, VCC = PVCC = VIN = 5V	-	0.5	1	mA
POWER-ON RESET						
POR_{VCC_R}	Rising VCC Threshold		2.79	-	2.89	V
POR_{VCC_F}	Falling VCC Threshold		2.59	-	2.69	V
POR_{VCC_H}	VCC Hysterisis		187	215	250	mV
POR_{PVCC_R}	Rising PVCC Threshold		2.79	-	2.91	V
POR_{PVCC_F}	Falling PVCC Threshold		2.59	-	2.70	V
POR_{PVCC_H}	PVCC Hysterisis		193	215	250	mV
POR_{VFF_R}	Rising VFF Threshold		1.48	-	1.54	V
POR_{VFF_F}	Falling VFF Threshold		1.35	-	1.41	V
POR_{VFF_H}	VFF Hysterisis		127	137	146	mV
ENABLE						
V_{EN_REF}	Input Reference Voltage		0.485	0.500	0.515	V
I_{EN_HYS}	Hysteresis Source Current		7.5	10	11.5	µA
V_{EN}	Maximum Input Voltage		-	VCC + 0.3	-	V

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted. Parts are 100% tested at +25°C. Temperature limits established by characterization and are not production tested. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OSCILLATOR						
OSC_{FMAX}	Nominal Maximum Frequency	(Note 3)	-	2000	-	kHz
OSC_{FMIN}	Nominal Minimum Frequency	(Note 3)	-	250	-	kHz
ΔOSC	Total Variation	FS = 250kHz to 2MHz, VFF = 3.3V to 20V	-17	-	+17	%
ΔV_{OSC}	Ramp Amplitude		-	0.16*VFF	-	V_{P-P}
V_{OSC_MIN}	Ramp Bottom		-	1.0	-	V
VFF	Minimum Usable VFF Voltage	VCC = 5V	-	3.3	-	V
PWM						
D_{MAX}	Maximum Duty Cycle	Leading and Trailing-edge Modulation	-	100	-	%
D_{MIN}	Minimum Duty Cycle	Leading and Trailing-edge Modulation	-	0	-	%
REFERENCE TRACKING						
V_{REFIN}	Input Voltage Range	VCC = 5V	0.068	-	VCC - 1.8V	V
V_{REFIN_OS}	External Reference Offset	REFIN = 0.6V	-1.8	0	2.2	mV
I_{REFOUT}	Maximum Drive Current	C_L = 1µF, VCC = 5V, REFOUT = 1.25V	-	19	-	mA
V_{REFOUT}	Output Voltage Range	C_L = 1µF	0.01	-	VCC - 1.8V	V
V_{REFOUT_OS}	Maximum Output Voltage Offset	C_L = 1µF REFOUT = 1.25V	-6	-	11	mV
C_{REFOUT_MIN}	Minimum Load Capacitance	REFOUT = 1.25V	-	1.0	-	µF
V_{REFIN_DIS}	Input Disable Voltage	VCC = 5V	VCC - 0.6	-	VCC - 0.58	V
REFERENCE						
V_{REF_COM}	Reference Voltage	T_A = 0°C to +70°C	0.587	0.591	0.595	V
V_{REF_IND}		T_A = -40°C to +85°C	0.585	0.591	0.597	V
V_{SYS_COM}	System Accuracy	T_A = 0°C to +70°C	-0.68	-	0.68	%
V_{SYS_IND}		T_A = -40°C to +85°C	-1.0	-	1.0	%
ERROR AMPLIFIER						
	DC Gain	R_L = 10k, C_L = 100p, at COMP Pin	-	88	-	dB
UGBW	Unity Gain-Bandwidth	R_L = 10k, C_L = 100p, at COMP Pin	-	15	-	MHz
SR	Slew Rate	R_L = 10k, C_L = 100p, at COMP Pin	-	6	-	V/µs
DIFFERENTIAL AMPLIFIER						
UG	DC Gain	Standard Instrumentation Amplifier	-	0	-	dB
UGBW	Unity Gain Bandwidth		-	20	-	MHz
SR	Slew Rate	COMP = 10pF	-	10	-	V/µs
V_{OFFSET_IND}	Offset		-1.9	0	1.9	mV
I_{VSEN-}	Negative Input Source Current		-	6	-	µA
	Input Common Mode Range Max		-	VCC - 1.8	-	V
	Input Common Mode Range Min		-	-0.2	-	V
V_{VSEN_DIS}	VSEN- Disable Voltage		-	VCC	-	V
INTERNAL LINEAR REGULATOR						
I_{VIN}	Maximum Current		-	200	-	mA
R_{LIN}	Saturated Equivalent Impedance	V_{IN} = 3.3V, Load = 100mA	-	2	3.9	Ω
PVCC	Linear Regulator Voltage	V_{IN} = 20V, Load = 100mA	5.30	5.50	5.71	V

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted. Parts are 100% tested at +25°C. Temperature limits established by characterization and are not production tested. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VIN_{DV/DT_Max}	Maximum VIN DV/DT	V_{IN} = 0 V to V_{IN} step, PVCC < 2.0V at V_{IN} application; V_{IN} > 6.5V	-	1	-	V/µs
		V_{IN} = 2.0 V to V_{IN} step, 2.0V < PVCC at V_{IN} application; V_{IN} > 6.5V	-	0.05	-	V/µs
EXTERNAL LINEAR REGULATOR						
LIN_DRV	Maximum Sinking Drive Current	LIN_DRV = VIN = 20V	1.30	4.17	5.30	mA
		LIN_DRV = VIN = 3.3V	1.67	3.88	4.67	mA
OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA)						
	DC Gain	C_{SS} = 0.1µF, at SS Pin	-	88	-	dB
	Drive Capability	C_{SS} = 0.1µF, at SS Pin	30	37	44	µA
GATE DRIVERS						
R_{UGATE}	Ugate Source Resistance	500mA Source Current, PVCC = 5.0V	-	1.0	-	Ω
I_{UGATE}	Ugate Source Saturation Current	$V_{UGATE-PHASE}$ = 2.5V, PVCC = 5.0V	-	2.0	-	A
R_{UGATE}	Ugate Sink Resistance	500mA Sink Current, PVCC = 5.0V	-	1.0	-	Ω
I_{UGATE}	Ugate Sink Saturation Current	$V_{UGATE-PHASE}$ = 2.5V, PVCC = 5.0V	-	2.0	-	A
R_{LGATE}	Lgate Source Resistance	500mA Source Current, PVCC = 5.0V	-	1.0	-	Ω
I_{LGATE}	Lgate Source Saturation Current	V_{LGATE} = 2.5V, PVCC = 5.0V	-	2.0	-	A
R_{LGATE}	Lgate Sink Resistance	500mA Sink Current, PVCC = 5.0V	-	0.4	-	Ω
I_{LGATE}	Lgate Sink Saturation Current	V_{LGATE} = 2.5V, PVCC = 5.0V	-	4.0	-	A
OVERCURRENT PROTECTION (OCP)						
I_{LSOC}	Low Side OCP (LSOC) Current Source	LSOC = 0V to VCC - 1.0V, T_A = 0°C to +70°C	86	100	107	µA
		LSOC = 0V to VCC - 1.0V, T_A = -40°C to +85°C	84	100	109	µA
I_{LSOC_OFSET}	LSOC Maximum Offset Error	VCC = 2.9V and 5.6V T_{SAMPLE} < 10µs	-	±2	-	mV
I_{HSOC}	High Side OCP (HSOC) Current Source	HSOC = 0.8V to 22V T_A = 0°C to +70°C	91	100	106	µA
		HSOC = 0.8V to 22V T_A = -40°C to +85°C	89	100	107	µA
I_{HSOC_LOW}		HSOC = 0.3V to 0.8V	84	-	107	µA
I_{HSOC_OFSET}	HSOC Maximum Offset Error	VCC = 2.9V and 5.5V T_{SAMPLE} < 10µs	-	±2	-	mV
MARGINING CONTROL						
V_{MARG}	Minimum Margining Voltage of Internal Reference	R_{MARG} = 10kΩ, R_{OFS-} = 6.01kΩ, MAR_CRTL = 0V	-187	-197	-209	mV
V_{MARG}	Maximum Margining Voltage of Internal Reference	R_{MARG} = 10kΩ, R_{OFS+} = 6.01kΩ, MAR_CRTL = VCC	185	197	208	mV
N_{MARG}	Margining Transfer Ratio	$N_{MARG} = (V_{OFS-}-V_{OFS+})/V_{MARG}$	4.84	5	5.22	SDR
MAR_CTRL	Positive Margining Threshold		1.51	1.8	2.02	V
MAR_CTRL	Negative Margining Threshold		0.75	0.9	1.05	V
MAR_CTRL	Tri-state Input Level	Disable Mode	1.21	1.325	1.40	V
POWER GOOD MONITOR						
V_{UVR}	Undervoltage Rising Trip Point		-7%	-9%	-11%	V_{SS}
V_{UVF}	Undervoltage Falling Trip Point		-13%	-15%	-17%	V_{SS}
V_{OVR}	Overvoltage Rising Trip Point		13%	15%	17%	V_{SS}
V_{OVF}	Overvoltage Falling Trip Point		7%	9%	11%	V_{SS}
T_{PG_DLY}	PGOOD Delay	C_{PG_DLY} = 0.1µF	-	7.1	-	ms
I_{PG_DLY}	PGOOD Delay Source Current		17	21	24	µA

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted. Parts are 100% tested at +25°C. Temperature limits established by characterization and are not production tested. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{PG_DLY}	PGOOD Delay Threshold Voltage		1.45	1.49	1.52	V
I_{PG_LOW}	PGOOD Low Output Voltage	I_{PGOOD} = 5mA	-	-	0.150	V
I_{PG_MAX}	Maximum Sinking Current	V_{PGOOD} = 0.8V	23	-	-	mA
V_{PG_MAX}	Maximum Open Drain Voltage	VCC = 3.3V	-	6	-	V

Functional Pin Description

VSEN+ (Pin 1)

This pin provides differential remote sense for the ISL6540A. It is the positive input of a standard instrumentation amplifier topology with unity gain, and should connect to the positive rail of the load/processor. The voltage at this pin should be set equal to the internal system reference voltage (0.591V typical).

VSEN- (Pin 2)

This pin provides differential remote sense for the regulator. It is the negative input of the instrumentation amplifier, and should connect to the negative rail of the load/processor. Typically 6µA is sourced from this pin. The output of the remote sense buffer is disabled (High Impedance) by pulling VSEN- to VCC.

REFOUT (Pin 3)

This pin connects to the unmargined system reference through an internal buffer. It has a 19mA drive capability with an output common mode range of GND to VCC. The REFOUT buffer requires at least 1µF of capacitive loading to be stable. This pin should not be left floating.

REFIN (Pin 4)

When the external reference pin (REFIN) is NOT within ~1.8V of VCC, the REFIN pin is used as the system reference instead of the internal 0.591V reference. The recommended REFIN input voltage range is ~68mV to VCC - 1.8V.

SS (Pin 5)

This pin provides soft-start functionality for the ISL6540A. A capacitor connected to ground along with the internal 37µA Operational Transconductance Amplifier (OTA), sets the soft-start interval of the converter. This pin is directly connected to the non-inverting input of the error amplifier. To prevent noise injection into the error amplifier the SS capacitor should be located next to the SS and GND pins.

OFS+ (Pin 6)

This pin sets the positive margining offset voltage. Resistors should be connected to GND (R_{OFS+}) and OFS- (R_{MARG}) from this pin. With MAR_CTRL logic low, the internal 0.591V reference is developed at the OFS+ pin across resistor R_{OFS+}. The voltage on OFS+ is driven from OFS- through R_{MARG}. The resulting voltage differential between OFS+ and OFS- is divided by 5 and imposed on the system reference. The maximum designed offset of 1V between OFS+ and OFS- pins translates to a 200mV offset.

OFS- (Pin 7)

This pin sets the negative margining offset voltage. Resistors should be connected to GND (R_{OFS-}) and OFS+ (R_{MARG}) from this pin. With MAR_CTRL logic low, the internal 0.591V reference is developed at the OFS- pin across resistor R_{OFS-}. The voltage on OFS- is driven from OFS+ through R_{MARG}. The resulting voltage differential between OFS+ and OFS- is divided by 5 and imposed on the system reference. The maximum designed offset of -1V between OFS+ and OFS- pins translates to a -200mV offset of the system reference.

VCC (Pin 8, Analog Circuit Bias)

This pin provides power for the ISL6540A analog circuitry. The pin should be connected to a 2.9V to 5.5V bias through an RC filter from PVCC to prevent noise injection into the analog circuitry. A 0.1µF capacitor is sufficient for decoupling of the VCC pin. The time constant of the RC filter should be no more than 10µs. This pin can be powered off the internal or external linear regulator options.

MARCTRL (Pin 9)

The MARCTRL pin controls margining function, a logic high enables positive margining, a logic low sets negative margining, a high impedance disables margining.

PG_DLY (Pin 10)

Provides the ability to delay the output of the PGOOD assertion by connecting a capacitor from this pin to GND. A 0.1µF capacitor produces approximately a 7ms delay.

PGOOD (Pin 11)

Provides an open drain Power-Good signal when the output is within 9% of nominal output regulation point with 6% hysteresis (15%/9%), and after soft-start is complete. PGOOD monitors the VMON pin.

EN (Pin 12)

This pin is compared with an internal 0.50V reference and enables the soft-start cycle. This pin also can be used for voltage monitoring. A 10µA current source to GND is active while the part is disabled, and is inactive when the part is enabled. This provides functionality for programmable hysteresis when the EN pin is used for voltage monitoring. In many applications, this pin is susceptible to excessive

transient voltages that could result in electrical overstress (EOS) damage. It is recommended that a 1kΩ resistor be placed in series with this pin.

VFF (Pin 13)

The voltage at this pin is used for input voltage feed-forward compensation and sets the internal oscillator ramp peak-to-peak amplitude at 0.16*VFF. An external RC filter may be required at this pin in noisy input environments. The minimum recommended VFF voltage is 2.97V.

VIN (Pin 14, Internal Linear Regulator Input)

This pin should be tied directly to the input rail when using the internal or external linear regulator options. It provides power to the External/Internal linear drive circuitry. When used with an external 3.3V to 5V supply, this pin should be tied directly to PVCC.

LIN_DRV (Pin 15, External Linear Regulator Drive)

This pin allows the use of an external pass element to power the IC for input voltages above 5.0V. It should be connected to GND when using an external 5V supply or the internal linear regulator. When using the external linear regulator option, this pin should be connected to the gate of a PMOS pass element, a pull-up resistor must be connected between the PMOS device's gate and source for proper operation.

PVCC (Pin 16, Driver Bias Voltage)

This pin is the output of the internal series linear regulator. It also provides the bias for both low side and high side MOSFET drivers. The maximum voltage differential between PVCC and PGND is 6V. Its recommended operational voltage range is 2.9V to 5.5V. At minimum, a 10µF capacitor is required for decoupling PVCC to PGND. For proper operation the PVCC capacitor should be located next to the PVCC and the PGND pins and should be connected to these pins with dedicated traces.

LGATE (Pin 17)

This pin provides the drive for the low side MOSFET and should be connected to its gate.

PGND (Pin 18, Power Ground)

This pin connects to the low side MOSFET's source and provides the ground return path for the lower MOSFET driver and internal power circuitries. In addition, PGND is the return path for the low side MOSFET's $r_{DS(ON)}$ current sensing circuit.

PHASE (Pin 19)

This pin connects to the source of the high side MOSFET and the drain of the low side MOSFET. This pin represents the return path for the high side gate driver. During normal switching, this pin is used for high side and low side current sensing.

UGATE (Pin 20)

This pin provides the drive for the high side MOSFET and should be connected to its gate.

BOOT (Pin 21)

This pin provides the bootstrap bias for the high side driver. The absolute maximum voltage differential between BOOT and PHASE is 6.0V (including the voltage added due to the overcharging of the bootstrap capacitor); its operational voltage range is 2.5V to 5.5V with respect to PHASE. Should overcharging of the BOOT capacitor occur, it is recommended that a 2.2Ω resistor be placed in series with the bootstrap diode.

HSOC (Pin 22)

The high side sourcing current limit is set by connecting this pin with a resistor and capacitor to the drain of the high side MOSFET. A 100µA current source develops a voltage across the resistor which is then compared with the voltage developed across the high side MOSFET. An initial ~120ns blanking period is used to eliminate sampling error due to the switching noise before the current is measured.

LSOC (Pin 23)

The low side source and sinking current limit is set by placing a resistor (R_{LSOC}) and capacitor between this pin and PGND. A 100µA current source develops a voltage across R_{LSOC} which is then compared with the voltage developed across the low side MOSFET when on. The sinking current limit is set at 1x of the nominal sourcing limit in ISL6540A. An initial ~120ns blanking period is used to eliminate the sampling error due to switching noise before the current is measured.

FS (Pin 24)

This pin provides oscillator switching frequency adjustment by placing a resistor (R_{FS}) from this pin to GND.

COMP (Pin 25)

This pin is the error amplifier output. It should be connected to the FB pin through the desired compensation network.

FB (Pin 26)

This pin is the inverting input of the error amplifier and has a maximum usable voltage of VCC - 1.8V. When using the internal differential remote sense functionality, this pin should be connected to VMON by a standard feedback network. In the event the remote sense buffer is disabled, the VMON pin should be connected to VOUT by a resistor divider along with FB's compensation network.

GND (Pin 27, Analog Ground)

Signal ground for the IC. All voltage levels are measured with respect to this pin. This pin should not be left floating.

VMON (Pin 28)

This pin is the output of the differential remote sense instrumentation amplifier. It is connected internally to the

OV/UV/PGOOD comparators. The VMON pin should be connected to the FB pin by a standard feedback network. In the event of the remote sense buffer is disabled, the VMON pin should be connected to VOUT by a resistor divider along with FB's compensation network. An RC filter should be used if VMON is to be connected directly to FB instead of to VOUT through a separate resistor divider network.

GND (Bottom Side Pad, Analog Ground)

Signal ground for the IC. All voltage levels are measured with respect to this pin. This pin should not be left floating.

Functional Description

Initialization

The ISL6540A automatically initializes upon receipt of power without requiring any special sequencing of the input supplies. The Power-On Reset (POR) function continually monitors the input supply voltages (PVCC, VFF, VCC) and the voltage at the EN pin. Assuming the EN pin is pulled to above ~0.50V, the POR function initiates soft-start operation after all input supplies exceed their POR thresholds.

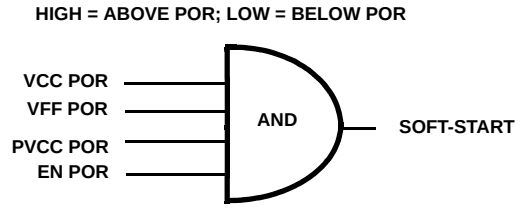
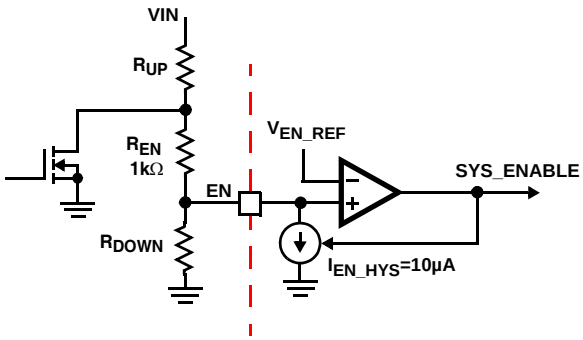


FIGURE 1. SOFT-START INITIALIZATION LOGIC



$$R_{UP} = \frac{V_{EN\_HYS}}{I_{EN\_HYS}} - 1k\Omega$$

$$R_{DOWN} = \frac{(R_{UP} + 1k\Omega) \bullet V_{EN\_REF}}{V_{EN\_FTH} - V_{EN\_REF}}$$

$$V_{EN\_FTH} = V_{EN\_RTH} - V_{EN\_HYS}$$

FIGURE 2. ENABLE POR CIRCUIT

With all input supplies above their POR thresholds, driving the EN pin above 0.50V initiates a soft-start cycle. In addition to normal TTL logic, the enable pin can be used as a voltage monitor with programmable hysteresis through the use of the internal 10µA sink current and an external resistor divider. This feature is especially designed for applications that have input rails greater than a 3.3V and require a specific input rail POR and Hysteresis levels for better undervoltage protection. Consider for a 12V application choosing R_{UP} = 97.6kΩ and R_{DOWN} = 5.76kΩ there by setting the rising threshold (V_{EN_RTH}) to ~10V and the falling threshold (V_{EN_FTH}) to ~9V, for ~1V of hysteresis (V_{EN_HYS}). Care should be taken to prevent the voltage at the EN pin from exceeding VCC when using the programmable UVLO functionality.

Soft-Start

The POR function activates the internal 37µA OTA which begins charging the external capacitor (C_{SS}) on the SS pin to a target voltage of VCC. The ISL6540A's soft-start logic continues to charge the SS pin until the voltage on COMP exceeds the bottom of the oscillator ramp, at which point, the driver outputs are enabled with the low side MOSFET first being held low for 200ns to provide for charging of the bootstrap capacitor. Once the driver outputs are enabled, the OTA's target voltage is then changed to the margined (if margining is being used) reference voltage (V_{REF_MARG}), and the SS pin is ramped up or down accordingly. This method reduces start-up surge currents due to a pre-charged output by inhibiting regulator switching until the control loop enters its linear region. By ramping the positive input of the error amplifier to VCC and then to V_{REF_MARG}, it is even possible to mitigate surge currents from outputs that are pre-charged above the set output voltage. As the SS pin connects directly to the non-inverting input of the error amplifier, noise on this pin should be kept to a minimum through careful routing and part placement. To prevent noise injection into the error amplifier the SS capacitor should be located within 150 mils of the SS and GND pins. Soft-start is declared done when the drivers have been enabled and the SS pin is within ±3mV of V_{REF_MARG}.

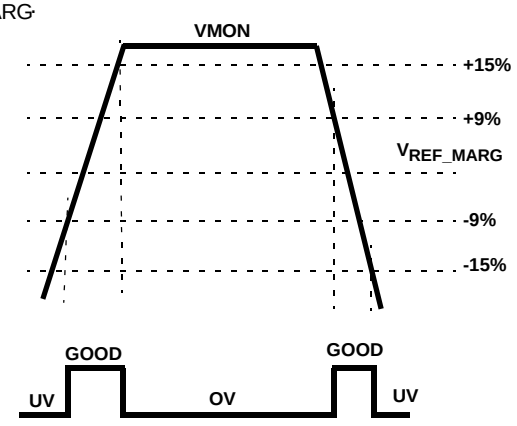


FIGURE 3. UNDERVOLTAGE-OVERVOLTAGE WINDOW

$$T_{PG\_DLY} = C_{PG\_DLY} \cdot \frac{1.49V}{21\mu A} \quad \text{(EQ. 1)}$$

Power-Good

The power-good comparator references the voltage on the soft-start pin to prevent accidental tripping during margining. The trip points are shown in Figure 3. Additionally, power-good will not be asserted until after the completion of the soft-start cycle. A 0.1µF capacitor at the PG_DLY pin will add an additional ~7ms delay to the assertion of power-good. PG_DLY does not delay the de-assertion of power-good.

Under and Overvoltage Protection

The Undervoltage (UV) and Overvoltage (OV) protection circuitry compares the voltage on the VMON pin with the reference that tracks with the margining circuitry to prevent accidental tripping. UV and OV functionality is not enabled until the end of soft-start.

An OV event is detected asynchronously and causes the high side MOSFET to turn off, the low side MOSFET to turn on (effectively a 0% duty cycle), and PGOOD to pull low. The regulator stays in this state and overrides sourcing and sinking OCP protections until the OV event is cleared.

An UV event is detected asynchronously and results in the PGOOD pulling low.

Overcurrent Protection

The ISL6540A monitors both the high side MOSFET and low side MOSFET for overcurrent events. Dual sensing allows the ISL6540A to detect overcurrent faults at the very low and very high duty cycles that can result from the ISL6540A's wide input range. The OCP function is enabled with the drivers at startup and detects the peak current during each sensing period. A resistor and a capacitor between the LSOC pin and GND set the low side source and sinking current limits. A 100µA current source develops a voltage across the resistor which is then compared with the voltage developed across the low side MOSFET at conduction mode. The measurement comparator uses offset correcting circuitry to provide precise current measurements with roughly ±2mV of offset error. An ~120ns blanking period, implemented on the upper and lower MOSFET current sensing circuitries, is used to reduce the current sampling error due to the leading-edge switching noise. An additional 120ns low pass filter is used to further reduce measurement error due to noise. In sourcing current applications, the LSOC voltage is inverted and compared with the voltage across the MOSFET while on. When this voltage exceeds the LSOC set voltage, a sourcing OCP fault is triggered. A 1000pF or greater filter capacitor should be used in parallel with R_{LSOC} to prevent on-chip parasitics from impacting the accuracy of the OCP measurement.

The ISL6540A's sinking current limit is set to the same voltage as its sourcing limit. In sinking applications, when the voltage across the MOSFET is greater than the voltage developed across the resistor (R_{LSOC}) a sinking OCP event is triggered. To avoid non-synchronous operation at light load, the peak-to-peak output inductor ripple current should not be greater than twice of the sinking current limit.

The high side sourcing current limit is set by connecting the HSOC pin with a resistor (R_{HSOC}) and a capacitor to the drain of the high side MOSEFT. A 100µA current source develops a voltage across the resistor which is then compared with the voltage developed across the high side MOSFET while on. When the voltage drop across the MOSFET exceeds the voltage drop across the resistor, a sourcing OCP event occurs. A 1000pF or greater filter capacitor should be used in parallel with R_{HSOC} to prevent on-chip parasitics from impacting the accuracy of the OCP measurement and to smooth the voltage across R_{HSOC} in the presence of switching noise on the input bus.

Simple Low Side OCP Equation

$$R_{LSOC} = \frac{I_{OC\_SOURCE} \bullet r_{DS(ON)LowSide}}{100\mu A} \quad \text{(EQ. 2)}$$

Detailed Low Side OCP Equations

$$R_{LSOC} = \frac{\left(I_{OC\_SOURCE} + \frac{\Delta I}{2}\right) \bullet r_{DS(ON),L}}{I_{LSOC} \bullet N_L}$$

$$\Delta I = \frac{V_{IN} - V_{OUT}}{F_S L} \bullet \frac{V_{OUT}}{V_{IN}} \quad \text{(EQ. 3)}$$

$$I_{OC\_SINK} = \frac{I_{LSOC} \bullet N_L \bullet R_{LSOC}}{r_{DS(ON),L}} - \frac{\Delta I}{2}$$

N_L = Number of low side MOSFETs

Sourcing OCP faults cause the regulator to disable (Ugate and Lgate drives pulled low, PGOOD pulled low, soft-start capacitor discharged) itself for a fixed period of time after which a normal soft-start sequence is initiated. The period of time the regulator waits before attempting a soft-start sequence is set by three charge and discharge cycles of the soft-start capacitor.

Simple High Side OCP Equation

$$R_{HSOC} = \frac{I_{OC\_SOURCE} \bullet r_{DS(ON)HighSide}}{100\mu A} \quad \text{(EQ. 4)}$$

Detailed High Side OCP Equation

$$R_{HSOC} = \frac{\left(I_{OC\_SOURCE} + \frac{\Delta I}{2}\right) \bullet r_{DS(ON),U}}{I_{HSOC} \bullet N_U} \quad \text{(EQ. 5)}$$

N_U = Number of high side MOSFETs

Sinking OCP faults cause the low side MOSFET drive to be disabled, effectively operating the ISL6540A in a non-synchronous manner. The fault is maintained for three clock cycles at which point it is cleared and normal operation is restored. OVP fault implementation overrides sourcing and sinking OCP events, immediately turning on the low side MOSFET and turning off the high side MOSFET. The OC trip

point varies mainly due to the MOSFETs $r_{DS(ON)}$ variations and system noise. To avoid overcurrent tripping in the normal operating load range, find the R_{HSOC} and/or R_{LSOC} resistor from the previous detailed equations with:

1. Maximum $r_{DS(ON)}$ at the highest junction temperature.
2. Minimum I_{LSOC} and/or I_{HSOC} from specification table on page 8.
3. Determine the overcurrent trip point greater than the maximum output continuous current at maximum inductor ripple current.

Frequency Programming

By tying a resistor to GND from FS pin, the switching frequency can be set between 250kHz and 2MHz.

Oscillator/VFF

The Oscillator is a triangle waveform, providing for leading and falling edge modulation. The bottom of the oscillator waveform is set at 1.0V. The ramp's peak-to-peak amplitude is determined from the voltage on the VFF (Voltage Feed-Forward) pin. See Equation 6:

$$\Delta Vosc = 0.16 \bullet VFF \quad \text{(EQ. 6)}$$

An internal RC filter of 233kΩ and 2pF (341kHz) provides filtering of the VFF voltage. An external RC filter may be required to augment this filter in the event that it is insufficient to prevent noise injection or control loop interactions. Voltages below 2.9V on the VFF pin may result in undesirable operation due to extremely small peak to peak oscillator waveforms. The oscillator waveform should not exceed VCC -1.0V. For high VFF voltages the internal/external 5.5V linear regulator should be used. 5.5V on VCC provides sufficient headroom for 100% duty cycle operation when using the maximum VFF voltage of 22V. In the event of sustained 100% duty cycle operation, defined as 32-clock cycles where no LG pulse is detected, LG will be pulsed on to refresh the design's bootstrap capacitor.

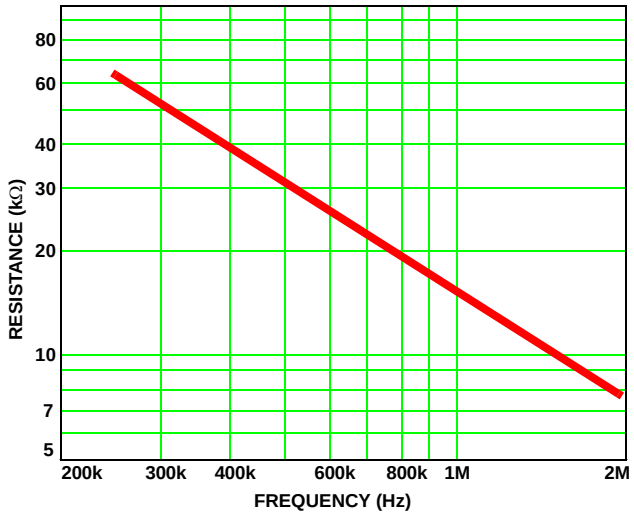


FIGURE 4. R_{FS} RESISTANCE vs FREQUENCY

$$Fs[Hz] \approx 1.178 \times 10^{10} \bullet R_T[\Omega]^{-0.973} \quad (R_T \text{ TO GND}) \quad \text{(EQ. 7)}$$

Internal Series Linear Regulator

The VIN pin is connected to PVCC with a 2Ω internal series linear regulator, which is internally compensated. The external series linear regulator option should be used for applications requiring pass elements of less than 2Ω. When using the internal regulator, the LIN_DRV pin should be connected directly to GND. The PVCC and VIN pins should have a bypass capacitor (at least 10µF on PVCC is required) connected to PGND. For proper operation the PVCC capacitor must be within 150 mils of the PVCC and the PGND pins, and be connected to these pins with dedicated traces. The internal series linear regulator's input (VIN) can range between 3.3V to 20V ±10%. The internal linear regulator is to provide power for both the internal MOSFET drivers through the PVCC pin and the analog circuitry through the VCC pin. The VCC pin should be connected to the PVCC pin with an RC filter to prevent high frequency driver switching noise from entering the analog circuitry. When VIN drops below 5.5V, the pass element will saturate; PVCC will track VIN, minus the dropout of the linear regulator: PVCC = VIN-2xI_{VIN}. When used with an external 5V supply, the VIN pin should be tied directly to PVCC.

At start-up (PVCC = 0V and VIN = 0V) the DV/DT on VIN should be kept below 1V/µs to prevent electrical overstress on PVCC. Care should be taken to keep the DV/DT on VIN below 0.05V/µs if the initial steady state voltage on PVCC is above 2.0V, as electrical overstress on PVCC is otherwise possible.

External Series Linear Regulator

The LIN_DRV pin provides sinking drive capability for an external pass element linear regulator controller. The external linear options are especially useful when the

internal linear dropout is too large for a given application. When using the external linear regulator option, the LIN_DRV pin should be connected to the gate of a PMOS device, and a resistor should be connected between its gate and source. A resistor and a capacitor should be connected from gate-to-source to compensate the control loop. A PNP device can be used instead of a PMOS device in which case the LIN_DRV pin should be connected to the base of the PNP pass element. The sinking capability of the LIN_DRV pin is 5mA, and should not be exceeded if using an external resistor for a PMOS device. The designer should take care in designing a stable system when using external pass elements. The VCC pin should be connected to the PVCC pin with an RC filter to prevent high frequency driver switching noise from entering the analog circuitry.

High Speed MOSFET Gate Driver

The integrated driver has similar drive capability and features to Intersil's ISL6605 stand alone gate driver. The PWM tri-state feature helps prevent a negative transient on the output voltage when the output is being shut down. This eliminates the Schottky diode that is used in some systems for protecting the microprocessor from reversed-output-voltage damage. See the ISL6605 datasheet for specification parameters that are not defined in the current ISL6540A “Electrical Specifications” table on page 6.

A 1Ω to 2Ω resistor is recommended to be in series with the bootstrap diode when using VCCs above 5.0V to prevent the bootstrap capacitor from overcharging due to the negative swing of the trailing edge of the phase node.

Margining Control

When the MAR_CTRL is pulled high or low, the positive or negative margining functionality is respectively enabled. When MAR_CTRL is left floating, the function is disabled. Upon UP margining, an internal buffer drives the OFS- pin from VCC to maintain OFS+ at 0.591V. The resistor divider, R_{MARG} and R_{OFS+}, causes the voltage at OFS- to be increased. Similarly, upon DOWN margining, an internal buffer drives the OFS+ pin from VCC to maintain OFS- at 0.591V. The resistor divider, R_{MARG} and R_{OFS-}, causes the voltage at OFS+ to be increased. In both modes, the voltage difference between OFS+ and OFS- is then sensed with an instrumentation amplifier and is converted to the desired margining voltage by a 5:1 ratio. The maximum designed margining range of the ISL6540A is ±200mV, this sets the MINIMUM value of R_{OFS+} or R_{OFS-} at approximately 5.9k for an R_{MARG} of 10k for a MAXIMUM of 1V across R_{MARG}.

The OFS pins are completely independent and can be set to different margining levels. The maximum usable reference voltage for the ISL6540A is VCC-1.8V, and should not be exceeded when using the margining functionality, for example: V_{REF_MARG} < VCC - 1.8V, as shown in Equation 8:

$$V_{MARG\_UP} = \frac{V_{REF}}{5} \bullet \frac{R_{MARG}}{R_{OFS+}}$$

$$V_{MARG\_DOWN} = \frac{V_{REF}}{5} \bullet \frac{R_{MARG}}{R_{OFS-}} \quad \text{(EQ. 8)}$$

An alternative calculation provides for a desired percentage change in the output voltage when using the internal 0.591V reference:

$$V_{PCT\_UP} = 20 \bullet \frac{R_{MARG}}{R_{OFS+}} \qquad V_{pct\_DOWN} = 20 \bullet \frac{R_{MARG}}{R_{OFS-}} \quad \text{(EQ. 9)}$$

When not used in a design OFS+, OFS-, and MARCTRL should be left floating. To prevent damage to the part, OFS+ and OFS- should not be tied to VCC or PVCC.

Reference Output Buffer

The internal buffer’s output tracks the unmargined system reference. It has a 19mA drive capability, with maximum and minimum output voltage capabilities of VCC and GND respectively. Its capacitive loading can range from 1µF to above 17.6µF, which is designed for 1 to 8 DIMM systems in DDR (Dual Data Rate) applications. 1µF of capacitance should always be present on REFOUT. It is not designed to drive a resistive load and any such load added to the system should be kept above 300kΩ total impedance. The Reference Output Buffer should not be left floating.

Reference Input

The REFIN pin allows the user to bypass the internal 0.591V reference with an external reference. Asynchronously, if REFIN is NOT within ~1.8V of VCC, the external reference pin is used as the control reference instead of the internal 0.591V reference. The minimum usable REFIN voltage is ~68mV, while the maximum is VCC - 1.8V - V_{MARG} (if present).

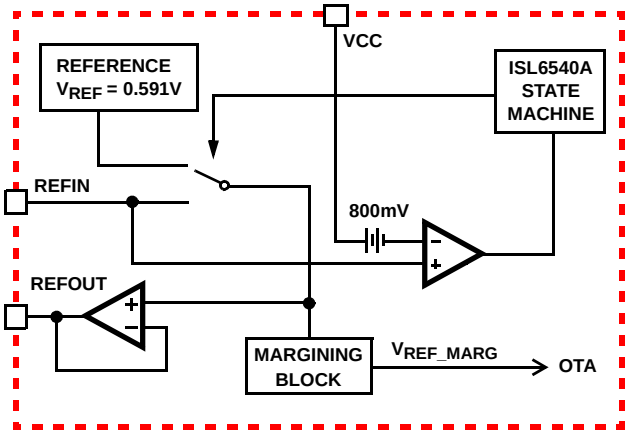


FIGURE 5. SIMPLIFIED REFERENCE BUFFER

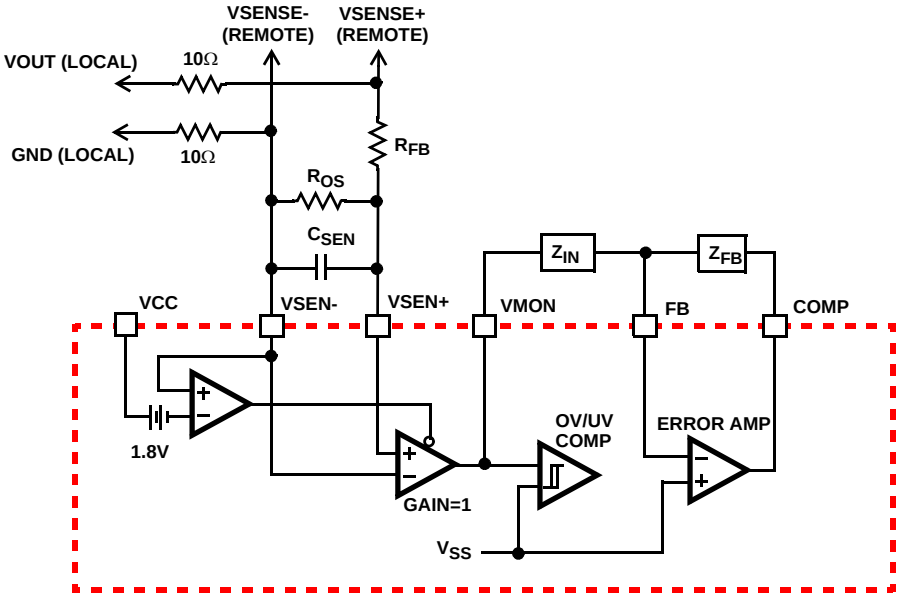


FIGURE 6. SIMPLIFIED UNITY GAIN DIFFERENITAL SENSING IMPLEMENTATION

Internal Reference and System Accuracy

The internal reference is trimmed to 0.591V. The total DC system accuracy of the system is within ±0.68% over commercial temperature range, and ±1.00% over industrial temperature range. System accuracy includes error amplifier offset, OTA error, and bandgap error. Differential remote sense offset error is not included. As a result, if the differential remote sense is used, then an extra 1.9mV of offset error enters the system. The use of REFIN may add up to 2.2mV of additional offset error.

Differential Remote Sense Buffer

The differential remote sense buffer is essentially an instrumentation amplifier with unity gain. The offset is trimmed to 1.5mV for high system accuracy. As with any instrumentation amplifier, typically 6µA are sourced from the VSEN- pin. The output of the remote sense buffer is connected directly to the internal OV/UV comparator. As a result, a resistor divider should be placed on the input of the buffer for proper regulation, as shown in Figure 6. The VMON pin should be connected to the FB pin by a standard feed-back network. A small capacitor, C_{SEN} in Figure 6, can be added to filter out noise, typically C_{SEN} is chosen so the corresponding time constant does not reduce the overall phase margin of the design, typically this is 2x to 10x switching frequency of the regulator.

As some applications will not use the differential remote sense, the output of the remote sense buffer can be disabled (high impedance) by pulling VSEN- within 1.8V of VCC. As the VMON pin is connected internally to the OV/UV/PGOOD comparator, an external resistor divider must then be connected to VMON to provide correct voltage information for the OV/UV comparator. An RC filter should be used if VMON is to be connected directly to FB instead of to VOUT through a separate resistor divider network. This filter prevents noise injection from disturbing the OV/UV/PGOOD comparators on VMON. VMON may also be connected to the SS pin, which completely bypasses the OV/UV/PGOOD functionality.

Application Guidelines

Layout Considerations

MOSFETs switch very fast and efficiently. The speed with which the current transitions from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, radiate noise into the circuit and lead to device overvoltage stress. Careful component layout and printed circuit design minimizes the voltage spikes in the converter. Consider, as an example, the turnoff transition of the upper PWM MOSFET. Prior to turnoff, the upper MOSFET is carrying the output inductor current. During the turnoff, current stops flowing in the upper MOSFET and is picked up by the lower MOSFET. Any inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selection, tight layout of the critical components, and short, wide circuit traces minimize the magnitude of voltage spikes.

There are two sets of critical components in a DC/DC converter using a ISL6540A controller. The power components are the most critical because they switch large currents and have the potential to create large voltage spikes, as well as induce noise into sensitive, high impedance adjacent nodes. Next are small signal

components that connect to sensitive nodes or supply critical bypassing current and signal coupling.

Equally important are the connections of the internal gate drives (UGATE, LGATE, PHASE, PGND, BOOT): since they drive the power train MOSFETs using short, high current pulses, it is important to size them accordingly and reduce their overall impedance. While not always esthetically pleasing, straightest connections encircling the least area result in the lowest parasitic inductance build-up, and, consequentially, are the better choice.

The power train components should be placed first. Locate the input capacitors close to the power switches. Minimize the length of the connections between the input capacitors, C_{IN}, especially the high frequency decoupling, and the power switches. Locate the output inductor and output capacitors between the MOSFETs and the load. Locate all the high-frequency decoupling capacitors (ceramics) as close as practicable to their decoupling target, making use of the shortest connection paths to any internal planes, such as vias to GND immediately next, or even onto the capacitor's grounded solder pad.

The critical small signal components include the bypass capacitors for VIN, VCC and PVCC. Locate the bypass capacitors, C_{BP}, close to the device. It is especially important to locate the components associated with the feedback circuit close to their respective controller pins, since they belong to a high-impedance circuit loop, sensitive to EMI pick-up. Place all the other highlighted components close to the respective pins of the ISL6540A.

A multi-layer printed circuit board is recommended. Figure 8 shows the connections of the critical components of the converter. Note that capacitors C_{xxIN} and C_{xxOUT} could each represent numerous physical capacitors. Dedicate one solid layer, usually the one underneath the component side of the board, to a ground plane and make all critical component ground connections with vias to this layer. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. Keep the PHASE island as small as practicable, while still allowing for proper heat-sinking of the lower MOSFET. The power plane should support the input power and output power nodes. Use copper-filled polygons on the top and bottom circuit layers for large current-carrying circuit nodes. Use the remaining printed circuit layers for small signal wiring.

Size the trace interconnects commensurate with the signals they are carrying. Use narrow (0.004" to 0.008") and short traces for the high-impedance, small-signal connections, such as the feedback, compensation, soft-start, frequency set, reference input, offset, etc. The wiring traces from the IC to the MOSFETs' gates and sources should be wide (0.02" to 0.05") and short, encircling the smallest area possible.

The metal pad of the ISL6540A's package should be connected to the ground plane via 6 to 9 small vias evenly placed in the bottom pad's footprint. The GND and PGND pins should be connected to this bottom pad to find a convenient, low inductance path to the rest of the circuitry. This recommended connection provides not only an electrically low impedance path, but a low thermal path as well, helping with the heat dissipation taking place in the part.

Compensating the Converter

The ISL6540A single-phase converter is a voltage-mode controller. This section highlights the design considerations for a voltage-mode controller requiring external compensation. To address a broad range of applications, a type-3 feedback network is recommended (see Figure 7).

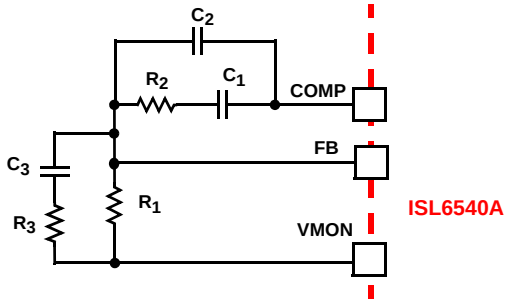


FIGURE 7. COMPENSATION CONFIGURATION FOR ISL6540A WHEN USING DIFFERENTIAL REMOTE SENSE

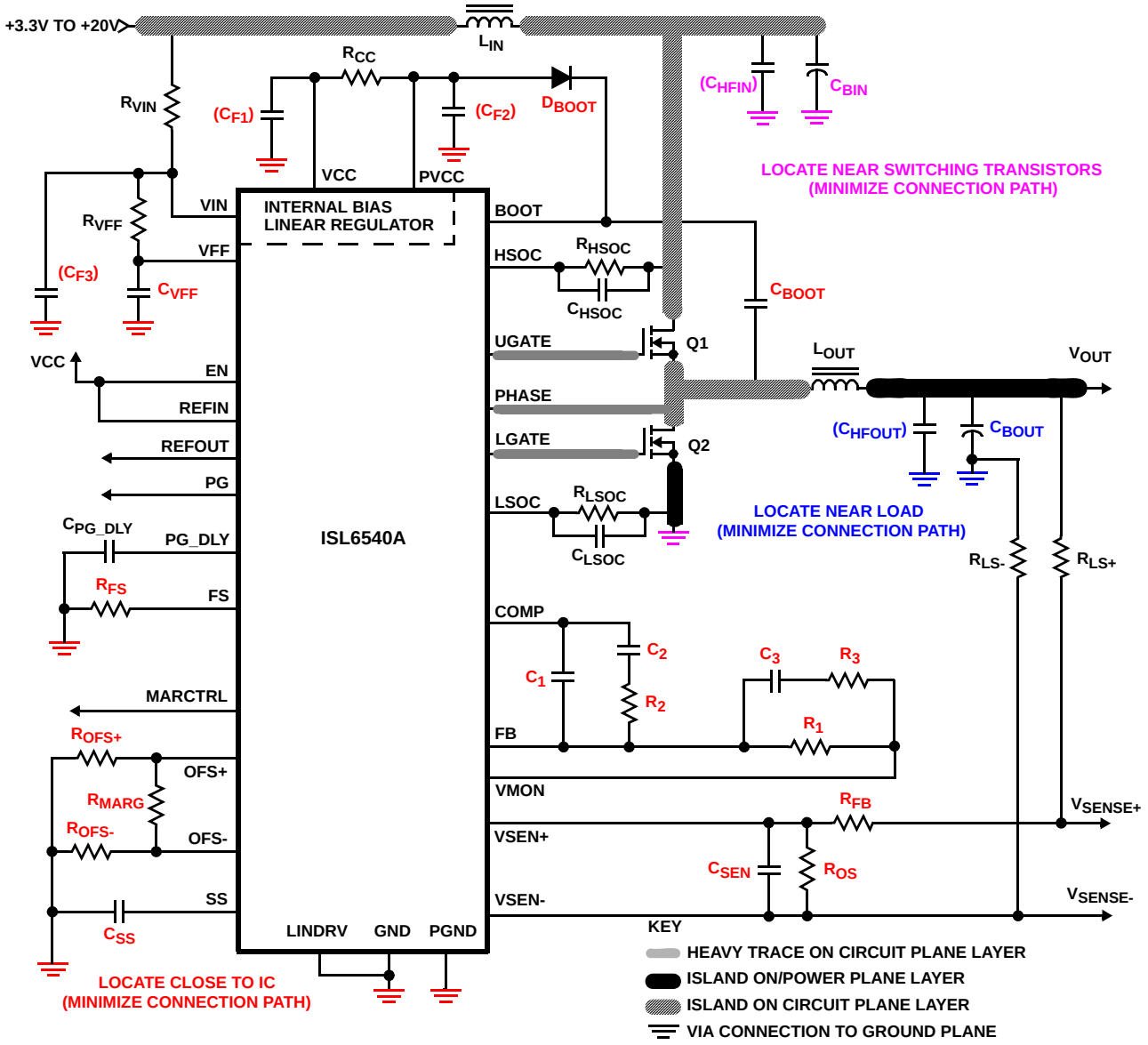


FIGURE 8. PRINTED CIRCUIT BOARD POWER PLANES AND ISLANDS

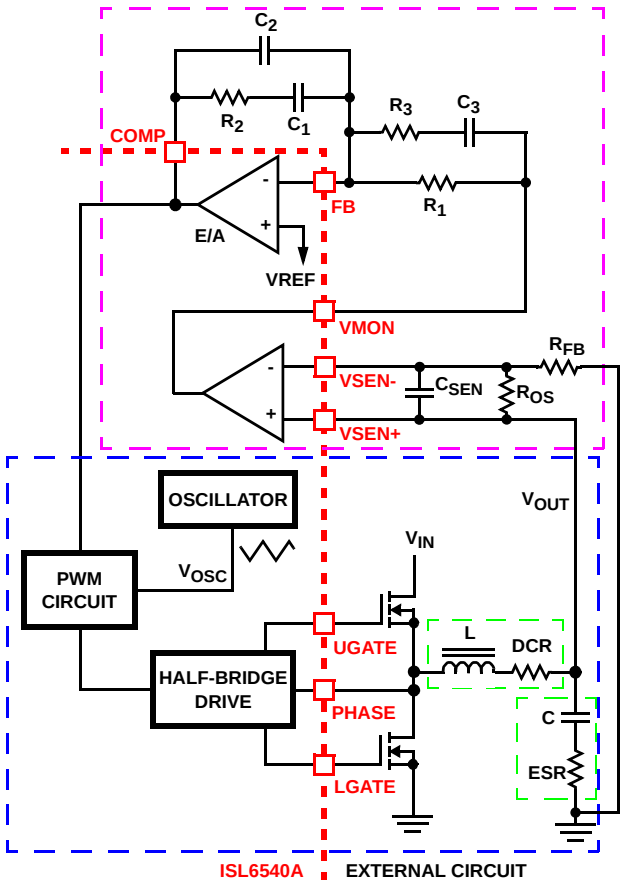


FIGURE 9. VOLTAGE-MODE BUCK CONVERTER COMPENSATION DESIGN

Figure 9 highlights the voltage-mode control loop for a synchronous-rectified buck converter, when using an internal differential remote sense amplifier. The output voltage (V_{OUT}) is regulated to the reference voltage, VREF, level. The error amplifier output (COMP pin voltage) is compared with the oscillator (OSC) triangle wave to provide a pulse-width modulated wave with an amplitude of V_{IN} at the PHASE node. The PWM wave is smoothed by the output filter (L and C). The output filter capacitor bank's equivalent series resistance is represented by the series resistor ESR.

The modulator transfer function is the small-signal transfer function of V_{OUT}/V_{COMP}. This function is dominated by a DC gain, given by $D_{MAX}V_{IN}/V_{OSC}$, and shaped by the output filter, with a double pole break frequency at F_{LC} and a zero at F_{CE}. For the purpose of this analysis C and ESR represent the total output capacitance and its equivalent series resistance.

$$F_{LC} = \frac{1}{2\pi \cdot \sqrt{L \cdot C}} \qquad F_{CE} = \frac{1}{2\pi \cdot C \cdot ESR} \qquad \text{(EQ. 10)}$$

The compensation network consists of the error amplifier (internal to the ISL6540A) and the external R_1 thru R_3, C_1 thru C_3 components. The goal of the compensation network is to provide a closed loop transfer function with high 0dB crossing frequency (F_0; typically 0.1 to 0.3 of F_{SW}) and adequate phase margin (better than 45°). Phase margin is the difference between the closed loop phase at F_{0dB} and 180°. The equations that follow relate the compensation network's poles, zeros and gain to the components (R_1, R_2, R_3, C_1, C_2, and C_3) in Figures 7 and 9. Use the following guidelines for locating the poles and zeros of the compensation network:

1. Select a value for R_1 (1kΩ to 10kΩ, typically). Calculate value for R_2 for desired converter bandwidth (F_0). If setting the output voltage to be equal to the reference set voltage as shown in Figure 7, the design procedure can be followed as presented. However, when setting the output voltage via a resistor divider placed at the input of the differential amplifier (as shown in Figure 9), in order to compensate for the attenuation introduced by the resistor divider, the below obtained R_2 value needs be multiplied by a factor of $(R_{OS}+R_{FB})/R_{OS}$. The remainder of the calculations remain unchanged, as long as the compensated R_2 value is used.

$$R_2 = \frac{V_{OSC} \cdot R_1 \cdot F_0}{d_{MAX} \cdot V_{IN} \cdot F_{LC}} \qquad \text{(EQ. 11)}$$

   A small capacitor, C_{SEN} in Figure 9, can be added to filter out noise, typically C_{SEN} is chosen so the corresponding time constant does not reduce the overall phase margin of the design, typically this is 2x to 10x switching frequency of the regulator. As the ISL6540A supports 100% duty cycle, d_{MAX} equals 1. The ISL6540A also uses feedforward compensation, as such V_{OSC} is equal to 0.16 multiplied by the voltage at the VFF pin. When tieing VFF to V_{IN}, the Equation 12 simplifies to:

$$R_2 = \frac{0.16 \cdot R_1 \cdot F_0}{F_{LC}} \qquad \text{(EQ. 12)}$$

2. Calculate C_1 such that F_{Z1} is placed at a fraction of the F_{LC}, at 0.1 to 0.75 of F_{LC} (to adjust, change the 0.5 factor to desired number). The higher the quality factor of the output filter and/or the higher the ratio F_{CE}/F_{LC}, the lower the F_{Z1} frequency (to maximize phase boost at F_{LC}).

$$C_1 = \frac{1}{2\pi \cdot R_2 \cdot 0.5 \cdot F_{LC}} \qquad \text{(EQ. 13)}$$

3. Calculate C_2 such that F_{P1} is placed at F_{CE}.

$$C_2 = \frac{C_1}{2\pi \cdot R_2 \cdot C_1 \cdot F_{CE} - 1} \qquad \text{(EQ. 14)}$$

4. Calculate R_3 such that F_{Z2} is placed at F_{LC}. Calculate C_3 such that F_{P2} is placed below F_{SW} (typically, 0.5 to 1.0 times F_{SW}). F_{SW} represents the regulator's switching frequency. Change the numerical factor to reflect desired placement of this pole. Placement of F_{P2} lower in frequency helps reduce the gain of the compensation network at high frequency, in turn reducing the HF ripple component at the COMP pin and minimizing resultant duty cycle jitter.

$$R_3 = \frac{R_1}{\frac{F_{SW}}{F_{LC}} - 1} \qquad C_3 = \frac{1}{2\pi \cdot R_3 \cdot 0.7 \cdot F_{SW}} \qquad \text{(EQ. 15)}$$

It is recommended that a mathematical model is used to plot the loop response. Check the loop gain against the error amplifier's open-loop gain. Verify phase margin results and adjust as necessary. The following equations describe the frequency response of the modulator (G_{MOD}), feedback compensation (G_{FB}) and closed-loop response (G_{CL}):

$$G_{MOD}(f) = \frac{D_{MAX} \cdot V_{IN}}{V_{OSC}} \cdot \frac{1 + s(f) \cdot ESR \cdot C}{1 + s(f) \cdot (ESR + DCR) \cdot C + s^2(f) \cdot L \cdot C}$$

$$G_{FB}(f) = \frac{1 + s(f) \cdot R_2 \cdot C_1}{s(f) \cdot R_1 \cdot (C_1 + C_2)} \cdot \frac{1 + s(f) \cdot (R_1 + R_3) \cdot C_3}{(1 + s(f) \cdot R_3 \cdot C_3) \cdot \left(1 + s(f) \cdot R_2 \cdot \left(\frac{C_1 \cdot C_2}{C_1 + C_2}\right)\right)}$$

$$G_{CL}(f) = G_{MOD}(f) \cdot G_{FB}(f) \qquad \text{where, } s(f) = 2\pi \cdot f \cdot j \qquad \text{(EQ. 16)}$$

As before when tieing VFF to VIN terms in the previous equations can be simplified as shown in Equation 17:

$$\frac{D_{MAX} \cdot V_{IN}}{V_{OSC}} = \frac{1 \cdot V_{IN}}{0.16 \cdot V_{IN}} = 6.25 \qquad \text{(EQ. 17)}$$

COMPENSATION BREAK FREQUENCY EQUATIONS

Figure 10 shows an asymptotic plot of the DC/DC converter's gain vs frequency. The actual modulator gain has a high gain peak dependent on the quality factor (Q) of the output filter, which is not shown. Using the previous guidelines should yield a compensation gain similar to the curve plotted. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at F_{P2} against the capabilities of the error amplifier. The closed loop gain, G_{CL}, is constructed on the log-log graph of Figure 10 by adding the modulator gain, G_{MOD} (in dB), to the feedback compensation gain, G_{FB} (in dB). This is equivalent to multiplying the modulator transfer function and the compensation transfer function and then plotting the resulting gain.

$$F_{Z1} = \frac{1}{2\pi \cdot R_2 \cdot C_1} \qquad F_{P1} = \frac{1}{2\pi \cdot R_2 \cdot \frac{C_1 \cdot C_2}{C_1 + C_2}}$$

$$F_{Z2} = \frac{1}{2\pi \cdot (R_1 + R_3) \cdot C_3} \qquad F_{P2} = \frac{1}{2\pi \cdot R_3 \cdot C_3} \qquad \text{(EQ. 18)}$$

A stable control loop has a gain crossing with close to a -20dB/decade slope and a phase margin greater than 45°. Include worst case component variations when determining phase margin. The mathematical model presented makes a number of approximations and is generally not accurate at frequencies approaching or exceeding half the switching frequency. When designing compensation networks, select target crossover frequencies in the range of 10% to 30% of the switching frequency, F_{SW}.

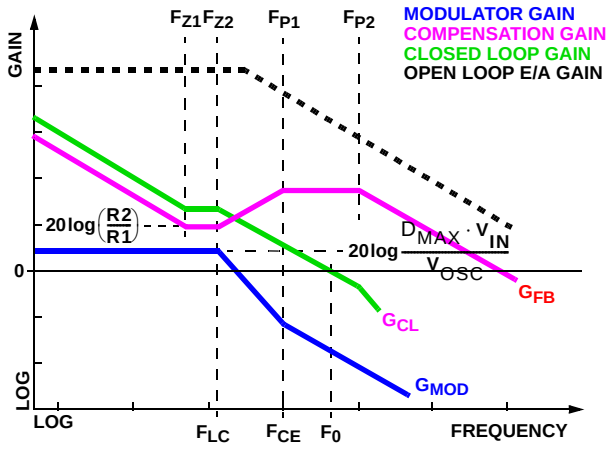


FIGURE 10. ASYMPTOTIC BODE PLOT OF CONVERTER GAIN

Component Selection Guidelines

Output Capacitor Selection

An output capacitor is required to filter the output and supply the load transient current. The filtering requirements are a function of the switching frequency and the ripple current. The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout.

Modern microprocessors produce transient load rates above 1A/ns. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (effective series resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements. For example, Intel recommends that the high frequency decoupling for the Pentium Pro be composed of at least forty (40) 1.0µF ceramic capacitors in the 1206 surface-mount package. Follow on specifications have only increased the number and quality of required ceramic decoupling capacitors.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate transient. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes.

However, the equivalent series inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. Unfortunately, ESL is not a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance with frequency to select a suitable component. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

Output Inductor Selection

The output inductor is selected to meet the output voltage ripple requirements and minimize the converter's response time to the load transient. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current. The ripple voltage and current are approximated by Equation 19:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{F_S \times L} \bullet \frac{V_{OUT}}{V_{IN}} \qquad \Delta V_{OUT} = \Delta I \times ESR \qquad \text{(EQ. 19)}$$

Increasing the value of inductance reduces the ripple current and voltage. However, the large inductance values reduce the converter's response time to a load transient.

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Given a sufficiently fast control loop design, the ISL6540A will provide either 0% or 100% duty cycle in response to a load transient. The response time is the time required to slew the inductor current from an initial current value to the transient current level. During this interval the difference between the inductor current and the transient current level must be supplied by the output capacitor. Minimizing the response time can minimize the output capacitance required.

The response time to a transient is different for the application of load and the removal of load. Equation 20 gives the approximate response time interval for application and removal of a transient load:

$$t_{RISE} = \frac{L_O \times I_{TRAN}}{V_{IN} - V_{OUT}} \qquad t_{FALL} = \frac{L_O \times I_{TRAN}}{V_{OUT}} \qquad \text{(EQ. 20)}$$

where: I_{TRAN} is the transient load current step, t_{RISE} is the response time to the application of load, and t_{FALL} is the response time to the removal of load. With a lower input source such as 1.8V or 3.3V, the worst case response time can be either at the application or removal of load and dependent upon the output voltage setting. Be sure to check both of these equations at the minimum and maximum output levels for the worst case response time.

Input Capacitor Selection

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high frequency decoupling and bulk capacitors

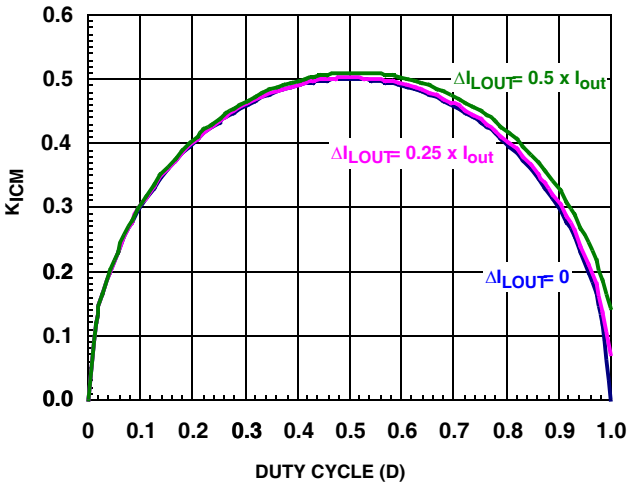


FIGURE 11. INPUT-CAPACITOR CURRENT MULTIPLIER FOR SINGLE-PHASE BUCK CONVERTER

to supply the current needed each time Q_1 turns on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of Q_1 and the source of Q_2.

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25x greater than the maximum input voltage and a voltage rating of 1.5x is a conservative guideline. The RMS current rating requirement for the input capacitor of a buck regulator is approximated in Equation 21.

$$I_{IN,RMS} = \sqrt{I_O^2(D - D^2) + \frac{\Delta I^2}{12}D} \qquad D = \frac{V_O}{VIN}$$

OR

$$I_{IN\overline{RMS}} = K_{ICM} \bullet I_O \qquad \text{(EQ. 21)}$$

For a through-hole design, several electrolytic capacitors (Panasonic HFQ series or Nichicon PL series or Sanyo MV-GX or equivalent) may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up. Figure 11 provides an easy graphical approximation of the input RMS requirements for a single-phase buck converter.

MOSFET Selection/Considerations

The ISL6540A requires 2 N-Channel power MOSFETs. These should be selected based upon $r_{DS(ON)}$, gate supply requirements, and thermal management requirements.

In high-current applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss

components; conduction loss and switching loss. The conduction losses are the largest component of power dissipation for both the upper and the lower MOSFETs. These losses are distributed between the two MOSFETs according to duty factor (see the equations below). The upper MOSFET exhibits turn-on and turn-off switching losses as well as the reverse recover loss, while the synchronous rectifier exhibits body-diode conduction losses during the leading and trailing edge dead times.

$$P_{LOWER} = \left(I_O^2 + \frac{\Delta I^2}{12}\right) \bullet \frac{r_{DS(ON),L}}{N_L} \bullet (1 - D) + P_{DEAD}$$

$$P_{DEAD} = \left[\left(I_O + \frac{\Delta I}{12}\right) \bullet V_{DT} \bullet t_{DT} + \left(I_O - \frac{\Delta I}{12}\right) \bullet V_{DL} \bullet t_{DL}\right] \bullet F_S$$

$$P_{UPPER} = \left(I_O^2 + \frac{\Delta I^2}{12}\right) \bullet \frac{r_{DS(ON),U}}{N_U} \bullet D + P_{SW} + P_{Qrr}$$

$$P_{SW} = \left[\left(I_O + \frac{\Delta I}{12}\right) \bullet t_{OFF} + \left(I_O - \frac{\Delta I}{12}\right) \bullet t_{ON}\right] \bullet VIN \bullet F_S$$

$$P_{Qrr} = Q_{rr} \bullet VIN \bullet F_S \qquad \text{(EQ. 22)}$$

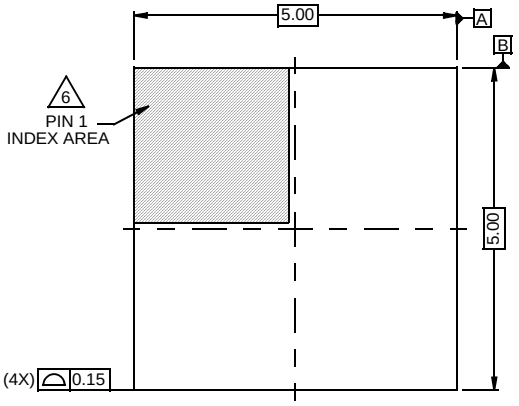
where D is the duty cycle = V_O/VIN; Q_{rr} is the reverse recover charge; $t_{DL}$and t_{DT} are leading and trailing edge dead time, and t_{ON} and t_{OFF} are the switching intervals.

These equations do not include the gate-charge losses that are proportional to the total gate charge and the switching frequency and partially dissipated by the internal gate resistance of the MOSFETs. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

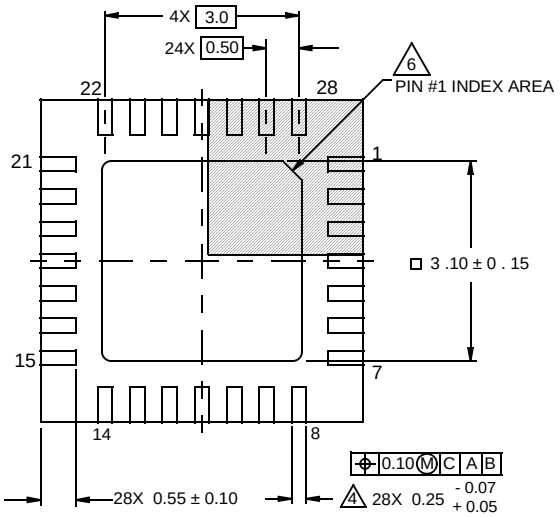
Package Outline Drawing

L28.5x5

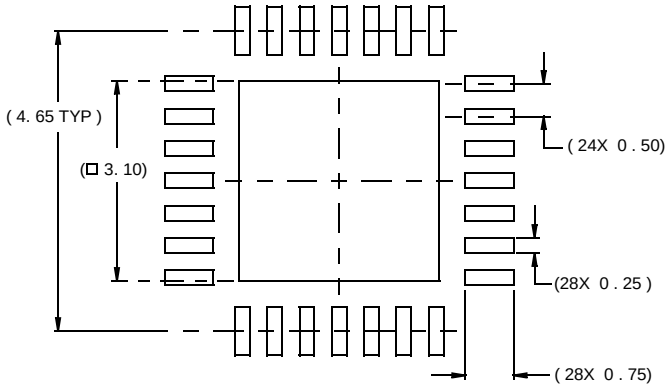
28 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 2, 10/07



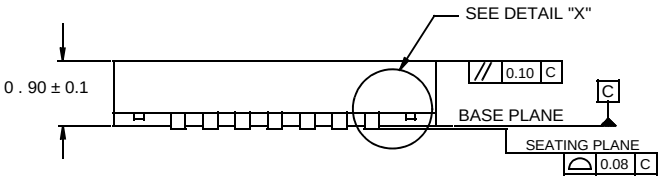
TOP VIEW



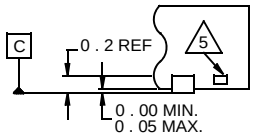
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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