ULTRASONIC-SENSOR SIGNAL CONDITIONER

Check for Samples: PGA450-Q1

FEATURES

- **Dual NMOS Low-Side Drivers**
- **Configurable Burst Generator**
- **Low-Noise Amplifier**
- **12-Bit SAR ADC**
- **Configurable Digital Band-Pass Filter**
- **Digital Signal Envelope Detect**
- **On-Chip 8-Bit Microprocessor**
- **LIN 2.1 Physical Interface and Protocol**
- **Watchdog Timer**
- **Four-Wire SPI for Testability / Programming**
- **8K Bytes OTP**
- **768 Bytes of FIFO RAM**
- **256 Bytes Scratchpad RAM**
- **8K Bytes of Development RAM**
- **32 Bytes of EEPROM for Application**

APPLICATIONS

- **Automotive Park Distance**
- **Blind Spot Detection**
- **Object Detection Applications**

DESCRIPTION

The PGA450-Q1 is a fully integrated interface device for ultrasonic transducers used in automotive park distance or object detection applications. It incorporates these system blocks: voltage regulators, a 12-bit SAR ADC, an 8-bit microcontroller, a digital band-pass filter, a DAC, dual NMOS low-side drivers, a low-noise amplifier, an oscillator, and a LIN 2.1 physical interface and protocol for interfacing.

The PGA450-Q1 possesses an 8-bit microcontroller and OTP memory for program storage for processing the echo signal and calculating the distance between the transducer and the object. This data is transmitted through the LIN 2.1 communication protocol. The LIN 2.1 physical layer is slave-only and does not implement the LIN wake-up feature. All other LIN 2.1 features can be implemented in software.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FUNCTIONAL BLOCK DIAGRAM

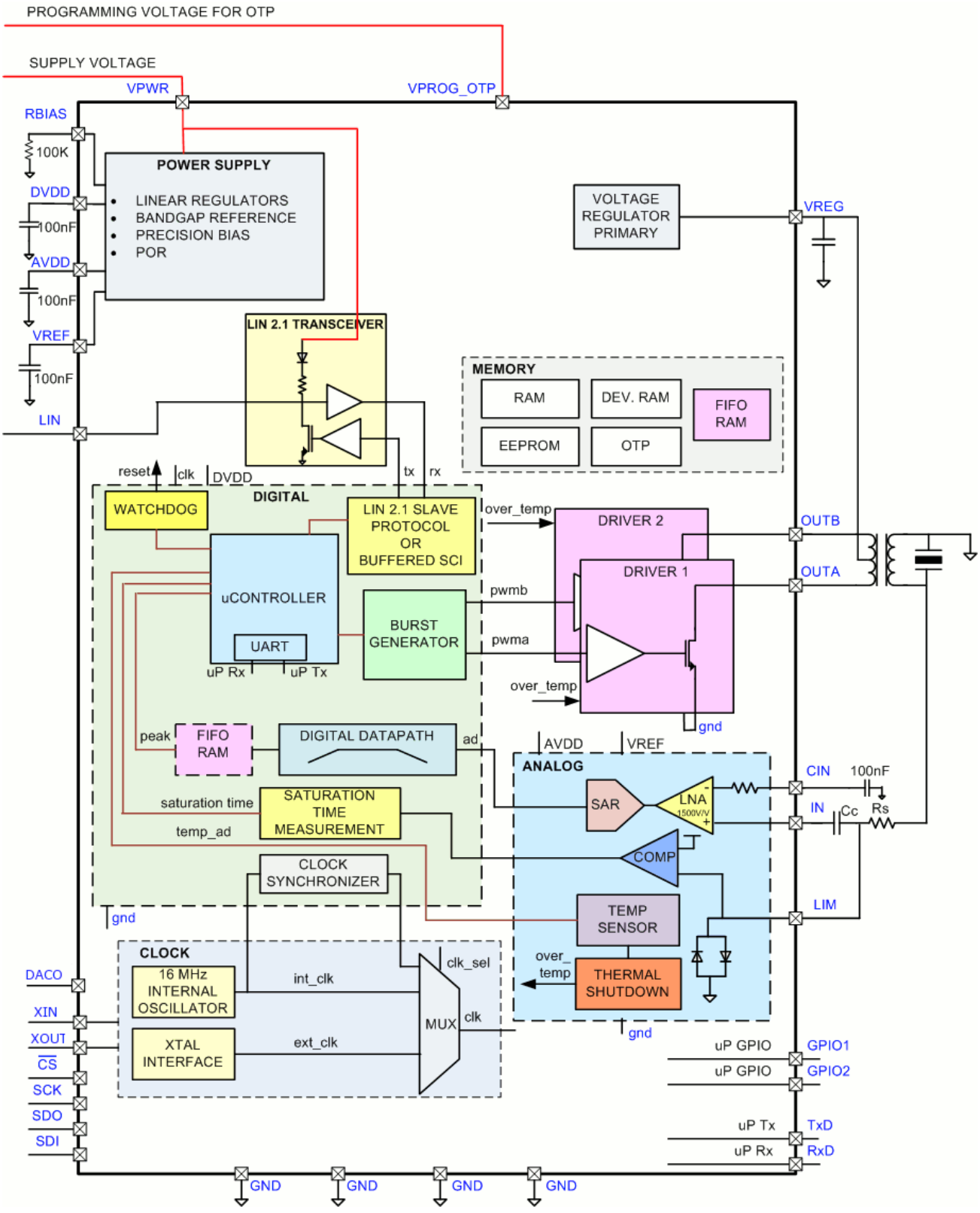


Figure 1.

PW PACKAGE
(TOP VIEW)

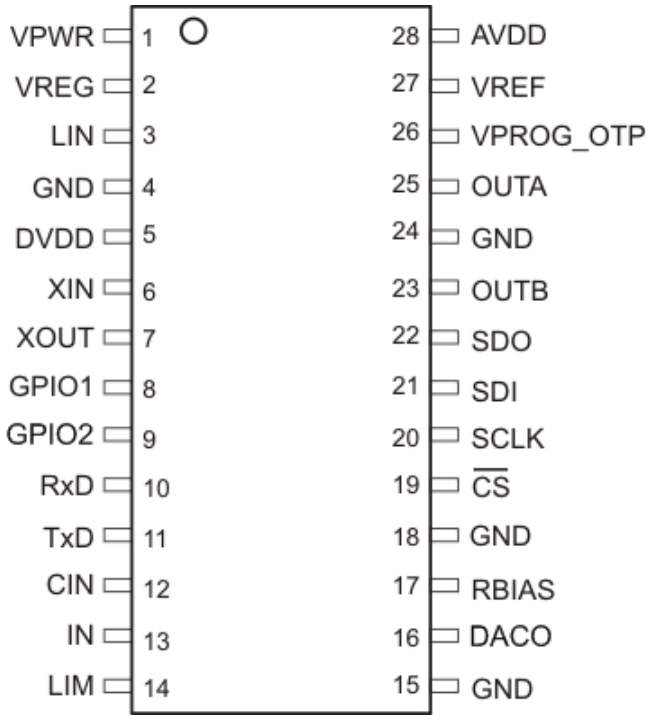


Table 1. TERMINAL FUNCTIONS

PIN NO.	PIN NAME	DESCRIPTION
1	VPWR	Supply voltage
2	VREG	Regulated voltage for transducer
3	LIN	LIN communication bus
4, 15, 18, 24	GND	Ground
5	DVDD	Regulated voltage for digital core
6	XIN	Crystal input
7	XOUT	Crystal out
8, 9	GPIO1, GPIO2	General-purpose I/O 1 and 2
10	RxD	8051W UART Rx (Port 3_0)
11	TxD	8051W UART Tx (Port 3_1)
12	CIN	Input capacitor
13	IN	Transducer receive input
14	LIM	Transducer receive limit
16	DACO	DAC output
17	RBIAS	Bias resistor (100 kΩ to ground)
19	$\overline{CS}$	SPI chip select
20	SCLK	SPI clock
21	SDI	SPI slave data in
22	SDO	SPI slave data out
23	OUTB	Transducer drive output B
25	OUTA	Transducer drive output A
26	VPROG_OTP	OTP programming voltage
27	VREF	Reference voltage for A/D converter
28	AVDD	Regulated voltage for analog

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	MAX	UNIT
VPWR	Power-supply voltage	Relative to GND	–0.3	40	V
VREG	Voltage on VREG, VPROG_OTP pin		–0.3	10	V
VLIN	Voltage on LIN		–27	40	V
VBIAS	Voltage on RBIAS, CIN, IN		–0.3	3	V
VDVDD	Voltage on DVDD, XIN, XOUT		–0.3	2	V
VOUT	Voltage on OUTA, OUTB		–0.3	40	V
VLIM	Voltage on LIM		–1.5	1.5	V
VMAX	Voltage on all other pins		–0.3	6	V
IFET	Low-side FET current			1.5	A
	ESD – HBM on all pins	AEC-Q100-002		2	kV
	ESD – HBM on LIN, per IEC61000-4-2:1995 specification, contact with no external capacitor			8	kV
	ESD – CDM all pins	AEC-Q100-011		500	V
	ESD – CDM corner pins			750	V
T_{Jmax}	Maximum operating junction temperature		-40	150	℃
T_{stg}	Storage temperature		-40	125	℃

(1) Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” are not implied. Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TYP	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	68.7	°C/W
$R_{\theta JC}$	Junction-to-case (top) thermal resistance	11.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	27.6	°C/W

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
VPWR	Power-supply voltage		7		18	V
IPWR	Power-supply current	Power up, T_A = 105°C			50	mA
		Active mode(1) temperature sensor off, T_A = 105°C, VPWR = 18 V			15	mA
		Quiet mode(2), T_A = 105°C, VPWR = 18 V			7.5	mA
$IPWR_{AVG}$	Average power-supply current(3)				10	mA
T_A	Operating ambient temperature		–40		105	℃
C_{VREG}	Capacitance on VREG pin		10		470	µF
C_{VPWR}	Capacitance on VPWR pin(4)		47		100	µF
C_{ESR}	ESR of capacitor on VREG pin			2		Ω

(1) The entire device is active.
(2) LNA, A/D, digital data path, and OUTA/B are OFF. Microprocessor and LIN are still active. Add 100 mA to these currents if capacitor on VREG is charging
(3) The average current is defined as: $I_{pwr}(Average) = 0.3I_{active} + 0.7I_{quiet}$
(4) The capacitor value must allow a discharge rate on VPWR to be 1 V/ms.

ELECTRICAL CHARACTERISTICS

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
$VPWR_{POR}$	VPWR voltage for POR to occur	POR is deasserted		3		4.2	V
V_{AVDD}	AVDD pin voltage	IAVDD = 5 mA		4.75	5	5.25	V
I_{AVDD}	AVDD pin load current					5	mA
V_{DVDD}	DVDD pin voltage				1.8		V
VREF	VREF pin voltage				3		V
t_{PU}	Power-up time – AVDD and DVDD reach regulation levels.	VPWR = 7 V to 18 V, VREG is not in regulation				10	ms
VREG							
$VREG_{TOL}$	Transducer primary voltage tolerance	IREG = 100 µA	VPWR = 7V VREG_SEL = 0_XXX for 4.7 V–5.4 V		±100		mV
			VPWR = 10V VREG_SEL = 1_XXX for 7.7 V–8.4 V		±150		
$VREG_{CHARGE}$	Transducer voltage droop while charging	IREG = 100 mA, below VREG_SEL setting			500		mV
$VREG_{READY}$	VREG_READY threshold	Below VREG_SEL setting			250		
I_{VREG}	VREG output current	VPWR > VREG_SEL + 2.5 V		90	100	110	mA
		VPWR > VREG_SEL + 2 V		100			µA
$VREG_{I\_S2G}$	VREG short-to-ground protection current	VPWR = 16 V, T_A = 105 °C, no burst				110	mA
CLOCK							
F_{OSC}	Internal oscillator frequency	25°C		15.8	16	16.2	MHz
F_{DUTY}	Internal oscillator duty cycle				50		%
	Internal oscillator frequency accuracy	Before LIN sync		–4		4	%
		LIN baud rate = 19.2 kBPS, after LIN sync		–0.5		0.5	%
LOW-SIDE DRIVE MOSFETs							
$r_{ds(on)}$	FET ON resistance	I_{load} = 500 mA, T_A = 105 °C				1.2	Ω
I_{PULSE}	Drain pulse current	50 kHz				1.5	A
	Drive clamping voltage	Vgs = 0 V, I_{dd} = 10 mA		40			V
	Leakage current					5	µA
LOW NOISE AMPLIFIER							
A_V	Gain	LNA_GAIN setting = 0b00		1680	1750	1820	V/V
		LNA_GAIN setting = 0b01		892	930	968	
		LNA_GAIN Setting = 0b10		496	517	538	
		LNA_GAIN Setting = 0b11		99	104	109	
R_{IN}	Input impedance	40 kHz		100			kΩ
	Clamp voltage			–1.5		1.5	V
I_{LIM}	Input current limit					200	mA
	Noise (input-referred of the signal chain)	IN pin = GND, T_A = 105 °C, center frequency = 40 kHz, Bandwidth = 10 kHz			0.7		µVrms
	Input-referred PSRR	VPWR = 7 V, LNA gain setting = 0b00			93		dB
12-bit A/D CONVERTER							
V_{ADCREF}	Input voltage range			0		3	V
	Conversion time				1		µs
	DNL	20% to 80% input range			2.5		LSB
	INL	20% to 80% input range, best-fit curve			4		LSB
	Gain	Best-fit curve		1373	1378	1383	LSB/V

ELECTRICAL CHARACTERISTICS (continued)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
	Offset	Best-fit curve		–15		LSB
8-bit D/A CONVERTER						
V_{DAC_MAX}	Output range		0.133		1.125	V
	Gain			3.9		mV/Code
	Settling time	Code 0x00 to 0xFF step. Output is 90% of full scale. R_{load} = kΩ to GND. C_{load} = 10 pF to GND			20	µs
	Offset voltage	Output when DAC code is 000h at R_{load} = 100 kΩ to GND		0.133		V
	Full-scale voltage	Output when DAC code is 0xFF R_{load} = 100 kΩ to GND		1.125		V
I_{DAC}	Output current	DAC Code = 0x00 DAC Code = 0xFF, R_{load} = 100 kΩ			12.5	µA
	INL		–2		2	LSB
	DNL		–1		1	LSB
	Capacitance load			10		pF
TRANSDUCER SATURATION TIME						
V_{SAT_TH}	Saturation threshold	SAT_SEL = 200 mV		200		mV
		SAT_SEL = 300 mV		300		mV
		SAT_SEL = 400 mV		400		mV
		SAT_SEL = 600 mV		600		mV
TEMPERATURE SENSOR						
	Temperature sensor range		–40		140	°C
	Temperature accuracy	–40°C to 105°C	–5		5	°C
	Temperature sensor code	30°C		0		LSB
	Temperature sensor LSB			1.75		°C/LSB
GPIOs, 8051 UART Tx & Rx						
VIH	GPIO input mode, Rx	R_{load} > 10 kΩ	3.5		5.3	V
VIL			–0.3		1.5	V
R_{PULLUP}	Internal pullup on input	Pullup is to AVDD		100		KΩ
VOH	GPIO strong-mode output, Tx	I_{OH} = 5 mA	4			V
VOL		I_{OL} = 5 mA			0.8	V
	Total current on GPIO1 + GPIO2 +Tx pin	No load on AVDD pin			5	mA
8051W WARP CORE						
F_{CORE_CLK}	Core frequency			16		MHz
	Memory interface			1		Wait State
MEMORY						
	OTP programming voltage		7.5	8	8.5	V
	OTP programming current		2		5	mA
	OTP programming time	1 byte	100			µs
	OTP data retention years	105 °C			10	Years
	EEPROM R/W cycles				1000	Cycles
	EEPROM data retention	105 °C			10	Years
	EEPROM programming time	32 Bytes			70	ms
DIAGNOSTICS						
VPWR_OV	VPWR overvoltage level		25	28	32	V
AVDD_UV	VPWR for AVDD undervoltage			5.6		V
AVDD_OC	AVDD Overcurrent		45	55	65	mA

ELECTRICAL CHARACTERISTICS (continued)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
RBIAS_OC	RBIAS Overcurrent		65	80	90	uA
	Low-side driver A/B drain monitor		2.2	2.5	2.8	V
	Low-side driver A/B monitor		2.2	2.5	2.8	V
	Low-side driver A/B fault deglitch time	LS_FAULT_TIMER_2 = 1 µs setting		1		µs
		LS_FAULT_TIMER_2 = 2 µs setting		2		µs
	Main oscillator underfrequency fault				14	MHz
	Main oscillator overfrequency fault		18			MHz
	Software watchdog time-out			250		ms
	Over temperature shut-off protection		150		200	℃

ELECTRICAL CHARACTERISTICS – LIN 2.1 SLAVE/BUFFERED SCI

PARAMETER		CONDITION	MIN	TYP	MAX	UNIT
LIN Mode: LIN 2.1 physical layer and LIN protocol (Section 2.1 of LIN 2.1) specification Exceptions: No wake-up (Section 2.6.2 of LIN 2.1) No transport layer in digital logic (Section 3 of LIN 2.1) No node configuration and identification services in digital (Section 4 of LIN 2.1) No diagnostic layer in digital logic (Section 5 of LIN 2.1) The device is not certified for LIN compliance. Communication baud rate is fixed at 19.2 kBPS. **SCI Mode:** None						
I_{BUS_LIM}	Param 12	V_{BUS}= 18 V	40		200	mA
$I_{BUS\_PAS\_dom}$	Param 13	Driver off, V_{BUS}= 0V, V_{PWR}= 12 V	–1			mA
$I_{BUS\_PAS\_rec}$	Param 14	Driver off, 7 V < V_{PWR} < 18 V, 8 V < V_{BUS} < 18 V, V_{BUS} > V_{PWR}			20	µA
$I_{BUS\_NO\_GND}$	Param 15	GND_{Device} = V_{PWR}, 0 < V_{BUS} < 18 V, V_{PWR} = 12 V	–1		1	mA
$I_{BUS\_NO\_BAT}$	Param 16	V_{PWR}= GND, 0 < V_{BUS} < 18 V			100	µA
V_{BUSdom}	Param 17	Receiver dominant state			0.4	V_{PWR}
V_{BUSrec}	Param 18	Receiver recessive state	0.6			V_{PWR}
V_{BUS_CNT}	Param 19	V_{BUS_CNT} = (V_{th_dom}+ V_{th_rec})/2	0.475	0.5	0.525	V_{PWR}
V_{HYS}	Param 20	V_{HYS} = V_{th_rec} – V_{th_dom}			0.175	V_{PWR}
R_{Slave}	Param 26	Serial resistor	20	30	60	KΩ
D1	Param 27	$TH_{Rec(max)}$ = 0.744 × V_{PWR}; $TH_{Dom(max)}$ = 0.581 × V_{PWR}; V_{PWR}= 7 V...18 V; t_{Bit}= 50 µs; D1 = $t_{Bus\_rec(min)}$/ (2 × t_{Bit}) $Load_1$; C_{BUS} = 1 nF; R_{BUS} = 1KΩ $Load_2$; C_{BUS} = 6.8 nF; R_{BUS} = 660 Ω $Load_3$: C_{BUS} = 10 nF; R_{BUS} = 500 Ω	0.396			
D2	Param 28	$TH_{Rec(min)}$= 0.522 × V_{PWR}; $TH_{Dom(min)}$ = 0.284 × V_{PWR}; V_{PWR}= 7.6 V...18 V; t_{Bit} = 50 µs; D2 = $t_{Bus\_rec(max)}$/ (2 × t_{Bit}) $Load_1$; C_{BUS} = 1 nF; R_{BUS} = 1 kΩ $Load_2$; C_{BUS} = 6.8 nF; R_{BUS} = 660 Ω $Load_3$; C_{BUS}=10 nF; R_{BUS} = 500 Ω			0.581	
D3	Param 29	$TH_{Rec(max)}$ = 0.778 × V_{PWR}; $TH_{Dom(max)}$ = 0.616 × V_{PWR}; V_{PWR}= 7 V...18 V; t_{Bit} = 96 µs; D4 = $t_{Bus\_rec(min)}$ / (2 × t_{Bit}) $Load_1$; C_{BUS} = 1 nF; R_{BUS} = 1 kΩ $Load_2$; C_{BUS} = 6.8 nF; R_{BUS} = 660 Ω $Load_3$; C_{BUS} = 10 nF; R_{BUS} = 500 Ω	0.417			

ELECTRICAL CHARACTERISTICS – LIN 2.1 SLAVE/BUFFERED SCI (continued)

PARAMETER		CONDITION	MIN	TYP	MAX	UNIT
D4	Param 30	$TH_{Rec(min)}$ = 0.389 × V_{PWR}; $TH_{Dom(min)}$ = 0.251 × V_{PWR}; V_{PWR} = 7.6 V...18 V; t_{Bit}= 96 µs; D4 = $t_{Bus\_rec(max)}$ / (2 × t_{Bit}) $Load_1$; C_{BUS} = 1 nF; R_{BUS} = 1 kΩ $Load_2$; C_{BUS} = 6.8 nF; R_{BUS} = 660 Ω $Load_3$; C_{BUS} = 10 nF; R_{BUS} = 500 Ω			0.590	
t_{rx_pd}	Param 31	Propagation delay of receiver R_{RXD} = 2.4 kΩ; C_{RXD} = 20 pF			6	µs
t_{rx_sym}	Param 32	Symmetry of receiver propagation delay rising edge with respect to falling edge R_{RXD} = 2.4 kΩ; C_{RXD} = 20 pF	–2		2	µs
C_{IN}		Input capacitance on LIN pin		60		pF

Figure 2 summarizes the LIN timing details.

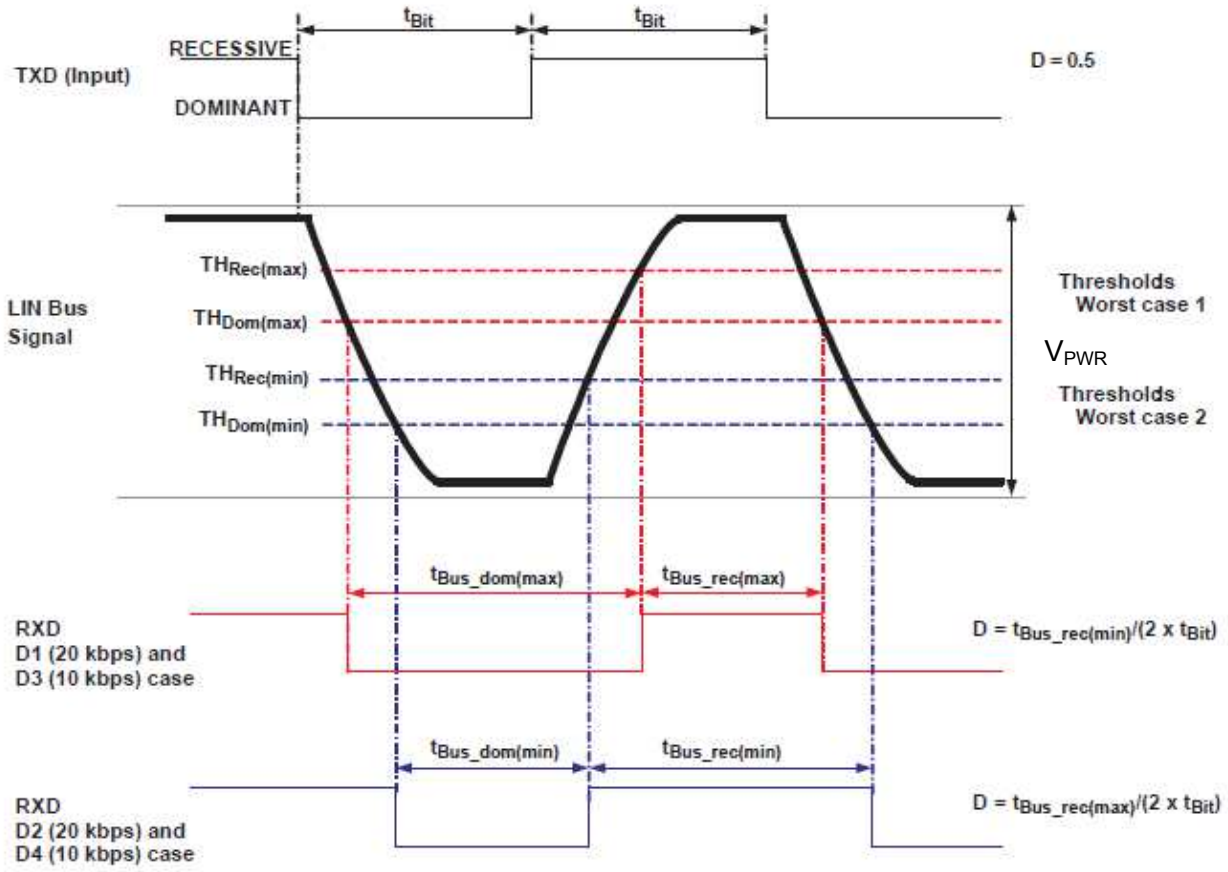


Figure 2. LIN Timing Diagram

ELECTRICAL CHARACTERISTICS – SPI INTERFACE

PARAMETER		CONDITION	MIN	TYP	MAX	UNIT
	High-level voltage ($\overline{CS}$, SCK, SDI, SDO)		3.5			V
	Low-level voltage ($\overline{CS}$, SCK, SDI, SDO)				1.5	V
f_{SCK}	SPI frequency				8	MHz

ELECTRICAL CHARACTERISTICS – SPI INTERFACE (continued)

PARAMETER		CONDITION	MIN	TYP	MAX	UNIT
$t_{\overline{CS}SCK}$	$\overline{CS}$ low to first SCK rising edge		125			ns
$t_{SCK\overline{CS}}$	Last SCK rising edge to $\overline{CS}$ rising edge		125			ns
$t_{\overline{CS}D}$	$\overline{CS}$ disable time		375			ns
t_{DS}	SDI setup time		25			ns
t_{DH}	SDI hold time		25			ns
t_{SDIS}	SDI fall/rise time				25	ns
t_{SCKR}	SCK rise time				7	ns
t_{SCKF}	SCK fall time				7	ns
t_{SCKH}	SCK high time		62.5			ns
t_{SCKL}	SCK low time		62.5			ns
t_{SDO}	SDO enable time				25	ns
t_{ACCS}	SCK rising edge to SDO data valid				25	ns
t_{SDOD}	SDO disable time				25	ns
t_{SDOS}	SDO rise/fall time	C_{SDO} = 10pF	1		15	ns
$C_{L(SDO)}$	Capacitive load for data output (SDO)			10		pF

Figure 3 summarizes the SPI clocking details.

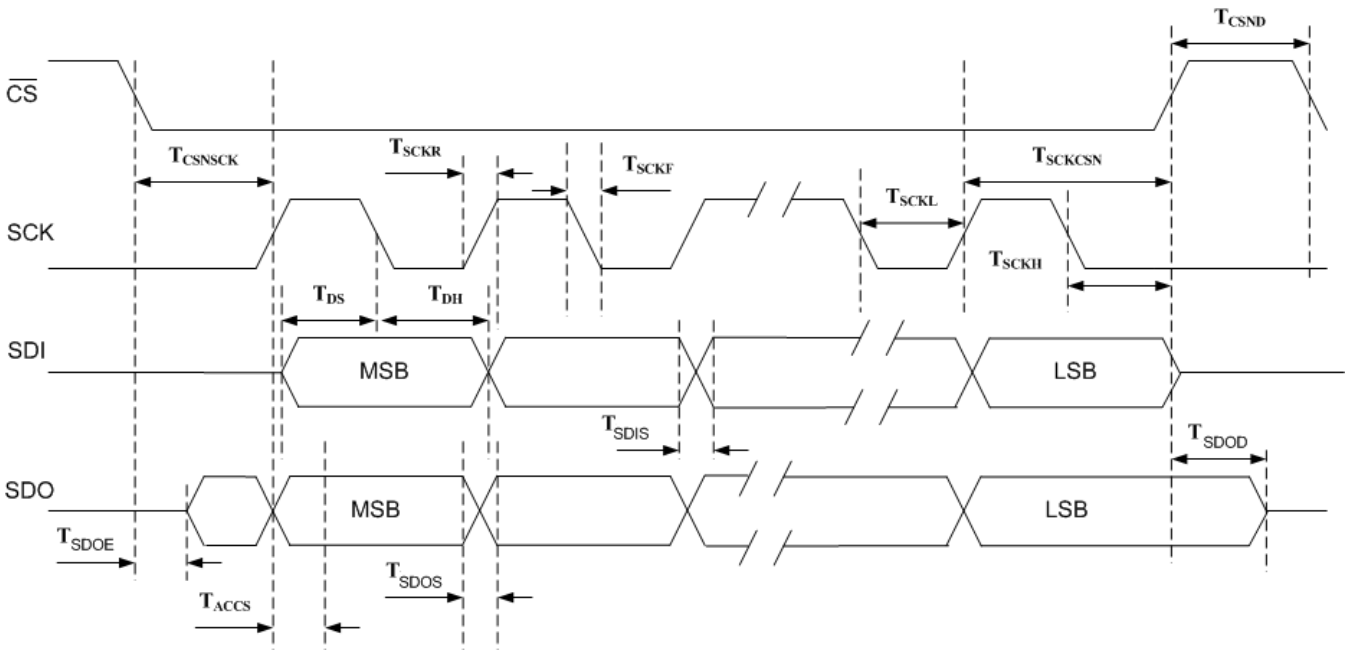


Figure 3. SPI Clocking Details

Typical Characteristics

VPWR = 12 V, T_A = 25°C

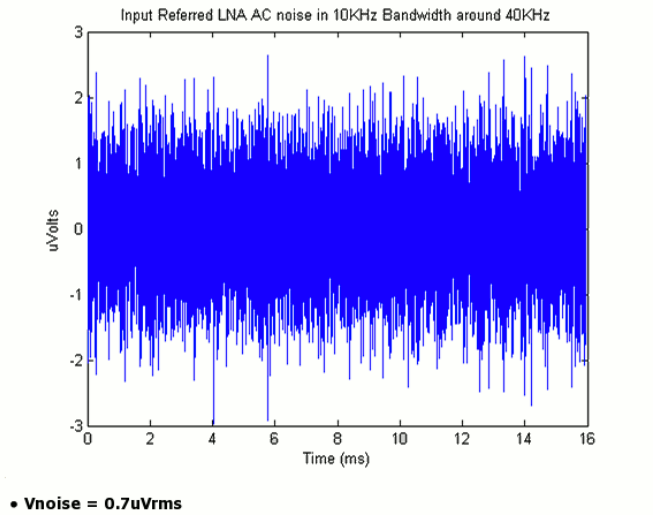


Figure 4. LNA Noise

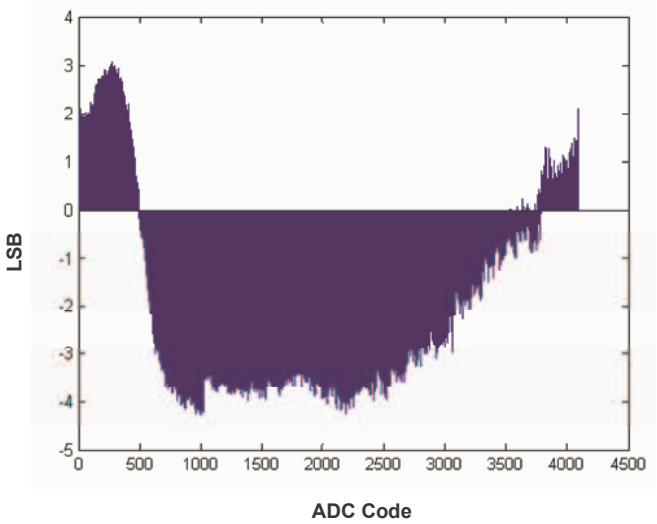


Figure 5. ADC INL

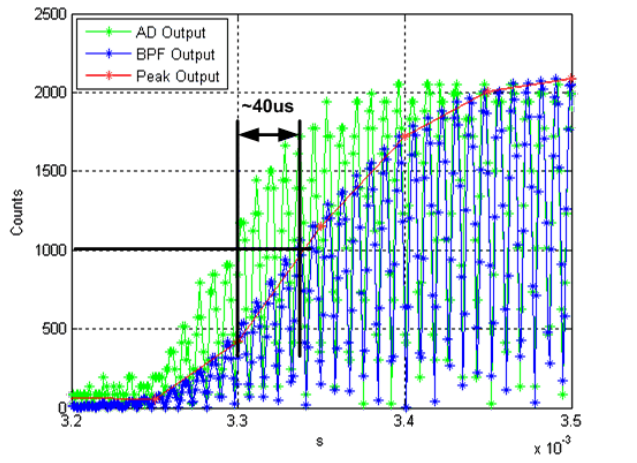


Figure 6. Data-Path Output, Downsample Rate = 40

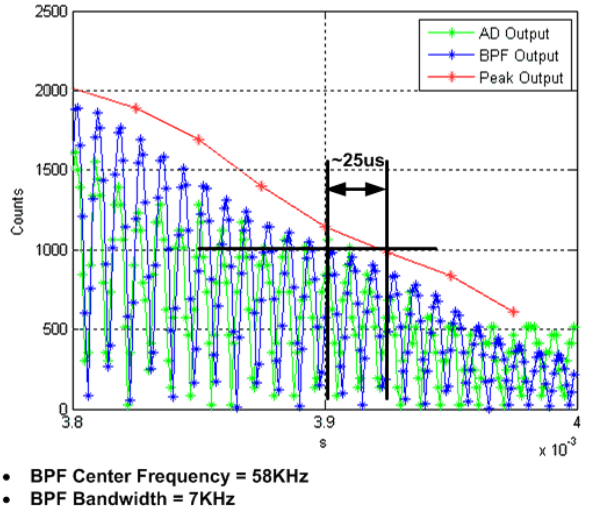


Figure 7. Data-Path Output, Downsample Rate = 25

Function Description

Power Supply Block

PGA450-Q1 uses three internal regulators (AVDD, DVDD, and VREF) as supplies for all the internal circuits. The power-supply block also generates a precision voltage reference, current bias, and internal clock. The internal power-on-reset (POR) signal is released when the internal power supplies, voltage reference, current bias, and internal clock come into regulation.

Figure 8 shows the relationships of the power supplies and the POR signal in the PGA450-Q1.

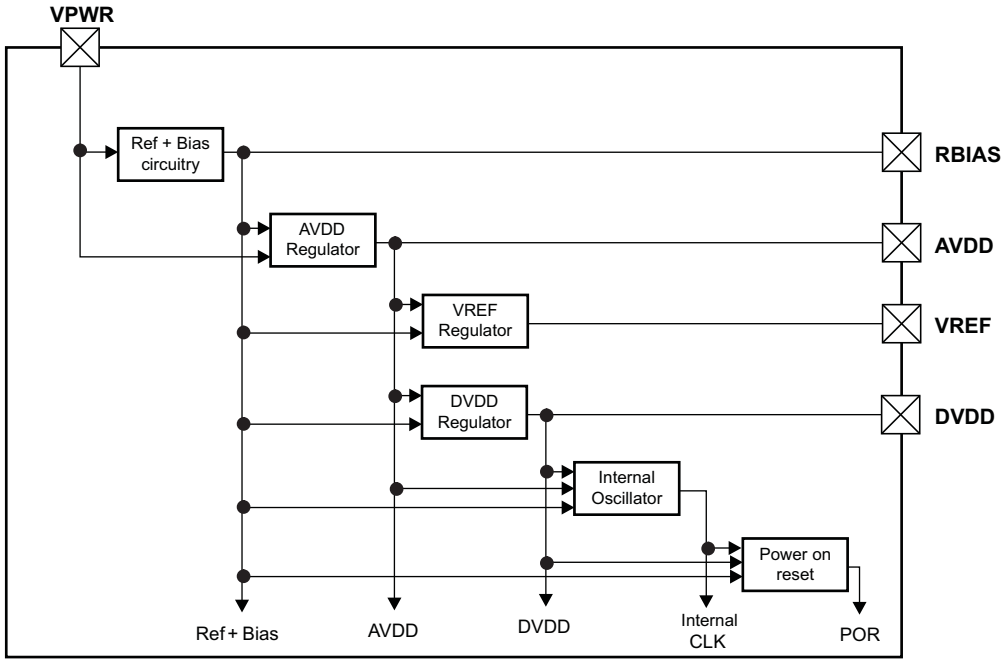
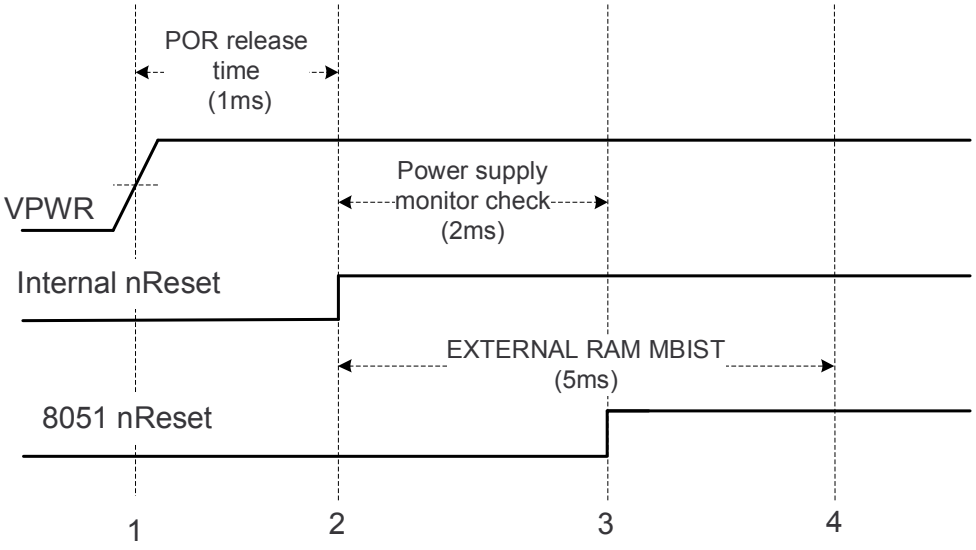


Figure 8. Power-Supply Block

The PGA450-Q1 begins to power up once a voltage is applied to the VPWR pin. A typical power-up diagram is shown in Figure 9. Power-up time is typically about 3 ms.



1. VPWR ramp reached POR level
2. Internal reset to the digital core is released and EXTERNAL RAM MBIST is initiated. SPI communication is available
3. 8051W Reset is deasserted. Software starts execution
4. EXTERNAL RAM MBIST complete. External Scratchpad RAM and FIFO RAM available for use

Figure 9. Power-Up Waveforms

The PGA450-Q1 provides two power-control bits for enabling different analog blocks to manage the total current consumption of the device. On power up, the device is in the *QUIET* mode with only the 8051W and LIN transceiver turned on. All other analog blocks are disabled. Setting the active bit enables the low-side drivers required for bursting as well as the echo-processing circuitry that includes the LNA and the ADC. In addition, a separate control bit is provided to enable the VREG circuitry, which is used to charge the external capacitor used during bursting.

The AVDD pin can be used to source current for up to 5 mA for resistive loads, including the loads on the GPIO and Tx pins.

Table 2. Power Modes

CONTROL BIT		DEFAULT	FUNCTION
1	VREG_EN	Disabled	Enables the VREG circuitry that provides the 100-mA current to charge the external capacitor used during bursting
2	ACTIVE_EN(1)	Disabled	Enables the LNA, ADC, ADC REF and other support circuitry related to burst generation and echo processing

(1) ACTIVE_EN bit must be set before enabling the burst / saturation or echo-enable bits.

VREG

The PGA450-Q1 provides a regulated voltage output which, along with an external capacitor, can be used to drive the primary of the transformer used to excite the transducer. The VREG regulator provides a 100-mA current, sourced from VPWR, to charge the external capacitor. The user can select the desired VREG voltage by setting the VREG_SEL register to the appropriate value.

Note that for VREG to be regulated to the selected voltage, VPWR must be at least 2 V above the selected VREG voltage.

The energy needed for the burst comes from the external capacitor. The device has a VREG_READY status bit in the STATUS2 register to indicate when the capacitor is fully charged and has reached the regulation voltage.

This block is disabled by default. Setting the VREG_EN bit in the PWR_MODE register to high, enables this regulator.

Clock

The clock block generates the system clock that is used in the generation of burst, communication, echo time measurement, and the microprocessor clock.Figure 10 shows the clock block in the PGA450-Q1.

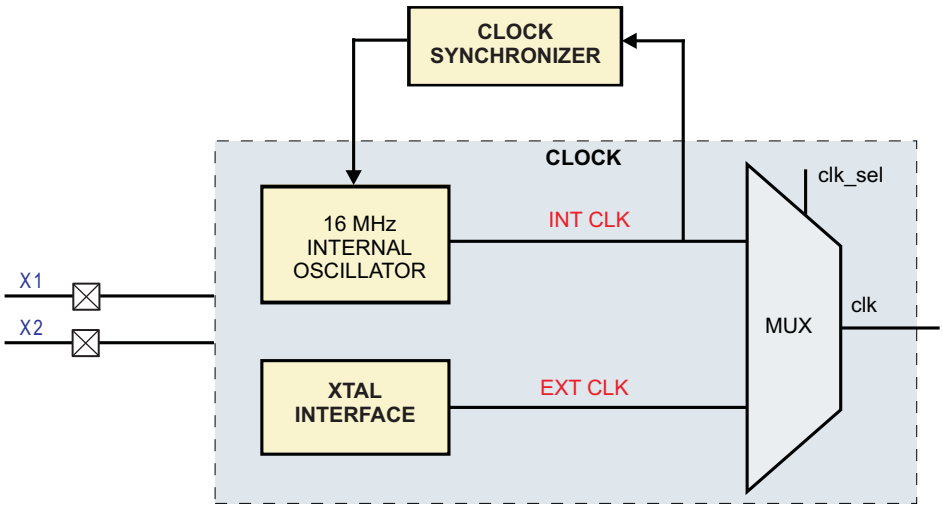


Figure 10. Clock Block in PGA450-Q1

The clk signal provided to various blocks inside the device is derived of one of the following sources:

1. Internal oscillator without synchronization with communication: In this mode, the internal oscillator output is the source for the system clock.
2. Internal oscillator with synchronization with communication: In this mode, the internal oscillator output is *corrected* for inaccuracy using time measurements of the communication bus. Note that this mode requires the implementation of *CLOCK SYNCHRONIZER* logic in the digital control block. The clock synchronizer uses the *SYNC FIELD* to measure the timer value and adjust the internal oscillator output
3. External crystal: In this mode, a 16-MHz external crystal is the source of system clock.

The clock source is controlled by the CLK_SEL register. Table 3 describes the settings of the CLK_SEL bits and the corresponding clock mode.

Table 3. Clock Selection

CLK_SEL BIT VALUES	CLOCK SOURCE
0b00	Internal clock. Ignore the synchronization pulse received on the LIN bus.
0b01	Internal clock. Process the synchronization pulse received on the LIN bus.
0b10	External crystal clock
0b11	Internal clock. Ignore the synchronization pulse received on the LIN bus.

Clock Synchronizer Using the SYNC Field in the LIN Bus

The clock synchronizer block adjusts the internal oscillator based on a SYNC field in the LIN frame received in the communication line. The internal clock is trimmed to 16 MHz with ±4% tolerance in the TI factory.

The clock synchronizer improves the instantaneous accuracy of the internal oscillator frequency to 16 MHz ±0.5% using the LIN SYNC field, assuming an ideal LIN baud rate of 19.2 kBPS. The synchronization algorithm uses the time between two falling edges of the LIN SYNC field to adjust the internal oscillator.

The SYNC_COUNT is available for the 8051W to determine the effectiveness of the synchronization process based on the LIN SYNC field. That is, if the synchronization was effective, then the SYNC COUNT value should be close to 1667 ±8 counts.

This OSC SYNC value can also be updated by the 8051W microprocessor; this field can be updated by the 8051W by setting the OVR bit in OSC_SYNC_CTRL ESFR.

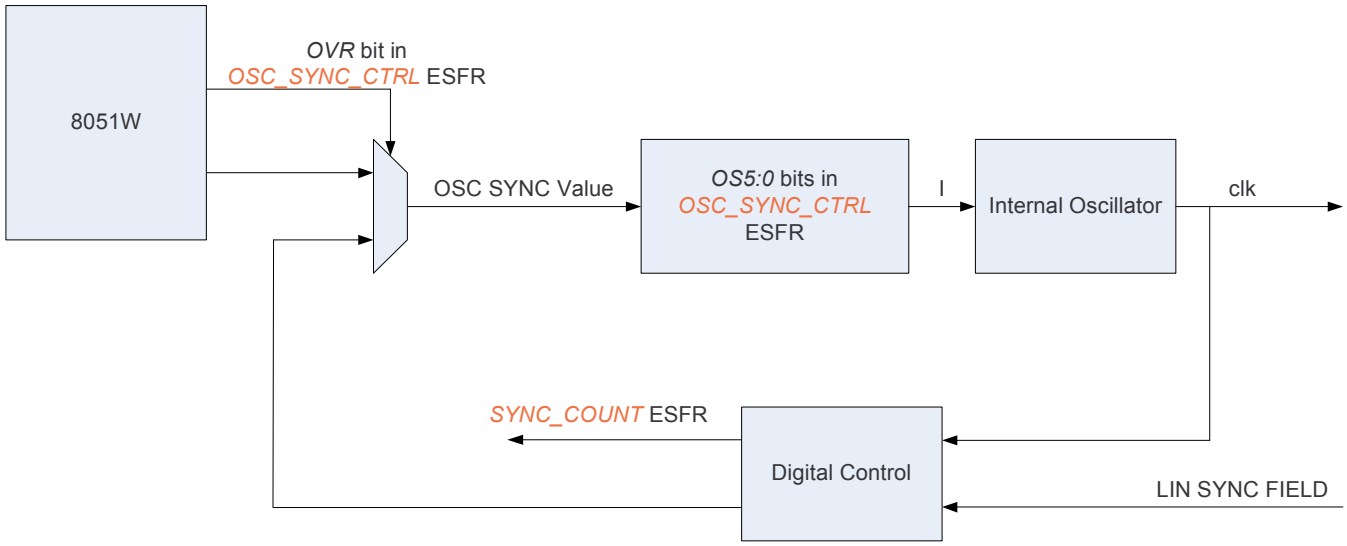


Figure 11. PGA450-Q1 Internal Clock Synchronization Control

The following table describes the value of OS<5:0> and the resulting change in frequency.

Table 4. OS<5:0> versus Delta System Clock Frequency

OS<5:0>	Delta Frequency
0	–3.84 MHz
..	..
31	–120 kHz
32	0 kHz
33	120 kHz
..	..
63	3.72 MHz

NOTE

The clock synchronization feature is not available if the device is configured in SCI buffered mode. (See LIN 2.1 Slave/Buffered SCI for details.)

Low-Side Drive FETs

The PGA450-Q1 provides two low-side drivers for driving the primary of a transformer or an equivalent load. The control/drive modes for the low-side drive are described in the Burst Generator section.

The low driver block also has diagnostics. See the *Diagnostics* section for a description of the diagnostics.

Figure 12 shows the schematic of the low side drive

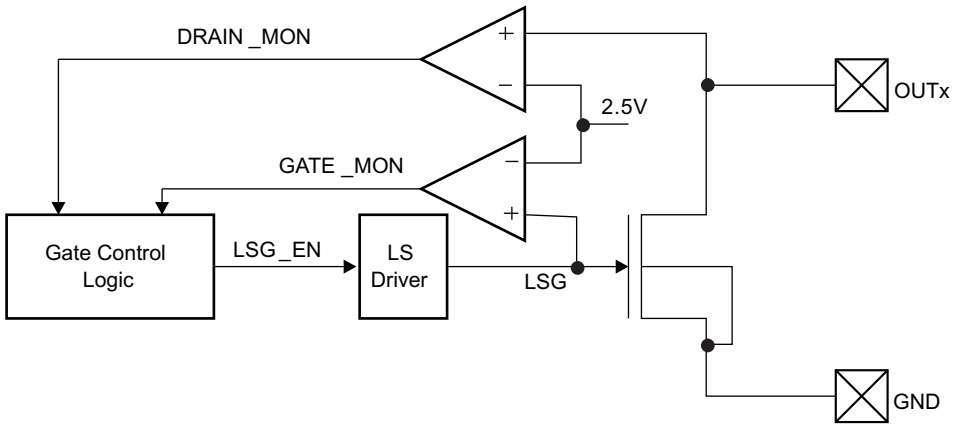


Figure 12. Low-Side Drive Block Diagram

Burst Generator

The burst generator block generates the high-frequency pulses used to drive the gates of the low-side FETs. The low-side FETs ultimately drive the transducer by modulating the primary of the transformer.

The PGA450-Q1 provides MODE bits in the BURST MODE register (see Programmer's Guide, SLDU006) to configure each low-side drive MOSFET in three possible drive modes.

The three possible drive modes are:

1. Single-ended: In this mode, one low-side switch is used to turn current on and off in the primary of the transformer. The rate of change of current in the primary generates a voltage in the secondary of the transformer, which is connected to the transducer.
2. Push-pull: In this mode, two low-side switches are used to turn current on and off in two primary coils in the transformer. The primary coils have the same number of turns. The rate of change of current in the primary generates a voltage in the secondary of the transformer, which is connected to the transducer. The direction of current in the secondary generates voltages of opposite polarity in the secondary, effectively doubling the peak-to-peak voltage in the secondary.
3. 8051W port drive: In this mode, the low-side switches are controlled via an 8051W port pin.

Figure 13 shows the block diagram of the burst generator. The figure shows that the burst generator has a number of registers which the user software must configure.

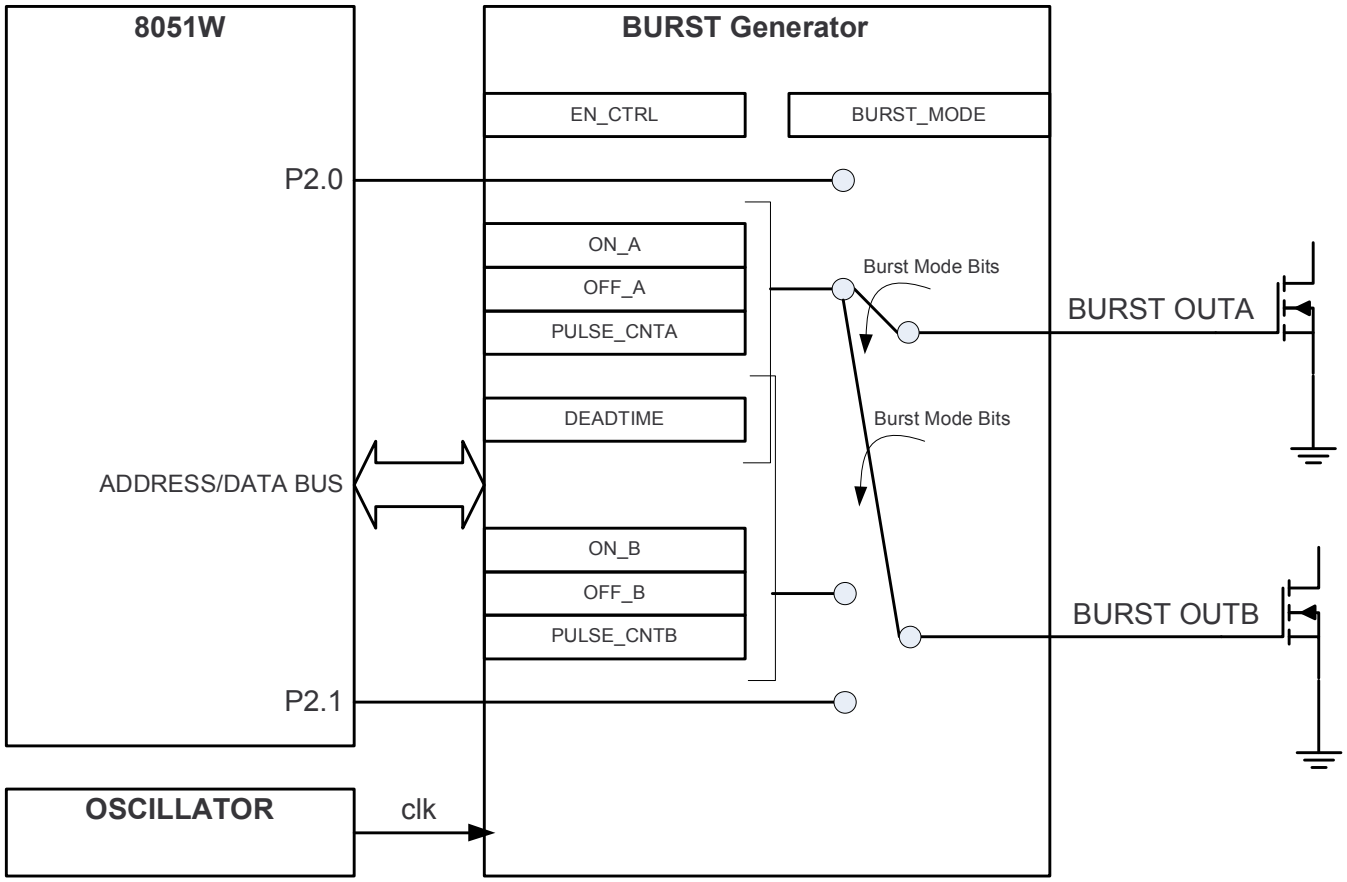


Figure 13. Burst Generator

The PGA450-Q1 provides 3 MODE bits in the BURST MODE register to select from the five burst configurations available. Table 5 describes the modes of operation of the two low-side gate drives of the burst generator. For an understanding of the configurations, see Figure 14 and for an understanding of the waveforms, see Figure 15.

Table 5. Low-Side MOSFET Gate Drive Modes

ITEM	DESCRIPTION
Mode Bits in BURST_MODE Register: 000	
Mode description	LS A and B are in push-pull
Low-side A trigger	Write 1 to BURST_A_EN bit in ENABLE CONTROL register
Low-side B trigger	Write 1 to BURST_A_EN bit in ENABLE CONTROL register
No. of pulses on A	Set by PULSE COUNT A (0–63 pulses) register
No. of pulses on B	Set by PULSE COUNT B (0–63 pulses) register
Low-side A frequency	Set by registers: • BURST_ONA (11 bits at 16 MHz) • BURST_OFFA (11 bits at 16 MHz) • DEADTIME (8 bits at 16 MHz)
Low-side B frequency	Set by registers: BURST_ONA (11 bits at 16 MHz), BURST_OFFA (11 bits at 16 MHz), DEADTIME (8 bits at 16 MHz)
Mode Bits in BURST_MODE Register: 001	
Mode description	LS A is controlled by burst generator A LS B through the internal micro P2.1 port
Low-side A trigger	Write 1 to BURST_A_EN bit in ENABLE CONTROL register
Low-side B trigger	Controlled by 8051W software

Table 5. Low-Side MOSFET Gate Drive Modes (continued)

ITEM	DESCRIPTION
No. of pulses on A	Set by PULSE COUNT A (0–63 pulses) register
No. of pulses on B	Controlled by 8051W software
Low-side A frequency	Set by registers: • BURST_ONA (11 bits at 16 MHz) • BURST_OFFA (11 bits at 16 MHz)
Low-side B frequency	Controlled by 8051W software
Mode Bits in BURST_MODE Register: 010	
Mode description	LS A through the internal micro P2.0 port LS B is controlled by burst generator B
Low-side A trigger	Controlled by 8051W software
Low-side B trigger	Write 1 to BURST_B_EN bit in ENABLE CONTROL register
No. of pulses on A	Controlled by 8051W software
No. of pulses on B	Set by SFR, PULSE COUNT B (0–63 pulses) register
Low-side A frequency	Controlled by 8051W software
Low-side B frequency	Set by registers: BURST_ONB (11 bits at 16 MHz) and BURST_OFFB (11 bits at 16 MHz)
Mode Bits in BURST_MODE Register: 011	
Mode description	LS A is controlled by burst generator A LS B is controlled by burst generator B
Low-side A trigger	Write 1 to BURST_A_EN bit in ENABLE CONTROL register
Low-Side B trigger	Write 1 to BURST_B_EN bit in ENABLE CONTROL register
No. of pulses on A	Set by SFR, PULSE COUNT A (0–63 pulses) register
No. of pulses on B	Set by SFR, PULSE COUNT B (0–63 pulses) register
Low-side A frequency	Set by registers: BURST_ONA (11 bits at 16 MHz) and BURST_OFFA (11 bits at 16 MHz)
Low-side B frequency	Set by registers: BURST_ONB (11 bits at 16 MHz) and BURST_OFFB (11 bits at 16 MHz)
Mode Bits in BURST_MODE Register: 100	
Mode description	LS A through the internal micro P2.0 port LS B through the internal micro P2.1 port
Low-side A trigger	Controlled by 8051W software
Low-side B trigger	Controlled by 8051W software
No. of pulses on A	Controlled by 8051W software
No. of pulses on B	Controlled by 8051W software
Low-side A frequency	Controlled by 8051W software
Low-side B frequency	Controlled by 8051W software
Mode Bits in BURST_MODE Register: 101	
Mode description	For TI Use Only
Low-side A trigger	
Low-side B trigger	
No. of pulses on A	
No. of pulses on B	
Low-side A frequency	
Low-side B frequency	
Mode Bits in BURST_MODE Register: 110	
Mode description	Reserved
Mode Bits in BURST_MODE Register: 111	
Mode description	Reserved

The relationship of BURST_OUTx is shown in Figure 14.

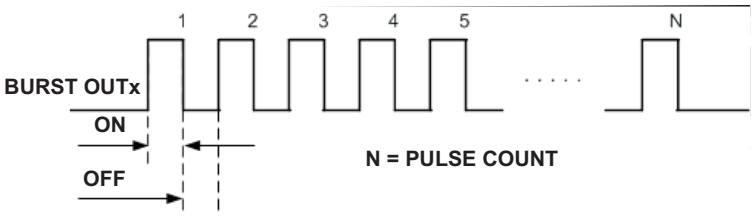


Figure 14. Timing Diagram Showing the Usage of ON Register, OFF Register and PULSE COUNT Register Values

The relationship between ONTIME, OFFTIME and DEADTIME values in the push-pull configuration is shown in Figure 15.

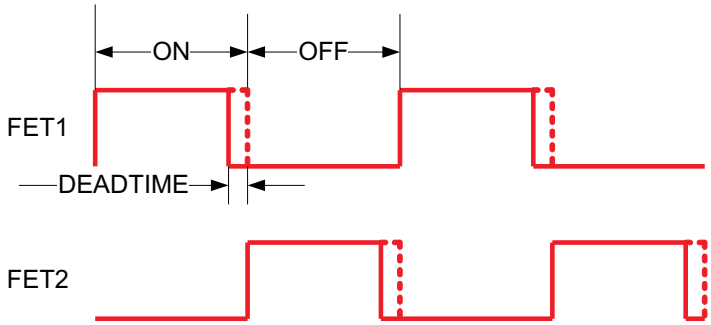


Figure 15. Timing Diagram Showing the Relationship Between ONTIME, OFFTIME, and DEADTIME Registers in the Push-Pull Configuration

In the 8051W drive mode, the 8051W port pins used to drive the OUTA and OUTB pins are listed in Table 6.

Table 6. OUTA/OUTB Pin Map

PGA450-Q1 PIN	8051W PORT
OUTA	2.0
OUTB	2.1

Low-Noise Amplifier

This block is the analog front-end that interfaces with the transducer directly. The echo signal is coupled through an external capacitor so that only the ac component of the transducer voltage is passed to the low-noise amplifier (LNA). The LNA outputs an amplified version of the transducer voltage with a dc offset that is equal to the mid-scale of the A/D converter.

The LNA gain is configurable by setting the LNA_GAIN1 and LNA_GAIN0 bits in the CONTROL_1 register to the appropriate values.

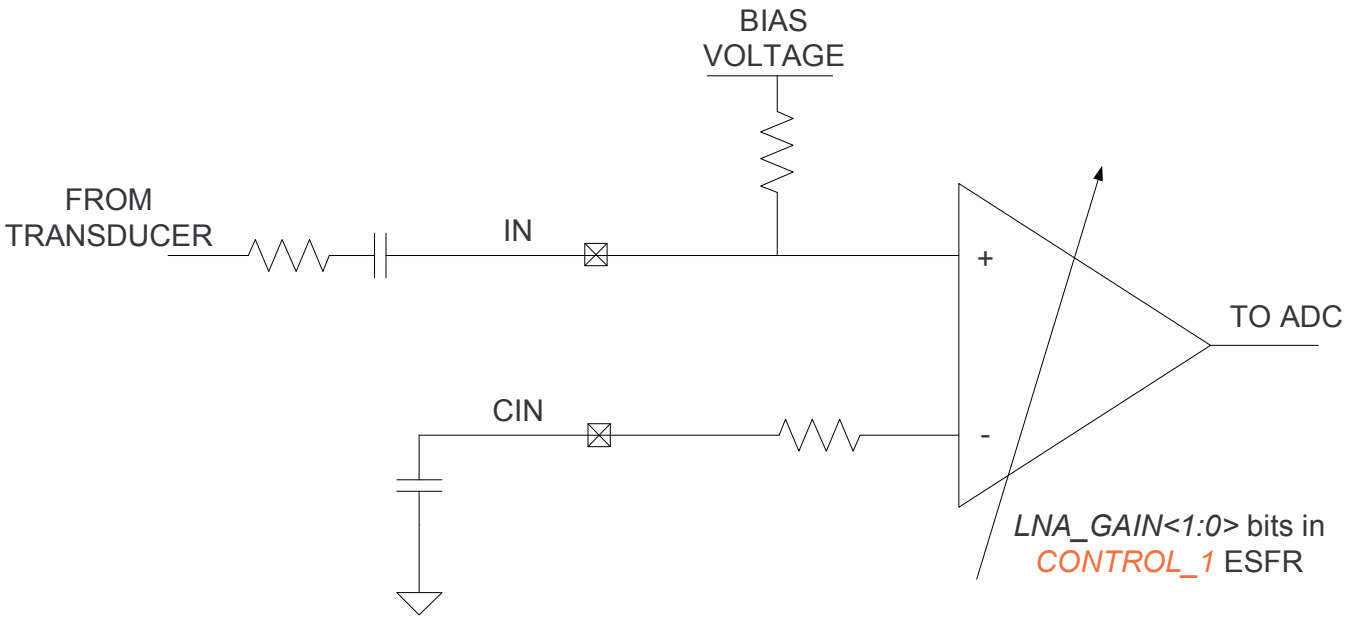


Figure 16. Low-Noise Amplifier

A/D Converter

The 12-bit successive approximation register (SAR) analog-to-digital converter converts the analog voltage from the echo-processing circuit into a digital word. The converted digital word is processed by the band-pass filter. The ADC is dedicated to the echo-processing signal path and is only enabled in active mode.

Digital Data Path

The digital data path processes the A/D sample to extract the peak profile of the echo. The output of the digital data path is stored in the FIFO RAM.

Figure 17 summarizes the digital data path.

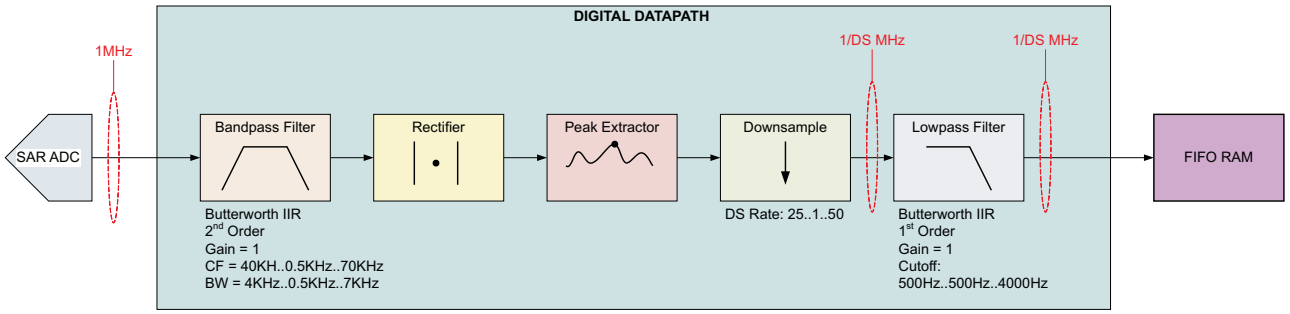


Figure 17. Digital Data Path

The digital data path has the following components:

- Band-pass filter
- Rectifier
- Peak extractor
- Downsampler
- Low-pass filter

Table 7. Digital Data-Path Filter Summary

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Band-pass filter						
Band-pass filter			Second-order Butterworth filter			
Banl-pass center frequency		Programmable	40		70	kHz
Band-pass center-frequency step size		Programmable		0.5		kHz
Band-pass filter bandwidth		Programmable	4		7	kHz
Band-pass filter bandwidth step size		Programmable		0.5		kHz
BPF gain				0		dB
Downsample						
Downsample rate			25		50	Samples
Downsample-rate step size				1		
Low-pass filter						
LPF cutoff frequency			0.5		4	KHz
LPF cutoff frequency step size		Programmable		0.5		KHz
LPF gain				0		dB

Each of the digital data-path components is described in the following subsections.

Band-Pass Filter (BPF)

The echo signal is an amplitude-modulated signal with the underlying carrier frequency equal to the drive frequency of the ultrasonic transducer. The band-pass filter block allows frequencies near the drive frequency to pass to downstream signal blocks.

The band-pass filter is a second-order Butterworth IIR filter. The user can configure the center frequency and the bandwidth of the filter by writing specific values to coefficient registers BPF_B1, BPF_A2, and BPF_A3.

Table 9 lists the values (in hex) that must be written to the coefficient registers to realize a bandpass filter of specific center frequency and bandwidth (or Q). It is noted that the stability of the filter is not assured if values other than those listed in Table 9 are written to the registers.

Table 8. Band-Pass Filter Coefficient Values

BW (kHz)	B1 (Hex)	A3 (Hex)
4.0	32D	F9A5
4.5	392	F8DD
5.0	3F6	F815
5.5	459	F74D
6.0	4BD	F687
6.5	520	F5C1
7.0	582	F4FB

Table 9. Band-Pass Filter Coefficient Values

CF (kHz)	BW (kHz)	A2 (Hex)
39	4	F54A
	5	F48B
	6	F3CD
	7	F311
40	4	F4E6
	5	F427
	6	F36A
	7	F2AE
41	4	F480
	5	F3C1
	6	F304
	7	F249
42	4	F417
	5	F358
	6	F29C
	7	F1E1
43	4	F3AC
	5	F2ED
	6	F231
	7	F176
44	4	F33E
	5	F280
	6	F1C4
	7	F10A

Table 9. Band-Pass Filter Coefficient Values (continued)

CF (kHz)	BW (kHz)	A2 (Hex)
45	4	F2CE
	5	F210
	6	F154
	7	F09A
46	4	F25B
	5	F19E
	6	F0E2
	7	F029
47	4	F1E6
	5	F129
	6	F06E
	7	EFB5
48	4	F16E
	5	F0B2
	6	EFF7
	7	EF3E
49	4	F0F4
	5	F038
	6	EF7E
	7	EEC5
50	4	F078
	5	EFBC
	6	EF02
	7	EE4A

Table 9. Band-Pass Filter Coefficient Values (continued)

CF (kHz)	BW (kHz)	A2 (Hex)
51	4	EFF9
	5	EF3E
	6	EE84
	7	EDCC
52	4	EF78
	5	EEBD
	6	EE03
	7	ED4C
53	4	EEF4
	5	EE39
	6	ED80
	7	ECC9
54	4	EE6E
	5	EDB4
	6	ECFB
	7	EC44
55	4	EDE5
	5	ED2B
	6	EC73
	7	EBBD
56	4	ED5A
	5	ECA1
	6	EBE9
	7	EB33
57	4	ECCD
	5	EC14
	6	EB5D
	7	EAA7
58	4	EC3D
	5	EB85
	6	EACE
	7	EA19
59	4	EBAB
	5	EAF3
	6	EA3D
	7	E988
60	4	EB16
	5	EA5F
	6	E9A9
	7	E8F5

Table 9. Band-Pass Filter Coefficient Values (continued)

CF (kHz)	BW (kHz)	A2 (Hex)
61	4	EA7F
	5	E9C8
	6	E913
	7	E85F
62	4	E9E6
	5	E930
	6	E87B
	7	E7C7
63	4	E94B
	5	E894
	6	E7E0
	7	E72D
64	4	E8AD
	5	E7F7
	6	E743
	7	E691
65	4	E80C
	5	E757
	6	E6A4
	7	E5F2
66	4	E769
	5	E6B5
	6	E602
	7	E551
67	4	E6C4
	5	E610
	6	E55E
	7	E4AD
68	4	E61D
	5	E569
	6	E4B8
	7	E407
69	4	E573
	5	E4C0
	6	E40F
	7	E35F
70	4	E4C7
	5	E415
	6	E364
	7	E2B5

Rectifier

The output of the band-pass filter is a signed number. The rectifier rectifies the output of the band-pass filter to create a positive number.

Peak Extractor

The peak extractor in the PGA450-Q1 is a simple moving-peak algorithm. Specifically, the output of the peak extractor is updated if the input to the peak extractor is greater than the previous output of the peak extractor. This algorithm is summarized in Equation 1:

$$y[k] = \{y[k-1], \text{ if } y[k-1] > Px[k], \text{ otherwise } x[k]\} \quad (1)$$

where *y* is the output of the Peak Extractor, *x* is the input to the Peak Extractor, and *k* is the discrete-time step.

The peak extractor algorithm is shown pictorially in Figure 18.

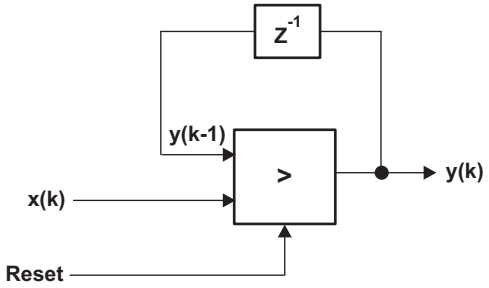


Figure 18. Peak Extractor

Downsample

The downsample block performs two functions:

- Generate reset signal for the peak extractor shown in Figure 18.
- Generate output

The downsample rate can be configured by the user by writing to the downsample register. If the output of the peak extractor must be low-pass filtered before storing it in the FIFO, then the allowable values for the downsample register for the low-pass filter correctly are from 25 to 50; that is,

$$25 \le \text{DOWNSAMPLE} \le 50$$

However, if the user does not need to low-pass filter the output before storing to the FIFO, then the user can configure the DOWNSAMPLE register value to any value between 1 and 63.

The downsample block has a counter which starts at 0 and counts up to the values programmed in the DOWNSAMPLE register. When the count reaches the value in the DOWNSAMPLE register, the counter inside the downsample block is reset to 0. Furthermore, the downsample block generates a reset to the peak extractor. This reset signal sets the output of the peak extractor to 0.

The data output rate of the downsample block is:

$$\text{OUTPUT RATE OF DOWNSAMPLE RATE} = \textit{DOWNSAMPLE} \times 1\ \mu s.$$

Low-Pass Filter

The output of the downsample block can be filtered by a low-pass filter. The low -ass filter in the PGA450-Q1 is a first-order Butterworth IIR filter with configurable cutoff frequency.

The user can configure the cutoff frequency of the filter by writing specific values to coefficient registers LPF_B1 and LPF_A2. Note that for the same desired cutoff frequency, the coefficient values depend on the configured DOWNSAMPLE register.

Table 10 lists the values (in hex) that must be written to the coefficient registers to realize a low-pass filter of specific cutoff frequency. Note that the stability of the filter is not assured if values other than those listed in the table are written to the registers.

Table 10. Low-Pass Filter Coefficient Values

CUTOFF (kHz)	DOWNSAMPLE (Hex)	B1 (Hex)	A2 (Hex)
0.5	19	4D7	7652
	1A	506	75F3
	1B	536	7594
	1C	565	7535
	1D	595	74D7
	1E	5C4	7479
	1F	5F3	741B
	20	622	73BD
	21	650	7360
	22	67F	7302
	23	6AD	72A5
	24	6DC	7249
	25	70A	71EC
	26	738	7190
	27	766	7134
	28	794	70D9
	29	7C1	707E
	2A	7EF	7022
	2B	81C	6FC8
	2C	84A	6F6D
	2D	877	6F13
	2E	8A4	6EB9
	2F	8D1	6E5F
	30	8FD	6E05
	31	92A	6DAC
	32	957	6D53

Table 10. Low-Pass Filter Coefficient Values (continued)

CUTOFF (kHz)	DOWNSAMPLE (Hex)	B1 (Hex)	A2 (Hex)
1.0	19	957	6D53
	1A	9B0	6CA1
	1B	A08	6BF0
	1C	A60	6B41
	1D	AB7	6A92
	1E	B0E	69E5
	1F	B64	6937
	20	BBA	688B
	21	C10	67E0
	22	C65	6736
	23	CBA	668C
	24	D0E	65E4
	25	D62	653C
	26	DB6	6495
	27	E09	63EF
	28	E5B	6349
	29	EAE	62A5
	2A	EFF	6201
	2B	F51	615E
	2C	FA2	60BC
	2D	FF3	601B
	2E	1043	5F7A
	2F	1093	5EDA
	30	10E2	5E3B
	31	1132	5D9D
	32	1180	5CFF

Table 10. Low-Pass Filter Coefficient Values (continued)

CUTOFF (kHz)	DOWNSAMPLE (Hex)	B1 (Hex)	A2 (Hex)
1.5	19	D8C	64E8
	1A	E09	63EF
	1B	E84	62F7
	1C	EFF	6201
	1D	F79	610D
	1E	FF3	601B
	1F	106B	5F2A
	20	1000	5E3B
	21	1159	5D4E
	22	11CF	5C62
	23	1244	5B78
	24	12B8	5A90
	25	132C	59A9
	26	139E	58C4
	27	1410	57E0
	28	1481	56FD
	29	14F2	561C
	2A	1562	553D
	2B	15D1	545E
	2C	163F	5381
	2D	16AD	52A6
	2E	171A	51CC
	2F	1786	50F3
	30	17F2	501C
	31	185D	4F45
	32	18C8	4E70

Table 10. Low-Pass Filter Coefficient Values (continued)

CUTOFF (kHz)	DOWNSAMPLE (Hex)	B1 (Hex)	A2 (Hex)
2.0	19	1180	5CFF
	1A	121D	5BC6
	1B	12B8	5A90
	1C	1352	595C
	1D	13EA	582B
	1E	1481	56FD
	1F	1517	55D1
	20	15AC	54A8
	21	163F	5381
	22	16D1	525D
	23	1762	513B
	24	17F2	501C
	25	1881	4EFE
	26	190F	4DE3
	27	199B	4CCA
	28	1A27	4BB3
	29	1AB1	4A9E
	2A	1B3A	498B
	2B	1BC3	487A
	2C	1C4A	476B
	2D	1CD1	465E
	2E	1D56	4553
	2F	1DDB	444A
	30	1E5F	4342
	31	1EE2	423C
	32	1F64	4138

Table 10. Low-Pass Filter Coefficient Values (continued)

CUTOFF (kHz)	DOWNSAMPLE (Hex)	B1 (Hex)	A2 (Hex)
2.5	19	153D	5587
	1A	15F6	5415
	1B	16AD	52A6
	1C	1762	513B
	1D	1816	4FD4
	1E	18C8	4E70
	1F	1978	4D10
	20	1A27	4BB3
	21	1AD3	4A59
	22	1B7F	4903
	23	1C29	47AF
	24	1CD1	465E
	25	1D78	4511
	26	1E1D	43C6
	27	1EC1	427E
	28	1F64	4138
	29	2005	3FF5
	2A	20A6	3EB5
	2B	2145	3D77
	2C	21E2	3C3B
	2D	227F	3B02
	2E	231A	39CB
	2F	23B5	3897
	30	244E	3764
	31	24E6	3633
	32	257E	3505

Table 10. Low-Pass Filter Coefficient Values (continued)

CUTOFF (kHz)	DOWNSAMPLE (Hex)	B1 (Hex)	A2 (Hex)
3.0	19	18C8	4E70
	1A	199B	4CCA
	1B	1A6C	4B28
	1C	1B3A	498B
	1D	1C07	47F3
	1E	1CD1	465E
	1F	1D99	44CE
	20	1E5F	4342
	21	1F23	41BA
	22	1FE5	4036
	23	20A6	3EB5
	24	2164	3D38
	25	2221	3BBE
	26	22DC	3A47
	27	2396	38D4
	28	244E	3764
	29	2505	35F7
	2A	25BA	348D
	2B	266E	3325
	2C	2720	31C0
	2D	27D1	305E
	2E	2881	2EFE
	2F	292F	2DA1
	30	29DD	2C46
	31	2A89	2AED
	32	2B35	2997

Table 10. Low-Pass Filter Coefficient Values (continued)

CUTOFF (kHz)	DOWNSAMPLE (Hex)	B1 (Hex)	A2 (Hex)
3.5	19	1C29	47AF
	1A	1D14	45D9
	1B	1DFC	4408
	1C	1EE2	423C
	1D	1FC5	4076
	1E	20A6	3EB5
	1F	2184	3CF8
	20	2260	3B41
	21	2339	398D
	22	2411	37DE
	23	24E6	3633
	24	25BA	348D
	25	268B	32E9
	26	275B	314A
	27	2829	2FAE
	28	28F5	2E15
	29	29C0	2C80
	2A	2A89	2AED
	2B	2B51	295E
	2C	2C17	27D2
	2D	2CDC	2648
	2E	2DA0	24C0
	2F	2E62	233C
	30	2F23	21B9
	31	2FE4	2039
	32	30A3	1EBB

Table 10. Low-Pass Filter Coefficient Values (continued)

CUTOFF (kHz)	DOWNSAMPLE (Hex)	B1 (Hex)	A2 (Hex)
4.0	19	1F64	4138
	1A	2066	3F35
	1B	2164	3D38
	1C	2260	3B41
	1D	2358	3950
	1E	244E	3764
	1F	2541	357E
	20	2632	339D
	21	2720	31C0
	22	280C	2FE8
	23	28F5	2E15
	24	29DD	2C46
	25	2AC2	2A7B
	26	2BA6	28B4
	27	2C88	26F0
	28	2D68	2530
	29	2E46	2373
	2A	2F23	21B9
	2B	2FFF	2002
	2C	30D9	1E4E
	2D	31B2	1C9D
	2E	3289	1AED
	2F	3360	1940
	30	3435	1796
	31	350A	15ED
	32	35DD	1446

Data-Path Output Format Control

The output of the data path is stored in the ECHO DATA register. Note that the output of the data-path register is updated at the rate determined by the value in the DOWNSAMPLE register.

The output of the digital data path is also stored in the FIFO RAM. The user can configure of the data stored in the FIFO RAM by writing values to the MODE bits in the FIFO CONTROL register.

Table 11 summarizes the output format of the digital data path that is stored in the FIFO.

Table 11. Digital Data-Path Output Format

MODE BITS	OUTPUT FORMAT	DESCRIPTION
0b00	12 bits	All 12 bits of the digital data-path output are stored in the FIFO. Note that storing 12 bits consumes 2 bytes of the FIFO RAM.
0b01	8 most-significant bits	The upper 8 bits of the 12-bit digital data-path output are stored in the FIFO.
0b10	8 least-significant bits	The lower 8 bits of the 12-bit digital data-path output are stored in the FIFO, if all the upper 4 bits of the digital data-path output are 0s. However, if one of the upper 4 bits of the digital data path is 1, then 0xFF is stored to the FIFO.
0b11	8 middle bits	Bits 10 through 3 of the 12-bit digital data-path output are stored in the FIFO, if the upper 2 bits of the digital data-path output are 0s. However, if one of the upper 2 bits of the digital data path is 1, then 0xFF is stored to the FIFO.

Data-Path Activation and Blanking Timer

The digital data-path calculations can be enabled or disabled using the ECHO_EN bit in the ENABLE CONTROL register. When the ECHO_EN bit is set to 0, the digital data path is disabled; that is, the data path does not perform the calculations and does not update the FIFO RAM. Furthermore, the history of the band-pass and low-pass filters is reset to 0.

When the user sets ECHO_EN to 1, the digital data path begins the computation. However, the output of the data path does not immediately start filling the FIFO RAM. Rather, the output of the digital data path is updated into the FIFO RAM when the user-configured BLANKING_TIMER value has expired.

The user-configurable BLANKING_TIMER register is an 8-bit-register with 16-µs resolution per bit. In other words, the user can set the blanking timer value from 0 µs to 4.08 ms in steps of 16 µs.

Figure 19 summarizes the state of the digital data path based on the enable or disable state of ECHO_EN and the BLANKING_TIMER register value.

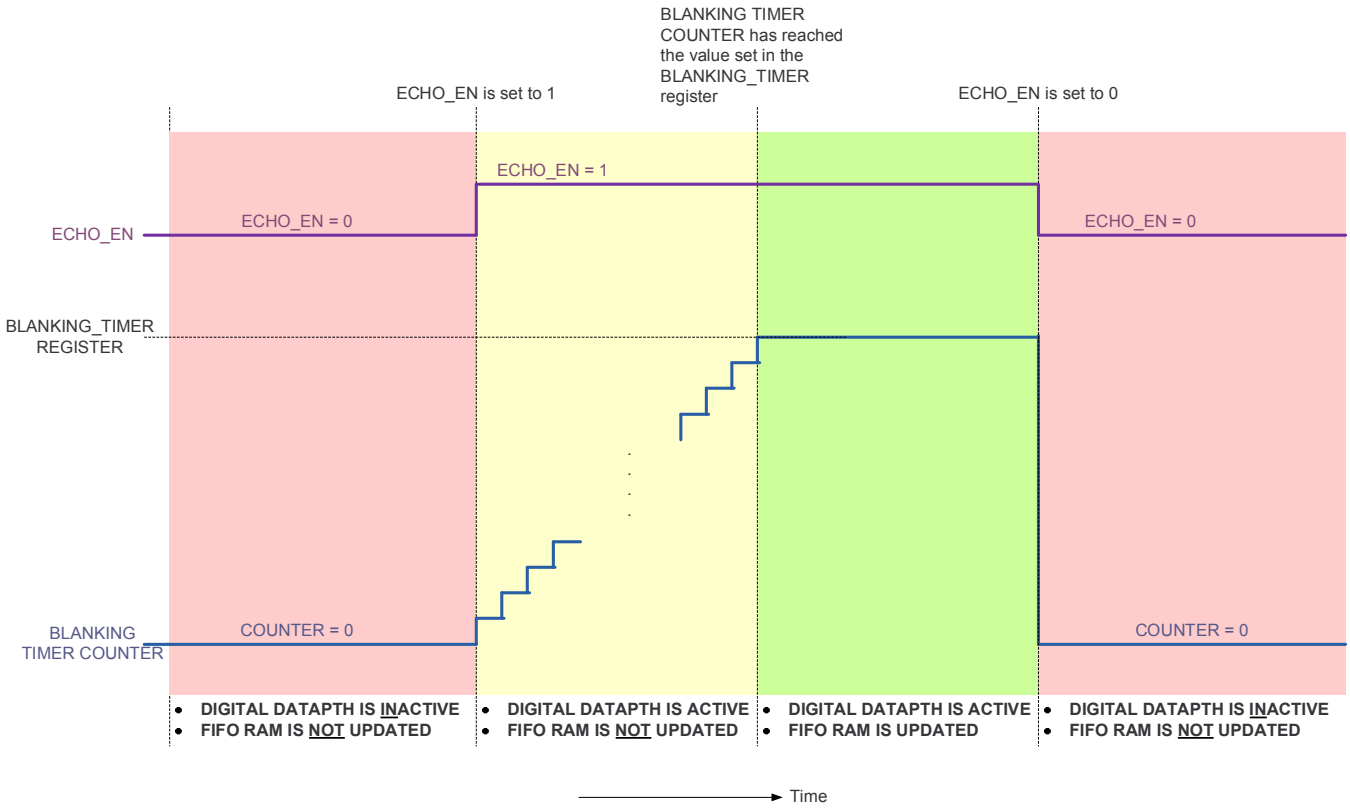


Figure 19. States of Digital Data Path

Digital Data-Path Output Mode

The digital data-path output is available in the analog-voltage mode on the DACO pin with the following constraints:

- The DAC is an 8-bit DAC. That is, the DAC output works only in the 8-bit MSB, 8-bit LSB, or 8-bit middle-significant-bits modes of the digital data-path output.
- The DAC output voltage range is 0.133 V to 1.125 V with 8-bit resolution. The digital data-path outputis directly scaled to the analog output voltage in this range.
- The DAC output voltage resolution is 1/255 V.
- An external amplifier/buffer may be needed before the output of the DAC can be used to drive a load or viewed on a scope.
- The ANALOG MUX ESFR is used to control the availability of the DAC output on DACO pin. The reset state of the DACO is NONE; that is, no internal signal is available until after POR.

- When the digital data-path output on DACO is enabled, the temperature sensor register (TEMP_SENS) is not updated.

In order to enable the TEMPERATURE SENSOR or the DIGITAL DATAPATH ouput, the TS_DAC_EN bit in TEMP_CTRL ESFR must be set to 1. The TS_DAC_MODE bit determines whether the DAC is used for the temperature sensor or the digital data-path output.

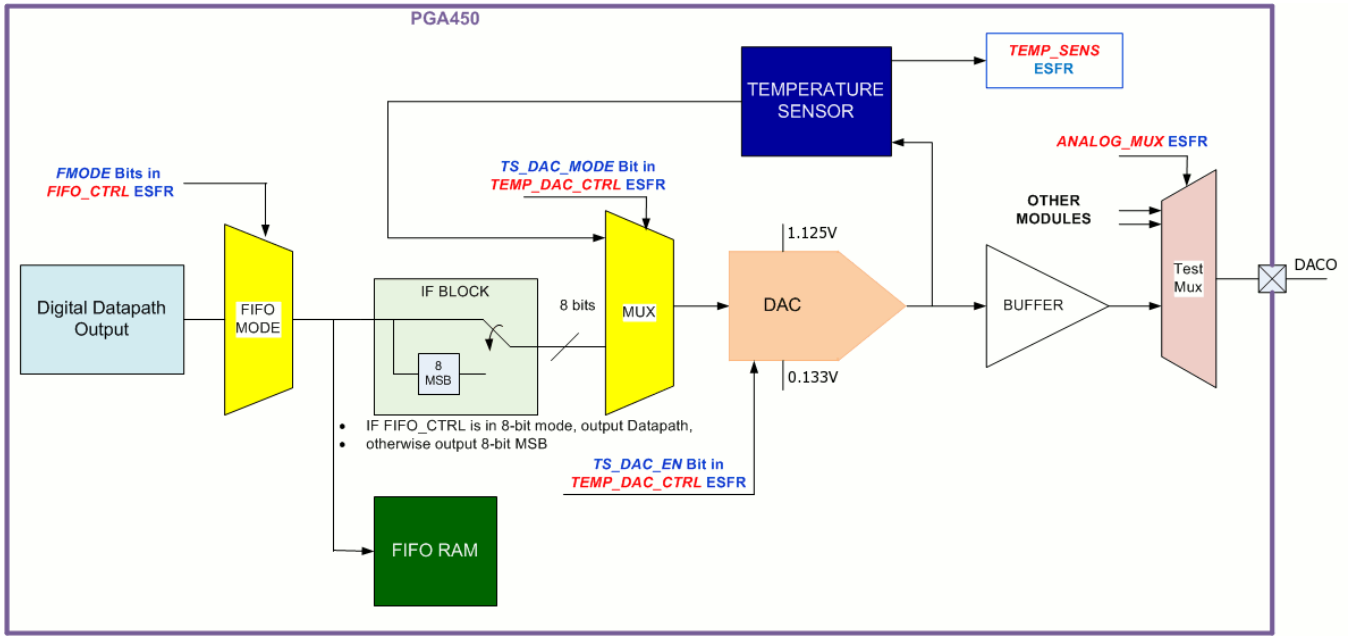


Figure 20. Availability of Digital Data-Path Output as an Analog Output on DACO

Transducer Saturation Time

The transducer saturation block is used to measure the *saturation time* of the transducer. The measurement is based on the voltage at the LIM pin of PGA450-Q1.

The transducer *saturation time* is defined as the time from when the SAT_EN bit in the ENABLE CONTROL register is set to 1 to the time when the voltage at LIM falls below the programmable threshold and stays below that threshold for the programmable deglitch time.

Figure 21 shows the block diagram of the transducer saturation-time measurement block. The saturation-time measurement is accomplished using the following registers.

- SAT_EN bit in ENABLE CONTROL register
- SATURATION THRESHOLD register
- SATURATION DEGLITCH TIME register (8 bits at 2 µs resolution)
- SATURATION TIME CAPTURE register (8 bits at 16 µs)
- SAT_DONE bit in STATUS 2 register

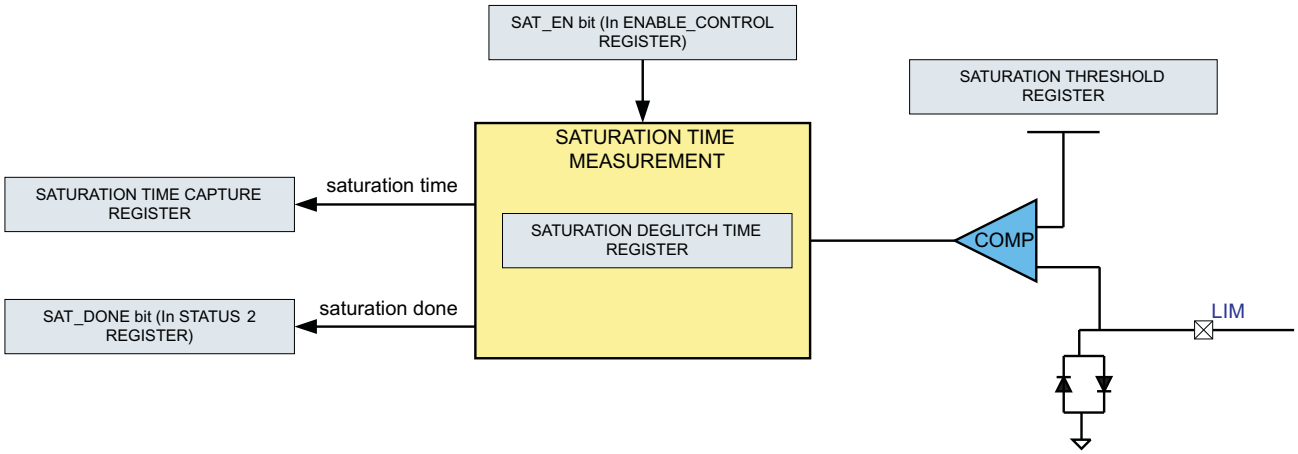


Figure 21. Transducer Saturation-Time Measurement Block

Figure 22 shows the timing diagram of the saturation-time measurement. The figure shows that an internal saturation timer starts when the SAT_EN bit in the ENABLE CONTROL register is set to 1. The saturation-time measurement block then monitors **only** the positive voltage on the LIM pin. When this voltage goes below the programmed threshold in the SATURATION THRESHOLD register, the saturation-time deglitch timer is started.

NOTES:

- When the deglitch timer reaches the programmed deglitch time in the SATURATION DEGLITCH TIME register, the value in the internal saturation timer is captured into the SATURATION TIME CAPTURE register and the SAT_DONE bit is set to 1.
- If the voltage at the LIM pin does not go below the programmed threshold after the SAT_EN bit is set to 1, then the SAT_DONE bit remains at 0. In this case, the maximum value of the SATURATION TIME CAPTURE register is 0xFF.
- Setting the SAT_EN bit to 0 resets the SATURATION TIME CAPTURE register to 0 and sets the SAT_DONE bit to 0.

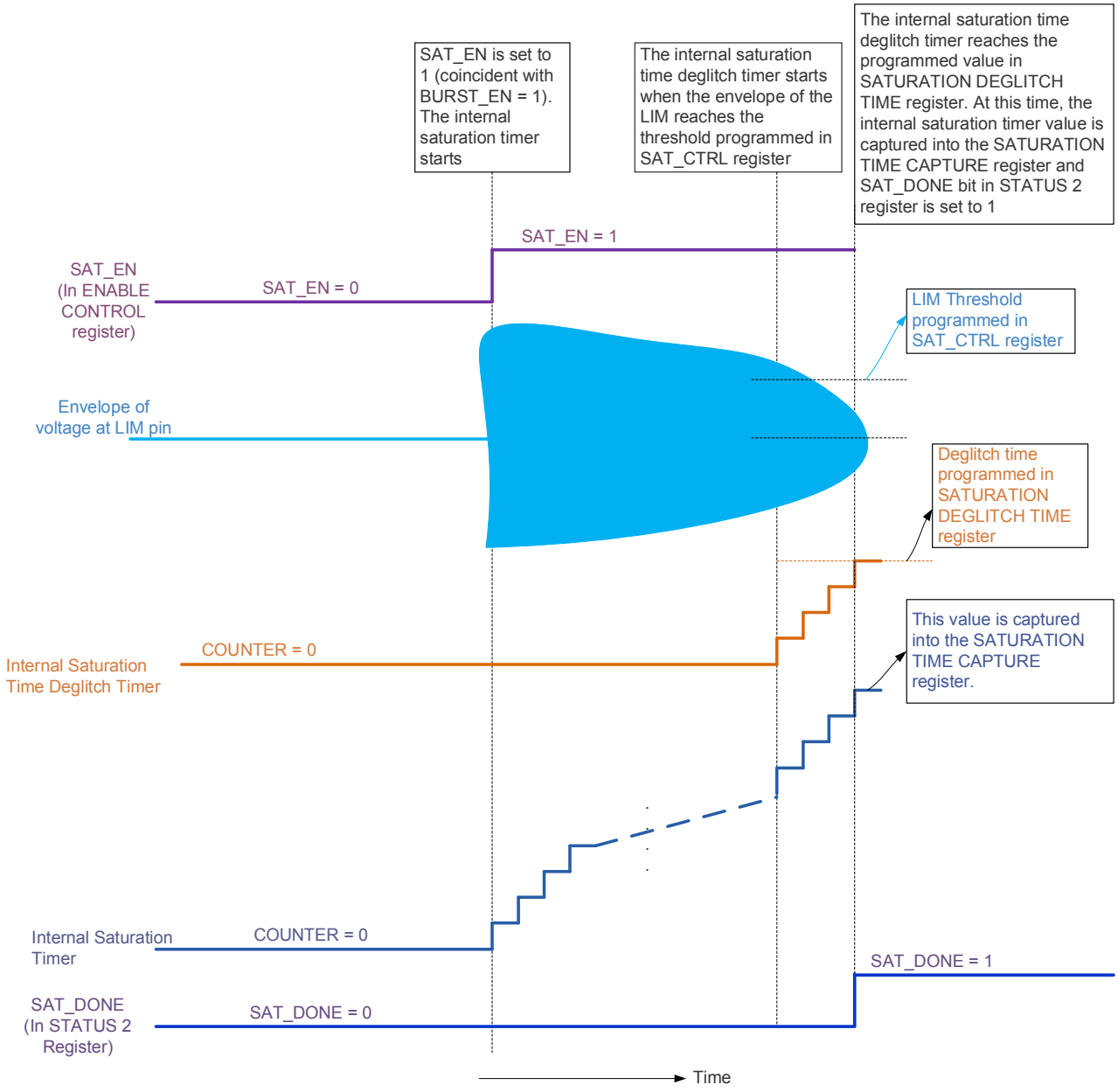


Figure 22. Timing Diagram Showing the Measurement of Transducer Saturation Time

Temperature Sensor

PGA450-Q1 has an on-chip temperature sensor that provides a signed 8-bit 2s-complement output (MSB is the sign bit) with code 0 corresponding to room temperature. The temperature sensor has a typical gain of 1.75°C / code. The temperature sensor is disabled by default. The TS_DAC_EN bit in the TEMP_DAC_CTRL register must be set to enable the temperature sensor. The conversion time is typically 1.4 ms.

The nominal equation for the temperature in °C is as follows:

Temperature = 0.75 × ADC_CODE + 30

Free-Running Timer

The PGA450-Q1 includes a 16-bit free-running timer that operates at a resolution of 1 µs. This timer can be used to synchronize echo transit times between two different PGA450-Q1s by the master ECU in triangulation applications.

This timer starts from a reset value of 0 at POR and counts up. When the timer values reaches 0xFFFF, the timer rolls over to 0x0000.

The value of the free-running timer is not visible to the 8051W. However, the instantaneous value of the free-running timer can be captured into the FREE RUNNING TIMER CAPTURE register by setting the CAP_FR_TIMER bit in the ENABLE CONTROL register to 1.

The FRT ESFR is a shadow of the FREE RUNNING TIMER. The shadow register is not updated continuously. To copy the current value of the FREE RUNNING TIMER into the ESFR, do the following:

- Write a 1 to the CAP_FR_TMR bit in the EN_CTRL register.
- Read the FRT register.

See the Programmer's Guide (SLDU006) for description of the registers.

Note: The reason for implementing the FRT register as a shadow register is to allow the reading of the MSB and LSB coherently. The transfer from the FREE RUNNING TIMER value to FRT register is 16-bit transfer and so is coherent. Because the 8051 can read only 1 byte at a time, coherency is maintained between two MSB and LSB reads of the FRT register because the FRT register value does not change between the reads of the MSB and LSB.

GPIOs

The GPIOx pins on the PGA450-Q1 can be used as either general-purpose inputs/outputs or can be used as inputs/outputs for specific functionality.

In the general-purpose inputs/outputs mode, the GPIOx pins are connected to specific 8051W port pins. User software can be used to control the state of the device pins by controlling the appropriate I/O port SFRs in the 8051W. Table 12 shows the mapping of the PGA450-Q1 GPIOx pins to specific 8051W ports.

Table 12. GPIOx Pin Map

PGA450-Q1 Pin	8051W PORT
GPIO1	3.4
GPIO2	3.5

8051W UART

The TxD and RxD pins on the PGA450-Q1 are connected to the 8051W UART. These two pins can be used either for software debugging or for implementing application-specific protocols.

Table 13. TxD and RxD Pin Functionality

PGA450-Q1 Pin	8051W PORT
TxD	3.1
RxD	3.0

8051 WARP Core

The 8051 WARP core is an exceptionally high-performance version of this popular 8-bit microcontroller, requiring just 2 clocks per machine cycle rather than the 12 clocks per cycle of the industry-standard device, while keeping functional compatibility with the standard part. The 8051W core in the PGA450-Q1 includes two 16-bit timers and a serial interface.

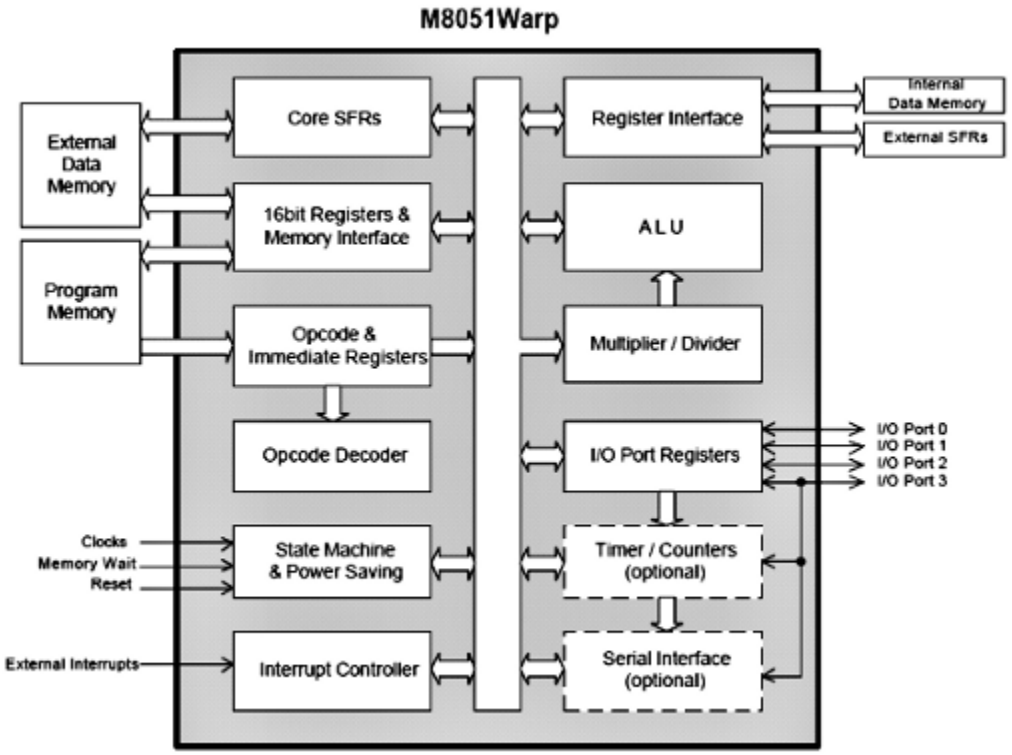


Figure 23. 8051W Core

Memory

PGA450-Q1 has the memory types described in Table 14:

Table 14. Memory

MEMORY	SIZE	DESCRITPTION
FIFO_RAM (1)	768 bytes	Digital data-path output
Scratchpad RAM	256 bytes	Used for software variables
OTP	8K bytes	Program code
EEPROM	32 bytes	Configuration data
DEVELOPMENT RAM	8K bytes	Program code during development

(1) FIFO is needed to allow a second scan of the digital data-path output. The minimum needed for the second scan is 512 bytes. Dual-port capability is needed so that digital data path can fill and the microprocessor can read simultaneously. If a true dual port cannot be implemented, then an interrupt once every X number of bytes are available works. X can be 32 to 128 bytes. 768 bytes are needed to address the microprocessor throughput issue. If throughput of the microprocessor can be improved, 256 bytes could be sufficient.

FIFO Memory for Digital Data-Path Output

The FIFO memory is volatile RAM memory. The output of the digital data path is stored in the FIFO memory.

The FIFO memory is memory-mapped to the 8051W external memory address space; that is, the contents of the FIFO memory are accessible to the 8051W core.

The FIFO memory is a dual-port RAM; that is, that the 8051W can read the FIFO contents while the digital data path is filling the memory.

The FIFO memory also has a FIFO pointer. The FIFO pointer behavior is as follows:

- The FIFO pointer has the address of the last FIFO byte that was filled by the digital data path.
- If the digital data path has been configured to output data in 12-bit format, the FIFO pointer value increases by 2.

- If the digital data path outputs data in 8-bit format, the FIFO pointer value increases by 1.

The FIFO pointer is reset to 0 at power up. Similarly, when the ECHO_EN bit in the EN_CTRL register is set to 1, the FIFO pointer value is reset to 0. However, the FIFO memory contents are not cleared to 0.

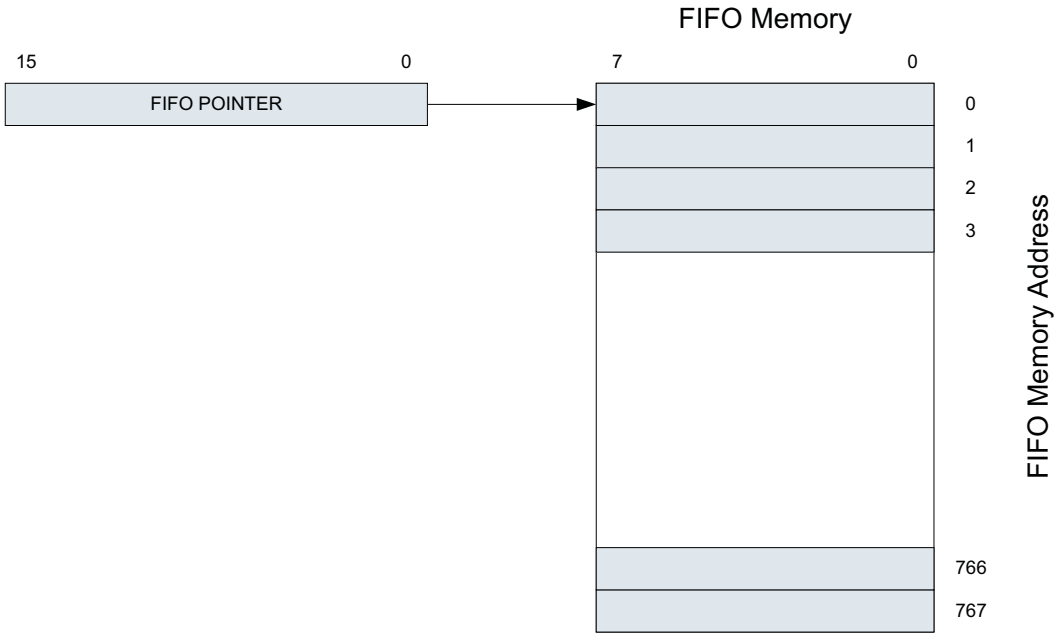


Figure 24. FIFO Memory Organization

OTP Memory for Program

The programming voltage for the OTP memory must be provided externally, because the device does not have a voltage regulator to generate the OTP programming voltage. This voltage must be provided on the VPROG_OTP pin.

OTP Security

PGA450-Q1 provides the ability to LOCK the OTP; that is, the OTP memory cannot be read or programmed via SPI. This feature is called OTP security.

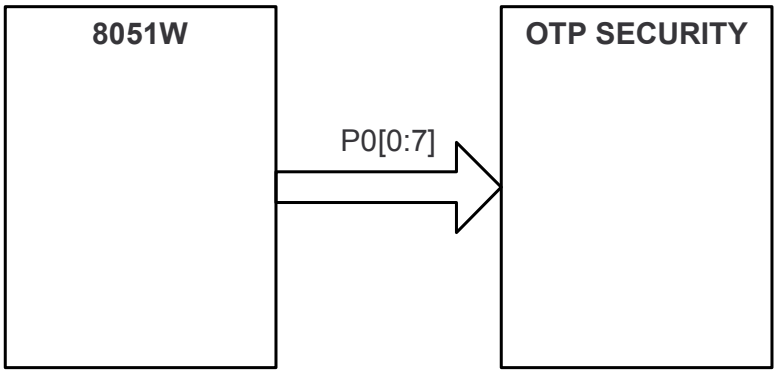


Figure 25. Connection Between the 8051W Core and OTP Security Block

The following is the procedure to LOCK and UNLOCK the OTP

- To LOCK the OTP memory, 8051W P0 should be set to 0xAA in software.
- To UNLOCK the OTP memory, 8051W P0 should be set to 0x00 in software.

NOTE

- It is recommended that P0 be written to appropriated immediately after the 8051W reset is deasserted (that is, immediately after the 8051W starts running software).
- When the OTP memory is in LOCK state, the 8051W processor has access to OTP memory; that is, program execution can continue.
- If the 8051W processor is put in the reset state after a LOCK instruction in software has been executed, the OTP memory cannot be accessed via SPI.

OTP Programming

Both the 8051W microprocessor and the SPI can access the 8K OTP memory. The 8051W has read access only. The SPI has read access and program access.

Prior to starting the OTP programming process, it is required to raise the VPROG_OTP pin on the PGA450-Q1 device to 7.5 V. Once the voltage on this device pin reaches this level, the OTP programming mode is enabled.

(Note that the OTP programming voltage should not be connected to the pin for an extended period of time.)

(Warning: Do not power up OR power down the PGA450-Q1 device with the VPROG_OTP pin set to 7.5V, This may cause unrecoverable corruption to the OTP data.)

Programming of the OTP must be done one address at a time. Each address can only be programmed once. After an address is programmed, it cannot be programmed again unless the entire OTP is erased by a UV-light EPROM eraser. It is possible to program a section of the OTP address space and then program an additional section of OTP address space at a later time.

An OTP programming process starts within the PGA450-Q1 device when an OTP write command is received via SPI.. This process targets the register addressed by the full 13-bit OTP address. The entire OTP programming process for one OTP address takes 100 µs to complete. No write operations to any address should take place during the 11-µs programming time. It takes approximately 1 s to program the entire 8K address space of the OTP with SPI at the 4-MHz SCK frequency.

The following is the OTP memory programming procedure:

1. After power up, set the VPROG_OTP pin to 7.5 V.
2. Send an OTP write command via SPI.
3. **The $\overline{CS}$ pin is set to HIGH at least 100 µs for the OTP programming process to complete**; that is, do not perform any SPI write operations to the OTP during the OTP programming process.
4. Repeat steps 2 and 3 until all desired OTP addresses have been programmed.
5. Before powering down the PGA450-Q1 device, disconnect the 7.5-V supply to VPROG_OTP terminal.

EEPROM Memory for Data

The EEPROM structure in the PGA450-Q1 is shown in Figure 26. The EEPROM structure in PGA450-Q1 includes volatile cache. The cache has one-to-one mapping with the nonvolatile EEPROM memory cells. The EEPROM cache is mapped into the external memory space of the 8051W memory map.

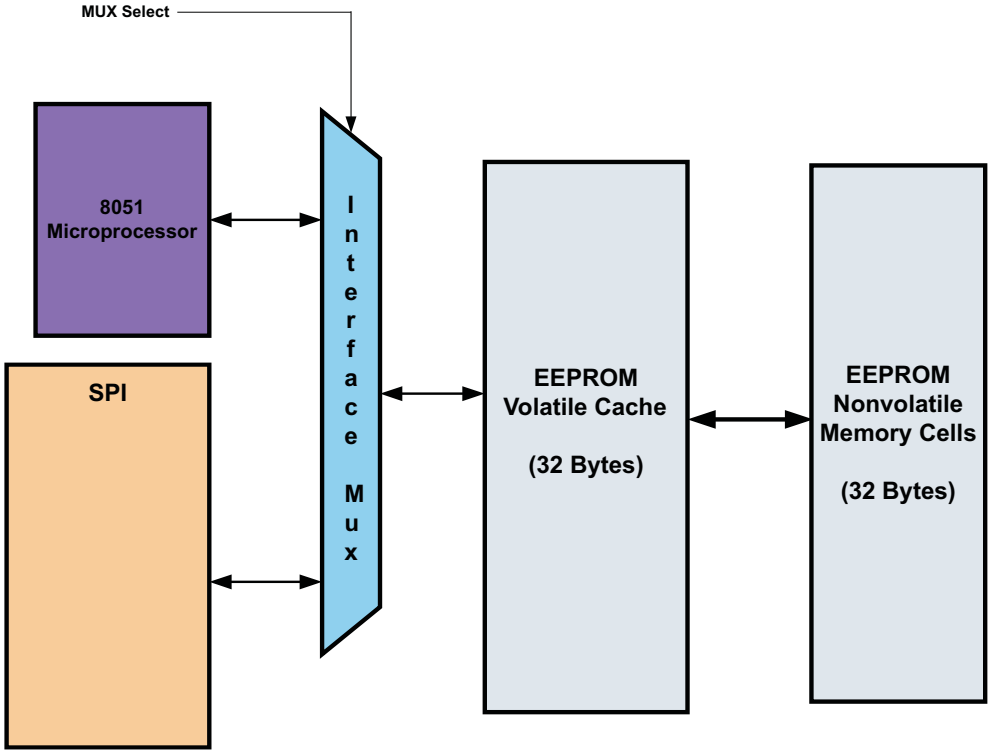


Figure 26. Structure of EEPROM Interface

EEPROM Memory Organization

EEPROM Cache

The EEPROM cache serves as temporary storage of data being transferred to or from EEPROM. Data transferred to the EEPROM cache from either SPI or from the M8051 is byte-addressable, and one byte at time can be written to or read from the EEPROM cache. Selection of the EEPROM cache interface is determined by the internally generated MUX-select bit. The MUX-select bit is by default set to 8051W access. The EEPROM cache is accessible to the SPI when the 8051W is put in reset in the test mode.

When programming an EEPROM via SPI, the EEPROM cache holds the programming data for the amount of time necessary to complete the EEPROM programming process.

EEPROM Memory Cells

The EEPROM memory cells are nonvolatile. The contents of the cache are programmed into the EEPROM when the 8051W requests the programming. The cache is loaded with the contents of the EEPROM memory cells at power up.

Programming EEPROM via 8051W and SPI

The following is the EEPROM memory programming procedure:

1. Write data to EEPROM cache
   - Use the 8051W MOVX assembly instruction to place data in external memory addresses 0x0400 through 0x041F.
2. Write a 1 tothe WRITE bit in the EE_CTRL register.
3. Continuously poll the EE_STATUS bit in EE_CTRL register for the programming status. The EEPROM programming requires 70 ms to complete.

Reloading From EEPROM Cells via 8051W and SPI

The following is the reloading procedure:

1. Write a 1 to the RELOAD bit in the EE_CTRL register. This causes the EEPROM cells to be loaded into cache. The reload operation requires 125 µs to complete.
   – Use MOVX commands to place data in external memory addresses 0x0400 through 0x041F.
2. Use the 8051W MOVX assembly instruction to transfer data from the cache to internal RAM.

LIN 2.1 Slave/Buffered SCI

PGA450-Q1 implements the LIN 2.1 compliant physical layer. This physical layer can be used to communicate data between PGA450-Q1 and the master ECU.

The PGA450-Q1 can be configured to operate in the LIN 2.1 slave-protocol mode or SCI buffered mode. If the device is configured in LIN 2.1 slave-protocol mode, then the protocol layer described in Section 2.1 of the LIN 2.1 specification must be used to communicate with the PGA450-Q1. The device can only be configured as a slave; that is, the PGA450-Q1 cannot be used as a master.

The LIN 2.1 slave protocol implemented in PGA450-Q1 has the following exceptions:

- No wake-up (Section 2.6.2 of LIN 2.1). That is, the device cannot be put to sleep and be woken via LIN.
- No transport layer in digital logic (Section 3 of LIN 2.1)
- No node configuration and identification services in digital (Section 4 of LIN 2.1)
- No diagnostic layer in digital logic (Section 5 of LIN 2.1)
- Communication baud rate is fixed at 19.2 kBPS. That is, the device baud rate is not configurable.

The PGA450-Q1 can also be configured to operate in SCI buffered mode. In this mode, no specific protocol is needed to communicate with the PGA450-Q1; it is up to the user to implement the protocol in software. The device provides the ability either to transmit or to receive 8 bytes of data without any intervention from 8051W software.

The user selects either LIN 2.1 slave mode or SCI buffered mode by setting the LIN_SCI bit in the LIN_SCI select register. If the LIN_SCI bit is changed from LIN mode to SCI mode or vice versa, the communication protocol is reset.

Physical Layer

The physical layer inside the PGA450-Q1 is compliant with the LIN 2.1 specification. Figure 27 shows the line driver/receiver schematic illustrated in the LIN 2.1 specification. The inner dashed box in Figure 27 identifies the part that has been implemented in PGA450-Q1.

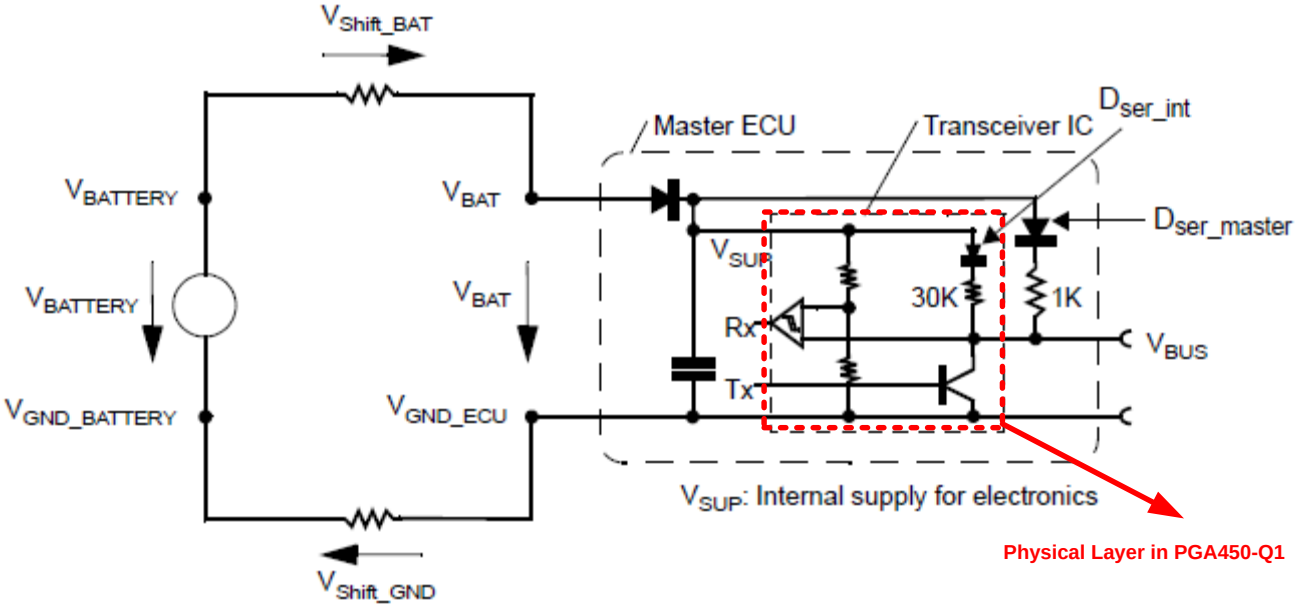


Figure 27. LIN Physical Layer in LIN 2.1 Specification

Figure 28 shows the schematic of the LIN 2.1 physical layer in PGA450-Q1. From this figure, one can infer that the PGA450-Q1 implements the LIN 2.1 slave physical layer.

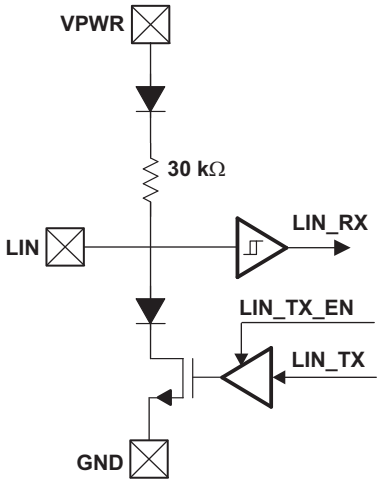


Figure 28. LIN Physical Layer in the PGA450-Q1

LIN Slave Mode

This section describes the LIN slave protocol mode of operation of PGA450-Q1.

LIN Frame

This peripheral handles the LIN 2.1 frames shown in Figure 29. The LIN 2.1 frame has a break field, sync field, PID field, data fields, and checksum field.

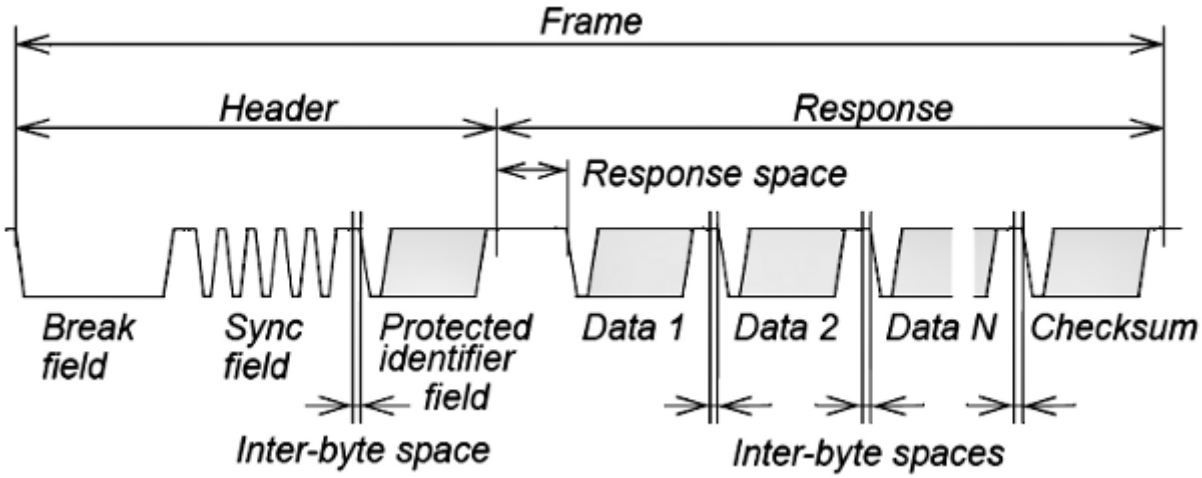


Figure 29. LIN Frame From the LIN 2.1 Specification

Figure 30 shows the LIN byte field. This figure shows that the LIN byte field has 1 start bit and 1 stop bit. The least-significant bit (LSB) is transmitted first.

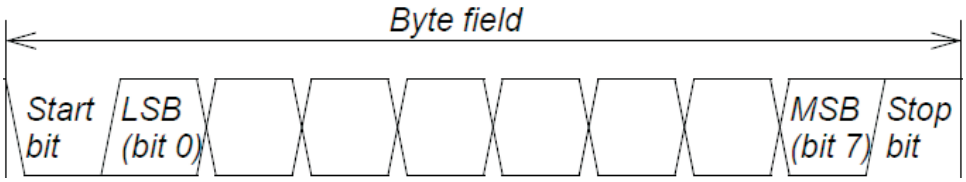


Figure 30. LIN Byte Field From the LIN 2.1 Specification

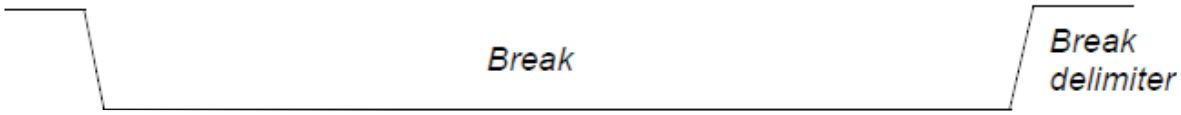


Figure 31. LIN Break Field From the LIN 2.1 Specification

A break field is always generated by the master task (in the master node) and it shall be at least 13 nominal bit times of dominant value, followed by a break delimiter.

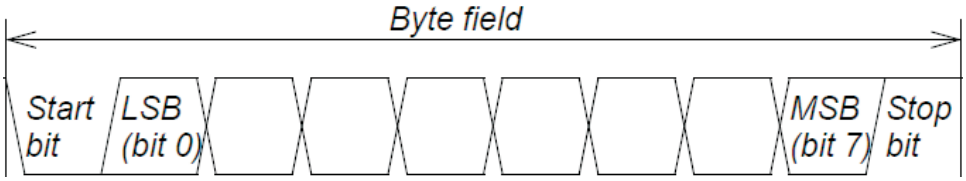


Figure 32. LIN Sync Field From the LIN 2.1 Specification

Sync is a byte field with the data value 0x55.

LIN Registers

Figure 33 shows all the registers associated with the LIN peripheral. From the figure, it can be seen that the LIN PID, RX DATA0–7 and TX DATA0–7 have unique registers associated with them.

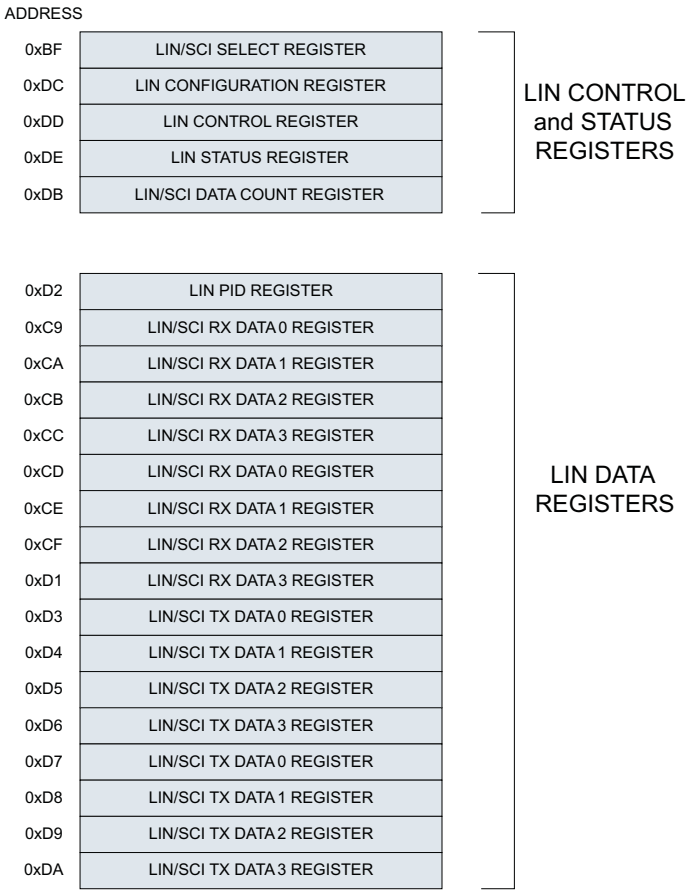


Figure 33. LIN Registers

NOTE

The PGA450-Q1 LIN slave protocol does not decode the LIN PID registers. That is, the decoding logic for the PID registers must be implemented in 8051W software.

LIN Interrupts

Figure 34 shows the four interrupts that the LIN slave protocol generates. These interrupt are:

- SYNC interrupt: This interrupt is generated by the LIN slave protocol when the SYNC field is received. Note that the SYNC field interrupt is generated regardless of whether the subsequent LIN frame fields are received. Thus, the customers can BREAK+SYNC field to synchronize the internal clock and use other protocol for communication.
- PID interrupt: This interrupt is generated by the LIN slave protocol when the PID is received and the PID does not have a parity error.
- RX interrupt: This interrupt is generated by the LIN slave protocol when the PGA450-Q1 is configured to receive the LIN data. The interrupt is generated only when the checksum is received and the checksum has no errors. The device performs the enhanced checksum calculation. According to the LIN 2.1 specification, the enhanced checksum is the checksum calculation over the data bytes and the protected identifier byte.
- TX interrupt: This interrupt is generated by the LIN slave protocol when the PGA450-Q1 is configured to transmit data. The interrupt is generated at the end of the checksum transmission.

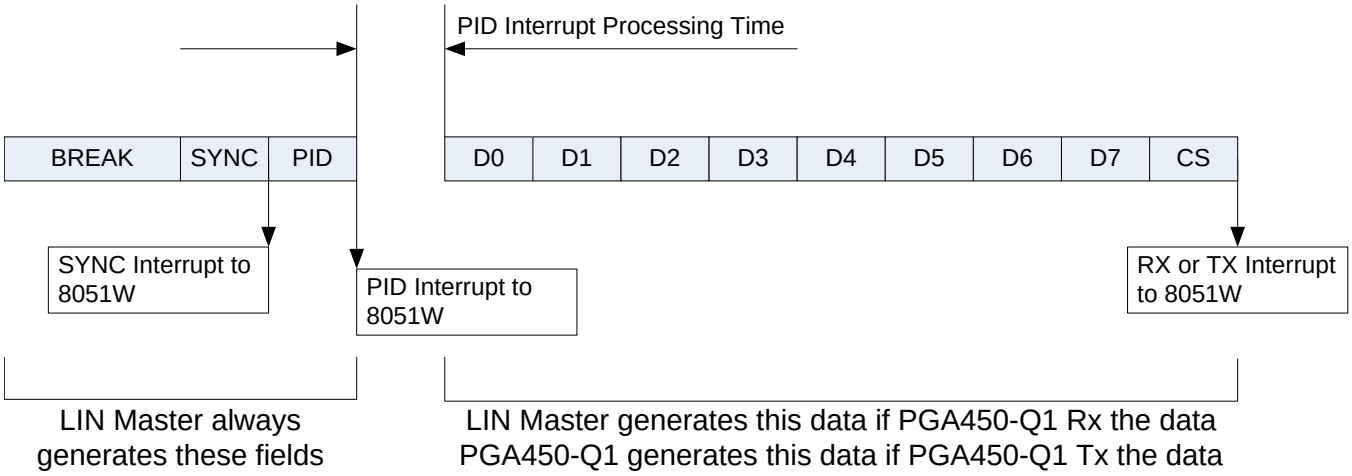


Figure 34. LIN Interrupts

The PID interrupt processing shown in this picture is for a transmit message.

LIN Slave Configuration

The LIN slave in the PGA450-Q1 is configurable. This section describes the available configurations. These configurations are not applicable if the PGA450-Q1 is set up to operate in SCI buffered mode.

The LIN configuration register, LIN_CFG, is used to configure the LIN slave in PGA450-Q1. The following sections describe the possible configurations.

LIN Frame-Control Configuration

The PGA450-Q1 has three bits that control the behavior of PGA450-Q1 when a LIN frame is received.

- **IGNORE_DIAG**: This bit controls the mode of operation of the LIN slave controller when the PID is received.
  If this bit is set to 0, then the LIN slave controller waits for data bytes after the PID field in the LIN frame is received.
  However, if this bit is set to 1, then the LIN slave controller finishes the current frame after the PID is received and waits for the next LIN frame.
- **HOLD:** This bit determines whether the LIN frame received by PGA450-Q1 is processed or ignored.
  If this bit is set to 0 (which is the power ON reset state), then the received LIN frame is ignored.
  If this bit is set to 1, then the received LIN frame is not ignored.
- **CS_METHOD**: This bit controls whether the checksum is classic checksum or enhanced checksum.
  If this bit is set to 0 (which is power ON reset state), the LIN protocol calculates and validates the checksum using the classic checksum method.
  If this bit is set to 1, the LIN protocol calculates and validates the checksum using the enhanced checksum method.

LIN Timing-Control Configuration

The PGA450-Q1 has two bits that control the various timing parameters of the LIN frame.

- **INTERBYTE_SPACE**: This bit controls the duration of the time between the data fields when PGA450-Q1 is transmitting data.
  If this bit is set to 0, then the interbyte space is equal to 1 bit.
  If this bit is set to 1, then the interbyte space is equal to 2 bits.
- **BIT_TOL**: This bit controls the tolerance of bit time that is used in the LIN frame timing diagnostics.
  If this bit is set to 0, the bit time tolerance is 15% of the bit time determined during the LIN SYNC field.
  If this bit is set to 1, the bit time tolerance is 30% of the bit time determined during the LIN SYNC field.

LIN Slave-Protocol State Machine

Figure 35 shows the LIN Slave Protocol state machine implemented inside PGA450-Q1. The figure shows that the protocol enters the Wait-for-Break-Field state on power up. When the master sends the break field, the state machine transitions into the Wait-for-Sync-Field state only if the HOLD bit in the LIN_CFG register is set to 0. Otherwise, the LIN protocol return to the Wait-for-Break-Field state.

After the sync field is received, the state machine generates the SYNC field interrupt and transitions into the Wait-for-PID-Field state. After the PID field is received, the PID parity is checked. If the parity has an error, then the state machine transitions back to the Wait-for-Break-Field state. If there is a parity error, then the state machine generates the PID interrupt to the 8051W.

The user must write software to service the PID interrupt. In the PID interrupt service routine, the user determines whether the received PID corresponds to Rx message or Tx message.

In the case of an Rx message, the state machine waits for all the data bytes to be received. The number of data bytes received is determined by the value in the DATA_CNT register. When all the data bytes are received, then the state machine calculates the checksum. If the calculated checksum matches the received checksum, then the state machine generates an Rx interrupt to the 8051W. Otherwise, the state machine transitions back to Wait-for-Break-Field state.

In the case of a Tx Message, the state machine calculates the checksum based on the data after the 8051W loads the transmit buffers and the DATA_CNT register. At the end of frame transmission (that is, when the checksum is transmitted), the state machine generates a Tx interrupt to the 8051W.

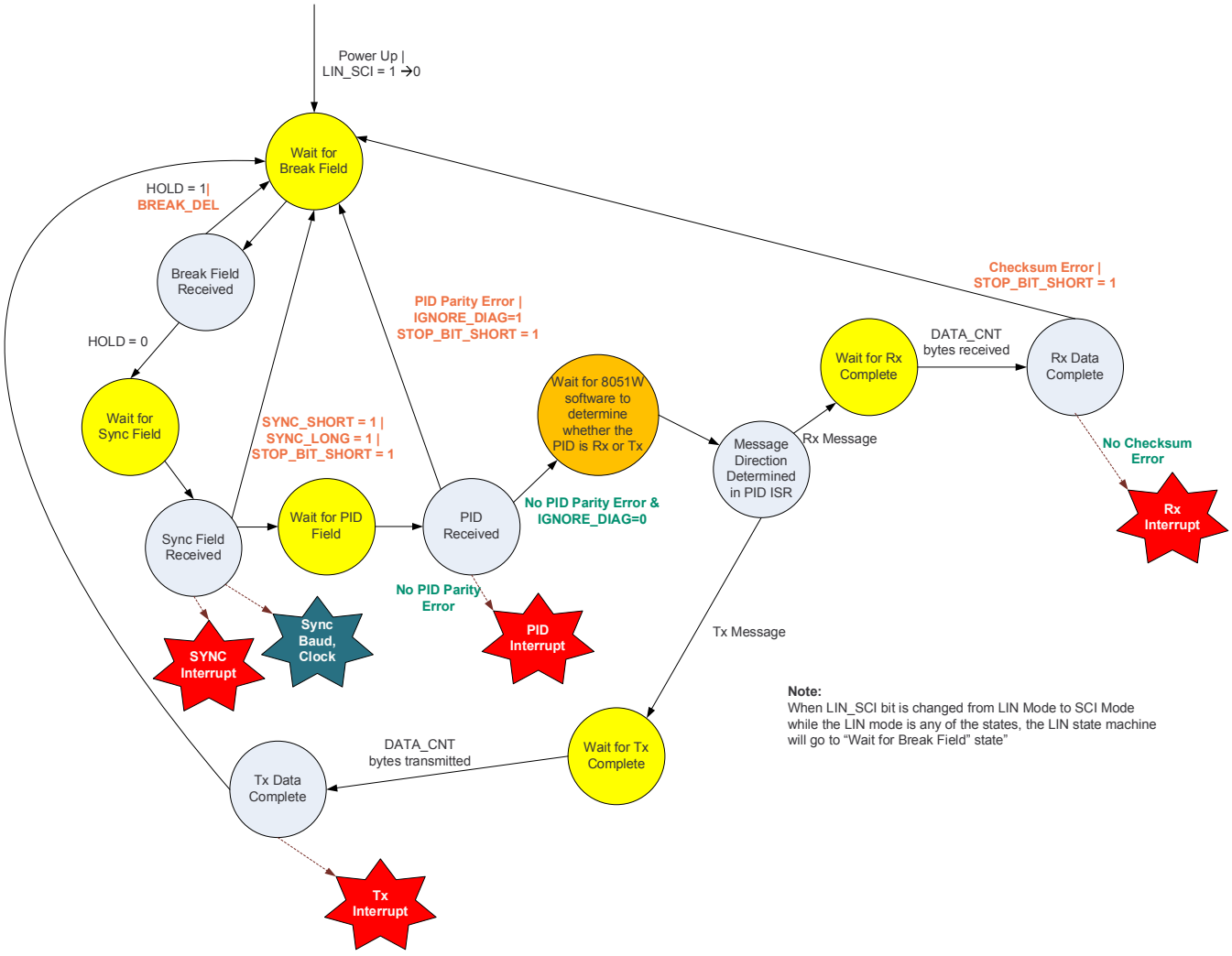


Figure 35. LIN Controller State Machine

LIN Slave Protocol Rx

If the PID field corresponds to an Rx message, the following are the steps to receive a LIN message.

In the PID interrupt service routine, do the following:

- Load DATA_CNT ESFR with the expected number of Rx data bytes.
- Set the RX_TX bit in LIN_CTRL ESFR to 0 to Rx a message.

In the Rx interrupt service routine, do the following:

- Transfer data from the RX_DATA buffers to RAM.

See the Programmer's Guide (SLDU006) for details on the ESFRs.

LIN Slave Protocol Tx

If the PID field corresponds to a Tx message, the following are the steps to receive a LIN message.

In the PID interrupt service routine, do the following:

- Load DATA_CNT ESFR with the number of data bytes to be transmitted.
- Load TX_DATA buffers with the data that is to be transmitted.
- Set the RX_TX bit in LIN_CTRL ESFR to 1 to Tx a message.

In the Tx interrupt service routine, do the following:

- User specific

See the Programmer's Guide (SLDU006) for details on the ESFRs.

NOTE

The LIN PID will be received and stored in the LIN_PID ESFR. This register will be cleared when the LIN message transmission/reception is complete. Therefore, to retain the value of the LIN_PID, the user has to copy the value of the ESFR to a RAM variable.

LIN Slave Status

The PGA450-Q1 has a LIN status register (LIN_STATUS) register that has the error status of the received LIN frame.

This LIN_STATUS register can be cleared at any time by setting the CLR_ERR bit in the LIN_CFG register to 1.

LIN Slave Framing Error Status

The LIN_STATUS register in the PGA450-Q1 has the following bits that reflect any framing errors in the received LIN message:

- **CHECKSUM**: This bit is set to 1 if the received checksum does not match the calculated checksum.
- **PARITY**: This bit is set to 1 if the received PID has a parity error.
- **STOP_BIT_VAL:** This bit is set to 1 if the LIN bus does not go high for a stop bit right after the 8th data bit is received/transmitted. This check is done at the end of the PID field of each Tx and Rx data byte.

LIN Slave Timing Error Status

The LIN_STATUS register in the PGA450-Q1 has bits that reflect any LIN timing errors in the received LIN message. The timing errors are based on the diagram show in Figure 36.

Table 15 describes the various timing errors in the received LIN message that are detected by the PGA450-Q1.

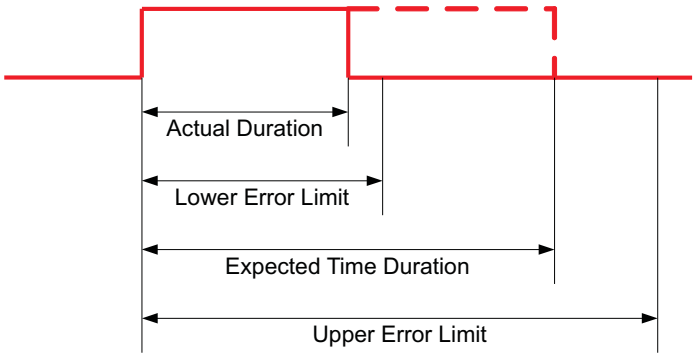


Figure 36. LIN Timing-Error Diagram

Table 15. LIN Timing Errors

ERROR BIT	DESCRIPTION	LOWER ERROR LIMIT	UPPER ERROR LIMIT
STOP_BIT_SHORT	STOP bit received in PID or data bytes is shorter than expected.	52 µs × (1 – BIT_TOL)	–
SYNC_SHORT	SYNC field duration is shorter than expected.	485 µs	–
SYNC_LONG	SYNC field duration is longer than expected.		555 µs
BREAK_DEL	BREAK FIELD delimiter is shorter than expected.	52 µs × (1 – BIT_TOL)	

SCI Buffered Mode

In the SCI buffered mode, the PGA450-Q1 does not implement any special frame or protocol. Up to 8 bytes can be received/transmitted without any 8051W software intervention. That is, the software either reads (in the case of receive) from the Rx data buffer or writes (in the case of transmit) to the Tx data buffer the appropriate number of bytes.

The DATA_CNT ESFR determines the buffer length. When data is received by the device, SCI generates an Rx data interrupt only after the number of bytes specified in DATA_CNT register is received.

SCI Buffered-Mode State Machine

Figure 37 shows the SCI buffered-mode state machine. If both the external device and the 8051W try to send data at the same time, a bus conflict occurs. This bus contention is not detected inside the PGA450-Q1.

If the external device sends more than 8 bytes (corresponding to the buffer length), then the data in the Rx data buffer is overwritten. Therefore, the 8051W has not had a chance to read the previous data in the buffer, so the data is lost.

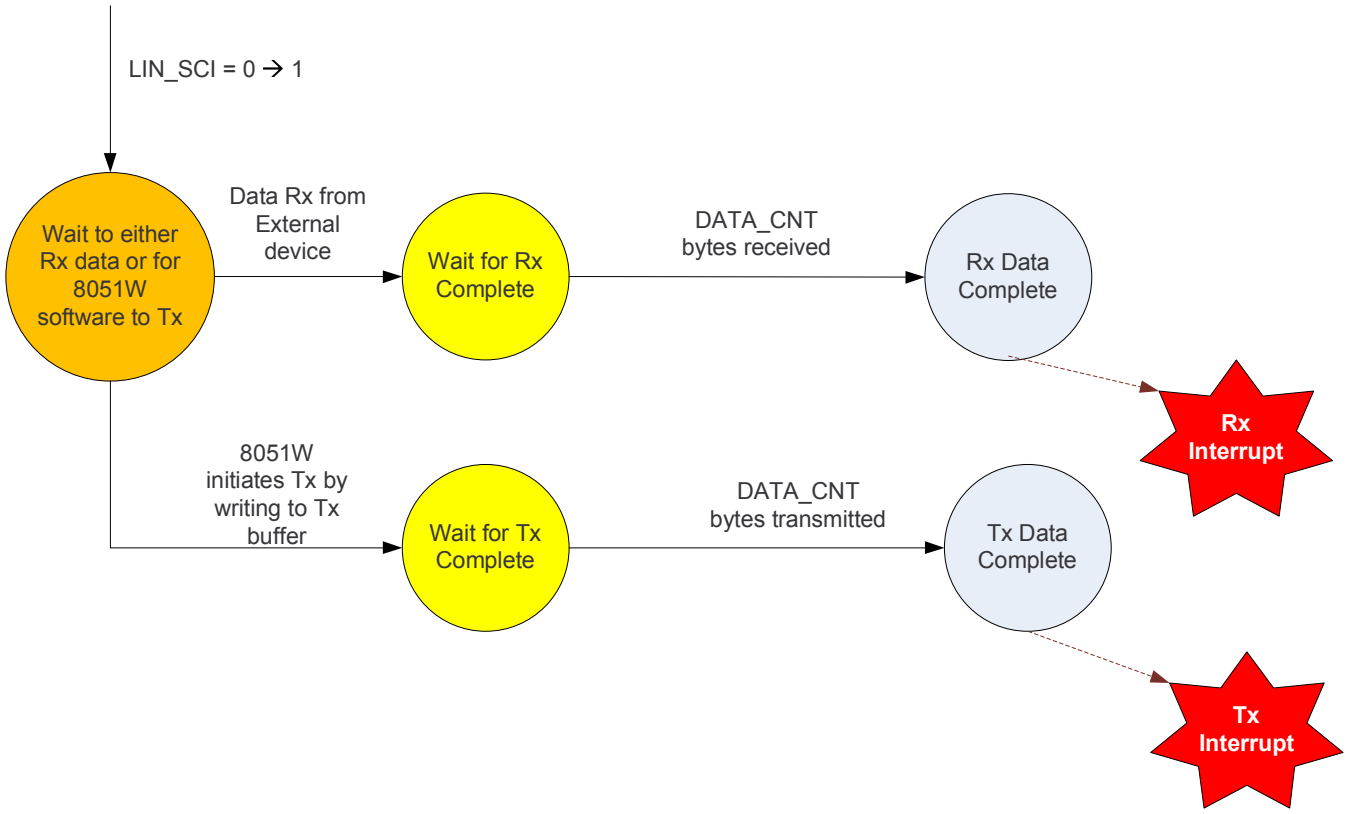


Figure 37. SCI Buffered-Mode State Machine

SCI Buffered-Mode Rx

The following are the steps to receive data on SCI:

- In software, do the following:
  - Load DATA_CNT ESFR with the expected number of Rx data bytes.
  - Set the RX_TX bit in LIN_CTRL ESFR to 0 to Rx a message.
- In the Rx interrupt service routine, do the following:
  - Transfer data from the RX_DATA buffers to RAM.

SCI Buffered-Mode Tx

The following are the steps to transmit data on SCI:

- In software, do the following:
  - Load DATA_CNT ESFR with the number of data bytes to be transmitted.
  - Load TX_DATA buffers with the data to be transmitted.
  - Set the SCI_TX_EN bit in DP_SCI_CTRL ESFR to 1 to Tx a message.
  - Set the RX_TX bit in LIN_CTRL ESFR to 1 to Tx a message.
- In the Tx interrupt service routine, do the following:
  - User specific

NOTE

DATA_CNT in SCI buffered mode: The minimum value for DATA_CNT in SCI buffered mode is 2; that is, when the device is configured to operate in SCI buffered mode, the device can receive or transmit a minimum of 2 bytes.

Connection of LIN pin to 8051W

The LIN transceiver is connected to the 8051W I/O as shown in Figure 38.

That is, the state of the LIN pin can be read by software by reading 8051W port 3, pin 2 and pin 3. Similarly, 8051W port 2, pin 3 can be used to drive the TX pin of the transceiver.

Note that the state of the Rx pin from the transceiver should be inverted before the signal is routed to port 3, pin 3.

Logic 0 on P2.3 sets the LIN bus to the LOW state, whereas logic 1 on P2.3 sets the LIN bus to the HIGH state.

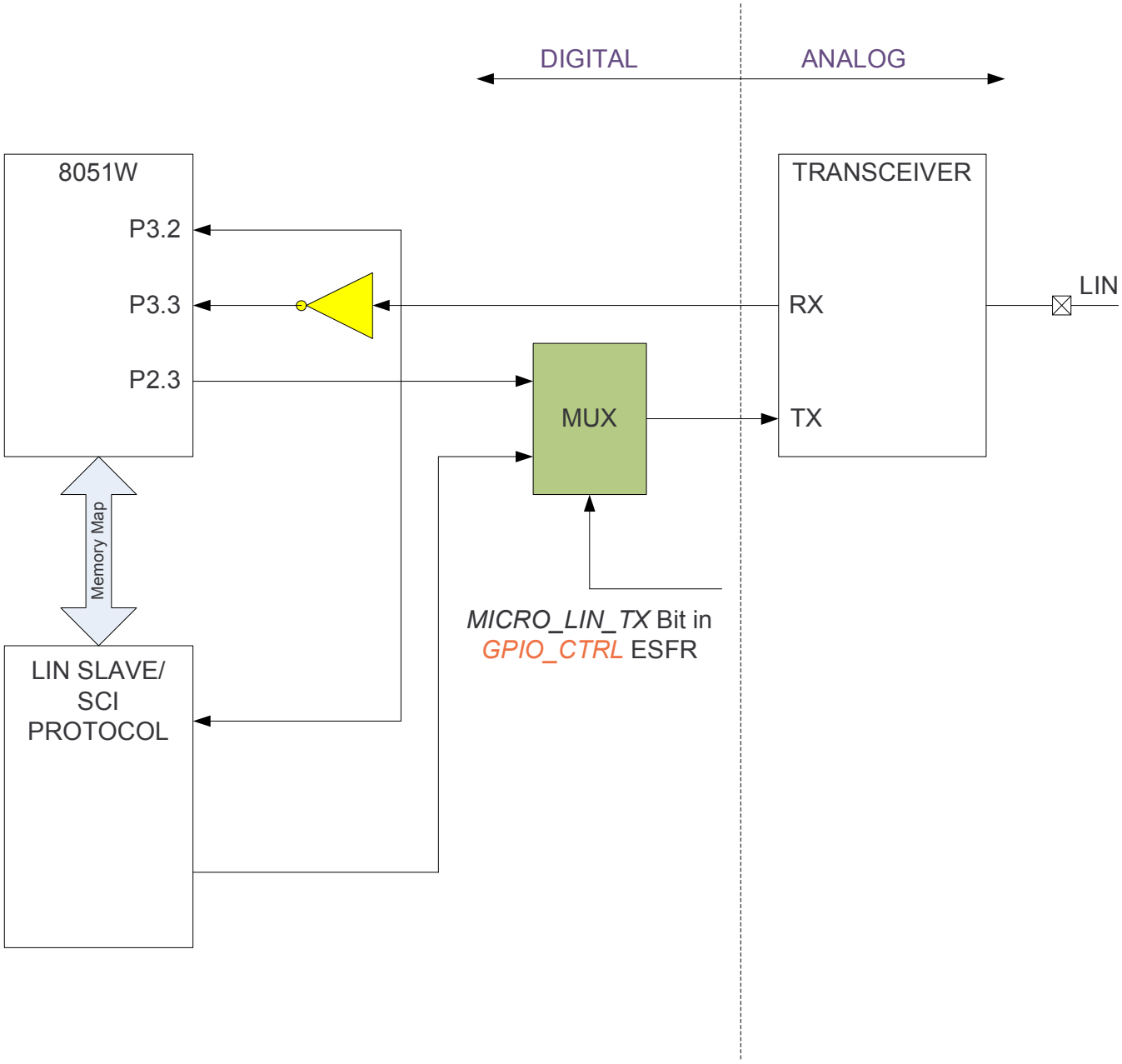


Figure 38. LIN Tx and Rx Pins Are Connected to 8051W Port Pins

The reason for routing the Rx pin to P3.2 and P3.3 is to allow the use of 8051W timer 1 to measure the durations of the LIN bus in the high or low state.

SPI Interface

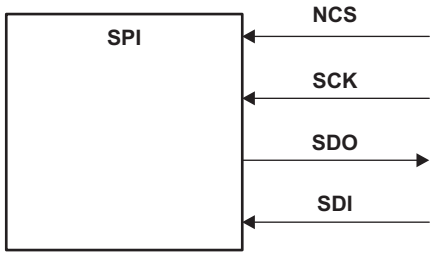


Figure 39. SPI Port in PGA450-Q1

The SPI block is used for communicating with the device during system development. The internal SPI acts as the slave in the communication of the device with an external SPI which is in master mode. To perform the communication, four external pins are necessary:

SDI: SPI slave-in master-out, serial-input pin

SDO: SPI slave-out master-in, serial-output pin (three-state output)

SCLK: SPI clock, which controls the communication

$\overline{CS}$: Chip select

The output data on the SDO pin (for example, check byte and read data) changes on the rising edge of SCLK. The input data on SDI is latched on the falling edge of SCLK. The data received during a write access is written to memory on the system clock after $\overline{CS}$ has gone high.

In the absence of active transmission, the master SPI resets the internal SPI with $\overline{CS}$ = high. MISO is in the high-impeance state during reset. Master and slave SPI transmit the MSB first.

NOTE

The PGA450-Q1 does not respond to SPI messages unless the 8051W microprocessor is in the reset state. The microprocessor can be put in the reset state by writing an appropriate value to the MICRO RESET test register. The MICRO RESET test register is the ONLY register that is accessible via SPI when the 8051W processor is not in the reset state.

SPI Interface Protocol

The serial peripheral interface (SPI) uses a 1-byte command word and 2 or 3 additional bytes for the complete command.

Table 16 describes the SPI protocol.

Table 16. SPI Protocol Command Word

BIT	FUNCTION
15:13	Always 3'b000
12:10	Memory access control: 3'b001: OTP 3'b010: EXTERNAL RAM (FIFO, general-purpose) 3'b011: EEPROM 3'b100: IRAM 3'b101: TEST registers 3'b110: ESFR 3'b111: Development RAM
9	**R/W Access**: Write = 1 Read = 0
8	Parity bit: Odd parity on bits 15:9

When accessing the memory (IRAM, ESFR, OTP, EEPROM, FIFO RAM, DEV RAM) the internal registers bits 15:13 must all be zero. If they are not, the SPI command is rejected and the SPI failure bit is set (see check byte below).

Transfer Width

Table 17 shows how the SPI transfer width (number of bytes) varies depending on whether the SPI is a read or write to the IRAM, ESFR, EEPROM, OTP, or FIFO data access.

Table 17. SPI Protocol Transfer Widths

MEMORY ACCESS MODE	REG ACCESS	MEMORY ACCESS	R/W	PARITY BIT				DATA	TOTAL NO. OF BYTES
	Byte #1 (Breakdown)				Bytes				
	Bits 15:13	Bits 12:10	Bit 9	Bit 8	Byte #1 (Hex)	Byte #2	Byte #3	Byte #4	
Internal RAM write	000	100	1	1	13	8-bit RAM Address	8-bit Write Data	–	3
Internal RAM read	000	100	0	0	10	8-bit RAM Address	8-bit Don't Care	–	3
ESFR write	000	110	1	0	1A	8-bit ESFR Address	8-bit Write Data	–	3
ESFR read	000	110	0	1	19	8-bit ESFR Address	8-bit Don't Care	–	3
OTP write	000	001	1	1	07	OTP Address 15:8	OTP Address 7:0	8-bit write data	4
OTP read	000	001	0	0	04	OTP Address 15:8	OTP Address 7:0	8-bit don't care	4
EEPROM cache write	000	011	1	0	0E	8-bit EEPROM Address	8-bit Write Data	–	3
EEPROM cache read	000	011	0	1	0D	8-bit EEPROM Address	8-bit Don't Care	–	3
External RAM write	000	010	1	1	0B	8-bit EXTERNAL RAM Address	8-bit Write Data	–	4
External RAM read	000	010	0	0	08	8-bit EXTERNAL Address	8-bit Don't Care	–	3
DEV RAM write	000	111	1	1	1F	DEV RAM Address 15:8	DEV RAM Address 7:0	8-bit write data	4
DEV RAM read	000	111	0	0	1C	DEV RAM Address 15:8	DEV RAM Address 7:0	8-bit don't care	4
TEST write (for TI use only)	000	101	1	0	16	8-bit TEST Address	8-bit Write Data	–	3
TEST read (for TI use only)	000	101	0	1	15	8-bit TEST Address	8-bit Don't Care	–	3

For a SPI transfer to the internal register file, the parity *P* depends on the address.

For SPI transfers to the memories (IRAM, ESFR, OTP), the read data is available on the next SPI transfer. That is, when reading from a memory location, the user must send a subsequent transfer to get the data back.

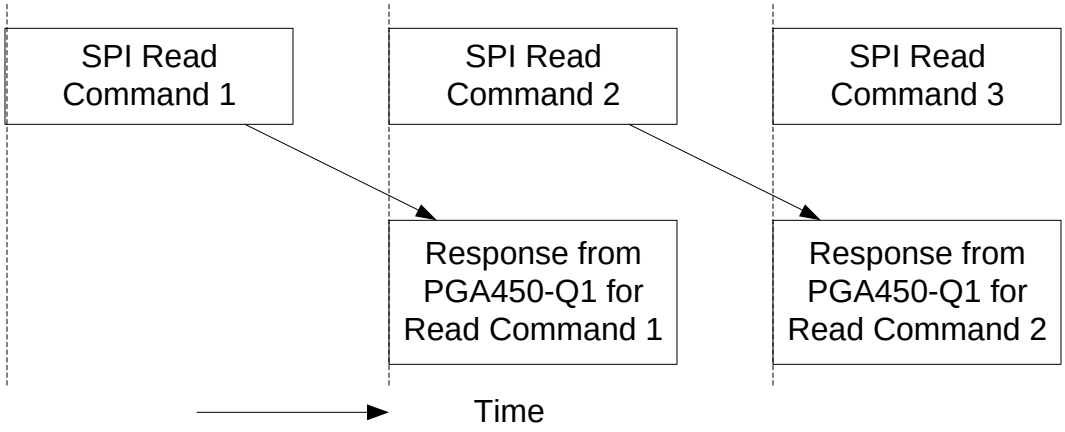


Figure 40. Response to SPI Read Commands Is Available When the Next Command Is Sent

Check Byte

On every SPI transfer, the PGA450-Q1 transmits a check byte which is in the 8 most significant bits of the transfer. For example, in a 16-bit transfer, the check byte is in bits 15:8 of the received data; similarly, for a 24 bit transfer the check byte is in bits 23:16 of the received data. The check byte can be used by the SPI master to detect SPI communication errors.

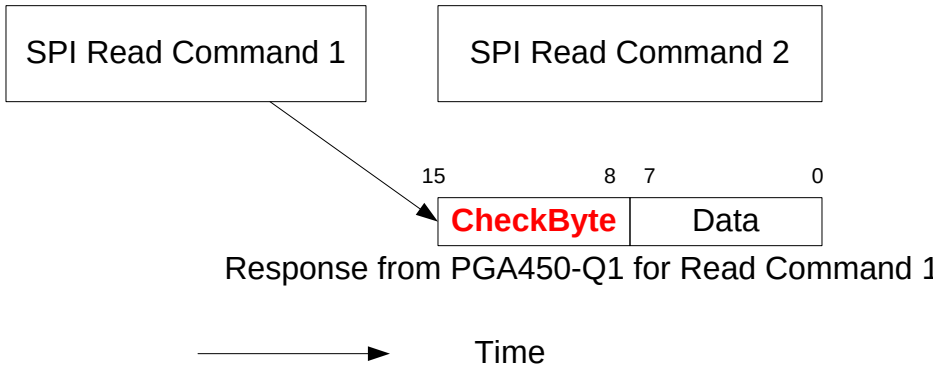


Figure 41. Check Byte Is Transmitted by PGA450-Q1 at the Beginning of Every Response

Table 18 describes the interpretation of each bit in the check byte transmitted by the PGA450-Q1.

Note that for a successful SPI transfer, the check byte reads 8'h02. Bit 9 of the check byte is always set in order to assist debugging in the lab. If the SPI transfer failed for some reason, the most significant bit (15) of the check byte is set. The reason for the failure is then described in bits 14:11.

Table 18. SPI Protocol, Check-Byte Field

CHECK-BYTE BIT	ERROR	DESCRIPTION
15 (or most significant bit)	SPI transfer failure	SPI transfer failure
14	Parity error	Parity error; command-byte parity incorrect
13	Illegal address	Illegal address; bits 15:13 and 12:10 cannot both be active
12	Illegal command	Illegal command; memory access bits 12:10 invalid
11	Wrong number of clocks	Wrong number clocks; must only receive 16, 24, or 32 clocks
10:8	Always 3'b010	Always 3'b010

Examples

Table 19 shows a few examples of SPI transfer:

Table 19. SPI Protocol Examples

COMMAND	SPI SLAVE TRANSFER
Read internal register 0 (revision id)	({3'h0, 3'h0, 1'b0, 1'b1}, 8'hXX)
Write 0x80 to internal register 1 (MicroConfig)	({3'h1, 3'h0, 1'b1, 1'b1}, 8'hC8)
Write 0x34 to internal RAM 0x7F	({3'h0, 3'h4, 1'b1, 1'b1}, 8'h7F, 8'h34)
Read from ESFR 0xC0	({3'h0, 3'h6, 1'b0, 1'b1}, 8'hC0)
Write 0xD9 to OTP 0x1765	({3'h0, 3'h1, 1'b1, 1'b1}, 8'h17, 8'h65, 8'hD9)
Failed write 0xC8 to internal register 1 (bad parity)	({3'h1, 3'h0, 1'b1, 1'b0}, 8'hC8)
Failed write 0xC8 to internal register 1 (illegal address)	({3'h1, 3'h1, 1'b1, 1'b0}, 8'hC8)
Failed write 0x34 to memory (illegal command)	({3'h0, 3'h7, 1'b1, 1'b1}, 8'h7F, 8'h34)

Diagnostics

Power-Block Monitors

The following operating-condition monitors have been implemented on the PGA450-Q1 to ensure reliable and robust performance over the lifetime of the device.

- VPWR overvoltage (greater than 28 V nominal, 20-µs deglitch time)
- VPWR level is such that AVDD is undervoltage (less than 6 V nominal, 2-ms deglitch time)
- AVDD overcurrent (greater than 55 mA nominal, 2-ms deglitch time)
- RBIAS overcurrent (greater than 63 µA nominal, 2-ms deglitch time)

Whenever these monitors sense a violation in the operating conditions, the microprocessor is held in reset. Also, a corresponding fault flag is set in the STATUS1 register.

The fault flags are cleared when the fault condition is removed or when the device is reset.

Low-Side Diagnostics

The PGA450-Q1 has diagnostics implemented on the LS driver to protect the LS FET from sinking excessive currents when it is enabled. A fault condition is sensed if both the Vgs voltage and the Vds voltage on the LS FET remain above 2.5 V for the duration of either 1 µs / 2 µs (selectable by setting the LS_FAULT_TIMER_SEL bit in the CONTROL_1 register) during a turnon event. If a fault is sensed, the LS FET is immediately turned off and a corresponding flag is set in the STATUS2 register. The fault is automatically cleared when the LS FET is commanded to turn on in the next cycle.

The LS diagnostics are turned off by default and can be enabled by setting the LS_FAULT_LOGIC_EN bit in the CONTROL_1 register.

Figure 42 shows the schematic of the low-side drive and Figure 43 shows the timing diagram of the low-side diagnostics.

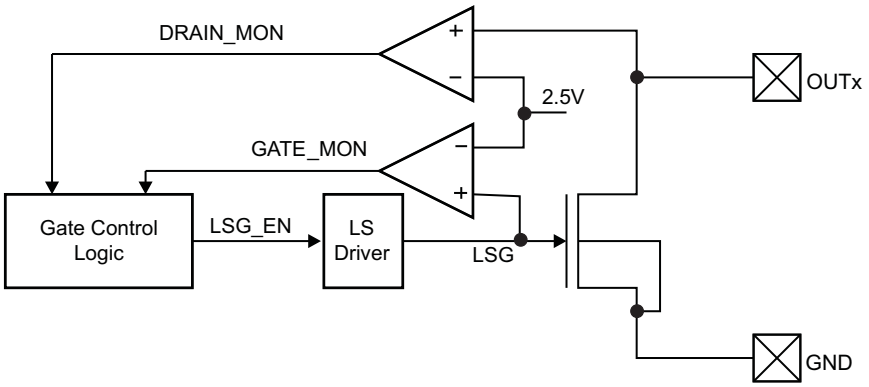
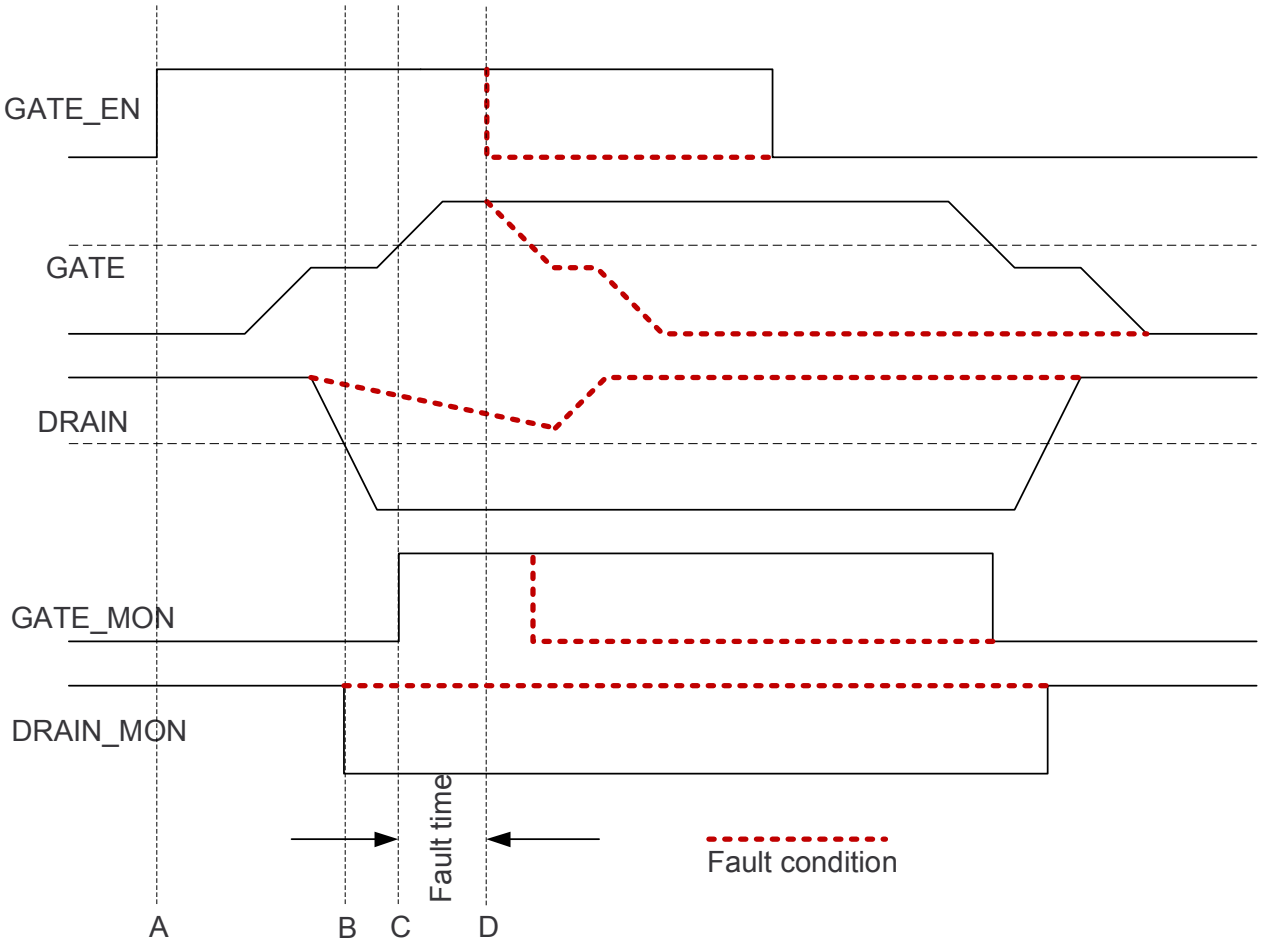


Figure 42. Low-Side Drive Schematic



A: Gate is commanded on by LS driver logic. This 0 -> 1 edge enables the LS fault diagnostic on the LS Driver if the LS_FAULT_LOGIC_EN is set.
B: Drain monitor (DRAIN_MON) senses that drain is below 2.5V for a normal scenario, where as the drain monitor output remains high for the fault scenario.
C: Gate monitor (GATE_MON) senses that gate is above 2.5V.
D: For the fault scenario, since GATE_MON and DRAIN_MON signals have remained high for the selected fault time (1u / 2u sec), a fault is sensed and the gate is immediately turned off.

Figure 43. Low-Side Fault Timing

Main Oscillator Watchdog

The PGA450-Q1 implements an internal free-running 500-kHz watchdog clock. This watchdog clock is used to monitor the internal 16-MHz main oscillator or the external crystal oscillator. When this frequency is outside this range, an internal reset is generated, which resets the entire digital core; this is equivalent to POR.

The main oscillator frequency fail limits have the following ranges as illustrated in Figure 44:

- If the main oscillator frequency is less than 5.4 MHz, the watchdog logic recognizes this as a low-frequency fail and resets the digital core.
- If the main oscillator frequency lies the range: 5.4 MHz < Main OSC Freq < 14 MHz, there is a possibility that the watchdog recognizes this as a low-frequency fail and resets the core, but reset is not assured.
- If the main oscillator frequency lies in the range: 14 MHz < Main Osc Freq < 18 MHz, the main osc watchdog does NOT reset the core, as this is seen as the nominal frequency of operation.
- If the main oscillator frequency lies in the range 18 MHz < Main Osc Freq < 43 MHz, there is a possibility that the watchdog recognizes this as a high-frequency fail and resets the core, but reset is not assured.
- If the main oscillator frequency is greater than 43 MHz, the watchdog logic recognizes this as a high-frequency fail and resets the digital core.

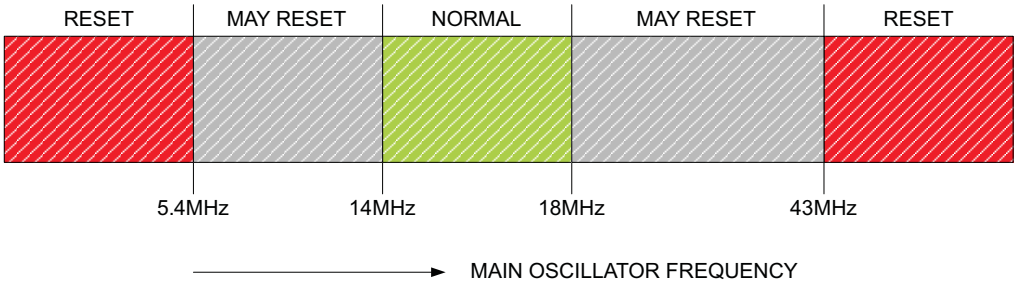


Figure 44. Main Oscillator Frequency and the Corresponding PGA450-Q1 Behavior

The main oscillator watchdog can be disabled using the OSC_WD_EN bit in the WD_EN register.

NOTE

A reset because of main oscillator watchdog failure causes an internal digital core reset; that is, all ESFRs revert back to their reset sate.

Software Watchdog

The PGA450-Q1 implements a software watchdog. This watchdog must be serviced by software every 250 ms. If the software does not service the watchdog within 250 ms of the last service, then the transducer drive FETs are turned OFF and the 8051W core is reset.

The software services the watchdog using port pin P3.7 as shown in Figure 45. The software services the watchdog by toggling the state of P3.7.

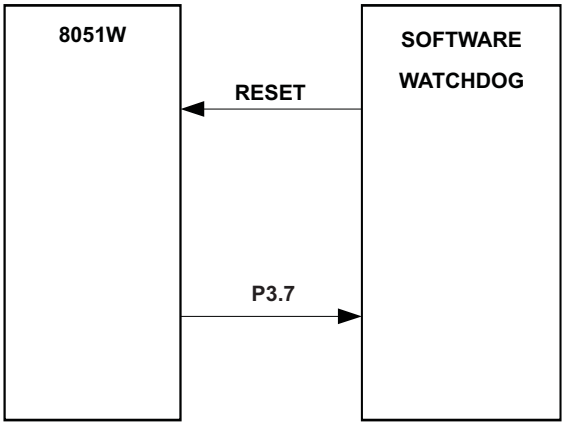


Figure 45. Connection Between the 8051W and the Software Watchdog

The software watchdog can be disabled using the CPU_WD_EN bit in the WD_EN register. The following is the behavior of this bit:

- The CPU_WD_EN bit is in the disabled state after power-on reset (POR).
- If the 8051W is reset via SPI, then CPU_WD_EN is disabled.
- If CPU_WD_EN is enabled and the 8051W is reset because the software watchdog has timed out, then CPU_WD_EN remains enabled.

NOTE

A reset of the 8051W does not change the state of the ESFR registers; that is, the ESFR registers continue to retain their state.

Internal ASIC TRIM Validity

The PGA450-Q1 has internal ASIC trim values. These trim values are used to fine-tune the operation of various blocks at TI manufacturing EOL.

The PGA450-Q1 checks the validity of these ASIC trim values after power up and before the 8051W reset is deasserted. If the internal trim values are not valid, the TRIM_FAIL bit in the STATUS1 register is set. The 8051W software can be used to check this bit after 8051W reset is deasserted and the software starts execution.

FIFO RAM and External SRAM MBIST

The PGA450-Q1 verifies the integrity of FIFO RAM and RAM in the external memory space (that is, all RAM in the external memory) with a RAM MBIST. The RAM MBIST starts immediately after POR is deasserted and takes approximately 5 ms. See Figure 9 for power-up waveforms. Note that the 8051W reset is deasserted while MBIST is ongoing.

MBIST sets the MBIST_DONE flag in STATUS1 upon completion of MBIST. The MBIST_FLAG is set to 1 if RAM MBIST fails.

NOTE

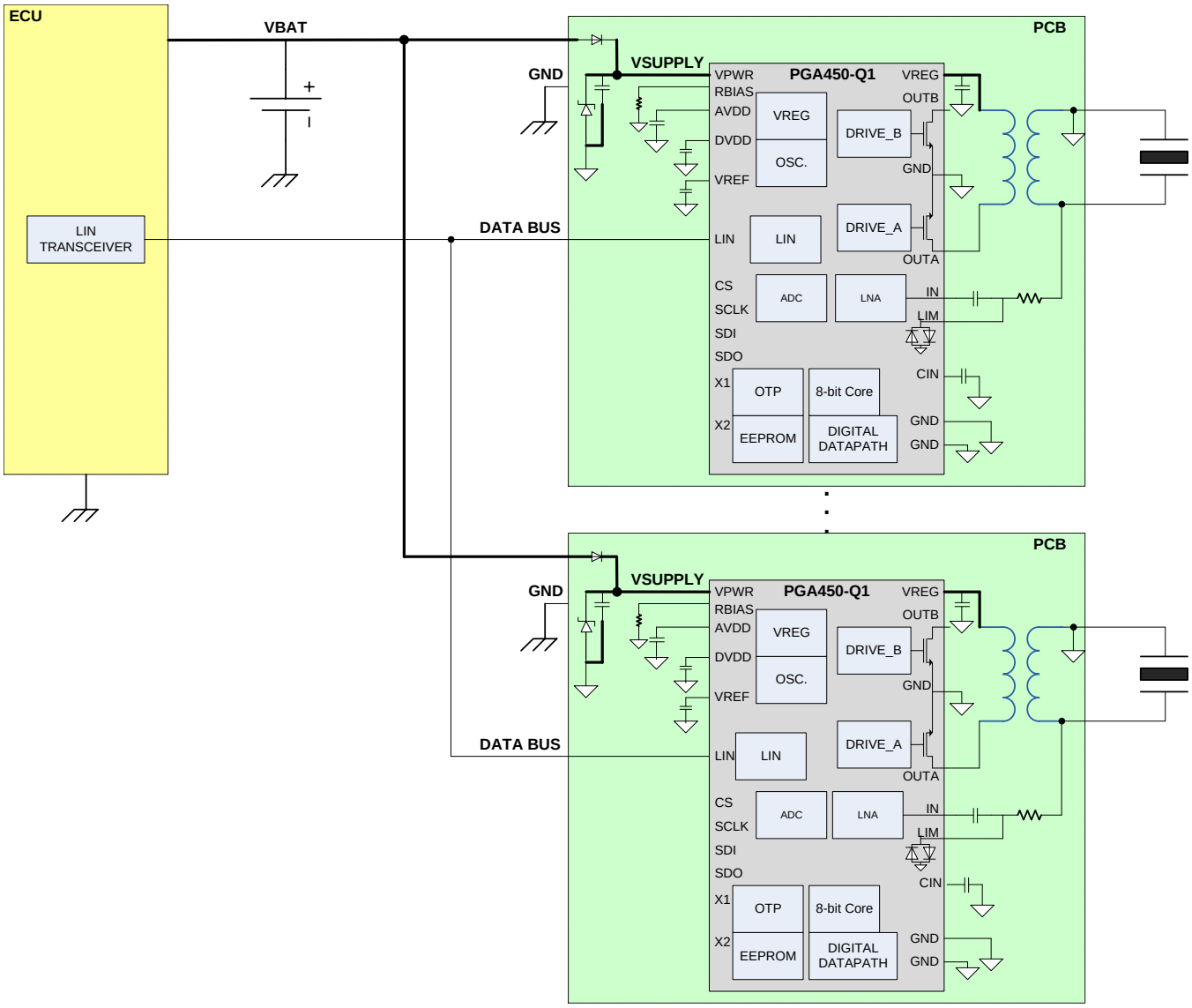
The 8051W microprocessor should not enable the digital data path, should not access the FIFO RAM, and should not access RAM in the external memory space until the RAM MBIST DONE flag is set.

Thermal Shutdown

The PGA450-Q1 also has an overtemperature protection feature implemented. An overtemperature violation causes a total shutdown of the part with the microprocessor held in reset. Once the device cools down below the overtemperature threshold, the part initiates a power up again.

APPLICATION INFORMATION

Application Schematic



PACKAGING INFORMATION

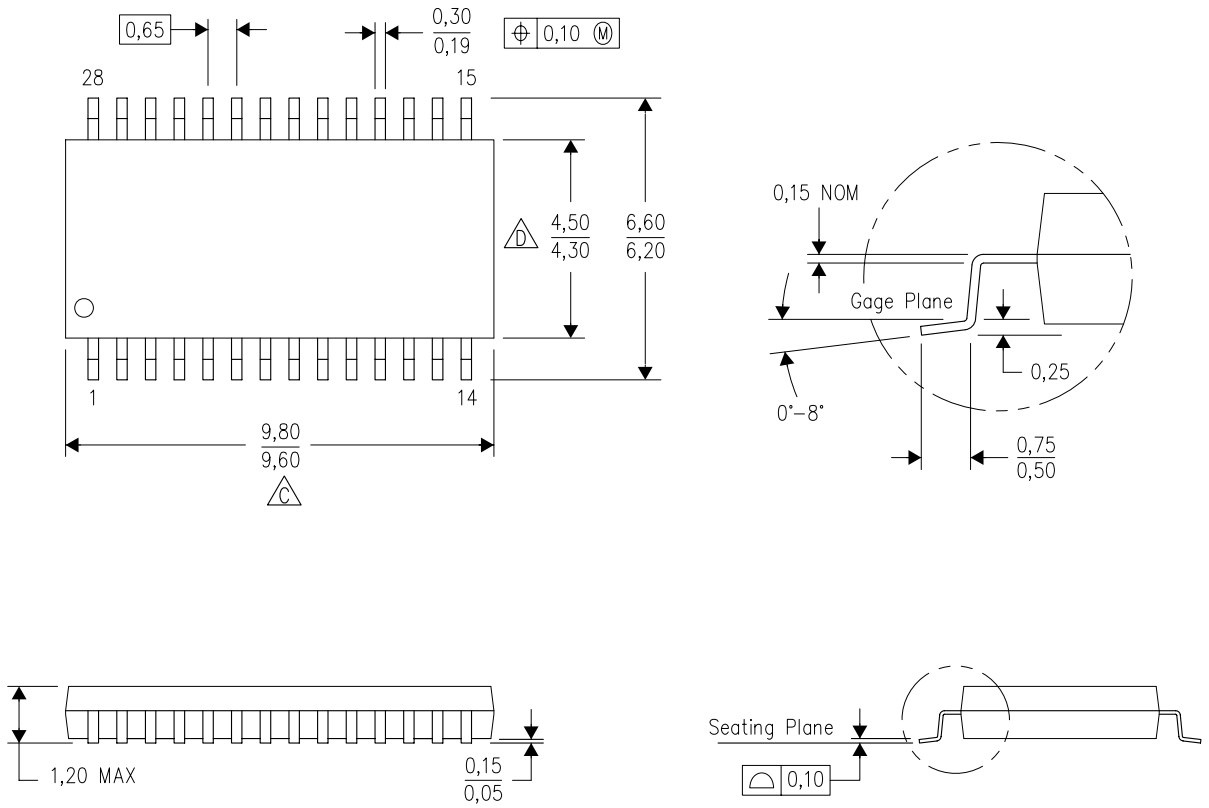
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
PGA450IPWRQ1	PREVIEW	TSSOP	PW	28	2000	TBD	Call TI	Call TI	
PGA450TPWRQ1	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

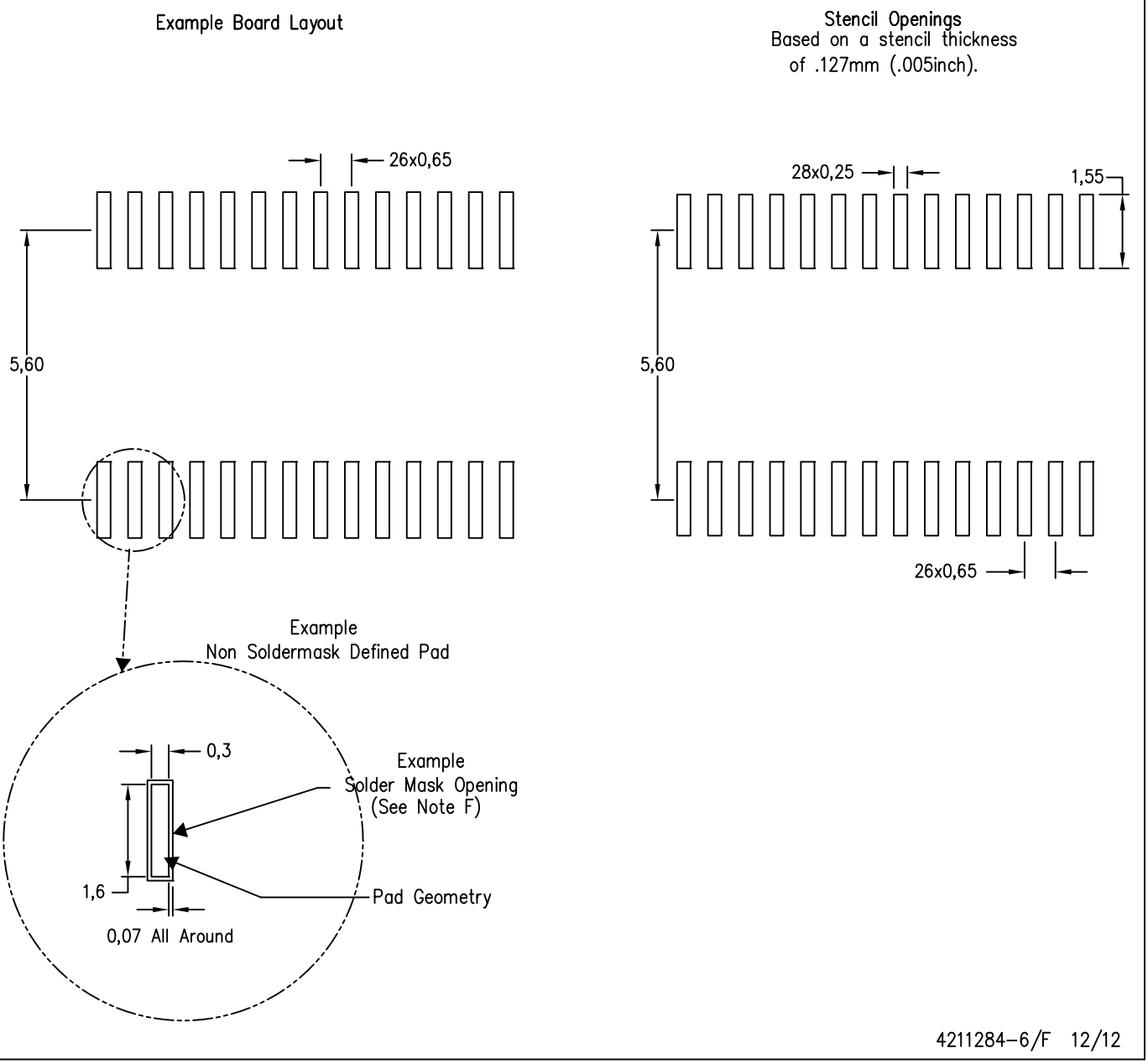
PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



4040064–7/G 02/11

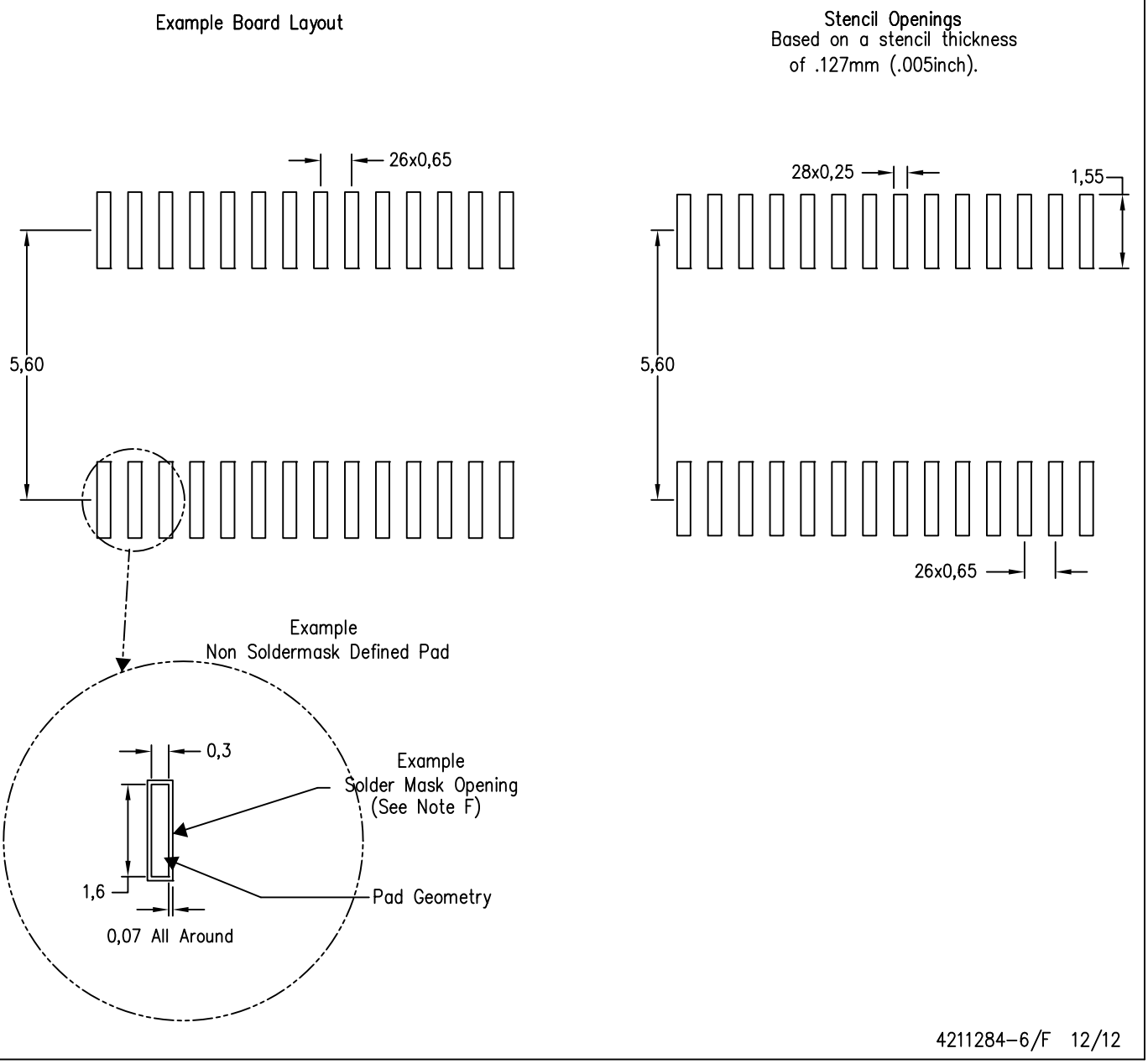
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



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