



FAN2103 — TinyBuck™

3 A, 24 V Input, Integrated Synchronous Buck Regulator

Features

- 3 A Output Current
- Over 95% Efficiency
- Fully Synchronous Operation with Integrated Schottky Diode on Low-side MOSFET Boosts Efficiency
- Programmable Frequency Operation (200 KHz to 600 KHz)
- Power-good Signal
- Accepts Ceramic Capacitors on Output
- External Compensation for Flexible Design
- Wide Input Range: 3 V to 24 V
- Output Voltage Range: 0.8 V to 90%V_{IN}
- Input Under-Voltage Lockout
- Programmable Over-Current Limit
- Under-Voltage, Over-Voltage, and Thermal Protections
- 5x6 mm, 25-pin, 3-Pad MLP

Applications

- Graphics Cards
- Battery-powered Equipment
- Set-top Boxes
- Point-of-load Regulation
- Servers

Description

The FAN2103 TinyBuck™ is an easy-to-use, cost- and space-efficient, 3 A synchronous buck solution. It enables designers to solve high current requirements in a small area with minimal external components.

External compensation, programmable switching frequency, and current limit features allow for design optimization and flexibility.

The summing current mode modulator uses lossless current sensing for current feedback and over-current, and includes voltage feedforward.

Fairchild's advanced BiCMOS power process, combined with low R_{DS(ON)} internal MOSFETs and a thermally efficient MLP package provide the ability to dissipate high power in a small package.

Output over-voltage, under-voltage, and thermal shutdown protections plus power-good, help protect the devices from damage during fault conditions.

Related Application Notes

- [TinyCalc™ Design Tool](#)
- [AN-6033 — TinyCalc™ Design Tool Guide](#)
- [AN-5067 – PCB Land Pattern Design and Surface Mount Guidelines for MLP Packages](#)

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN2103MPX	-10°C to 85°C	25-Pin Molded Leadless Package (MLP) 5x6 mm	Tape and Reel
FAN2103EMPX	-40°C to 85°C	25-Pin Molded Leadless Package (MLP) 5x6 mm	Tape and Reel

Typical Application Diagram

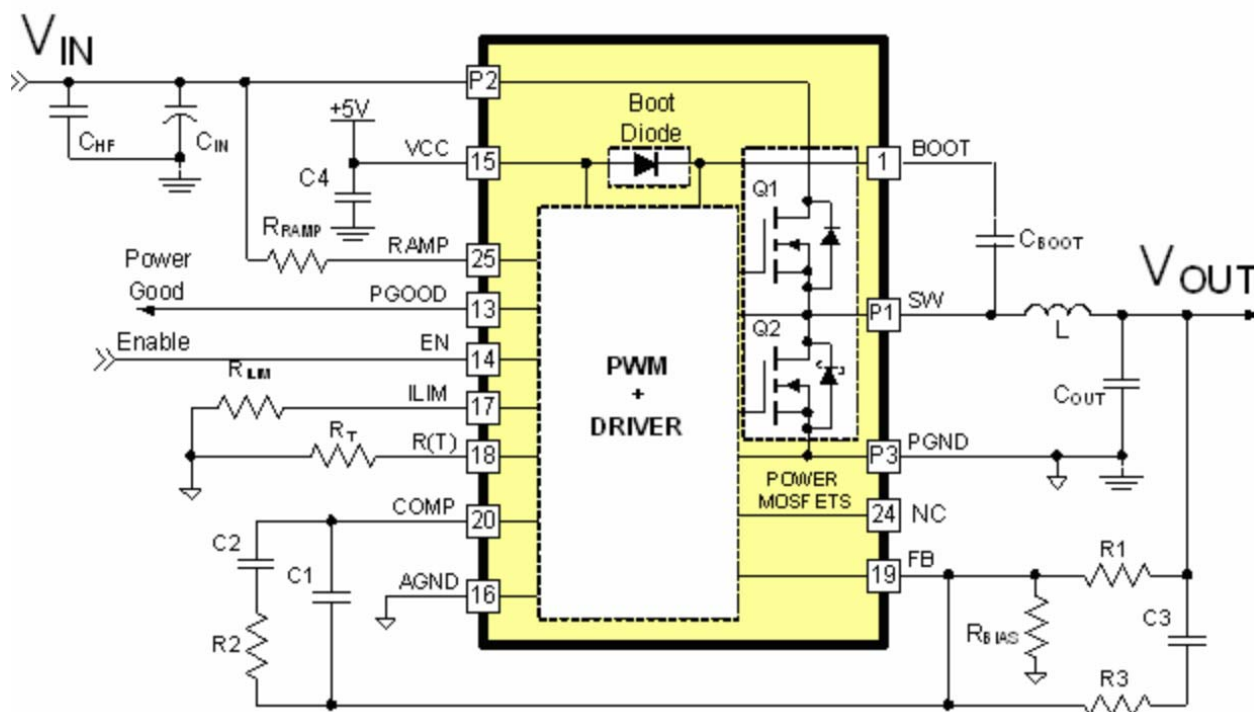


Figure 1. Typical Application

Block Diagram

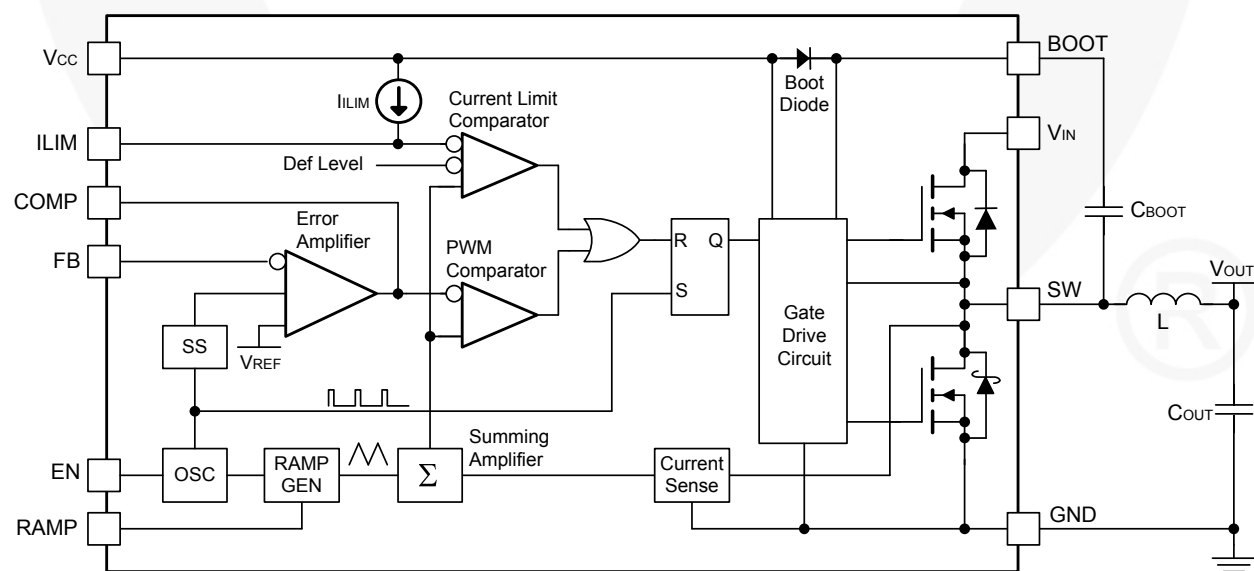


Figure 2. Block Diagram

Pin Configuration

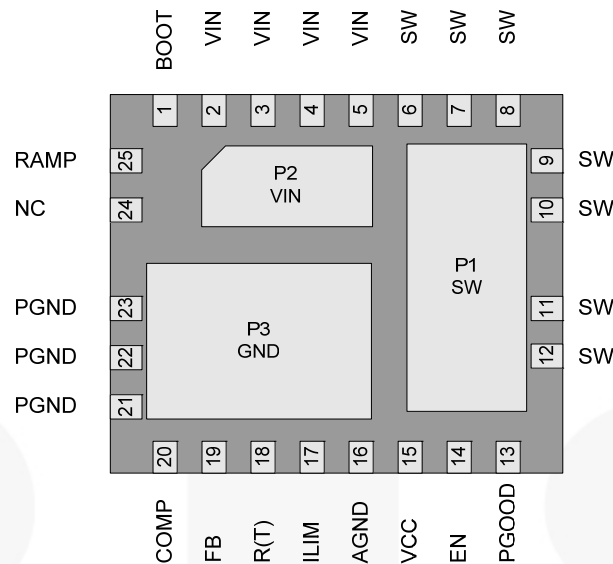


Figure 3. MLP 5x6 mm Pin Configuration (Bottom View)

Pin Definitions

Pin	Name	Description
P1, 6-12	SW	Switching Node.
P2, 2-5	VIN	Power Input Voltage. Connect to the main input power source.
P3, 21-23	PGND	Power Ground. Power return and Q2 source.
1	BOOT	High-side Drive BOOT Voltage. Connect through capacitor (C_{BOOT}) to SW. The IC includes an internal synchronous bootstrap diode to recharge the capacitor on this pin to V_{CC} when SW is LOW.
13	PGOOD	Power-Good Flag. An open-drain output that pulls LOW when FB is outside a $\pm 10\%$ range of the reference when EN is HIGH. PGOOD does not assert HIGH until the fault latch is enabled.
14	EN	ENABLE. Enables operation when pulled to logic HIGH or left open. Toggling EN resets the regulator after a latched fault condition. This input has an internal pull-up when the IC is functioning normally. When a latched fault occurs, EN is discharged by a current sink.
15	VCC	Input Bias Supply for IC. The IC's logic and analog circuitry are powered from this pin.
16	AGND	Analog Ground. The signal ground for the IC. All internal control voltages are referred to this pin. Tie this pin to the ground island/plane through the lowest impedance connection.
17	ILIM	Current Limit. A resistor (R_{ILIM}) from this pin to AGND can be used to program the current-limit trip threshold lower than the default setting.
18	R(T)	Oscillator Frequency. A resistor (R_T) from this pin to AGND sets the PWM switching frequency.
19	FB	Output Voltage Feedback. Connect through a resistor divider to the output voltage.
20	COMP	Compensation. Error amplifier output. Connect the external compensation network between this pin and FB.
24	NC	No Connect. This pin is not used.
25	RAMP	Ramp Amplitude. A resistor (R_{RAMP}) connected from this pin to VIN sets the ramp amplitude and provides voltage feedforward functionality.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Parameter	Conditions	Min.	Max.	Unit
VIN to PGND			28	V
VCC to AGND	AGND = PGND		6	V
BOOT to PGND			35	V
BOOT to SW		-0.3	6.0	V
SW to PGND	Transient (t < 20 ns, f < 600 KHz)	-5	30	V
All other pins		-0.3	V _{CC} +0.3	V
ESD	Human Body Model, JEDEC JESD22-A114	2.0		kV
	Charged Device Model, JEDEC JESD22-C101	2.5		

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V _{CC}	Bias Voltage	VCC to AGND	4.5	5.0	5.5	V
V _{IN}	Supply Voltage	VIN to PGND	3		24	V
T _A	Ambient Temperature	FAN2103M	-10		+85	°C
		FAN2103EM	-40		+85	°C
T _J	Junction Temperature				+125	°C

Thermal Information

Symbol	Parameter		Min.	Typ.	Max.	Unit
T _{STG}	Storage Temperature		-65		+150	°C
T _L	Lead Soldering Temperature, 10 Seconds				+300	°C
T _{VP}	Vapor Phase, 60 Seconds				+215	°C
T _I	Infrared, 15 Seconds				+220	°C
θ _{JC}	Thermal Resistance: Junction-to-Case	P1 (Q2)		4		°C/W
		P2 (Q1)		7		°C/W
		P3		4		°C/W
θ _{J-PCB}	Thermal Resistance: Junction-to-Mounting Surface			35 ⁽¹⁾		°C/W
P _D	Power Dissipation, T _A = 25°C				2.8 ⁽¹⁾	W

Note:

1. Typical thermal resistance when mounted on a four-layer, two-ounce PCB, as shown in Figure 26. Actual results are dependent on mounting method and surface related to the design.

Electrical Specifications

Recommended operating conditions are the result of using the circuit shown in Figure 1 unless otherwise noted.

Parameter	Conditions	Min.	Typ.	Max.	Unit
Power Supplies					
V _{CC} Current	SW = Open, FB = 0.7 V, V _{CC} = 5 V, f _{SW} = 600 KHz		8	12	mA
	Shutdown: EN = 0, V _{CC} = 5 V		7	10	μA
V _{CC} UVLO Threshold	Rising V _{CC}	4.1	4.3	4.5	V
	Hysteresis		300		mV
Oscillator					
Frequency	R _T = 50 KΩ	255	300	345	KHz
	R _T = 24 KΩ	540	600	660	KHz
Minimum On-Time ⁽²⁾			50	65	ns
Ramp Amplitude, pk-pk	16 V _{IN} , 1.8 V _{OUT} , R _T = 30 KΩ, R _{RAMP} = 200 KΩ		0.53		V
Minimum Off-Time ⁽²⁾			100	150	ns
Reference					
Reference Voltage (V _{FB})	FAN2103M, 25°C	794	800	806	mV
	FAN2103EM, 25°C	795	800	805	mV
Temperature Coefficient	FAN2103M, -10 to +85°C		50		PPM
	FAN2103EM, -40 to +85°C		70		PPM
Error Amplifier					
DC Gain ⁽²⁾	V _{CC} = 5 V	80	85		dB
Gain Bandwidth Product ⁽²⁾		12	15		MHz
Output Voltage (V _{COMP})		0.4		3.2	V
Output Current, Sourcing	V _{CC} = 5 V, V _{COMP} = 2.2 V	1.5	2.2		mA
Output Current, Sinking	V _{CC} = 5 V, V _{COMP} = 1.2 V	0.8	1.2		mA
FB Bias Current	V _{FB} = 0.8 V, 25°C	-850	-650	-450	nA
Protection and Shutdown					
Current Limit	R _{LIM} Open	3.8	5.0	7.0	A
I _{LIM} Current	25°C, V _{CC} = 5 V	9	10	11	μA
Over-Temperature Shutdown	Internal IC Temperature		+160		°C
Over-Temperature Hysteresis			+30		°C
Over-Voltage Threshold	2 Consecutive Clock Cycles	110	115	120	%V _{OUT}
Under-Voltage Shutdown	16 Consecutive Clock Cycles	68	73	78	%V _{OUT}
Fault Discharge Threshold	Measured at FB Pin		250		mV
Fault Discharge Hysteresis	Measured at FB Pin (V _{FB} ~500 mV)		250		mV
Soft-Start					
V _{OUT} to Regulation (T0.8)	Frequency = 600 KHz		5.3		ms
Fault Enable/SSOK (T1.0)			6.7		ms

Note:

- Specifications guaranteed by design and characterization; not production tested.

Electrical Specifications (Continued)

Recommended operating conditions are the result of using the circuit shown in Figure 1 unless otherwise noted.

Parameter	Conditions	Min.	Typ.	Max.	Unit
Control Functions					
EN Threshold, Rising			1.35	2.00	V
EN Hysteresis			250		mV
EN Pull-up Resistance			800		K Ω
EN Discharge Current	Auto-restart Mode		1		μ A
FB OK Drive Resistance				800	Ω
PGOOD Threshold (Compared to V_{REF})	$FB < V_{REF}$	-14	-11	-8	% V_{REF}
	$FB > V_{REF}$	+7	+10	+13	% V_{REF}
PGOOD Output Low	$I_{OUT} \leq 2$ mA			0.4	V

Typical Characteristics

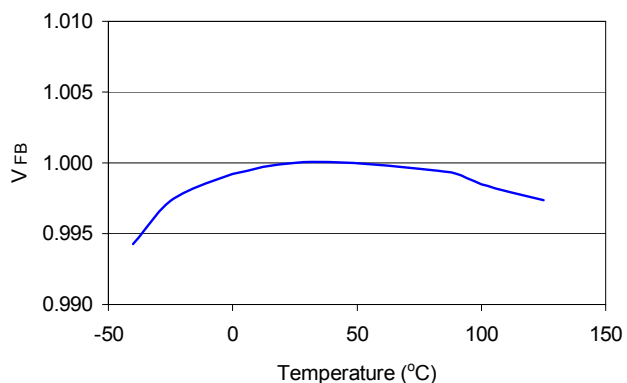


Figure 4. Reference Voltage (V_{FB}) vs. Temperature, Normalized

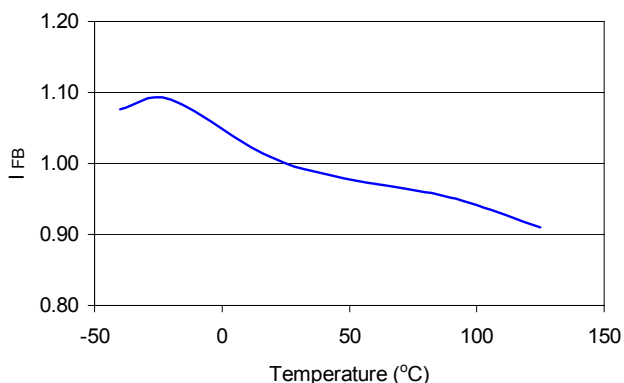


Figure 5. Reference Bias Current (I_{FB}) vs. Temperature, Normalized

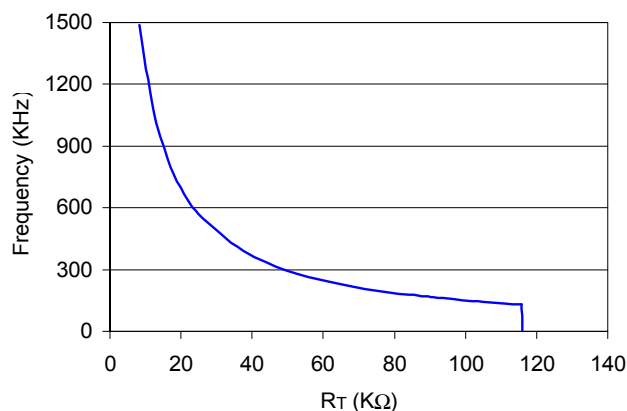


Figure 6. Frequency vs. R_T

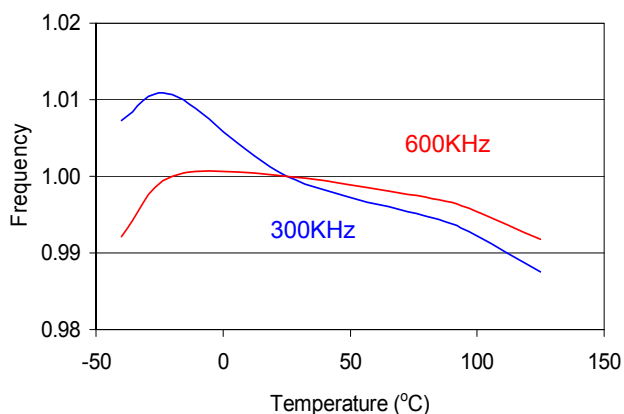


Figure 7. Frequency vs. Temperature, Normalized

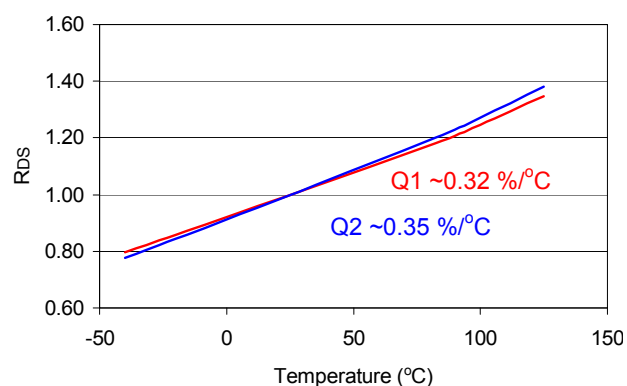


Figure 8. R_{DS} vs. Temperature, Normalized ($V_{CC} = V_{GS} = 5\text{ V}$)

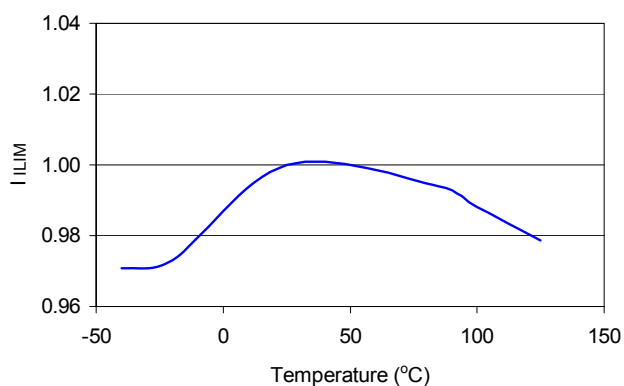


Figure 9. I_{LIM} Current (I_{LIM}) vs. Temperature, Normalized

Application Circuit

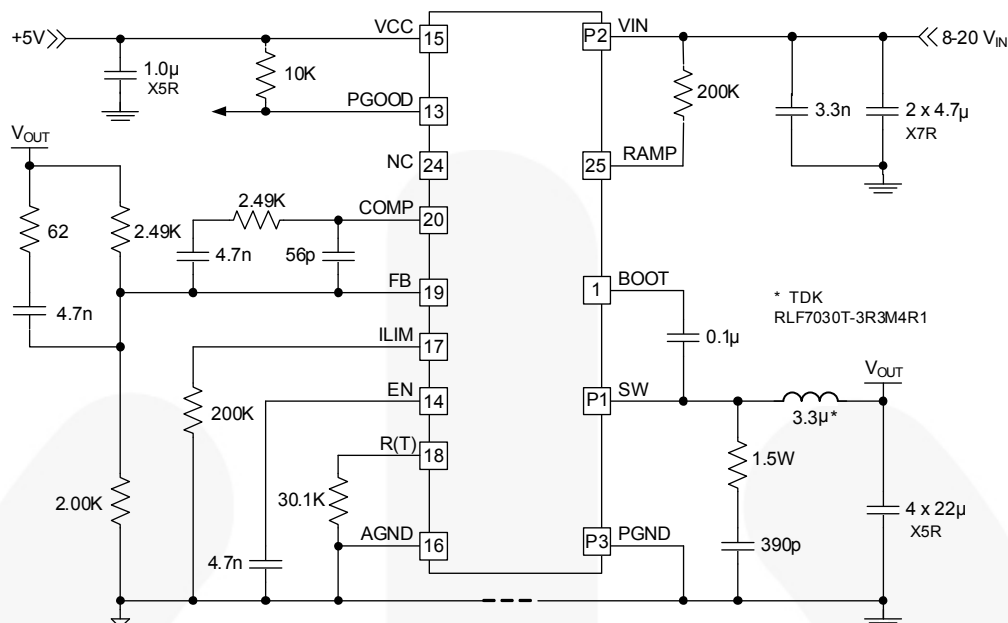


Figure 10. Application Circuit: 1.8 V_{OUT}, 500 KHz

Typical Performance Characteristics

Typical operating characteristics using the circuit shown in Figure 10. $V_{IN}=16\text{ V}$, $V_{CC}=5\text{ V}$, unless otherwise specified.

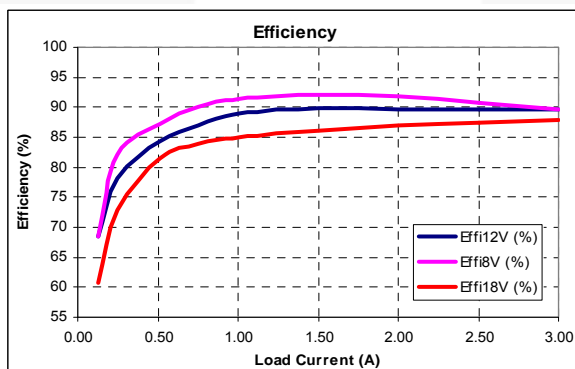


Figure 11. 1.8 V_{OUT} Efficiency Over V_{IN} vs. Load

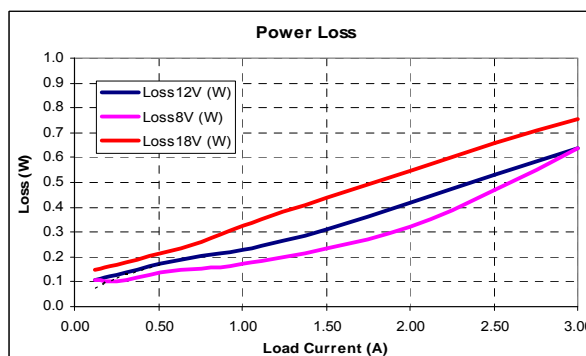


Figure 12. 1.8 V_{OUT} Dissipation Over V_{IN} vs. Load

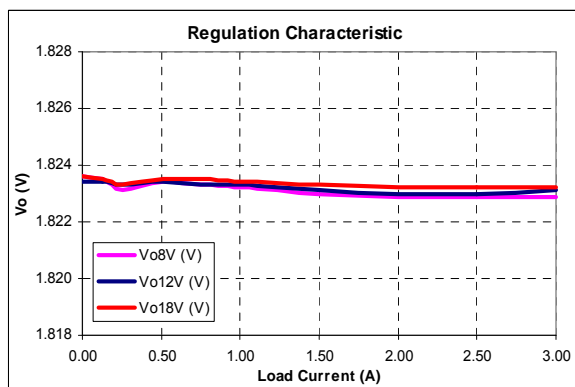
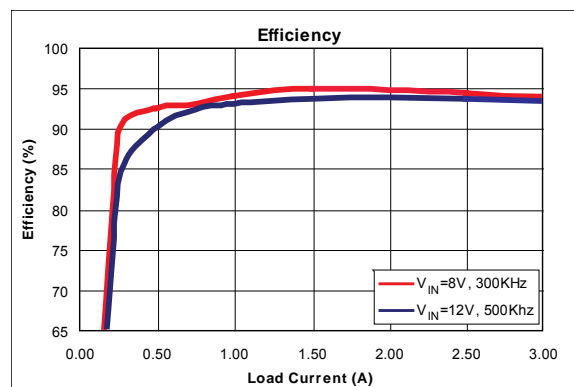
Figure 13. 1.8 V_{OUT} Regulation vs. Load

Figure 14. 3.3 V_{OUT} Efficiency vs. Load
(Circuit Values Changed)

Typical Performance Characteristics (Continued)

Typical operating characteristics using the circuit shown in Figure 10. $V_{IN}=12\text{ V}$, $V_{CC}=5\text{ V}$, unless otherwise specified.

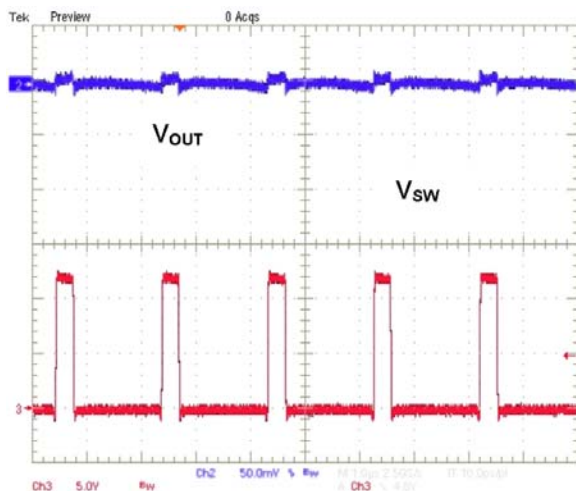


Figure 15. SW and V_{OUT} Ripple, 3 A Load

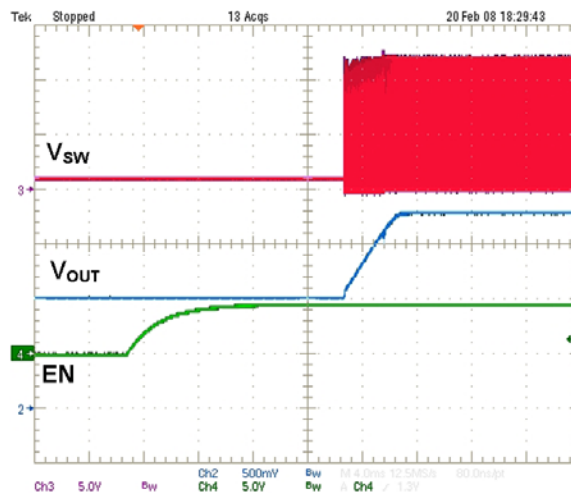


Figure 16. Startup with 1 V Pre-Bias on V_{OUT}

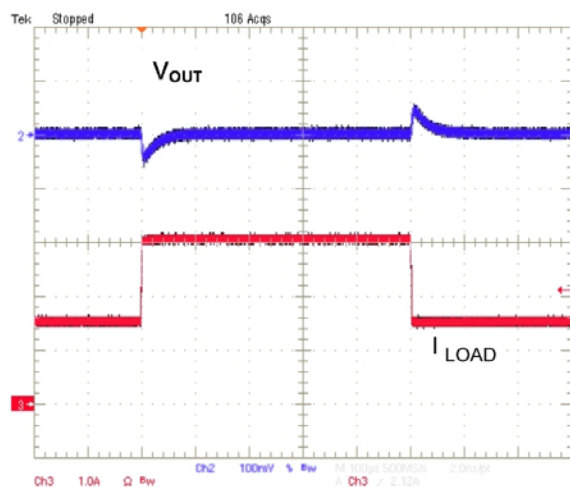


Figure 17. Transient Response, 1.5-3 A Load
(Circuit Values Changed)

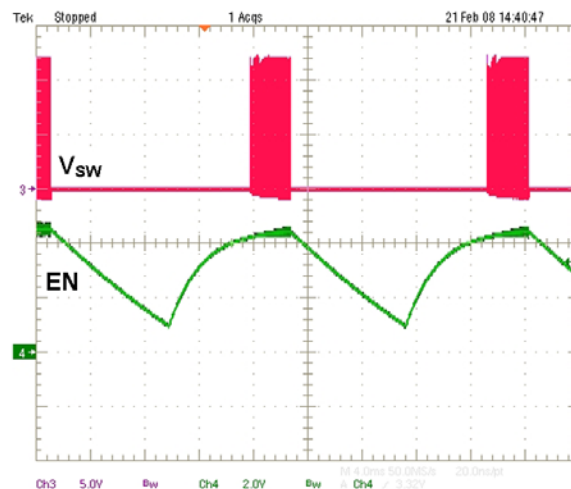


Figure 18. Re-start on Fault

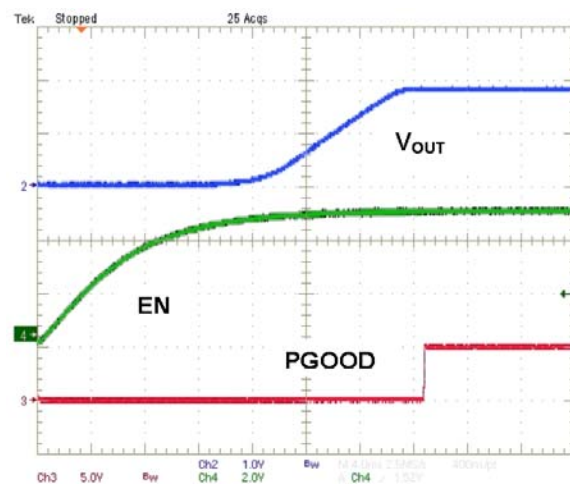


Figure 19. Startup, 3 A Load

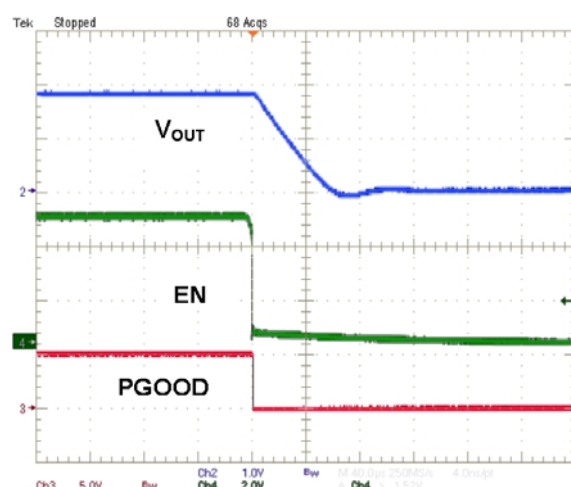


Figure 20. Shutdown, 3 A Load

Circuit Description

Initialization

Once V_{CC} exceeds the UVLO threshold and EN is HIGH, the IC checks for an open or shorted FB pin before releasing the internal soft-start ramp (SS).

If R1 is open (as shown in Figure 1), the error amplifier output (COMP) is forced LOW and no pulses are generated. After the SS ramp times out (T1.0), an under-voltage latched fault occurs.

If the parallel combination of R1 and R_{BIAS} is $\leq 1K\Omega$, the internal SS ramp is not released and the regulator does not start.

Soft-Start

Once internal SS ramp has charged to 0.8 V (T0.8), the output voltage is in regulation. Until SS ramp reaches 1.0 V (T1.0), the "Fault Latch" is inhibited.

To avoid skipping the soft-start cycle, it is necessary to apply V_{IN} before V_{CC} reaches its UVLO threshold.

Soft-start time is a function of oscillator frequency.

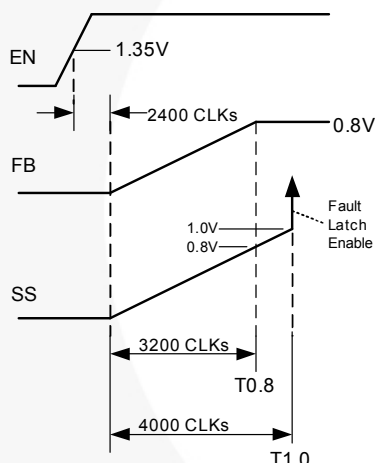


Figure 21. Soft-Start Timing Diagram

The regulator does not allow the low-side MOSFET to operate in full synchronous rectification mode until internal SS ramp reaches 95% of V_{REF} (~0.76 V). This helps the regulator start against pre-biased outputs (as shown in Figure 16) and ensures that inductor current does not "ratchet" up during the soft-start cycle.

V_{CC} UVLO or toggling the EN pin discharges the SS and resets the IC.

Bias Supply

The FAN2103 requires a 5 V supply rail to bias the IC and provide gate-drive energy and controller power. Connect a $\geq 1.0 \mu\text{F}$ X5R or X7R decoupling capacitor between V_{CC} and PGND. Whenever the EN pin is pulled up to V_{CC} , the 5 V supply connected to V_{CC} should be turned ON after V_{IN} comes up. If the power supply is turned ON using EN pin with an external control after V_{CC} and V_{IN} come up, the V_{CC} and V_{IN} power sequencing is not relevant.

Since V_{CC} is used to drive the internal MOSFET gates, supply current is frequency and voltage dependent. Approximate V_{CC} current (I_{CC}) can be calculated using:

$$I_{CC}(\text{mA}) = 4.58 + \left[\left(\frac{V_{CC} - 5}{227} + 0.013 \right) \cdot (f - 128) \right] \quad (1)$$

where frequency (f) is expressed in KHz.

Setting the Output Voltage

The output voltage of the regulator can be set from 0.8 V to ~80% of V_{IN} by an external resistor divider (R1 and R_{BIAS} in Figure 1).

The internal reference is 0.8 V with 650 nA, sourced from the FB pin to ensure that if the pin is open, the regulator does not start.

The external resistor divider is calculated using:

$$\frac{0.8V}{R_{BIAS}} = \frac{V_{OUT} - 0.8V}{R1} + 650\text{nA} \quad (2)$$

Connect R_{BIAS} between FB and AGND.

Setting the Frequency

Oscillator frequency is determined by an external resistor, R_T , connected between the R(T) pin and AGND:

$$f(\text{KHz}) = \frac{10^6}{(65 \cdot R_T) + 135} \quad (3)$$

where R_T is expressed in $K\Omega$.

$$R_{T(K\Omega)} = \frac{(10^6 / f) - 135}{65} \quad (4)$$

where frequency (f) is expressed in KHz.

The regulator does not start if R_T is left open.

Calculating the Inductor Value

Typically the inductor is set for a ripple current (ΔI_L) of 10% to 35% of the maximum DC load. Regulators requiring fast transient response use a value on the high side of this range, while regulators that require very low output ripple and/or use high-ESR capacitors restrict allowable ripple current:

$$\Delta I_L = \frac{V_{OUT} \cdot (1 - D)}{L \cdot f} \quad (5)$$

where f is the oscillator frequency and:

$$L = \frac{V_{OUT} \cdot (1 - D)}{\Delta I_L \cdot f} \quad (6)$$

Setting the Ramp Resistor Value

The internal ramp voltage excursion (ΔV_{RAMP}) during t_{ON} should be set to 0.6 V. R_{RAMP} is approximately:

$$R_{RAMP}(K\Omega) = \frac{(V_{IN} - 1.8) \cdot V_{OUT}}{18 \times 10^{-6} \cdot V_{IN} \cdot f} - 2 \quad (7)$$

where frequency (f) is expressed in KHz.

Setting the Current Limit

The current limit system involves two comparators. The MAX I_{LIMIT} comparator is used with a V_{ILIM} fixed-voltage reference and represents the maximum current limit allowable. This reference voltage is temperature compensated to reflect the $R_{DS(on)}$ variation of the low-side MOSFET. The ADJUST I_{LIMIT} comparator is used where the current limit needs to be set lower than the V_{ILIM} fixed reference. The 10 μA current source does not track the $R_{DS(on)}$ changes over temperature, so change is added into the equations for calculating the ADJUST I_{LIMIT} comparator reference voltage, as is shown below. Figure 22 shows a simplified schematic of the over-current system.

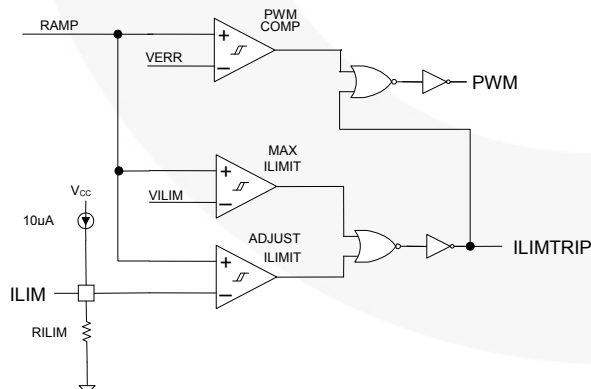


Figure 22. Current-Limit System Schematic

Since the I_{ILIM} voltage is set by a 10 μA current source into the R_{ILIM} resistor, the basic equation for setting the reference voltage is:

$$V_{RILIM} = 10\mu A \cdot R_{ILIM} \quad (8)$$

To calculate R_{ILIM} :

$$R_{ILIM} = V_{RILIM} / 10\mu A \quad (9)$$

The voltage V_{RILIM} is made up of two components, V_{BOT} (which relates to the current through the low-side MOSFET) and V_{RMPEAK} (which relates to the peak current through the inductor). Combining those two voltage terms results in:

$$R_{ILIM} = (V_{BOT} + V_{RMPEAK}) / 10\mu A \quad (10)$$

$$R_{ILIM} = \{0.96 + (I_{LOAD} \cdot R_{DS(on)} \cdot K_T \cdot 8)\} + \{D \cdot (V_{IN} - 1.8) / (f_{SW} \cdot 0.03 \cdot R_{RAMP})\} / 10\mu A \quad (11)$$

where:

$$V_{BOT} = 0.96 + (I_{LOAD} \cdot R_{DS(on)} \cdot K_T \cdot 8);$$

$$V_{RMPEAK} = D \cdot (V_{IN} - 1.8) / (f_{SW} \cdot 0.03 \cdot R_{RAMP});$$

I_{LOAD} = the desired maximum load current;

$R_{DS(on)}$ = the nominal $R_{DS(on)}$ of the low-side MOSFET;

K_T = the normalized temperature coefficient for the low-side MOSFET (on datasheet graph);

$D = V_{OUT} / V_{IN}$ duty cycle;

f_{SW} = Clock frequency in kHz; and

R_{RAMP} = chosen ramp resistor value in k Ω .

After 16 consecutive, pulse-by-pulse, current-limit cycles, the fault latch is set and the regulator shuts down. Cycling V_{CC} or EN restores operation after a normal soft-start cycle (refer to the Auto-Restart section).

The over-current protection fault latch is active during the soft-start cycle. Use 1% resistor for R_{ILIM} .

Loop Compensation

The loop is compensated using a feedback network around the error amplifier. Figure 23 shows a complete Type-3 compensation network. Type-2 compensation eliminates R_3 and C_3 .

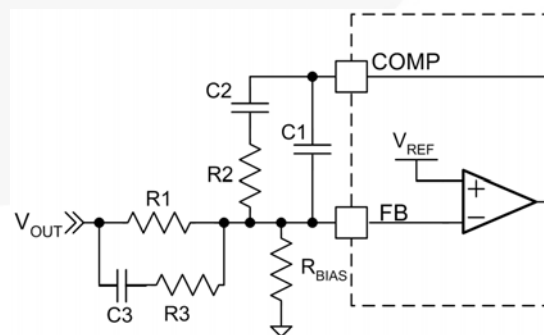


Figure 23. Compensation Network

Physical Dimensions

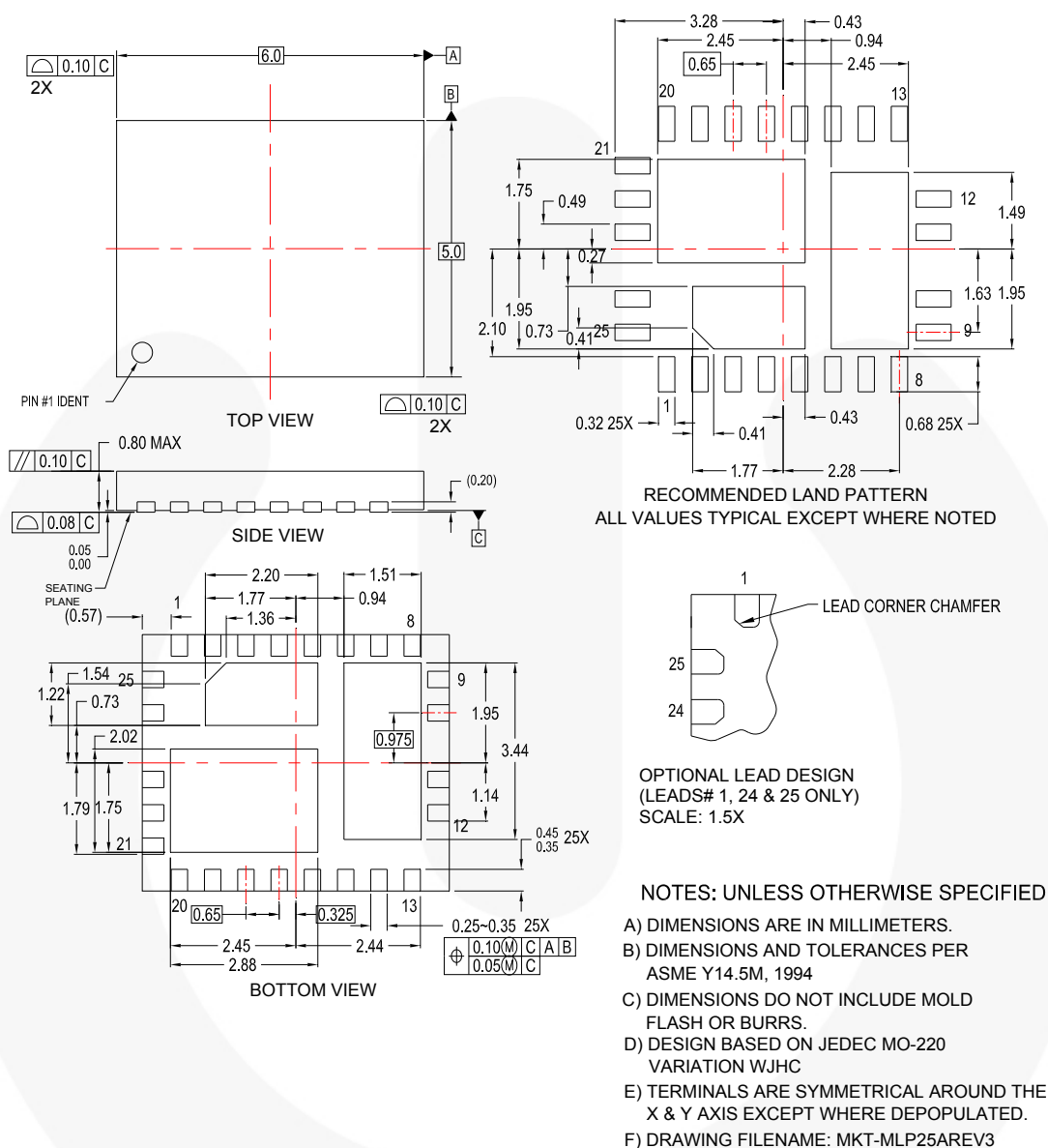


Figure 27. 5x6 mm Molded Leadless Package (MLP)

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

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CROSSVOL™	GTO™		TinyPower™
CTL™	IntelliMAX™	Saving our world, 1mW/kW at a time™	TinyPWM™
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Dual Cool™	MegaBuck™	SMART START™	TriFault Detect™
EcoSPARK®	MICROCOUPLER™	Solutions for Your Success™	TRUECURRENT®*
EfficientMax™	MicroFET™	SPM®	µSerDes™
ESBC™	MicroPak™	STEALTH™	
 Fairchild®	MicroPak2™	SuperFET®	UHC™
Fairchild Semiconductor®	MillerDrive™	SuperSOT™-3	Ultra FRFET™
FACT Quiet Series™	MotionMax™	SuperSOT™-6	UniFET™
FACT®	mWSaver™	SuperSOT™-8	VCX™
FAST®	OptoHiT™	SupreMOS®	VisualMax™
FastvCore™	OPTOLOGIC®	SyncLock™	VoltagePlus™
FETBench™	OPTOPLANAR®	 SYSTEM GENERAL®*	XS™
FlashWriter®*			
FPS™			

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I62

AMEYA360

Components Supply Platform

Authorized Distribution Brand :



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Welcome to visit www.ameya360.com

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