May 2014

# FDMC86265P

## P-Channel PowerTrench® MOSFET

### -150 V, -1 A, 1.2 Ω

### Features

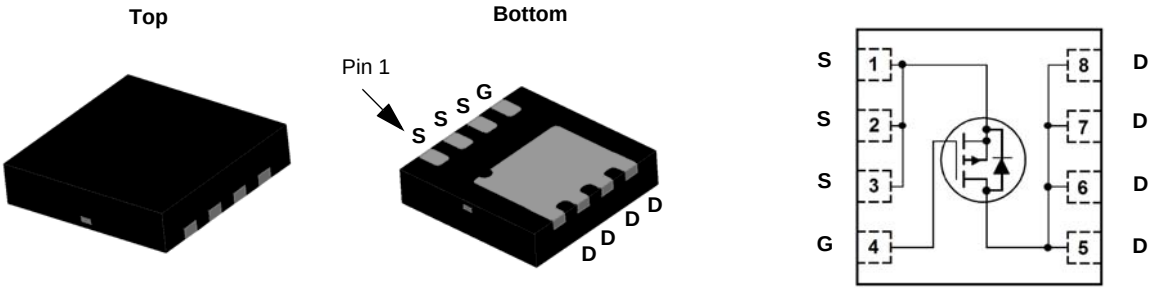
- Max $r_{DS(on)}$ = 1.2 Ω at $V_{GS}$ = -10 V, $I_D$ = -1 A
- Max $r_{DS(on)}$ = 1.4 Ω at $V_{GS}$ = -6 V, $I_D$ = -0.9 A
- Very low RDS-on mid voltage P-channel silicon technology optimised for low Qg
- This product is optimised for fast switching applications as well as load switch applications
- 100% UIL Tested
- RoHS Compliant

### General Description

This P-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been optimized for the on-state resistance and yet maintain superior switching performance.

### Applications

- Active Clamp Switch
- Load Switch




MLP 3.3x3.3

## MOSFET Maximum Ratings $T_A$ = 25 °C unless otherwise noted

| Symbol | Parameter | | | Ratings | Units |
|---|---|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | | | -150 | V |
| $V_{GS}$ | Gate to Source Voltage | | | ±25 | V |
| $I_D$ | Drain Current -Continuous | $T_C$ = 25 °C | | -1.8 | A |
| | -Continuous | $T_A$ = 25 °C | (Note 1a) | -1 | |
| | -Pulsed | | | -2 | |
| $E_{AS}$ | Single Pulse Avalanche Energy | | (Note 3) | 6 | mJ |
| $P_D$ | Power Dissipation | $T_C$ = 25 °C | | 16 | W |
| | Power Dissipation | $T_A$ = 25 °C | (Note 1a) | 2.3 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | | -55 to + 150 | °C |

### Thermal Characteristics

| | | | | |
|---|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | | 7.5 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | (Note 1a) | 53 | |

### Package Marking and Ordering Information

| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|
| FDMC86265P | FDMC86265P | Power 33 | 13 ” | 12 mm | 3000 units |

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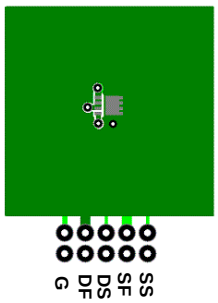
## Electrical Characteristics $T_J$ = 25 °C unless otherwise noted

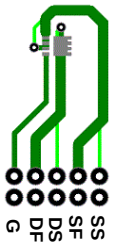
| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = -250 μA, $V_{GS}$ = 0 V | -150 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = -250 μA, referenced to 25 °C | | -125 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = -120 V, $V_{GS}$ = 0 V | | | -1 | μA |
| $I_{GSS}$ | Gate to Source Leakage Current | $V_{GS}$ = ±25 V, $V_{DS}$ = 0 V | | | ±100 | nA |
| **On Characteristics** | | | | | | |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = -250 μA | -2 | -3.2 | -4 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D$ = -250 μA, referenced to 25 °C | | 5 | | mV/°C |
| $r_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS}$ = -10 V, $I_D$ = -1 A | | 0.86 | 1.2 | Ω |
| | | $V_{GS}$ = -6 V, $I_D$ = -0.9 A | | 0.95 | 1.4 | |
| | | $V_{GS}$ = -10 V, $I_D$ = -1 A, $T_J$ = 125 °C | | 1.53 | 2.2 | |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = -10 V, $I_D$ = -1 A | | 1.9 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = -75 V, $V_{GS}$ = 0 V, f = 1 MHz | | 158 | 210 | pF |
| $C_{oss}$ | Output Capacitance | | | 16 | 25 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 0.7 | 5 | pF |
| $R_g$ | Gate Resistance | | 0.1 | 3 | 7.5 | Ω |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = -75 V, $I_D$ = -1 A, $V_{GS}$ = -10 V, $R_{GEN}$ = 6 Ω | | 5.8 | 12 | ns |
| $t_r$ | Rise Time | | | 2.2 | 10 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 8 | 16 | ns |
| $t_f$ | Fall Time | | | 6.4 | 13 | ns |
| $Q_{g(TOT)}$ | Total Gate Charge | $V_{GS}$ = 0 V to -10 V; $V_{DD}$ = -75 V, $I_D$ = -1 A | | 2.8 | 4 | nC |
| $Q_{gs}$ | Total Gate Charge | | | 0.8 | | nC |
| $Q_{gd}$ | Gate to Drain “Miller” Charge | | | 0.7 | | nC |
| **Drain-Source Diode Characteristics** | | | | | | |
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = -1 A (Note 2) | | -0.87 | -1.3 | V |
| $t_{rr}$ | Reverse Recovery Time | $I_F$ = -1 A, di/dt = 100 A/μs | | 50 | 80 | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | | 78 | 124 | nC |

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 $in^2$ pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.




a) 53 °C/W when mounted on a 1 $in^2$ pad of 2 oz copper




b) 125 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

3. Starting $T_J$ = 25 °C; P-ch: L =3 mH, $I_{AS}$ = -2 A, $V_{DD}$ = -150 V, $V_{GS}$ = -10 V. 100% test at L = 0.1 mH, $I_{AS}$ = -9 A.

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## Typical Characteristics $T_J$ = 25 °C unless otherwise noted

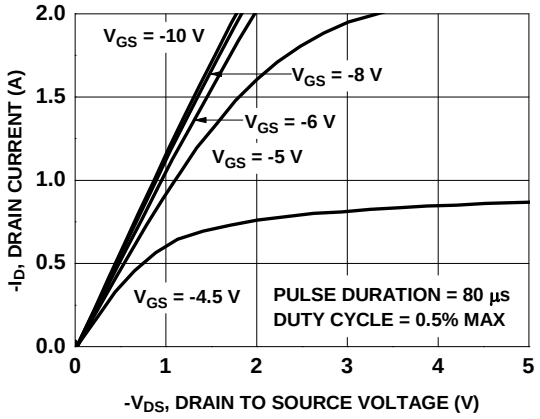



**Figure 1. On Region Characteristics**

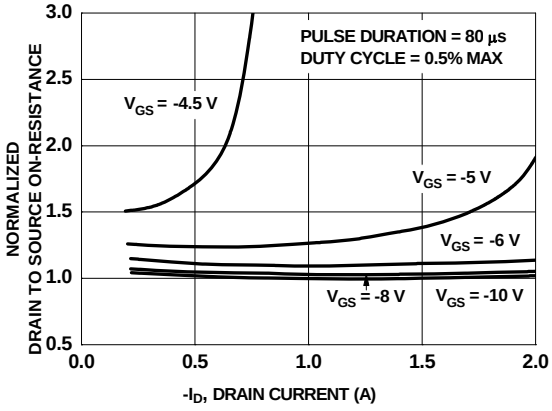



**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**

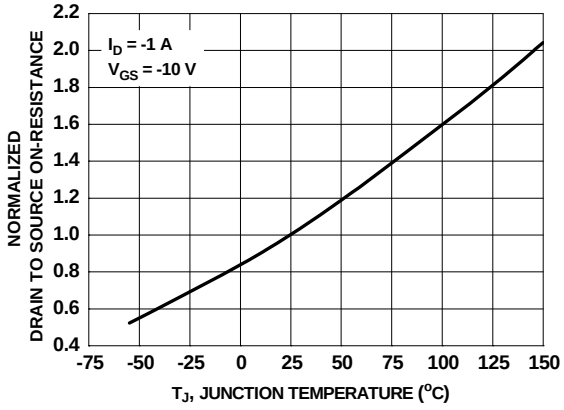



**Figure 3. Normalized On Resistance vs Junction Temperature**

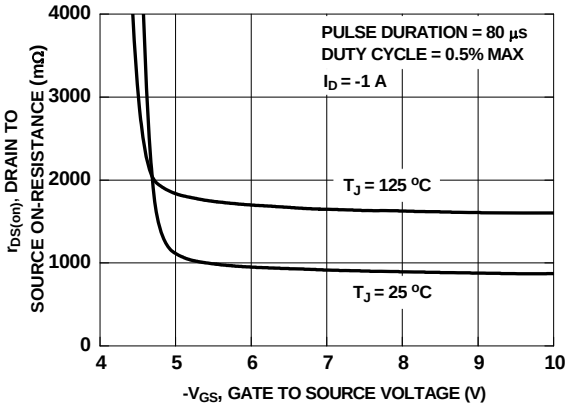



**Figure 4. On-Resistance vs Gate to Source Voltage**

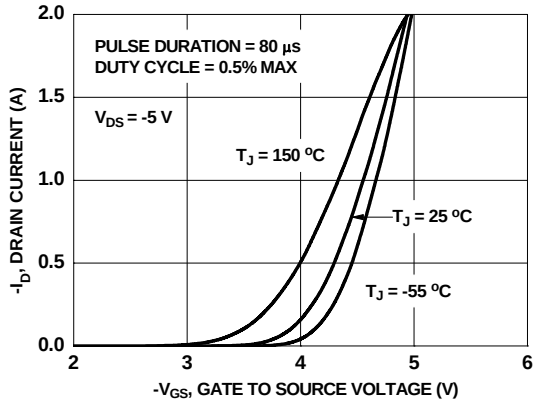



**Figure 5. Transfer Characteristics**

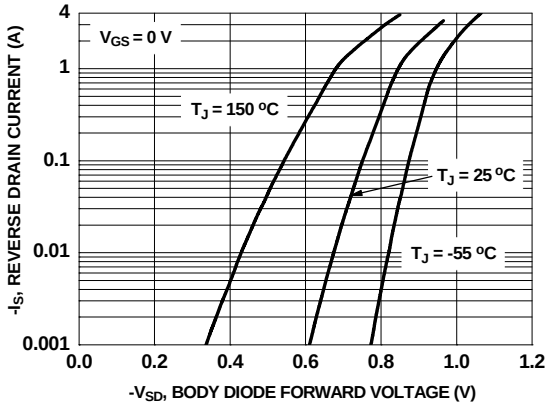



**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

## Typical Characteristics $T_J$ = 25 °C unless otherwise noted

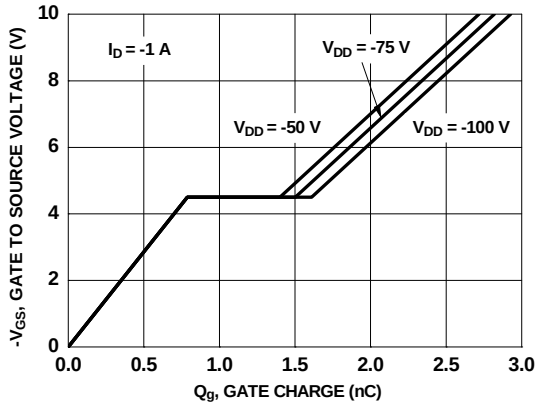



**Figure 7. Gate Charge Characteristics**

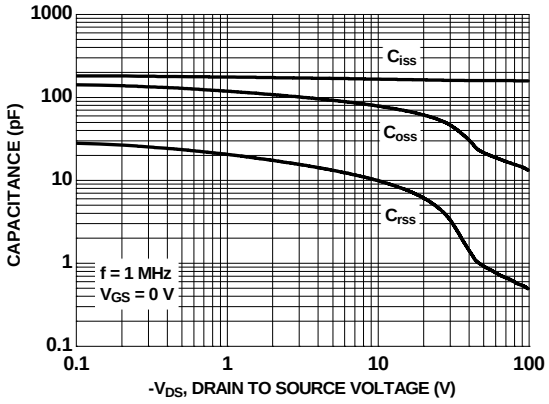



**Figure 8. Capacitance vs Drain to Source Voltage**

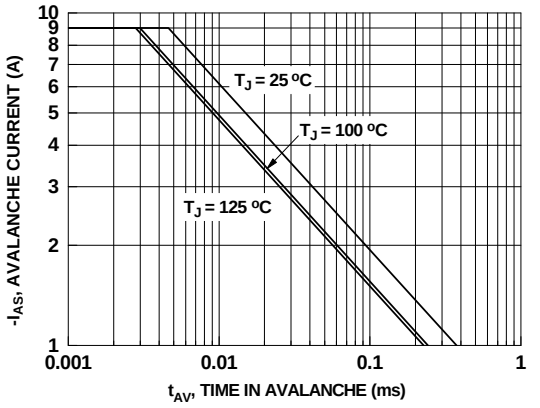



**Figure 9. Unclamped Inductive Switching Capability**

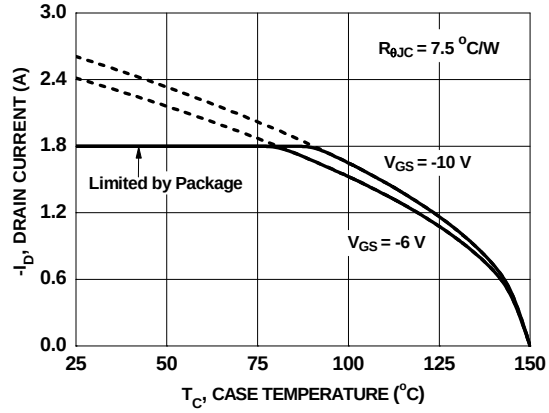



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

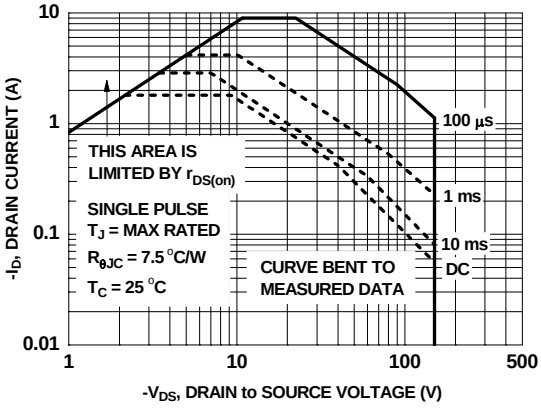



**Figure 11. Forward Bias Safe Operating Area**

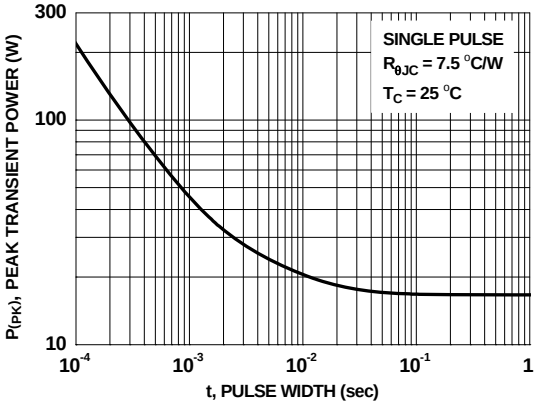



**Figure 12. Single Pulse Maximum Power Dissipation**

## Typical Characteristics $T_J$ = 25 °C unless otherwise noted

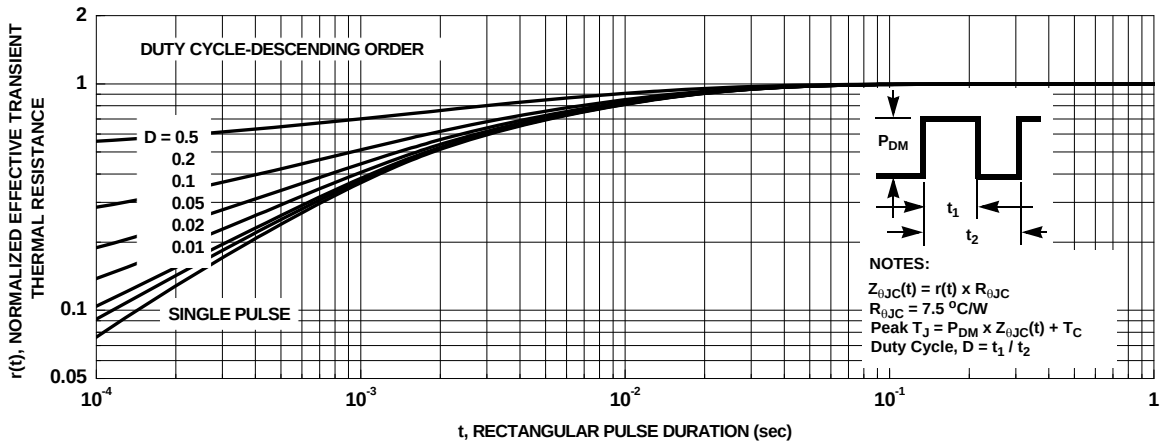
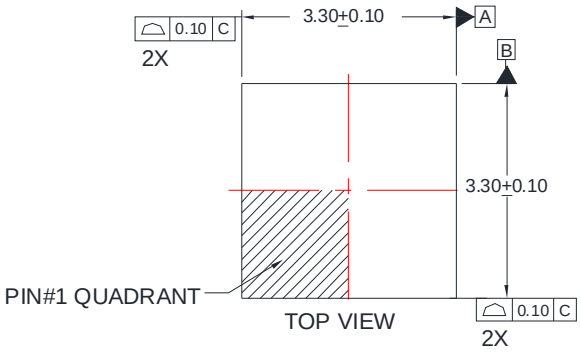
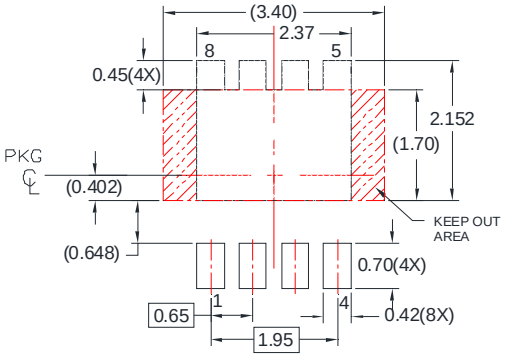


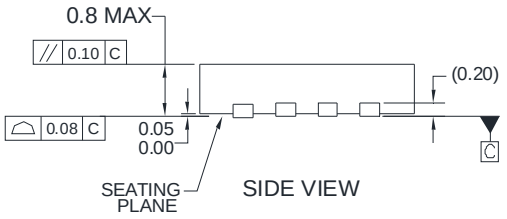

**Figure 13. Junction-to-Case Transient Thermal Response Curve**

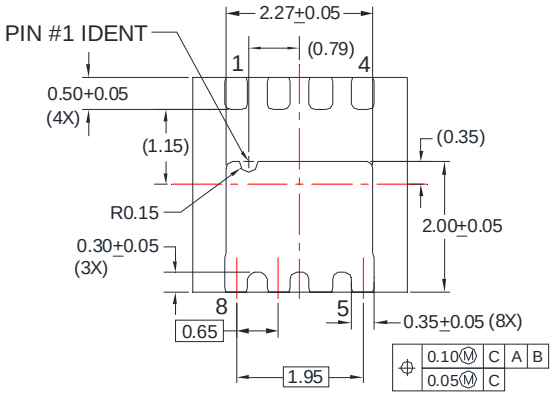
## Dimensional Outline and Pad Layout




RECOMMENDED LAND PATTERN




BOTTOM VIEW

NOTES:

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B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

D. LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY

E. DRAWING FILE NAME : MKT-MLP08Srev2

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Rev. I68

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