



# STB230NH03L

N-channel 30 V, 2.3 m $\Omega$ , 80 A D<sup>2</sup>PAK  
STripFET™ Power MOSFET

## Features

Order code	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STB230NH03L	30V	< 3m $\Omega$	80A <sup>(1)</sup>

- This value is limited by package
- R<sub>DS(on)</sub> Qg industry's benchmark
  - Conduction losses reduced
  - Switching losses reduced
  - Low threshold device

## Applications

- Switching applications
  - Specifically designed and optimized for high efficiency DC/DC converters
- OR-ing

## Description

This N-channel enhancement mode Power MOSFET benefits from the latest refinement of STMicroelectronics' unique "single feature size" strip-based process, which decreases the critical alignment steps to offer exceptional manufacturing reproducibility. The result is a transistor with extremely high packing density for low on-resistance, rugged avalanche characteristics and low gate charge.

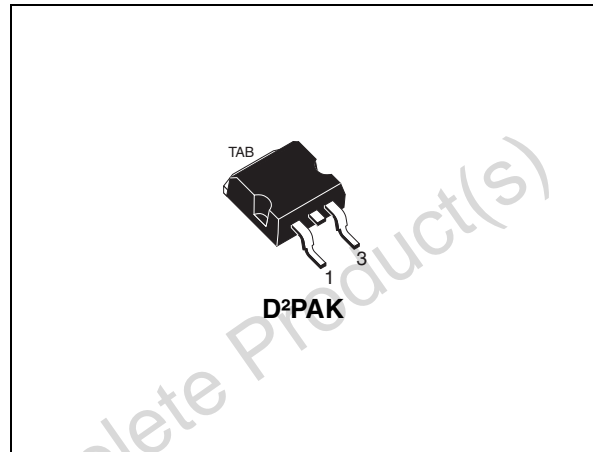


Figure 1. Internal schematic diagram

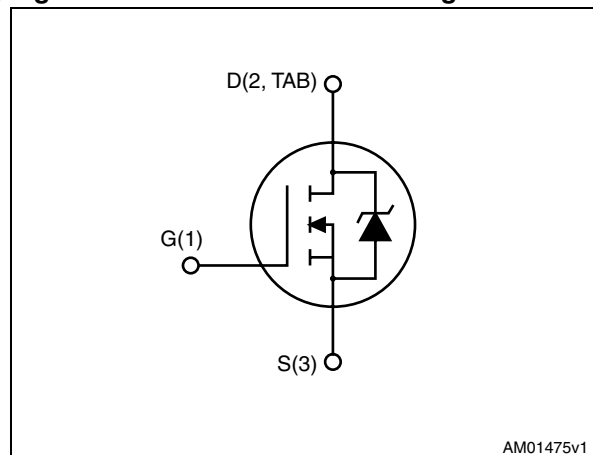


Table 1. Device summary

Order code	Marking	Package	Packaging
STB230NH03L	B230NH03L	D <sup>2</sup> PAK	Tape and reel

# Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>3</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>4</b>
2.1	Electrical characteristics (curves) .....	6
<b>3</b>	<b>Test circuit</b> .....	<b>8</b>
<b>4</b>	<b>Package mechanical data</b> .....	<b>9</b>
<b>5</b>	<b>Packaging mechanical data</b> .....	<b>12</b>
<b>6</b>	<b>Revision history</b> .....	<b>14</b>

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	30	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	80	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	178	A
$I_{DM}^{(2)}$	Drain current (pulsed)	320	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	300	W
	Derating factor	2	W/ $^\circ\text{C}$
$T_J$	Operating junction temperature	-55 to 175	$^\circ\text{C}$

1. This value is limited by package.
2. Pulse width limited by safe operating area.

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance junction-case max	0.5	$^\circ\text{C}/\text{W}$
$R_{thJA}$	Thermal resistance junction-ambient max	62.5	$^\circ\text{C}/\text{W}$

**Table 4. Avalanche data**

Symbol	Parameter	Value	Unit
$I_{AS}$	Avalanche current	60	A
$E_{AS}^{(1)}$	Single pulse avalanche energy	1150	mJ

1. Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $I_D = I_{AV}$ ,  $V_{DD} = 24\text{ V}$ .

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ( $V_{GS} = 0$ )	$I_D = 1 \text{ mA}$	30			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 30 \text{ V}$ , $V_{DS} = 30 \text{ V}, T_C = 125^{\circ}C$			1 10	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20 \text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	1	1.5	2.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}, I_D = 40 \text{ A}$		2.3	3	$\text{m}\Omega$
		$V_{GS} = 4.5 \text{ V}, I_D = 40 \text{ A}$		2.75	3.4	$\text{m}\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 10 \text{ V}, f = 1 \text{ MHz}$ , $V_{GS} = 0$		4700		pF
$C_{oss}$	Output capacitance		-	1600	-	pF
$C_{rss}$	Reverse transfer capacitance				85	
$Q_g$	Total gate charge	$V_{DD} = 15 \text{ V}, I_D = 60 \text{ A}$		72		nC
$Q_{gs}$	Gate-source charge	$V_{GS} = 10 \text{ V}$	-	15	-	nC
$Q_{gd}$	Gate-drain charge	(see Figure 15)		11		nC
$R_G$	Gate input resistance	$f = 1 \text{ MHz}$ Gate DC Bias = 0 Test signal level = 20 mV open drain	-	5.5	-	$\Omega$

**Table 7. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=15\text{ V}$ , $I_D=60\text{ A}$ , $R_G=4.7\ \Omega$ , $V_{GS}=10\text{ V}$ <i>(see Figure 14)</i>	-	11	-	ns
$t_r$	Rise time			322		ns
$t_{d(off)}$	Turn-off delay time		-	123	-	ns
$t_f$	Fall time			102		ns

**Table 8. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		250	A
$I_{SDM}^{(2)}$	Source-drain current (pulsed)				1000	A
$V_{SD}^{(3)}$	Forward on voltage	$I_{SD}=40\text{ A}$ , $V_{GS}=0$	-		1.3	V
$t_{rr}$	Reverse recovery time	$I_{SD}=120\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD}=20\text{ V}$ <i>(see Figure 19)</i>	-	42		ns
$Q_{rr}$	Reverse recovery charge			34.7		nC
$I_{RRM}$	Reverse recovery current			1.6		A
$t_{rr}$	Reverse recovery time	$I_{SD}=120\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD}=20\text{ V}$ , $T_j=150\text{ }^\circ\text{C}$ <i>(see Figure 19)</i>	-	47		ns
$Q_{rr}$	Reverse recovery charge			41.3		nC
$I_{RRM}$	Reverse recovery current			1.8		A

1. This value is silicon limited.
2. Pulse width limited by safe operating area.
3. Pulsed; pulse duration=300 $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

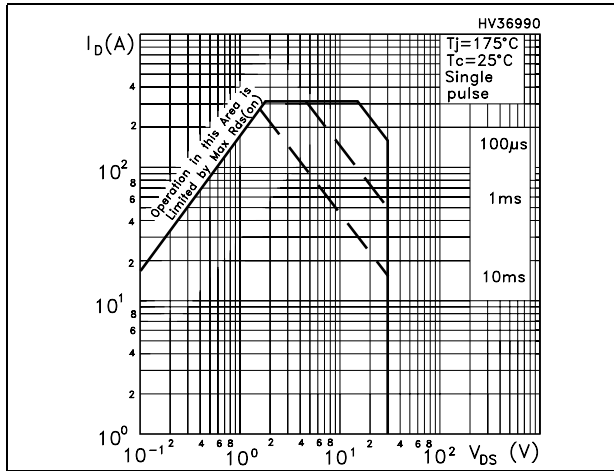


Figure 3. Thermal impedance

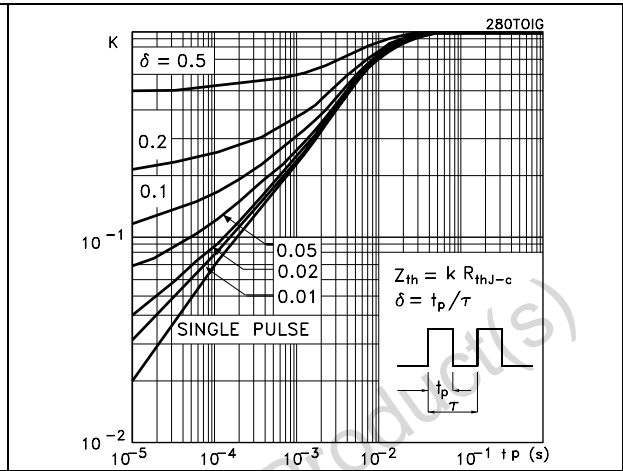


Figure 4. Output characteristics

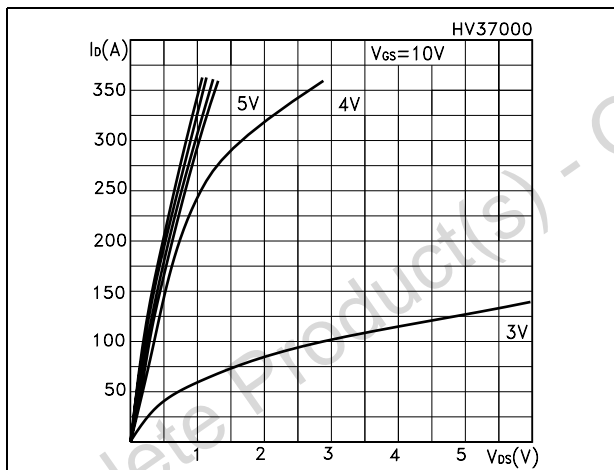


Figure 5. Transfer characteristics

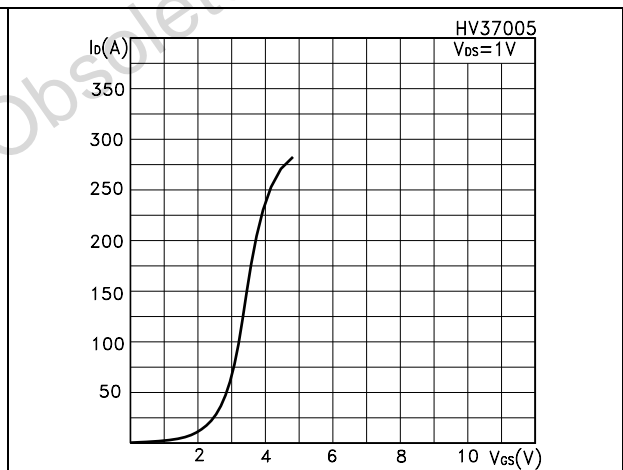


Figure 6. Static drain-source on resistance @  $V_{GS} = 4.5\text{ V}$

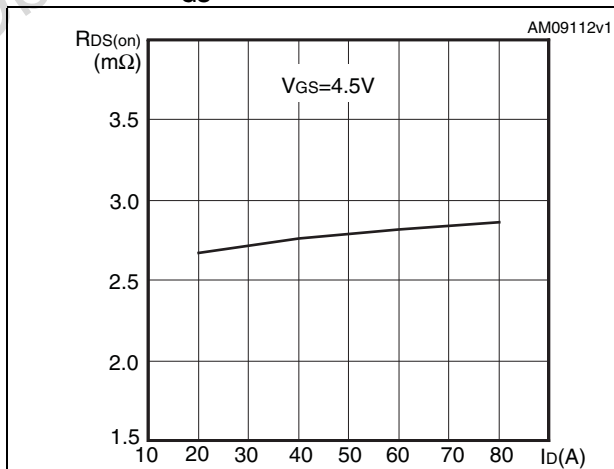


Figure 7. Static drain-source on resistance @  $V_{GS} = 10\text{ V}$

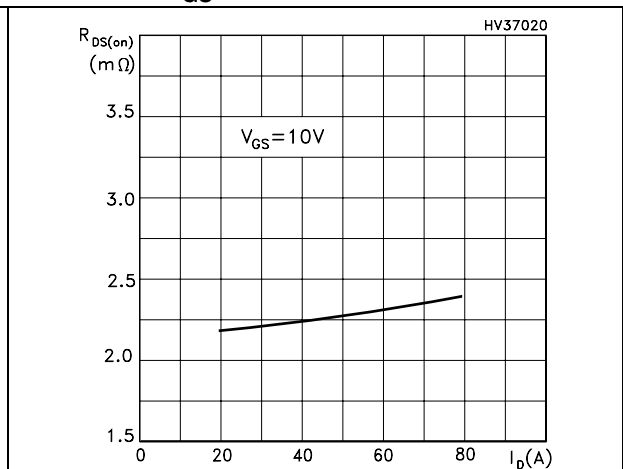


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

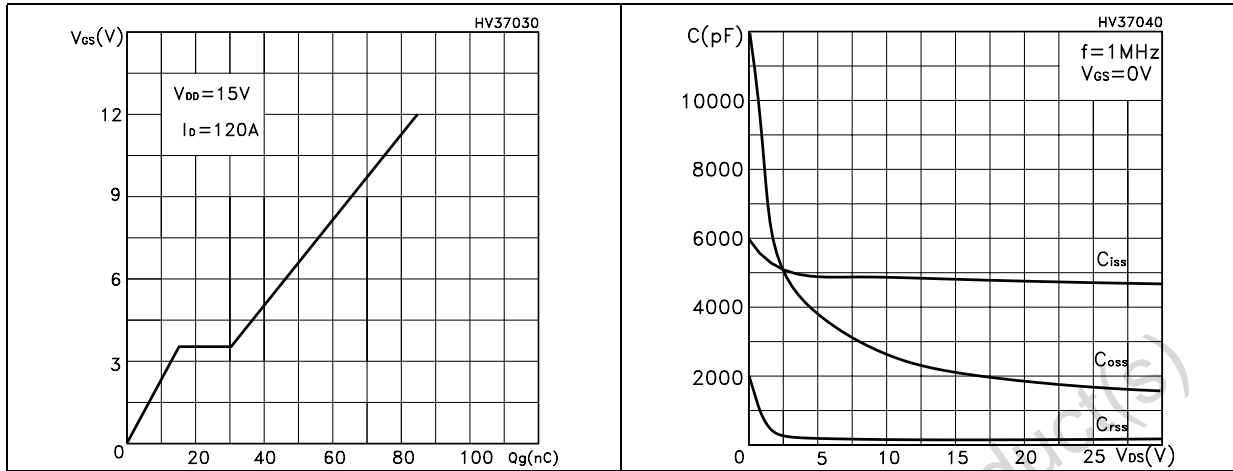


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

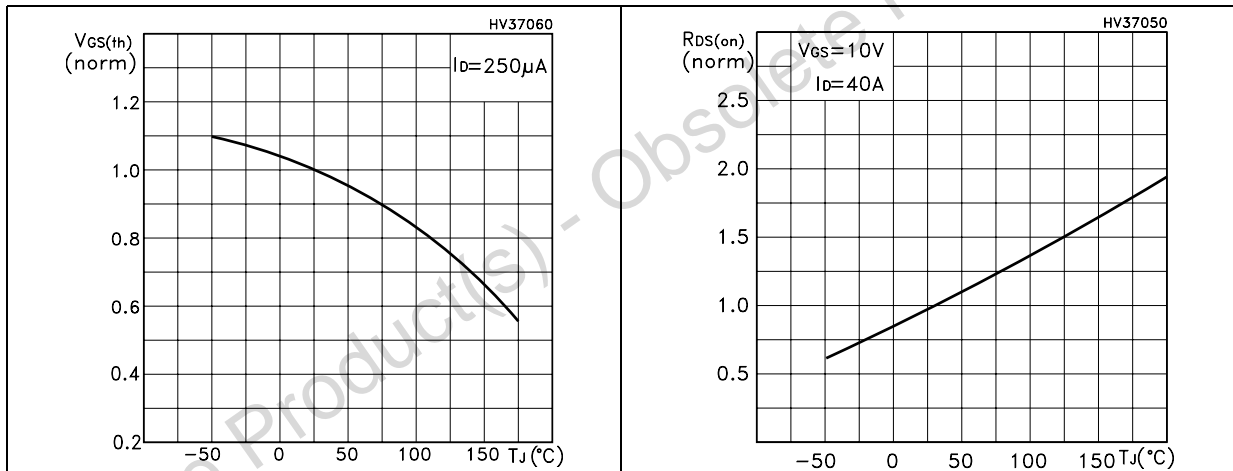
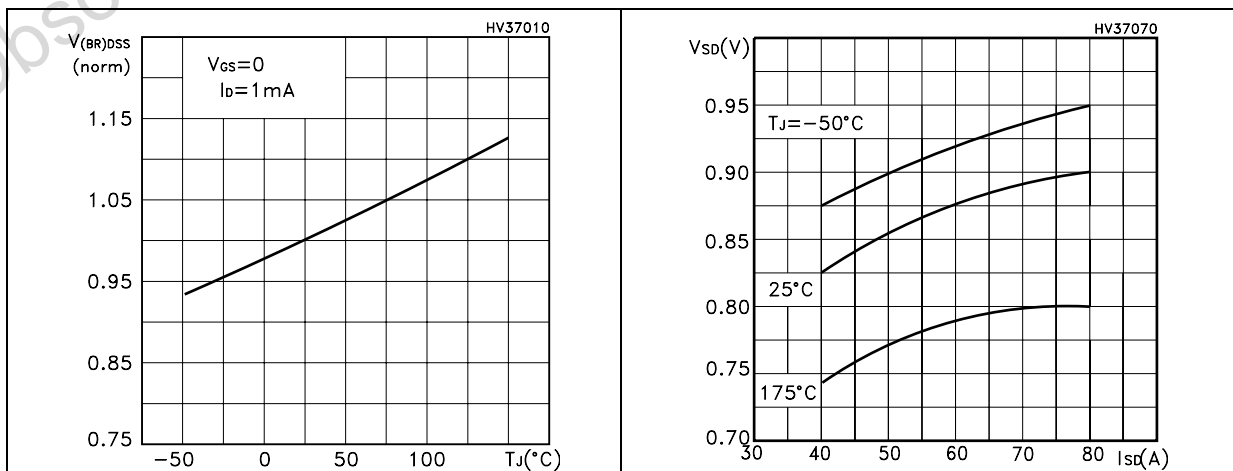
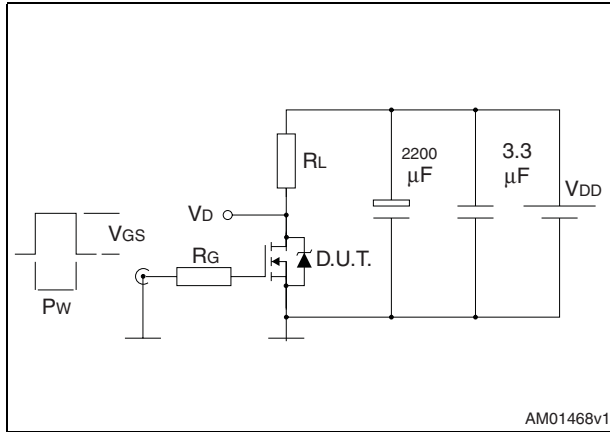


Figure 12. Normalized  $BV_{DSS}$  vs temperature Figure 13. Source-drain diode forward characteristics

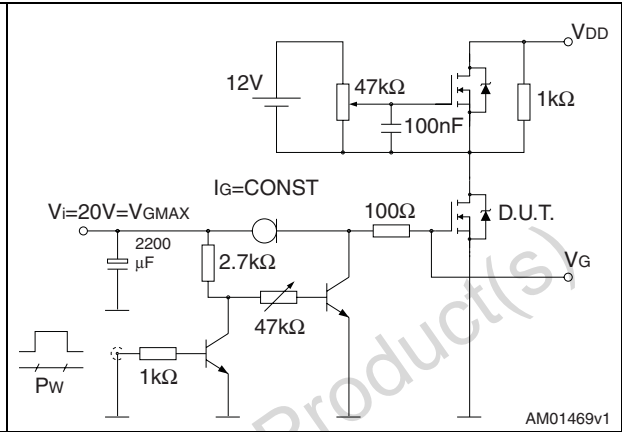


### 3 Test circuit

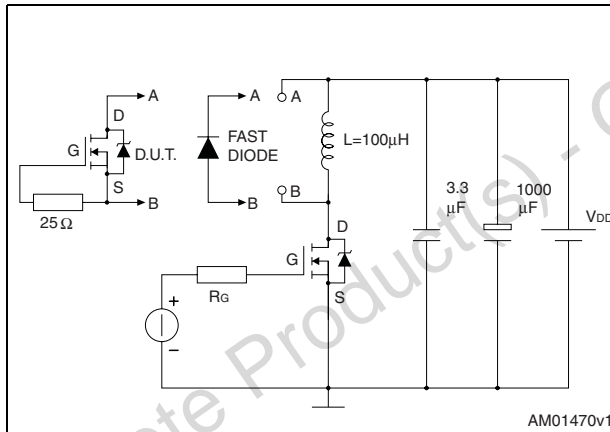
**Figure 14. Switching times test circuit for resistive load**



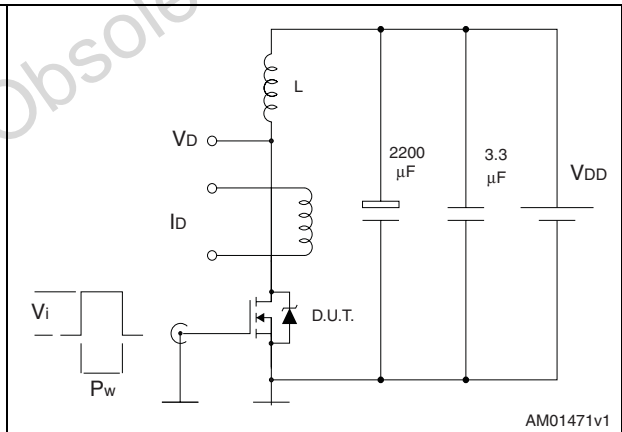
**Figure 15. Gate charge test circuit**



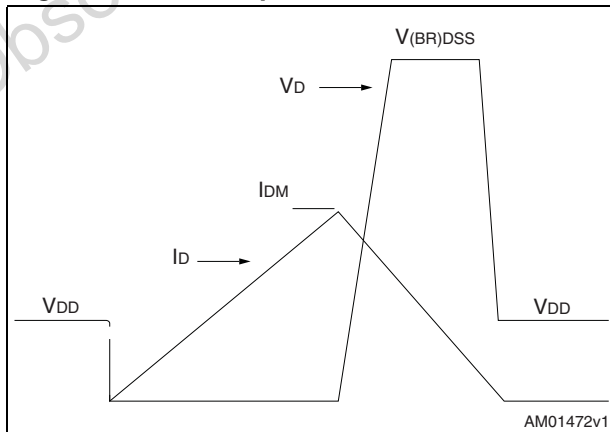
**Figure 16. Test circuit for inductive load switching and diode recovery times**



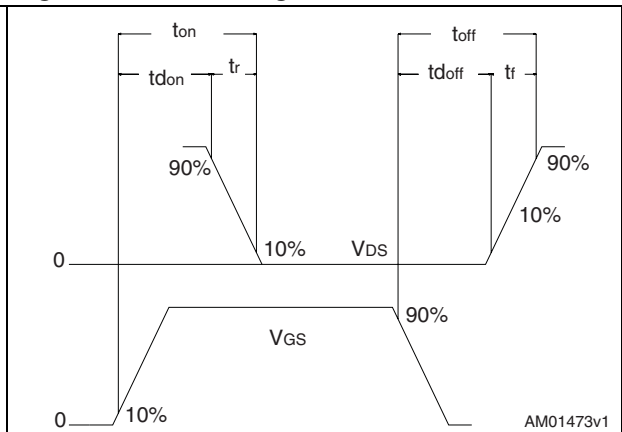
**Figure 17. Unclamped Inductive load test circuit**



**Figure 18. Unclamped inductive waveform**



**Figure 19. Switching time waveform**



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

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Table 9. D<sup>2</sup>PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 20. D<sup>2</sup>PAK (TO-263) drawing

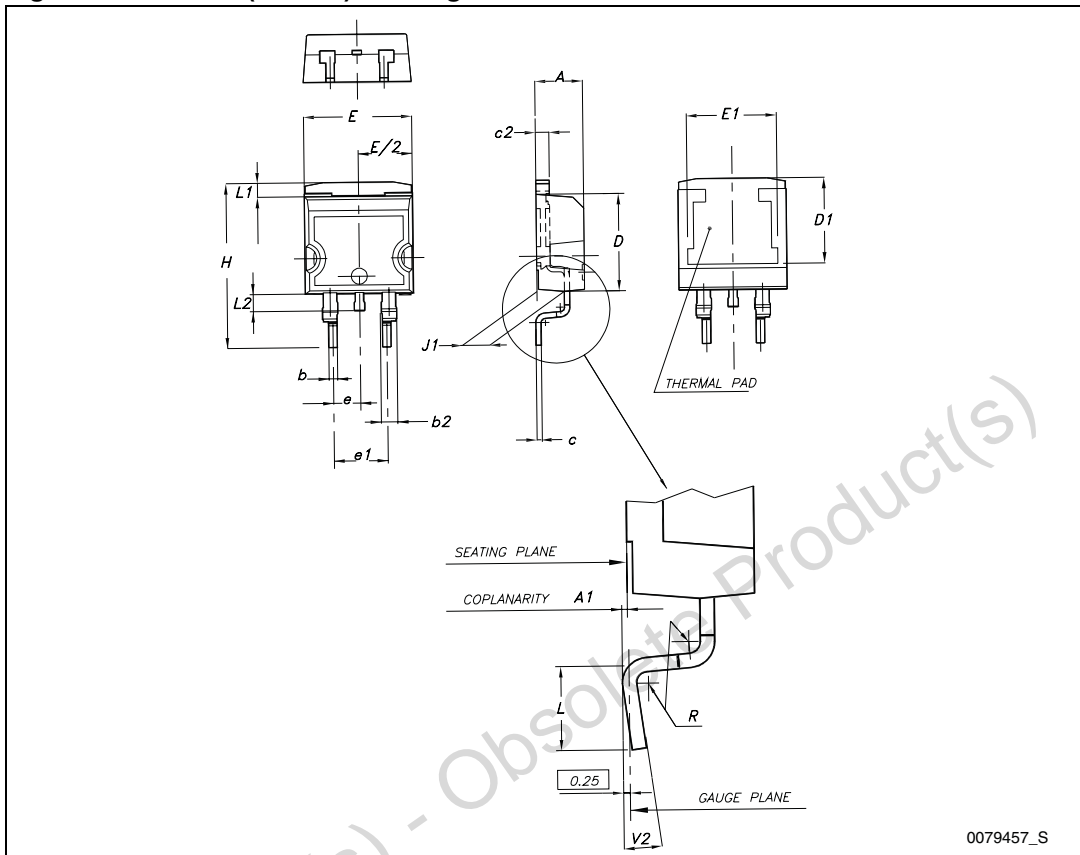
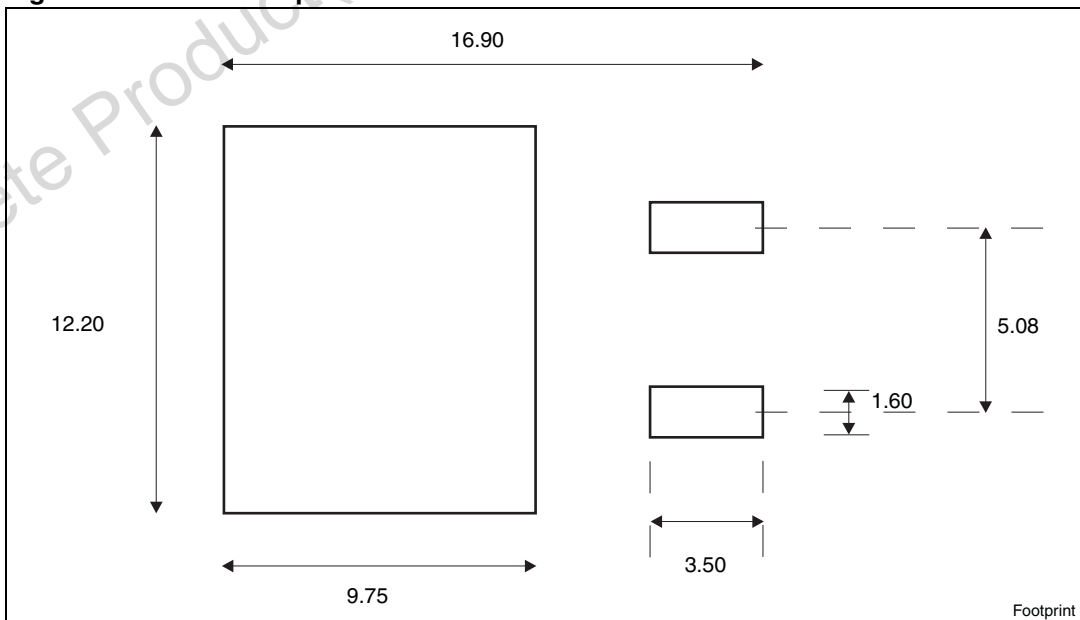


Figure 21. D<sup>2</sup>PAK footprint<sup>(a)</sup>



a. All dimension are in millimeters

## 5 Packaging mechanical data

Table 10. D<sup>2</sup>PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1		Base qty	1000
P2	1.9	2.1		Bulk qty	1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Figure 22. Tape

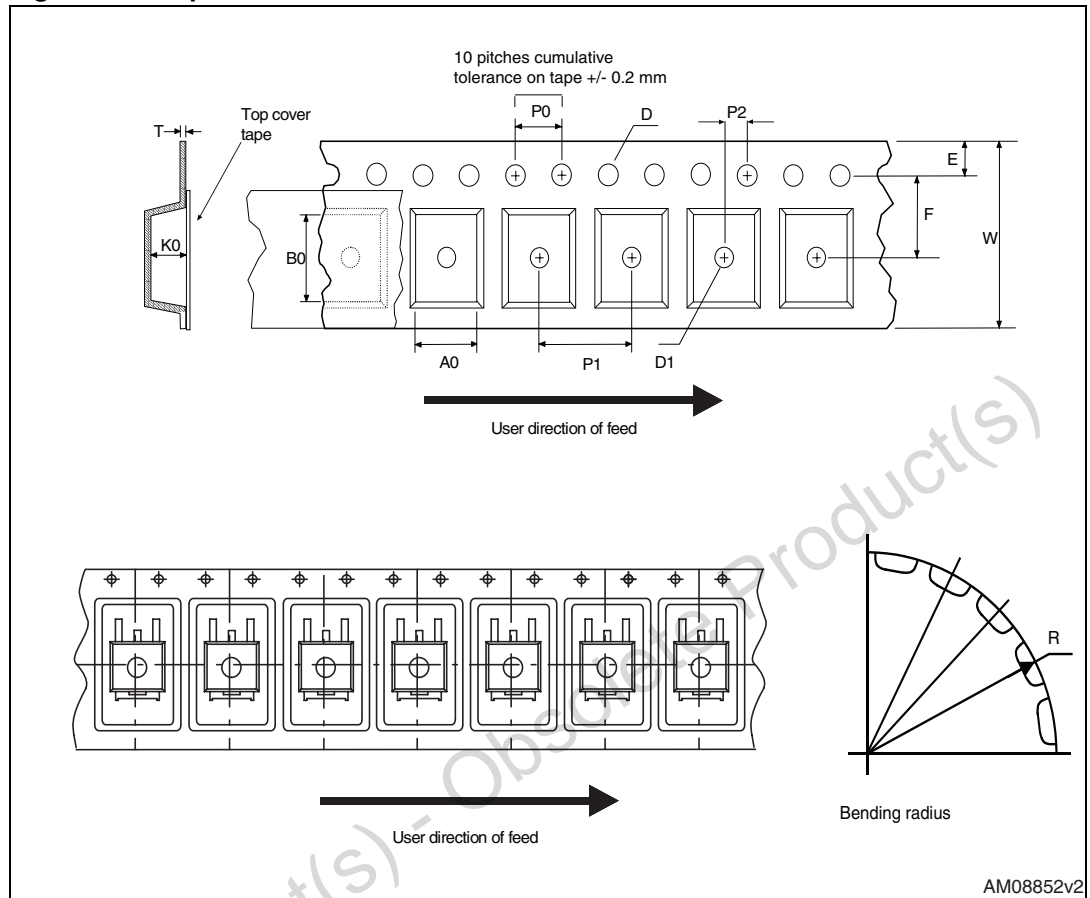
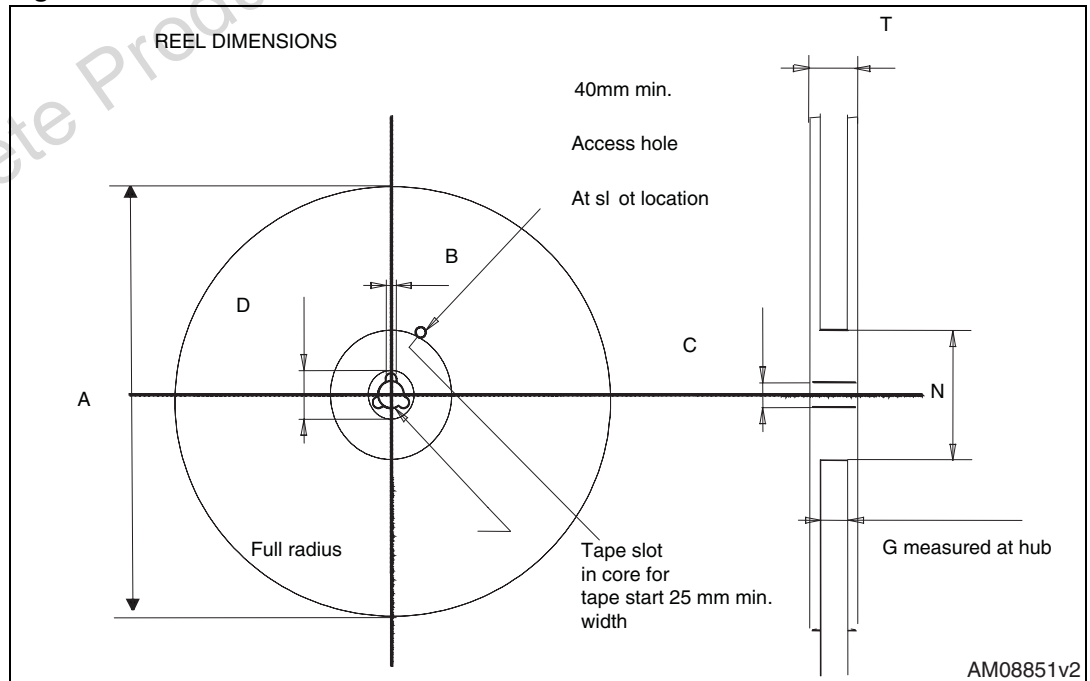


Figure 23. Reel



## 6 Revision history

Table 11. Revision history

Date	Revision	Changes
08-Jun-2007	1	Initial release.
27-Sep-2011	2	<ul style="list-style-type: none"><li>– <i>Figure 6: Static drain-source on resistance @ <math>V_{GS} = 4.5 V</math></i> has been added.</li><li>– Minor text change.</li></ul>

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