

Dual FET Bus Switch 2.5-V/3.3-V Low-Voltage High-Bandwidth Bus Switch

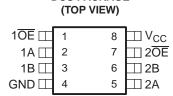
Check for Samples: SN74CB3Q3306A

FEATURES

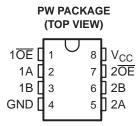
- High-Bandwidth Data Path (up to 500 MHz⁽¹⁾)
- 5-V-Tolerant I/Os With Device Powered Up or Powered Down
- Low and Flat ON-State Resistance (r_{on})
 Characteristics Over Operating Range (r_{on} = 4 Ω Typ)
- Rail-to-Rail Switching on Data I/O Ports
 - 0- to 5-V Switching With 3.3-V V_{CC}
 - 0- to 3.3-V Switching With 2.5-V V_{CC}
- Bidirectional Data Flow With Near-Zero Propagation Delay
- Low Input/Output Capacitance Minimizes Loading and Signal Distortion (C_{io(OFF)} = 3.5 pF Typ)
- Fast Switching Frequency (f = 20 MHz Max)
- (1) For additional information regarding the performance characteristics of the CB3Q family, refer to the TI application report, CBT-C, CB3T, and CB3Q Signal-Switch Families, literature number SCDA008.

Data and Control Inputs Provide Undershoot Clamp Diodes

- Low Power Consumption (I_{CC} = 0.25 mA Typ)
- V_{CC} Operating Range From 2.3 V to 3.6 V
- Data I/Os Support 0- to 5-V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)
- Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
- Supports Both Digital and Analog Applications: USB Interface, Differential Signal Interface, Bus Isolation, Low-Distortion Signal Gating



DCU PACKAGE



ORDERING INFORMATION

T _A	PAC	KAGE ⁽¹⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING		
	TSSOP – PW	Tube	SN74CB3Q3306APW	- BU306A		
40°C to 05°C	1330P – PW	Tape and reel	SN74CB3Q3306APWR			
–40°C to 85°C	1100 0011	Tana and mad	SN74CB3Q3306ADCUR	- GA6R ⁽²⁾		
	US8-DCU	Tape and reel	74CB3Q3306ADCURE4			

⁽¹⁾ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

(2) The last character designates assembly/test site.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION/ORDERING INFORMATION

The SN74CB3Q3306A is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (ron). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q3306A provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

The SN74CB3Q3306A is organized as two 1-bit switches with separate output-enable $(1\overline{OE}, 2\overline{OE})$ inputs. It can be used as two 1-bit bus switches or as one 2-bit bus switch. When \overline{OE} is low, the associated 1-bit bus switch is ON and the A port is connected to the B port, allowing bidirectional data flow between ports. When \overline{OE} is high, the associated 1-bit bus switch is OFF, and a high-impedance state exists between the A and B ports.

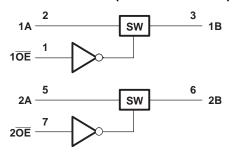
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Table 1. FUNCTION TABLE (EACH BUS SWITCH)

INPUT OE	INPUT/OUTPUT A	FUNCTION
L	В	A port = B port
Н	Z	Disconnect

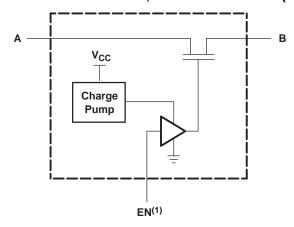
LOGIC DIAGRAM (POSITIVE LOGIC)



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SIMPLIFIED SCHEMATIC, EACH FET SWITCH (SW)



(1) EN is the internal enable signal applied to the switch.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	4.6	V
V_{IN}	Control input voltage range ^{(2) (3)}				V
V _{I/O}	Switch I/O voltage range ^{(2) (3) (4)}				V
I _{IK}	Control input clamp current	V _{IN} < 0		-50	mA
I _{I/OK}	I/O port clamp current	V _{I/O} < 0		-50	mA
I _{I/O}	ON-state switch current ⁽⁵⁾			±64	mA
	Continuous current through each V _{CC} or GND			±100	mA
0	Declare the real impact (6)	DCU		TBD	9 0 // //
θ_{JA}	Package thermal impedance ⁽⁶⁾	PW		88	°C/W
T _{stg}	Storage temperature range		-65	150	°C

- Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- All voltages are with respect to ground, unless otherwise specified.
- The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- V_I and V_O are used to denote specific conditions for $V_{I/O}$.
- $I_{\rm l}$ and $I_{\rm O}$ are used to denote specific conditions for $I_{\rm l/O}$. The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V _{IH} High-level contr voltage	High-level control input	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7	5.5	V
	voltage	V _{CC} = 2.7 V to 3.6 V	2	5.5	v
V	V _{IL} Low-level control input voltage	V _{CC} = 2.3 V to 2.7 V	0	0.7	V
VIL		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	0	8.0	v
V _{I/O}	Data input/output voltage		0	5.5	V
T _A	Operating free-air temperatu	re	-40	85	°C

All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



ELECTRICAL CHARACTERISTICS(1)

over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER		TEST CONDITIO	NS	MIN TYP ⁽²⁾	MAX	UNIT
V _{IK}		$V_{CC} = 3.6 \text{ V},$	I _I = -18 mA			-1.8	V
I _{IN}	Control inputs	$V_{CC} = 3.6 \text{ V},$	$V_{IN} = 0 \text{ to } 5.5 \text{ V}$			±1	μΑ
I _{OZ} (3)		V _{CC} = 3.6 V,	$V_O = 0 \text{ to } 5.5 \text{ V},$ $V_I = 0,$	Switch OFF, V _{IN} = V _{CC} or GND		±1	μΑ
I _{off}		$V_{CC} = 0$,	$V_O = 0 \text{ to } 5.5 \text{ V},$	V _I = 0		1	μΑ
I _{CC}		V _{CC} = 3.6 V,	$I_{I/O} = 0$, Switch ON or OFF,	$V_{IN} = V_{CC}$ or GND	0.25	0.7	mA
$\Delta I_{CC}^{(4)}$	Control inputs	$V_{CC} = 3.6 \text{ V},$	One input at 3 V,	Other inputs at V _{CC} or GND		25	μА
I _{CCD} (5)	Per control input	V _{CC} = 3.6 V, Control input switching	A and B ports open,		0.03	0.1	mA/ MHz
C _{in}	Control inputs	$V_{CC} = 3.3 \text{ V},$	$V_{IN} = 5.5 \text{ V}, 3.3 \text{ V}, \text{ or}$	0	2.5	3.5	pF
C _{io(OFF)}		V _{CC} = 3.3 V,	Switch OFF, V _{IN} = V _{CC} or GND,	V _{I/O} = 5.5 V, 3.3 V, or 0	3.5	5	pF
C _{io(ON)}		V _{CC} = 3.3 V,	Switch ON, V _{IN} = V _{CC} or GND,	V _{I/O} = 5.5 V, 3.3 V, or 0	8	10.5	pF
r _{on} ⁽⁶⁾		V _{CC} = 2.3 V,	$V_{I} = 0,$	$I_O = 30 \text{ mA}$	4	8	
		TYP at $V_{CC} = 2.5 \text{ V}$	$V_{I} = 1.7 V,$	$I_O = -15 \text{ mA}$		9	Ω
		V 2.V	$V_I = 0$,	I _O = 30 mA	4	6	Ω
		$V_{CC} = 3 V$	V _I = 2.4 V,	$V_1 = 2.4 \text{ V}, \qquad I_0 = -15 \text{ mA}$		8	

- V_{IN} and I_{IN} refer to control inputs. $V_I,\,V_O,\,I_I,$ and I_O refer to data pins. All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C. For I/O ports, the parameter I_{OZ} includes the input leakage current.
- This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
- This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 2).
- Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 2 ± 0.2	2.5 V V	V _{CC} = 3.3 V ± 0.3 V		UNIT
	(INFOI)	(001F01)	MIN	MAX	MIN	MAX	i
f OE (1)	ŌĒ	A or B		10		20	MHz
t _{pd} ⁽²⁾	A or B	B or A		0.2		0.2	ns
t _{en}	ŌĒ	A or B	1.5	6.5	1.5	5.5	ns
t _{dis}	ŌĒ	A or B	1	6	1	5	ns

- Maximum switching frequency for control input ($V_O > V_{CC}$, $V_I = 5$ V, $R_L \ge 1$ M Ω , $C_L = 0$)
- The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

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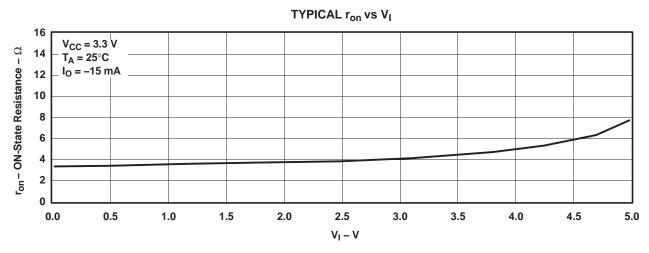


Figure 1. Typical ron vs VI

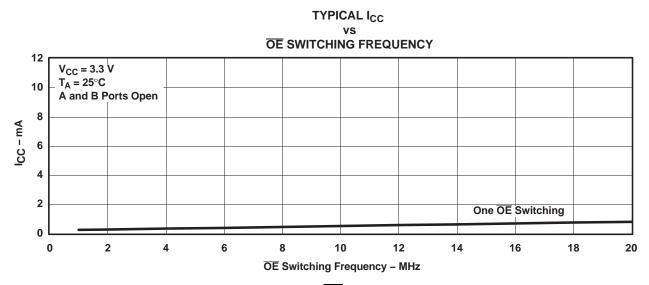
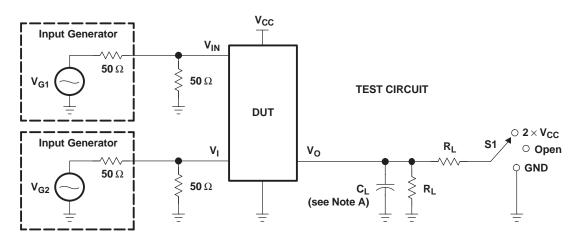


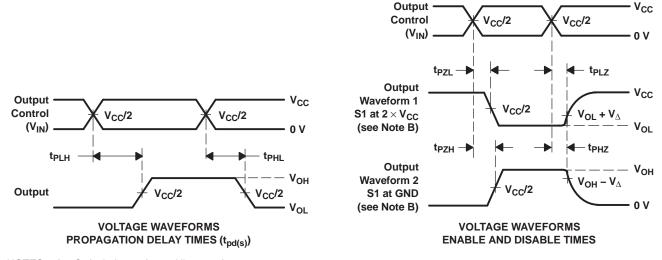
Figure 2. Typical I_{CC} vs \overline{OE} Switching Frequency



PARAMETER MEASUREMENT INFORMATION



TEST	V _{CC}	S1	R _L	VI	CL	$oldsymbol{V}_\Delta$
t _{pd(s)}	$\begin{array}{c} t_{\text{pd(s)}} \\ \end{array} \begin{array}{c} \text{2.5 V} \pm \text{0.2 V} \\ \text{3.3 V} \pm \text{0.3 V} \end{array}$		500 Ω 500 Ω	V _{CC} or GND V _{CC} or GND	30 pF 50 pF	
t _{PLZ} /t _{PZL}	$\begin{array}{c} \textbf{2.5 V} \pm \textbf{0.2 V} \\ \textbf{3.3 V} \pm \textbf{0.3 V} \end{array}$	$\begin{array}{c} 2 \times \mathbf{V_{CC}} \\ 2 \times \mathbf{V_{CC}} \end{array}$	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t _{PHZ} /t _{PZH}	$\begin{array}{c} \textbf{2.5 V} \pm \textbf{0.2 V} \\ \textbf{3.3 V} \pm \textbf{0.3 V} \end{array}$	GND GND	500 Ω 500 Ω	V _{CC}	30 pF 50 pF	0.15 V 0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd(s)}. The t_{pd} propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms





REVISION HISTORY

Changes from Revision D (April 2005) to Revision E					
•	Added DCU package ordering information.	········ ·			





7-Nov-2014

PACKAGING INFORMATION

Orderable Device	Status	Package Type	_		Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
74CB3Q3306ADCURE4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	GA6R	Samples
74CB3Q3306ADCURG4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	GA6R	Samples
74CB3Q3306APWRE4	ACTIVE	TSSOP	PW	8		TBD	Call TI	Call TI	-40 to 85		Samples
SN74CB3Q3306ADCUR	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 85	(A6 ~ GA6Q ~ GA6R) GZ	Samples
SN74CB3Q3306APW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU306A	Samples
SN74CB3Q3306APWG4	ACTIVE	TSSOP	PW	8		TBD	Call TI	Call TI	-40 to 85		Samples
SN74CB3Q3306APWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 85	BU306A	Samples
SN74CB3Q3306APWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU306A	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.



PACKAGE OPTION ADDENDUM

7-Nov-2014

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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OTHER QUALIFIED VERSIONS OF SN74CB3Q3306A:

Enhanced Product: SN74CB3Q3306A-EP

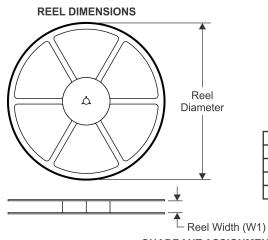
NOTE: Qualified Version Definitions:

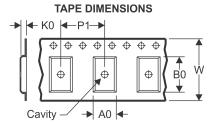
• Enhanced Product - Supports Defense, Aerospace and Medical Applications

PACKAGE MATERIALS INFORMATION

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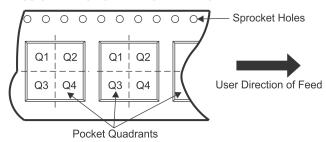
TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

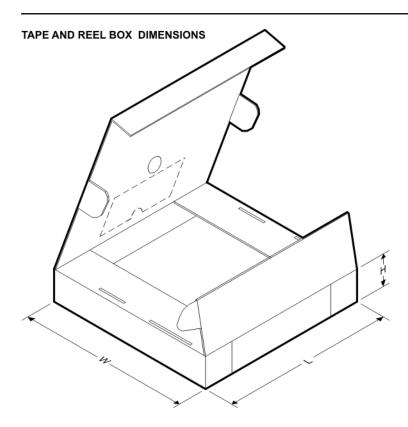
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74CB3Q3306ADCURG4	US8	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74CB3Q3306ADCUR	US8	DCU	8	3000	178.0	9.5	2.25	3.35	1.05	4.0	8.0	Q3
SN74CB3Q3306ADCUR	US8	DCU	8	3000	180.0	9.0	2.05	3.3	1.0	4.0	8.0	Q3
SN74CB3Q3306APWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

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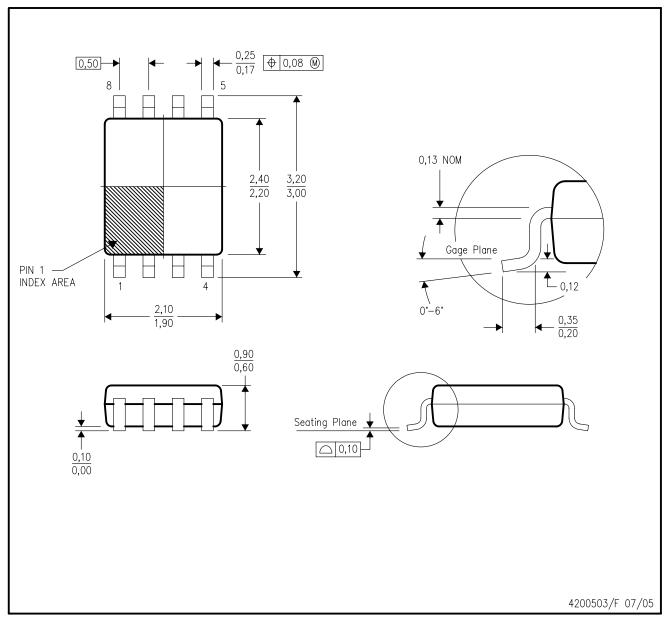


*All dimensions are nominal

Device Package Type		Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74CB3Q3306ADCURG4	US8	DCU	8	3000	202.0	201.0	28.0
SN74CB3Q3306ADCUR	US8	DCU	8	3000	202.0	201.0	28.0
SN74CB3Q3306ADCUR	US8	DCU	8	3000	182.0	182.0	20.0
SN74CB3Q3306APWR	TSSOP	PW	8	2000	364.0	364.0	27.0

DCU (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



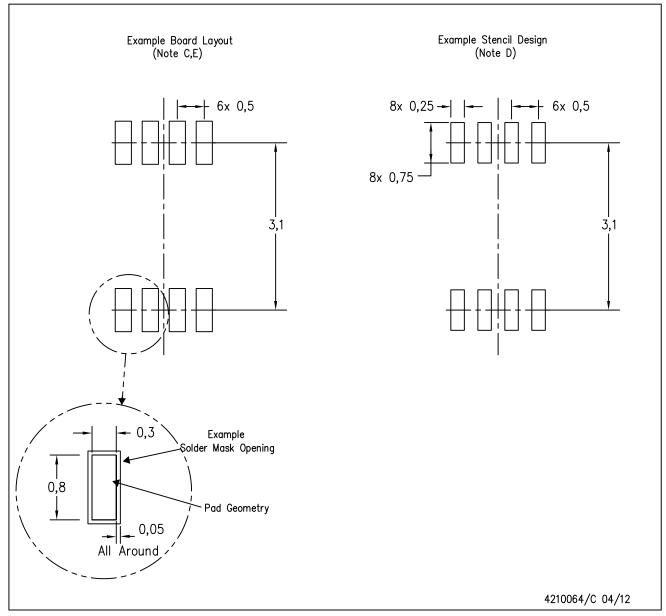
NOTES:

- : A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-187 variation CA.



DCU (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



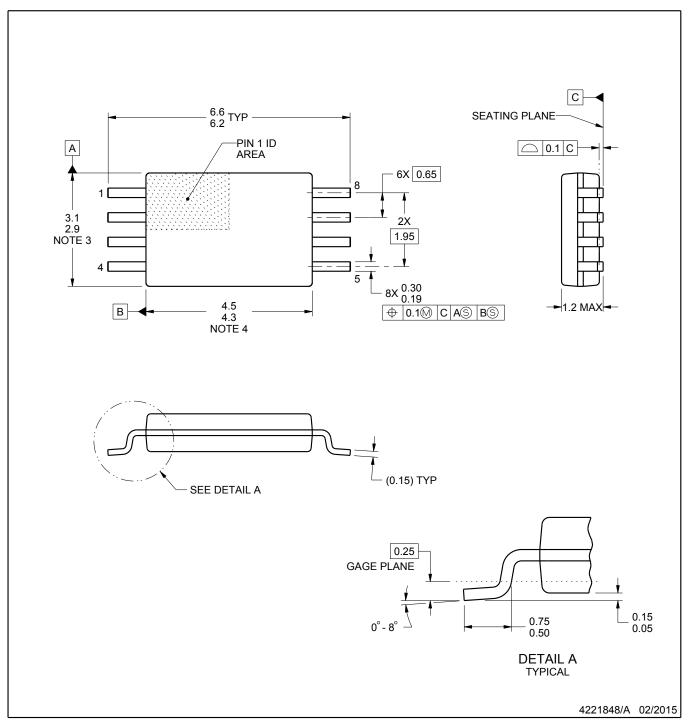
NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.





SMALL OUTLINE PACKAGE



NOTES:

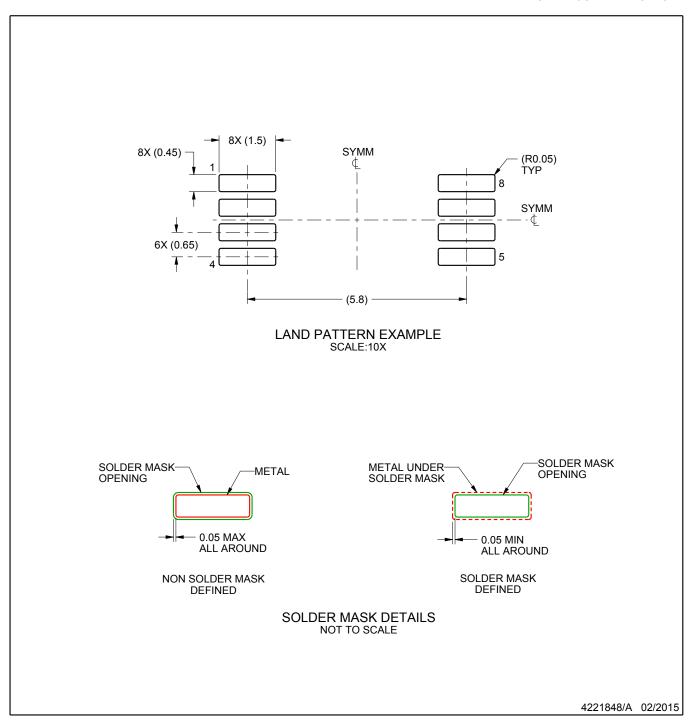
- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153, variation AA.



SMALL OUTLINE PACKAGE



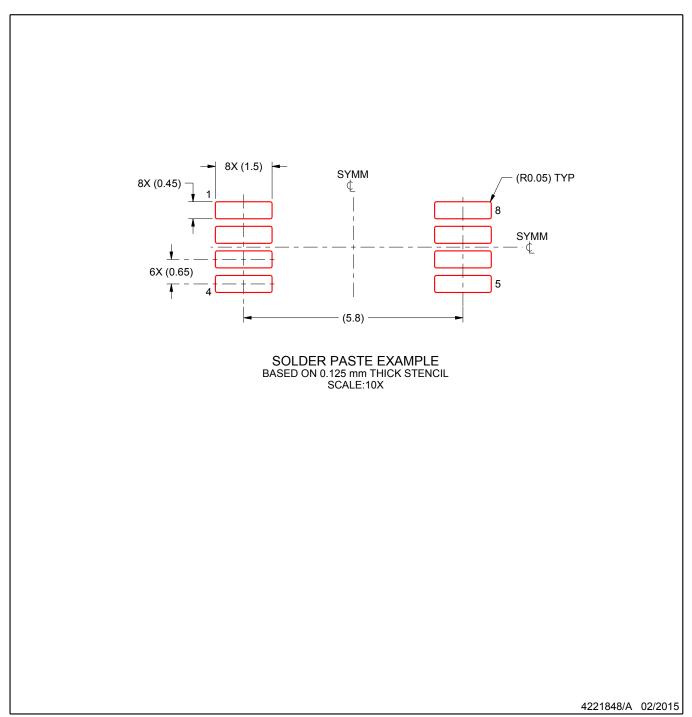
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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