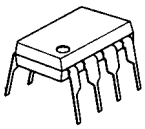
V-F / F-V CONVERTOR

■ GENERAL DESCRIPTION

The **NJM4151** provide a simple low-cost method of A/D conversion. They have all the inherent advantages of the voltage-to-frequency conversion technique. The Output of **NJM4151** is a series of pulses of constant duration. The frequency of the pulses is proportional to the applied input voltage. These converters are designed for use in a wide range of data conversion and remote sensing applications.

■ PACKAGE OUTLINE



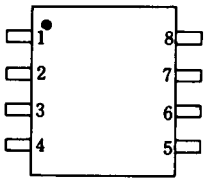
NJM4151D

NJM4151M

■ FEATURES

- Operating Voltage (8V to 22V)
- Frequency Operation from (1.0Hz to 100kHz)
- Package Outline DIP8, DMP8
- Bipolar Technology

■ PIN CONFIGURATION

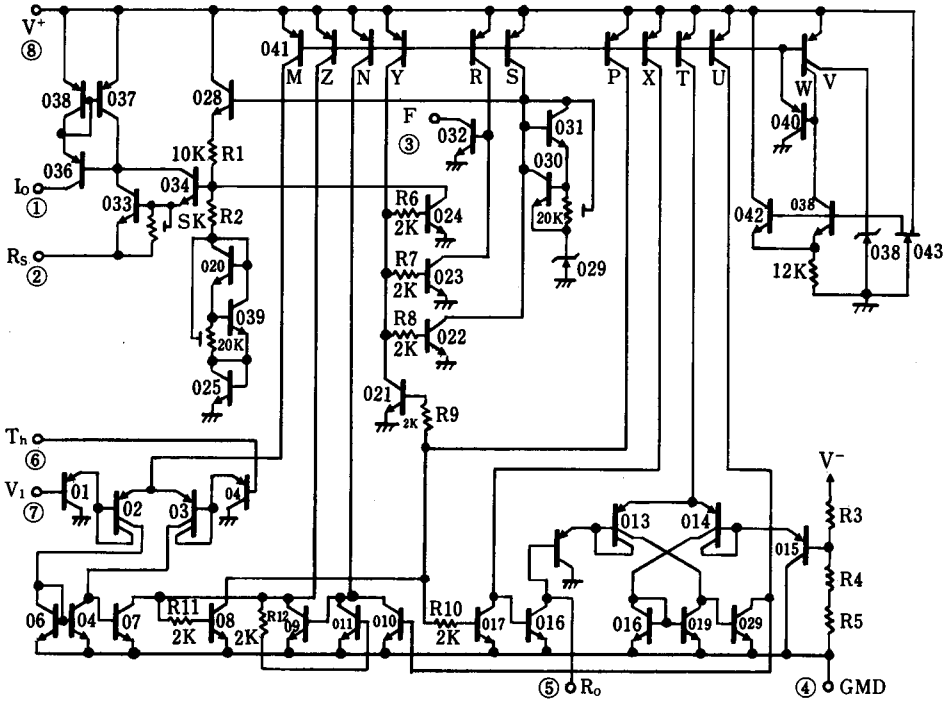


NJM4151D
NJM4151M

PIN FUNCTION

1	Current Source
2	Scale Factor
3	Logic Output
4	Ground
5	One-Shot R, C
6	Threshold
7	Input Voltage
8	V^+

■ EQUIVALENT CIRCUIT



■ ABSOLUTE MAXIMUM RATINGS (T_a = 25ºC)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	22	V
Output Sink Current	I_{SINK}	20	mA
Power Dissipation	P_D	(DIP8) 500 (DMP8) 300	mW mW
Input Voltage	V_I	-0.2 to V^+	(V)
Operating Temperature Range	T_{opr}	-40 to + 85	ºC
Storage Temperature Range	T_{stg}	-40 to +125	ºC

■ ELECTRICAL CHARACTERISTICS (V^+ = +15V, Ta = 25ºC)

PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	8V < V^+ < 15V	2.0	3.5	6.0	mA
	15V < V^+ < 22V	2.0	4.5	7.5	mA
Conversion Accuracy Scale Factor	V_{IN} = 10V R_S = 14.0kΩ	0.90	1.00	1.10	kHz/V
Drift with Temperature	V_{IN} = 10V	-	±100	-	ppM/ºC
Drift with V^+	V_{IN} = 1.0V 8V < V^+ <18V	-	0.2	1.0	%/V
Input Comparator Offset Voltage		-	5	10	mV
Offset Current		-	±50	±100	nA
Input Bias Current		-	-100	-300	nA
Common Mode Range (Note 1)		0 to V^+-3	0 to V^+-2	-	V
One-Shot Threshold Voltage, Pin 5		0.63	0.66	0.70	xV^+
Input Bias Current, Pin5		-	-100	-500	nA
Reset V_{SAT}	Pin 5, I = 2.2mA	-	0.15	0.50	V
Current Source Output Current (Rs = 14.0kΩ)	Pin 1, V^+ = 0V	-	138.7	-	µA
Change with Voltage	Pin 1, V^+ = 0V to V^+ = 10V	-	1.0	2.5	µA
Off Leakage	Pin 1, V^+ = 0V	-	1	50.0	nA
Reference Voltage	Pin 2	1.70	1.90	2.08	V
Logic Output V_{SAT}	Pin 3, I = 3.0mA	-	0.15	0.50	V
V_{SAT}	Pin 3, I = 2.0mA	-	0.10	0.30	V
Off Leakage		-	0.1	1.0	µA

Note 1 : Input Common Mode Range includes ground.

■ PRINCIPLE OF OPERATION

Single Supply Mode Voltage-to-Frequency Conversion

In this application the **NJM4151** functions as a stand-alone voltage to frequency converter operating on a single positive power supply. Refer to Figure 1, the simplified block diagram. The **NJM4151** contains a voltage comparator, a one-shot, and a precision switched current source. The voltage comparator compares a positive input voltage applied at pin 7 to the voltage at pin 6. If the input voltage is higher, the comparator will fire the one-shot. The output of the one-shot is connected to both the logic output and the precision switched current source. During the one-shot period, T, the logic output will go low and the current source will turn on with current I.

At the end of the one-shot period the logic output will go high and the current source will shut off. At this time the current source has injected an amount of charge $Q = I_0T$ into the network R_B-C_B. If this charge has not increased the voltage V_B such that $V_B > V_I$, the comparator again fires the one-shot and the current source injects another lump of charge, Q, into the R_B-C_B network. This process continues until $V_B > V_I$.

When this condition is achieved the current source remains off and the voltage V_B decays until V_B is again equal to V_I. This completes one cycle. The VFC will now run in a steady state mode. The current source dumps lumps of charge into the capacitor C_B at rate fast enough to keep $V_B \geq V_I$. Since the discharge rate of capacitor C_B is proportional to V_B/R_B, the frequency at which the system runs will be proportional to the input voltage.

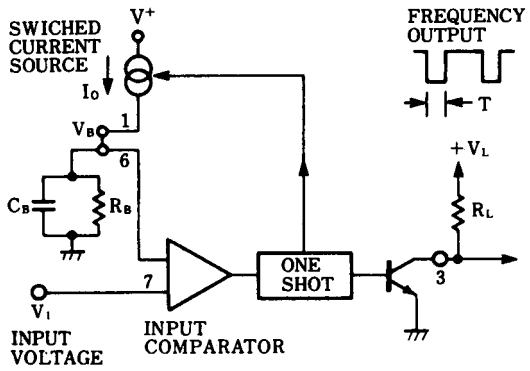


Figure 1. Simplified Block Diagram, Single Supply Mode

The NJM4151 VFC is easy to use and apply if you understand the operation of it through the block diagram, Figure 1. Many users, though, have expressed the desire to understand the workings of the internal circuitry. The circuit can be divided into five sections: the internal biasing network, input comparator, one-shot, voltage reference, and the output current source.

The internal biasing network is composed of Q39-Q43. The N-channel FET Q43 supplies the initial current for zener diode Q39. The NPN transistor Q38 senses the zener voltage to derive the current reference for the multiple collector current source Q41. This special PNP transistor provides active pull-up for all of the other sections of the NJM4151.

The input comparator section is composed of Q1-Q7. Lateral PNP transistors Q1-Q4 form the special ground-sensing input which is necessary for VFC operation at low input voltages, NPN transistors Q5 and Q6 convert the differential signal to drive the second gain stage Q7. If the voltage on input pin 7 is less than that on threshold pin 6, the comparator will be off and the collector of Q7 will be in the high state. As soon as the voltage on pin 7 exceeds the voltage on pin 6, the collector of Q7 will go low and trigger the one-shot.

The one-shot is made from a voltage comparator and an R-S latch, Transistors Q12-Q15 and Q18-Q20 form the comparator, while Q8-Q11 and Q16-Q17 make up the R-S latch. One latch output, open-collector reset transistor Q16, is connected to a comparator input and to the terminal, pin 5. Timing resistor R_O is tied externally from pin 5 to V^+ and timing capacitor C_O is tied from pin 5 to ground. The other comparator input is tied to a voltage divider R_3-R_5 which sets the comparator threshold voltage at $0.667V^+$. One-shot operation is initiated when the collector of Q7 goes low and sets the latch. This causes Q16 to turn off, releasing the voltage at pin 5 to charge exponentially towards V^+ through R_O. As soon as this voltage reaches 0.667 V^+, comparator output Q20 will go high causing Q10 to reset the latch. When the latch is reset, Q16 will discharge C_O to ground. The one-shot has now completed its function of creating a pulse of period $T=1.1 R_OC_O$ at the latch output, Q21. This pulse is buffered through Q23 to drive the open-collector logic circuit transistor Q32. During the one-shot period the logic output will be in the low state. The one-shot output is also used to switch the reference voltage by Q22 and Q24. The low T. C. reference voltage is derived from the combination of a 5.5V zener diode with resistor and diode level shift networks. A stable 1.89 volts is developed at pin 2, the emitter of Q33.

Connecting the external current-setting resistor R_S = 14.0Ω from pin 2 to ground gives 135μA from the collectors of Q33 and Q34. This current is reflected in the precision current mirror Q35-Q37 and produces the output current I_O at pin 1. When the R-S latch is reset, Q22 and Q24 will hold the reference voltage off, pin 2 will be at 0V, and the current will be off. During the one-shot period T, the latch will be set, the voltage of pin 2 will go to 1.89V, and the output current will be switched on.

■ TYPICAL APPLICATION

1. Single supply Voltage-to-Frequency Converter

Figure 2 shows the simplest type of VFC that can be made with the NJM4151. Input voltage range is from 0 to +10V, and output frequency is from 0 to 10kHz. Full scale frequency can be tuned by adjusting R_s, the output current set resistor. This circuit has the advantage of being simple and low in cost, but it suffers from inaccuracy due to a number of error sources. Linearity error is typically 1%. A frequency offset will also be introduced by the input comparator offset voltage. Also, response time for this circuit is limited by the passive integration network R_BC_B. For the component values shown in Figure 2, response time for a step change input from 0 to +10V will be 135msec. For applications which require fast response time and high accuracy, use the circuits of Figure 3 and 4.

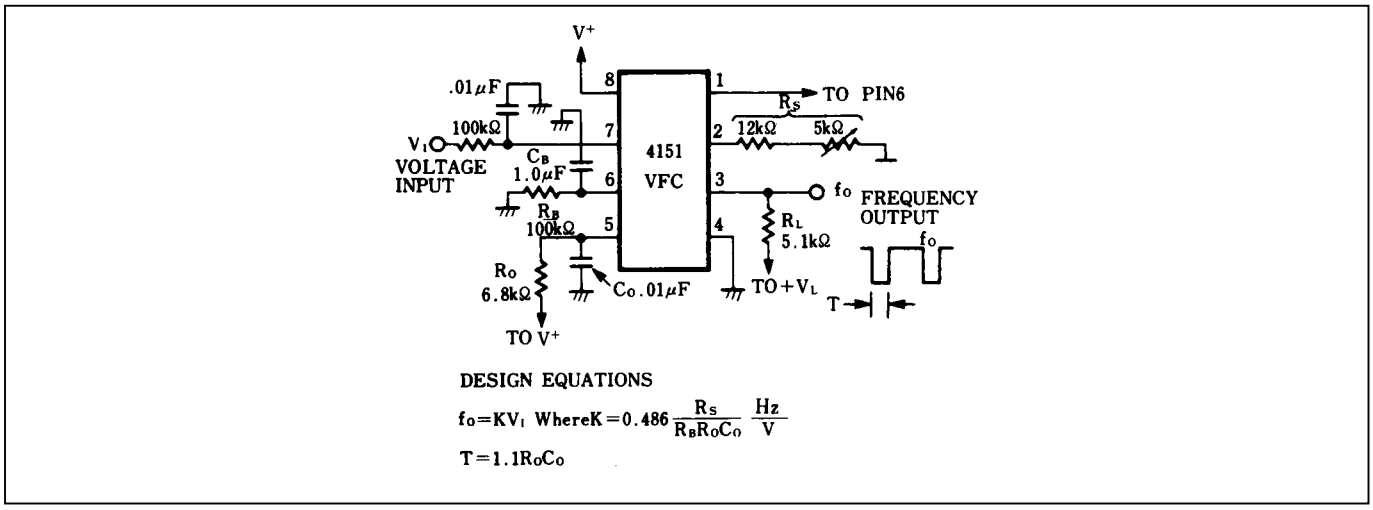


Figure 2. Single Supply Voltage-to-Frequency Converter

2. Precision VFC with Single Supply Voltage

For applications which require a VFC which will operate from a single positive supply with positive input voltage, the circuit of Figure 3 will give greatly improved linearity, frequency offset, and response time. Here, an active integrator using one section of the **NJM3403A** quad ground-sensing op-amp has replaced the R_B-C_B network in Figure 2. Linearity error for this circuit is due only to the NJM4151 current source output conductance. Frequency offset is due only to the op-amp input offset and can be nulled to zero by adjusting R_B. This technique uses the op-amp bias current to develop the null voltage, so an op-amp with stable bias current, like the **NJM3403A**, is required.

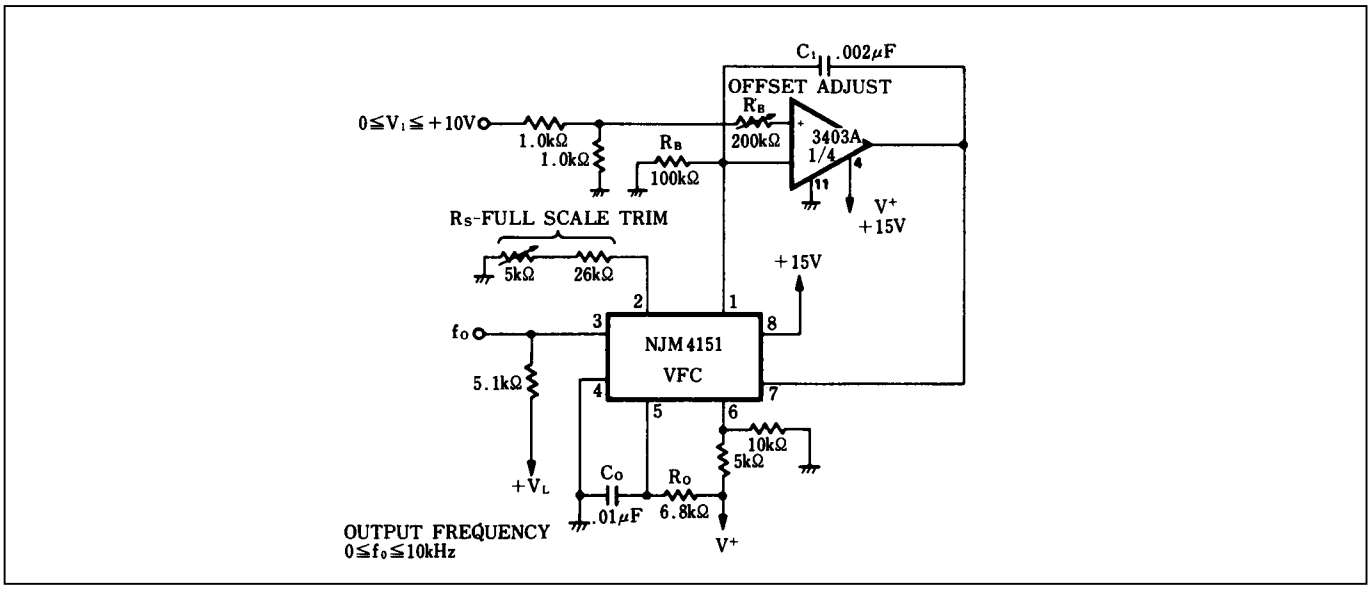


Figure 3. Precision Voltage-to-Frequency Converter Single Supply

3. Precision Voltage-to-Frequency Converter

In this application (Figure 4) the NJM4151 VFC is used with an operational amplifier integrator to provide typical linearity of 0.05% over the range of 0 to -10V. Offset is adjustable to zero. Unlike many VFC designs which lose linearity below 10mV, this circuit retains linearity over the full range of input voltage, all the way to 0V.

Trim the full scale adjust pot at V_I = -10V for an output frequency of 10kHz. The offset adjust pot should be set for 10Hz with an input voltage of -10mV.

The operational amplifier integrator improves linearity of this circuit over that of Figure 2 by holding the output of the source, Pin 1, at a constant 0V. Therefore linearity error due to the current source output conductance is eliminated. The diode connected around the op-amp prevents the voltage at NJM4151 pin 7 from going below 0. Use a low-leakage diode here, since any leakage will degrade the accuracy. This circuit can be operated from a single positive supply if an **NJM3403A** ground-sensing op-amp is used for the integrator. In this case, the diode can be left out. Note that even though the circuit itself will operate from a single supply, the input voltage is necessarily negative. For operation above 10kHz, bypass NJM4151 pin 6 with 0.01μF.

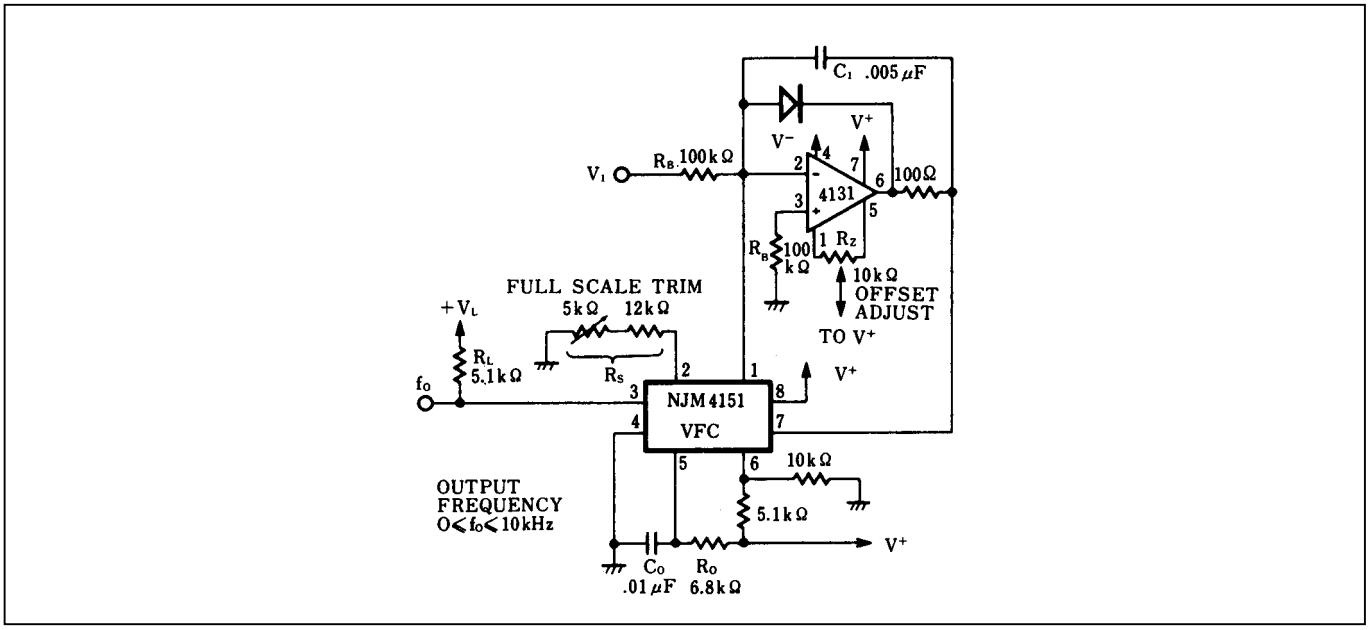


Figure 4. Precision Voltage-to-Frequency Converter

4. Comparison of Voltage-to-Frequency Application Circuits

Table 1 compares the VFC applications circuits for typical linearity, frequency offset, response time for a step input from 0 to 10 volts, sign of input voltage, and whether the circuit will operate from a single positive supply or split supplies.

Table 1

	Figure 2	Figure 3	Figure 4
Linearity	1%	0.2%	0.05%
Frequency Offset	+10Hz	0	0
Response Time	135msec	10msec	10msec
Input Voltage	+	+	-
Single supply	yes	yes	yes
Split Supply	-	-	yes

5. Frequency-to-Voltage Conversion

The NJM4151 can be used as a frequency-to-voltage converter. Figure 5 shows the single-supply FVC configuration. With no signal applied, the resistor bias networks tied to pins 6 and 7 hold the input comparator in the off state. A negative going pulse applied to pin 6 (or positive pulse to pin 7) will cause the comparator to fire the one-shot. For proper operation, pulse width must be less than the period of the one-shot, T=1.1 R_OC_O. For a $5V_{p-p}$ square-wave input the differentiator network formed by the input coupling capacitor and the resistor bias network will provide pulses which correctly trigger the one-shot. An external voltage comparator such as the **NJM311** of **NJM2901** can be used to "square-up" sinusoidal input signals before they are applied to the NJM4151. Also, the component values for the input signal differentiator and bias network can be altered to accommodate square waves with different amplitudes and frequencies. The passive integrator network R_BC_B filters the current pulses from the pin 1 output. For less output ripple, increase the value of C_B.

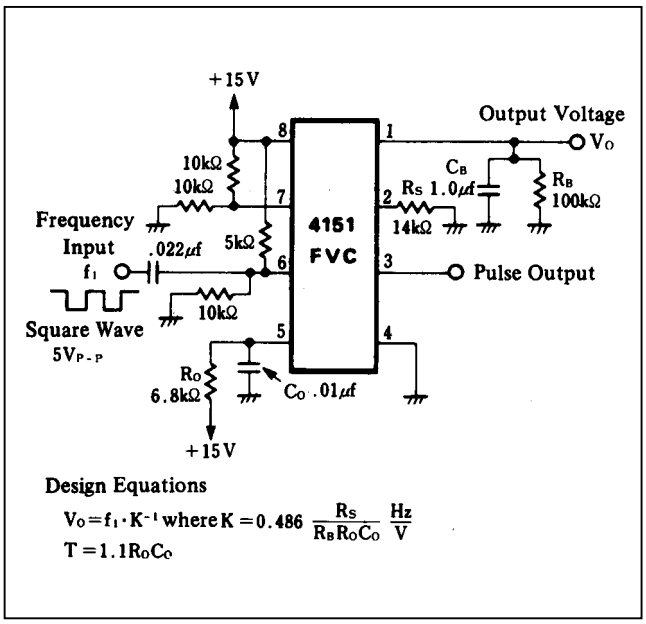


Figure 5. Single Supply Frequency-to-Voltage Converter

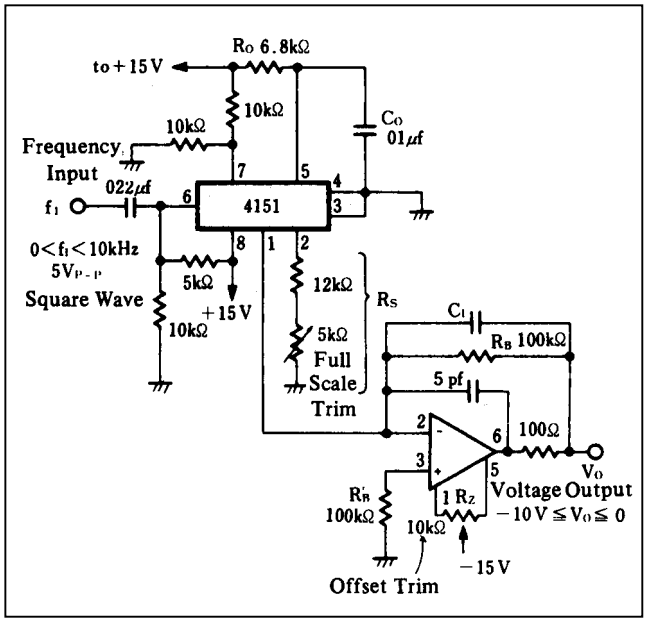


Figure 6. Precision Frequency-to-Voltage Converter

6. Precision Frequency-to-Voltage Converter

For increased accuracy and linearity, use an operational amplifier integrator as shown in Figure 6, the precision FVC configuration. Trim the offset to give -10mV out with 10Hz in and trim the full scale adjust for -10V out with 10kHz in. Input signal conditioning for this circuit is necessary just as for the single supply mode, and scale factor can be programmed by the choice of component values. A tradeoff exists between output ripple and response time, through the choice of integration capacitor C_1. If C_1 = -0.1µF the ripple will be about 100mV. Response time constant $t_R=R_B \bullet C_1$. For R_B = 100kΩ and C_1 = 0.1µF, t_R = 10ms.

■ PRECAUTIONS

1. The voltage applied to comparator input pins 6 and 7 should not be allowed to go below ground by more than 0.3 volt.
2. Pins 3 and 5 are open-collector outputs. Shorts between these pins and V^+ can cause overheating and eventual destruction.
3. Reference voltage terminal pin 2 is connected to the emitter of an NPN transistor and is held at approximately 1.9 volts. This terminal should be protected from accidental shorts to ground or supply voltages. Permanent damage may occur if current in pin 2 exceeds 5mA.
4. Avoid stray coupling between NJM4151 pins 5 and 7, which could cause false triggering. For the circuit of Figure 2, bypass pin 7 to ground with at least 0.01µF. If false triggering is experienced with the precision mode circuits, bypass pin 6 to ground with at least 0.01µF. This is necessary for operation above 10kHz.

PROGRAMMING THE NJM4151

The NJM4151 can be programmed to operate with a full scale frequency anywhere from 1.0Hz to 100kHz. In the case of the VFC configuration, nearly any full scale input voltage from 1.0V and up can be tolerated if proper scaling is employed. Here is how to determine component values for any desired full scale frequency.

1. Set Rs = 14kΩ or use a 12kΩ resistor and 5kΩ pot as shown in the figures. (The only exception to this is Figure 4.)
2. Set $T=1.1R_0C_0 = 0.75\ [1 / f_0]$ where f_0 is the desired full scale frequency. For optimum performance make 6.8kΩ < R_0 < 680kΩ and 0.001µF < C_0 < 1.0µF
3. a) For the circuit of Figure 2 make $C_B = 10^{-2}\ [1 / f_0]$ Farads.
   Smaller values of C_B will give faster response time, but will also increase frequency offset and nonlinearity.
   b) For the active integrator circuits make $C_1 = 5 \times 10^{-5}\ [1 / f_0]$ Farads. The op-amp integrator must have a slew rate of at least $135 \times 10^{-6}\ [1/C_1]$ volts per second where the value of C_1 is again give in Frads.
4. a) For the circuits of Figure 2 and 3 keep the values of R_B and R_B' as shown and use an input attenuator to give the desired full scale input voltage.
   b) For the precision mode circuit of Figure 4, set $R_B = V_{10}/100\mu A$ where V_{10} is the full scale input voltage. Alternately the op-amp inverting input (summing node) can be used as a current input with full scale input current I_{10} = -100µA.
5. For the FVC_S, pick the value of C_B or C_1 to give the optimum tradeoff between response time and output ripple for the particular application.

■ DESIGN EXAMPLE

I. Design a precision VFC (from Figure 4) with f_0 = 100kHz and V_{10} = -10V.
   1. Set R_S = 14.0kΩ.
   2. $T = 0.75\ (1/10^5)$=7.5µsec Let R_0 = 6.8kΩ and C_0 = 0.001µF
   3. $C_1 = 5 \times 1^{-5}\ (1/10^5)$ = 500pF Op-amp slew rate must be at lease $SR=135 \times 10^{-6}\ (1/500pF)$=0.27V/µsec
   4. R_B = 10V/100µA = 100kΩ

II. Design a precision VFC with f_0=1Hz and V_{10} = -10V.
   1. Let R_S = 14.0kΩ
   2. T = 0.75(1/1) = 0.75sec Let R_0 = 680kΩ and C_0 = 1.0µF
   3. $C_1 = 5 \times 10^{-5}\ (1/1)$ F = 50µF
   4. R_B = 100kΩ

III. Design a single supply FVC to operate with a supply voltage of 8V and full scale input frequency f_0 = 83.3Hz. The output voltage must reach at least 0.63 of its final value in 200msec. Determine the output ripple.

1. Set R_S = 14.0kΩ
2. T = 0.75 (1/83.3) = 9msec Let R_0 = 82kΩ and C_0 = 0.1μF
3. Since this FVC must operate from 8.0V, we shall make the full scale output voltage at pin 6 equal to 5.0V.
4. R_B = 5V/100μA = 50kΩ
5. Output response time constant is t_R < 20msec Therefore $C_B < t_R / R_B = 200 \times 10^{-3} / 50 \times 10^3 = 4\mu F$ Worst case ripple voltage is: V_R = 9mSx135μA / 4μF = 304mV

IV. Design an opto-isolated V_{FC} with high linearity which accepts a full scale input voltage of +10V. See Figure 7 for the final design. This circuit uses the precision mode VFC configuration for maximum linearity. The **NJM3403A** quad op-amp provides the functions of inverter, integrator, regulator, and LED driver.

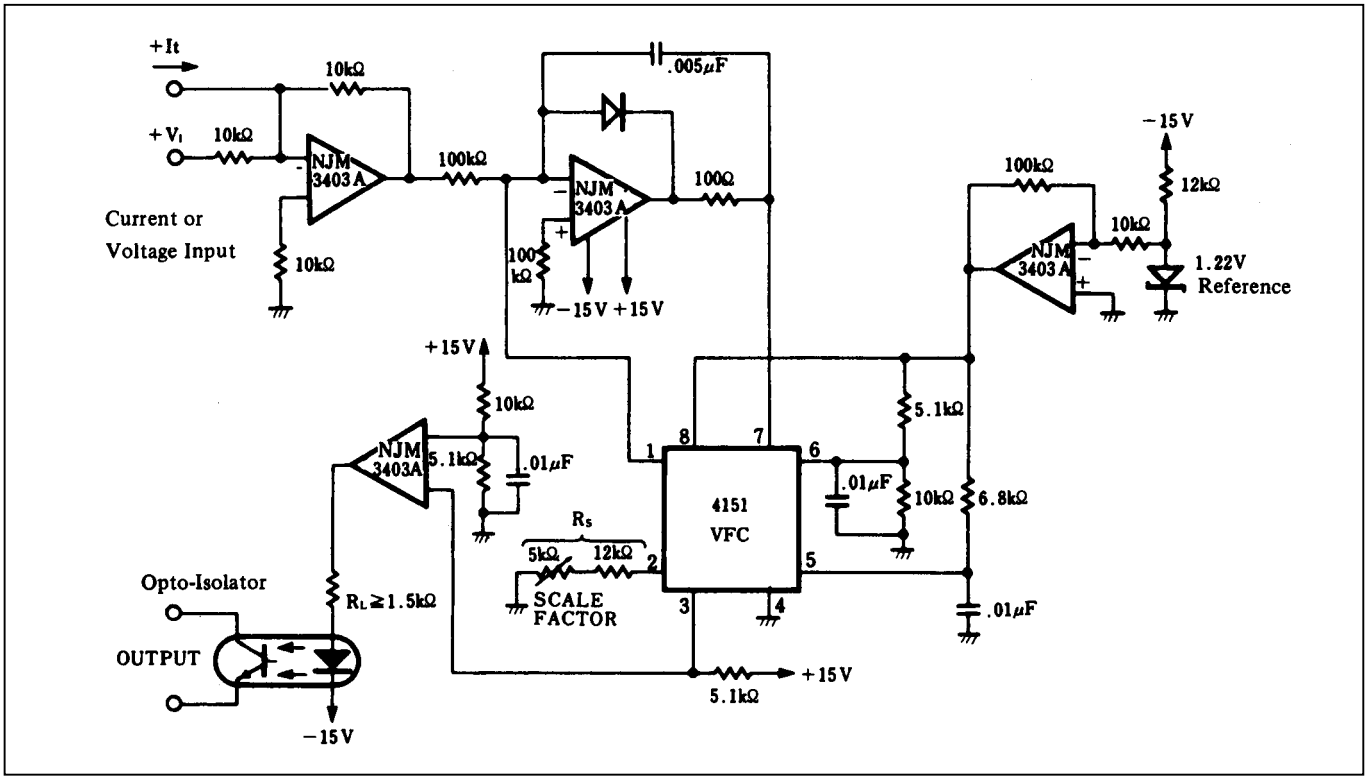


Figure 7. Opto-Isolated VFC

■ APPLICATION EXAMPLE

1. FSK Demodulator

FSK(Frequency Shift Keying) data demodulator shows as an example. This is one of continuous input of two frequencies. Transmission of this signal is often used a telephone line. Therefore, the fluctuation amplitude, noise may occur. Therefore, it may experience noise and amplitude fluctuations. FSK demodulator must sense the frequency of which was entered. And it is “0” “1” must be shown at the level of logic. Figure 8 is a circuit diagram FSK. It uses the 2-channel operational amplifier and NJM4151. The FSK signal through a filter to remove noise and high frequency. NJM4151 is the frequency-voltage converter configuration. DC output voltage through a low-frequency filter is converted to a logic output levels. Output op amp will work with hysteresis. The value of parts such as resistors, please determine the following as an example.

Two input frequencies, the magnitude of the noise, the response time.

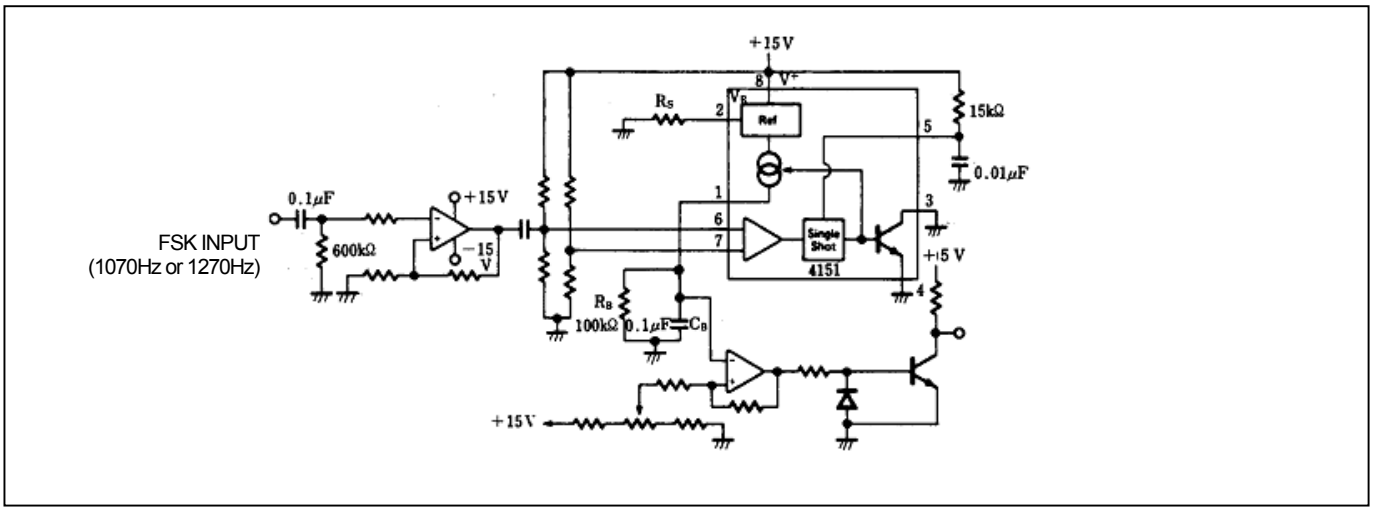


Figure 8. FSK demodulator

2. Motor Control

Changes in the axis of rotation is changed to pulse train by Trans Deuce. Pulse frequency is proportional to the rotation speed. Pulse train can be changed to a DC voltage proportional to the frequency by the NJM4151.

Please refer to Figure 9.

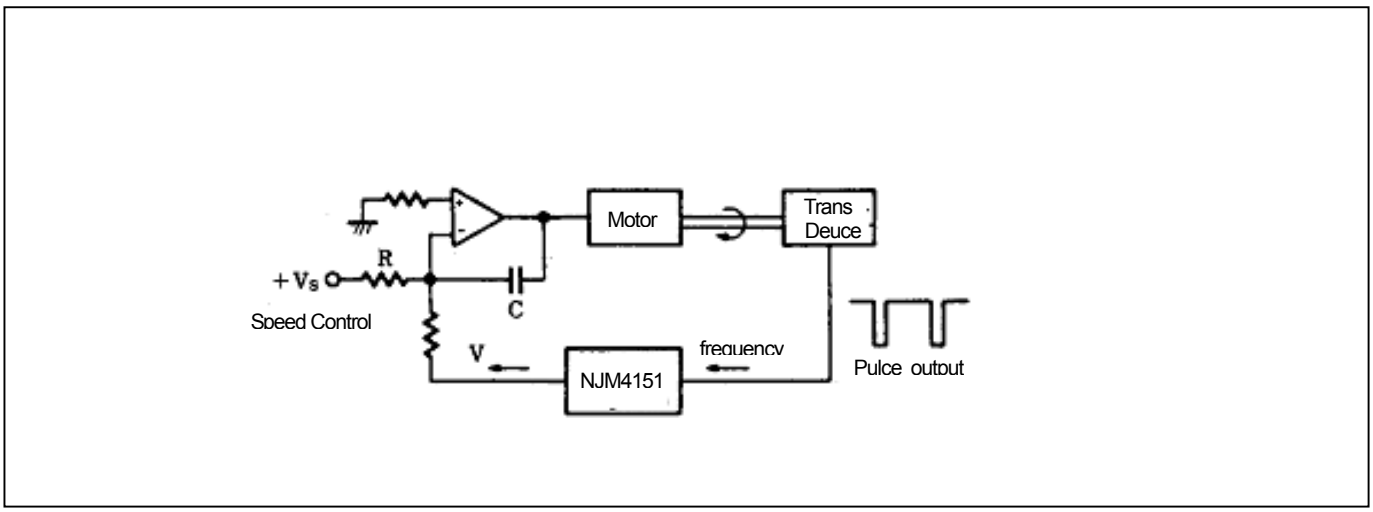


Figure 9. Motor Control

3. A/D Converter

One example is to connect the microprocessor to analog converter output. A / D converer is required are as follows. Good noise rejection, high stability, low cost. Many industrial systems are sufficient for an 8-bit·1/256. A typical microprocessor works with 8-bit input. Data from the AD converter should be parallel with TTL logic levels. Digital data should be controlled by logic input. Typically, the input is called STATUS. Request conversion rate depends on applied field. Digital voltmeter is converted into digital signals per second to 2.3 times. AD converter for the radar pulse must be converted within 100 nanoseconds. AD converter can be configured with a parallel 8-bit output by using the NJM4151.
If the slow conversion of the AD converter by using the NJM4151, noise removal is good, better linearity and better isolation can be configured at low cost. Also, you can easily increase the degree of decomposition. If you use the NJM4151, the conversion time is 1s to 10ms. Please refer to Figure 10. Single-digit or further of NJM4151 will be coupled to the counter through a photo coupler.

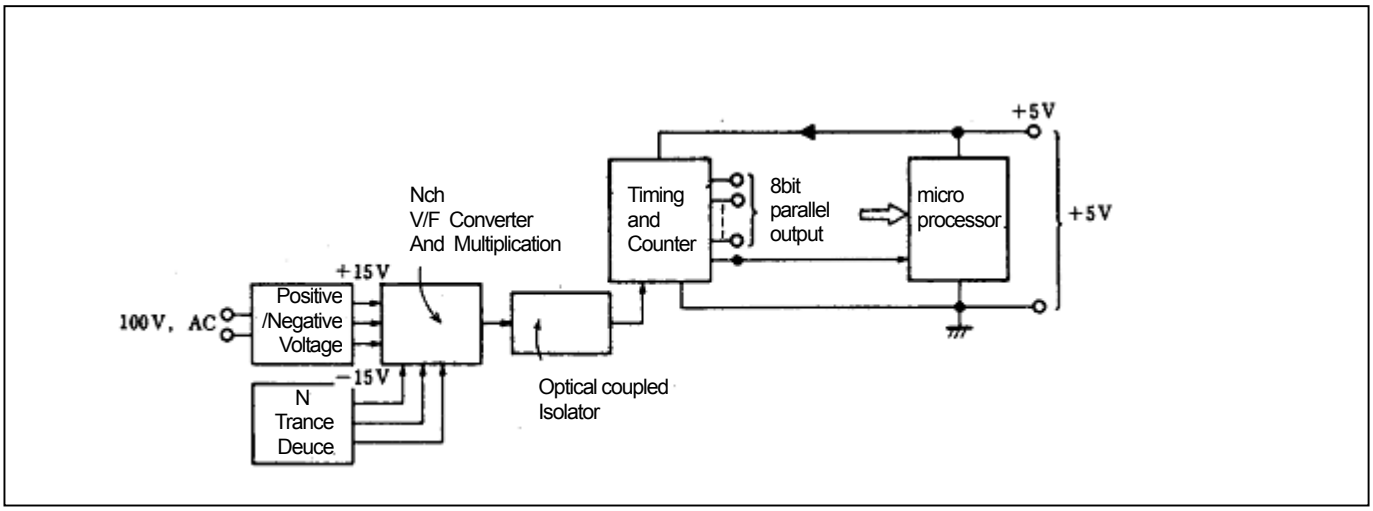


Figure 10. Connect to Micro Processor

In many applications, the counter circuit / timing make time division for each channel. Photo coupler is not absolutely necessary. Help to separated the counter / timing circuit and VF-encoder. Thus, VF encoder does not matter even if the contact point away. Therefore, can be used in distance away from the microprocessor.

Encoder output pulse train must be parallel to the digital signal. The 8-bit counter is set to 0. Then, only a fixed time to count the pulses from the encoder. Condition that the gate is ON, the counter is only for the specified duration. The higher the input voltage to the encoder, the encoder output frequency is higher. The digital readout of the counters at the end of a certain duration will be directly proportional to the input frequency. To make the best operating, the duration and the encoder scale factor recommend choose to become the maximum count of 255(as an 8-bit binary) at maximum input voltage.

Figure 11 is a data conversion system of N channels. A number of transducers is coded each by VFC. N-channel multiplexer is coupling to 8-bit counter. At that time, any one of the encoder output go through with photo-coupler. Channel selection method is as follows. Microprocessor, or manually enter the address of the digital. Timing will be performed by a number of different things. The most accurate way is as follows. It is to be used as a low-frequency by dividing high frequency with the accurate high frequency crystal oscillator. A similar method, it attached divider circuit to a tuning fork oscillator . The most inexpensive way to make the timing is as follows. It is way to drive a one-shot use the optocouplers from the line voltage for AC. Maximum error is less than 0.5% so AC voltage is about 0.2% in most areas.Please note that this method is affected because of the AC line transient response. In addition, NJM555 (Timer IC) can also be used in the astable mode.

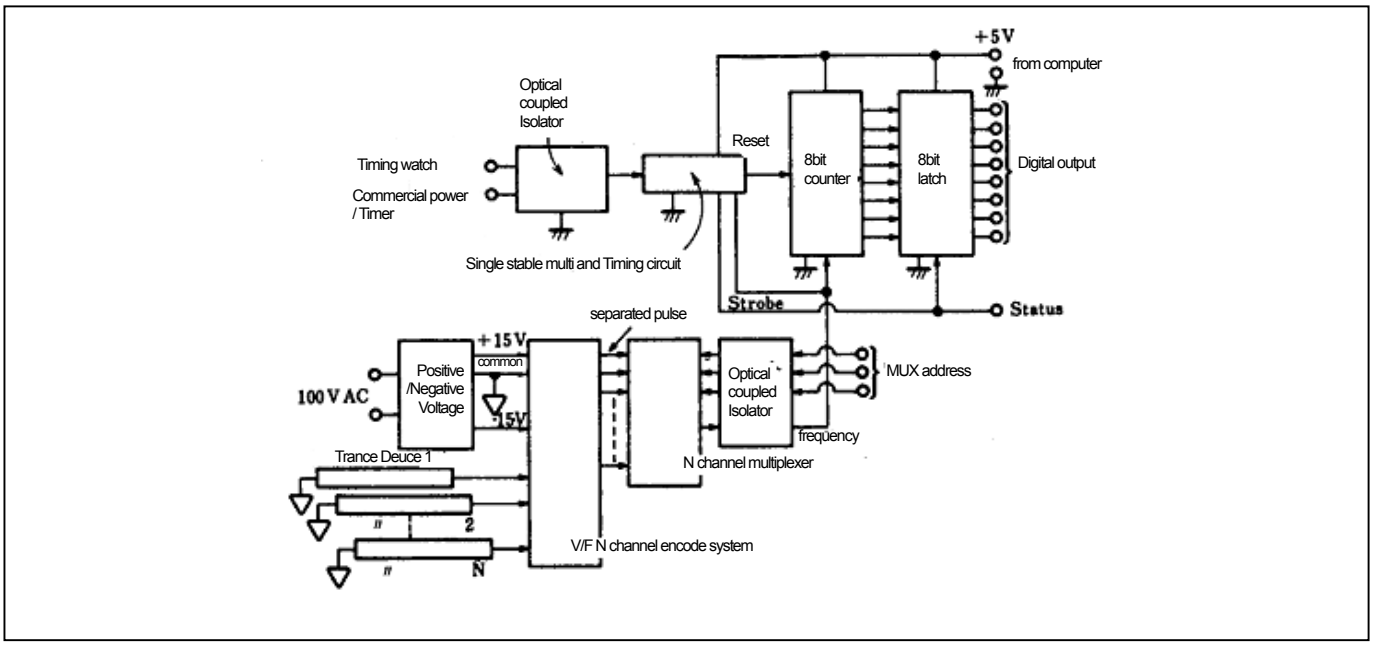


Figure 11. Multi channel ADC system

Figure 12 shows 1-channel ADC. Commercial power supply frequency has been used to generate the timing. NJM556 (Dual timer IC) is used to strobe and reset pulse generator. Latch circuit is the same as the output data of a counter circuit when the strobe pulse is high level. The counter data is latched when the strobe pulse is a low level.

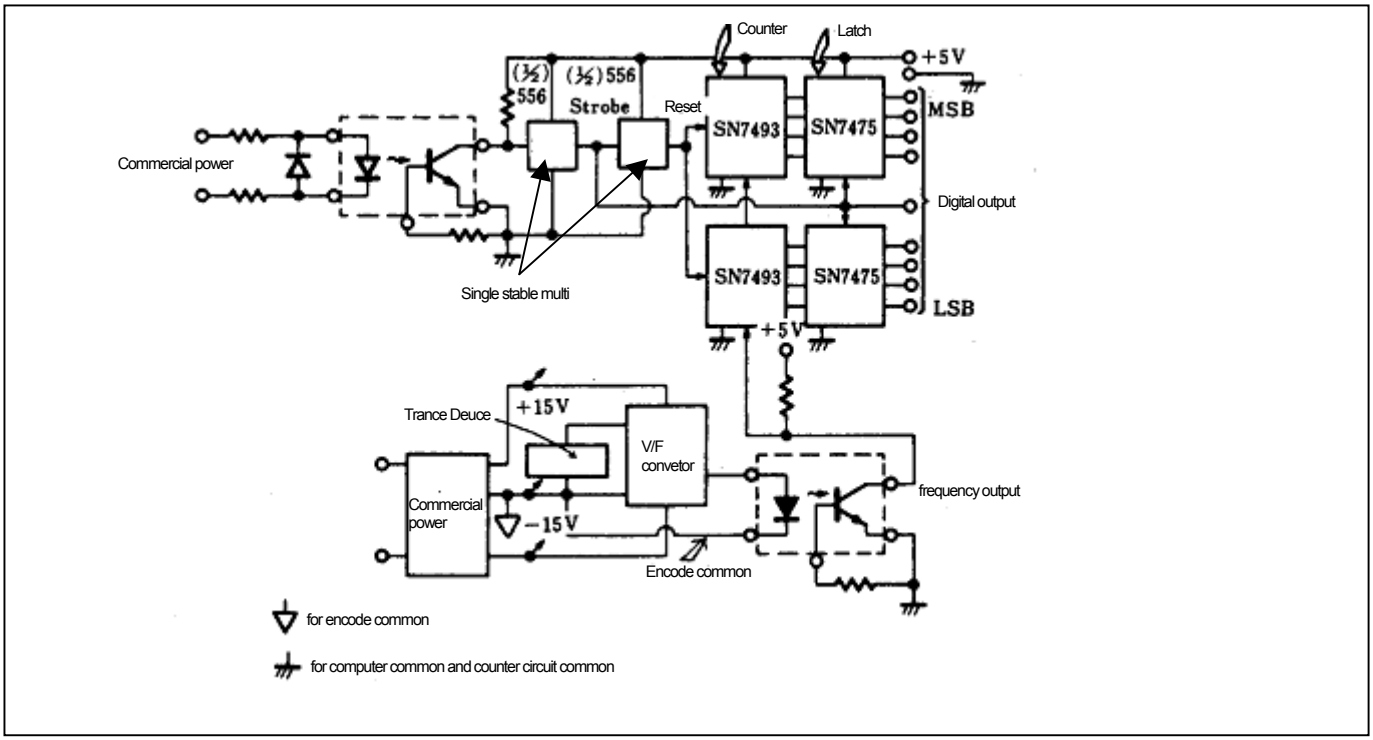


Figure 12. 8-bit ADC system (for 1-channel)

This pulse is used to the microprocessor status monitor. After the counter output is latched, the counter is reset by a reset pulse. Then becomes the first status again. This alternate get started the counter under the action of microprocessor instructions. The best logic sequence is determined by individual applications. To illustrate the calculation of the scale factor, try to assume the resolution of 8 bits at 1 / 60 s convert time. Maximum output will be 1+2+4+8+16+32+64+128=255. The maximum output frequency is 255 × 60Hz, and 15.3kHz.

Accuracy and stability of the ADC is determined by NJM4151 (VFC) chip, an external R,C components, and the timing circuit. Please discuss the error at the following contents: offset, scale factor, linearity, noise. Please consider that there is uncertainty of ± 0.195% for to put into the prediction error. The approximate ADC has linearity error of ± 1 / 2 LSB at corresponding to ± 0.195%. NJM4151 can easily design by linearity of ± 0.05% or linearity of ± 0.1%. Most of linearity is not an issue. Offset drift is determined by input offset drift of the external OP-AMP. So in most cases is very small. The largest source of error are gain drift of NJM4151, and temperature coefficient of external R,C components. NJM4151 has a gain drift of 100ppm / °C average approximately. Error goal of 100ppm / °C can be improved by choosing the external components very well. At 200ppm / °C stability of the timing, gain drift of the total will be 400ppm / °C. This is the maximum gain variation of 2.8% at 70°C from 0°C. If the ADC gain drift is too high, you should try and see the power of the microprocessor. Coupled to the input of the VFC at the reference value of zener diodes of low drift at periodically. To calculate the gain error, impress the digital value of the supplied reference voltage to microprocessor and memory circuit. It is easy. The correct term of scale factor calculated is used to correct gain drift.

The computer can be used to remove noise. It is time and again to convert the same signal voltage. Next, remove the ones far off the average. Then calculate the average. Using computer technology to all of these applications are not required. However, it is often used to improve the accuracy of the system without increasing the cost of the hardware set. NJM4151 is achieved ADC by a very low cost channel. The accuracy of the system conforms to the resolution of the 8-bit. If necessary, Computer receives the data conversion will reduce in many errors. It can be used to improve the overall accuracy of the system.

4. ADC for proportional meter

The accuracy of the systems is better on used proportional method, for measurement equipment. Use the NJM4151, Figure 13 shows the proportion by weight measurement system. First, the strain gauge bridge circuit, and the cells of weight detecting detect the weight. Then generates a difference voltage. The Difference voltage (VD) for the converting bridge approximated VBΔR / RT in a small range of resistance changes of strain - gauge. Necessary information is ΔR / RT and the voltage (VB) across the bridge must be stable. Instrumentation - amplifier amplify the low input differential voltage (VD). It is used to eliminate the common mode input voltage. The voltage across the bridge (VB) converted to frequency (fB). Then, the output voltage amplitude (V0) converted to frequency (f0). Hereby, ADC is designed for proportional meter. The voltage across the bridge converter is 1Hz / V. Amplifier voltage converter is 1kHz / V conversion factor. Proportional counter and frequency meter type of proportional will be used to convert frequency ratio f0/fB. The first advantage of conversion technology by the proportional method is that it is independent of the voltage across the bridge. Frequency (fB) is proportional to the bridge voltage (VB). Output frequency (f0) is proportional to the VB. f0/fB is independent of VB, only proportional to ΔR / RT.

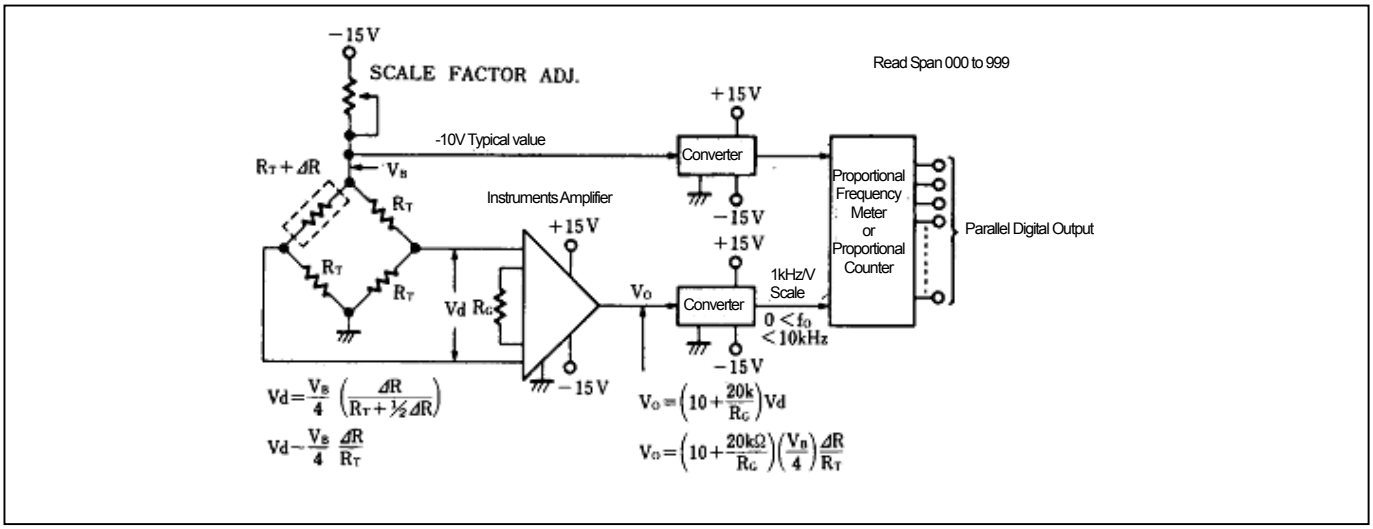


Figure 13. Proportional meter system

5. Temperature to Frequency converter

Temperature is a physical variable that is most commonly measured. Therefore, the transmitter (transducer) is used. However, it each has advantages and disadvantages. Sensitivity, measuring range, linearity, reproducibility, cost, depends on the transducer. Monolithic transistor pair can be used as temperature sensors. Figure 14 shows the circuit.
The advantage of used this circuit linearity and repeatability. AD converter is used so that VFC displayed digital to temperature. Technique of temperature measurement based on a constant characteristic of the transistor. One of dual transistor acts as a temperature-sensitive element. Another dual transistor supplies a constant current to temperature-sensitive portions. High precision amplifier stabilized the voltage difference between the base-emitter's voltage of temperature-sensitive portions. Also, it is amplified at good linearity. It is used to zero to the voltage drop of a fixed I_1R_E, when the output voltage of the amplifier is 0°C. This extra voltage canceled out the absolute temperature. It is necessary to obtain Celsius temperature, when need to read of the absolute temperature can be ignored.

V_{BE}=KT/q * 1n * Ic/Is'
Except Ic/Is >> 1

K= Boltzmann constant (1.38062 * 10^{-23} Joule/°K)
T= Absolute temperature (°K)
q= Charge of Electron (1.60219 * 10^{-19} coulomb)
Is= Reverse saturation current (≅ 1.87 * 10^{-19}μA)
Ic= Collector current

When running in the range of collector current is 1μA to 1mA, monolithic transistor pair is close to this formula. Transistor pair is high β. It is matched pair has a low offset voltage. In addition, IS low, and β is also consistent. ΔVBE integrity is within 1mV at a typical value. In addition, the drift is ±3μV / °C, the difference in β is less than 10%.
The differential input to a precision amplifier,

V_{+IN}-V_{-IN}=KT/q * 1n * I_1R_E+KT/q * 1n * I_2/I_{S2}
=KT/q (1n * I_2/I_1 + 1n * I_{S1}/I_{S2}) - I_1R_E

When Transistor pairs are consistent, IS2 IS1 is the same and the second term 1n1 is zero.
The above equation,

V_{+IN}-V_{-IN}=KT/q * 1n * I_2/I_{S2} - I_1R_E

KT/q is 86.171μV / °C. It is 198.4μV / °K when ratio of I1 versus I2 are 10 versus 1. It subtracted 273.15°C when the absolute - temperature want back to Celsius. It is 54.193mV, when Constant current (I1) and RE multiplied. In that case, the amplifier's input voltage is changed to Celsius. 0.1V / °C is convenient as the scale factor. It generates a voltage of 0 to 7V at 0 to 70 °C ranges. High-precision amplifier input common mode rejection takes 0.5 to 0.6. Then take 504 as an amplifier. The amplifier input bias current should be low in relation to the emitter current of transistor temperature sensitive pair. This temperature measurement method can be applied to other applications. Sensitivity can be adjusted easily by changing the gain of the amplifier or changing the ratio of the collector current. Linearity of output voltage and temperature are within ±0.01% linearity in the range of 0 to +70°C at circuit of Figure 14. Application will be at large by introducing microprocessors. It can change the sensitivity of the transducer at the computer, and program can also be automated.

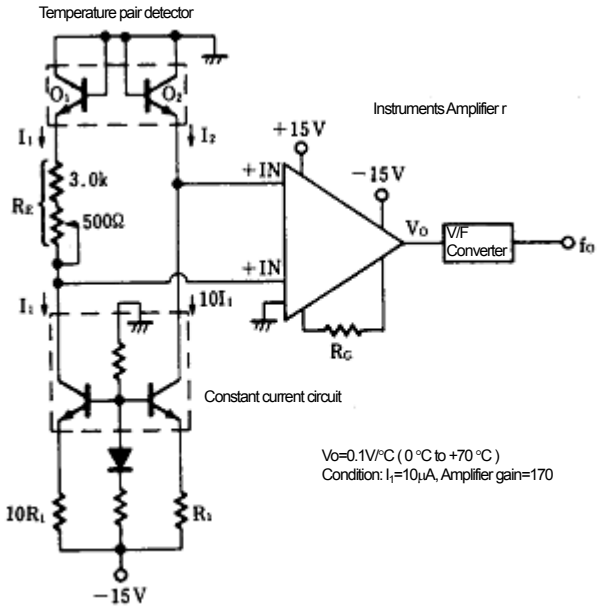
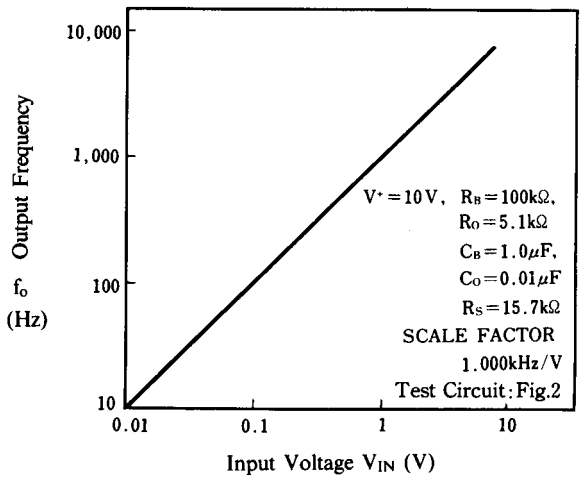


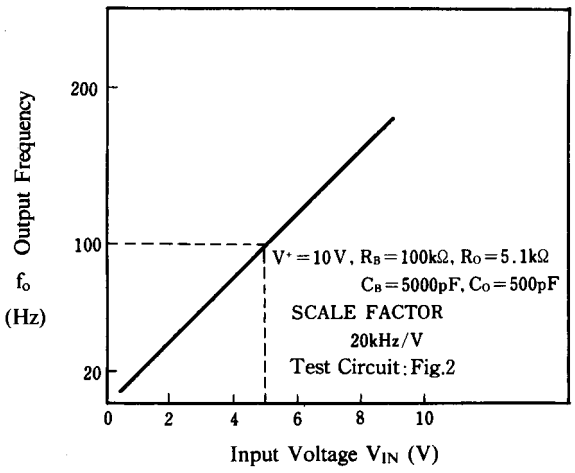
Figure 14. Temperature to Frequency converter

■ TYPICAL CHARACTERISTICS

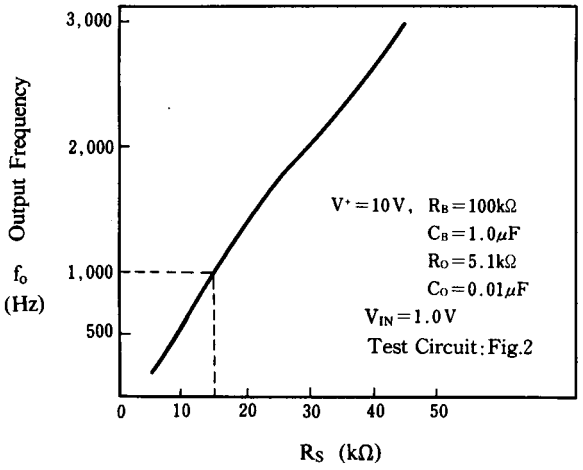
V_{IN}-fo Characteristics (VFC)



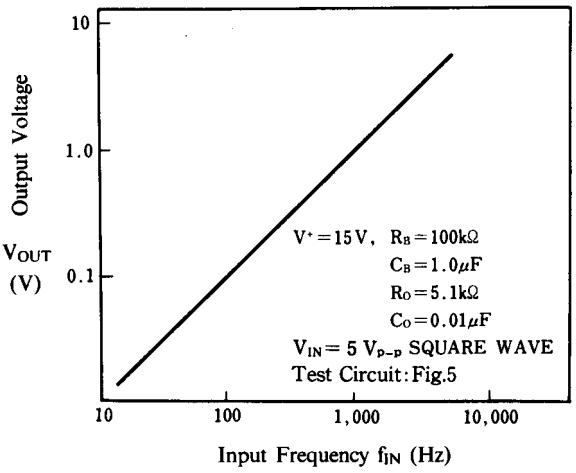
V_{IN}-fo Characteristics (VFC)



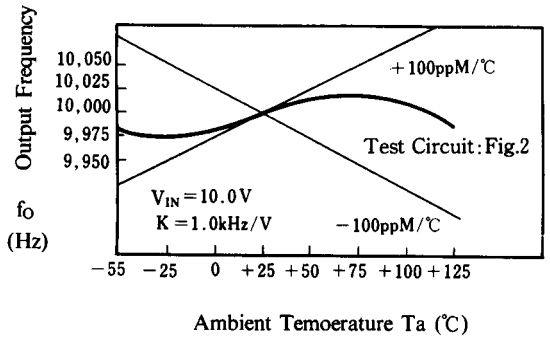
Scale Factor Characteristics



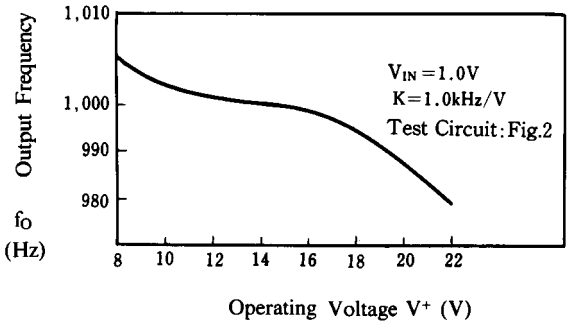
Input Frequency vs. Output Voltage (FVC)



Ambient Temperature Characteristics



fo vs. Operating Voltage



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