

## High-Speed CMOS Logic 4-Bit Parallel Access Register

### Features

- Asynchronous Master Reset
- J,  $\bar{K}$ , (D) Inputs to First Stage
- Fully Synchronous Serial or Parallel Data Transfer
- Shift Right and Parallel Load Capability
- Complementary Output From Last Stage
- Buffered Inputs
- Typical  $f_{MAX} = 50\text{MHz}$  at  $V_{CC} = 5\text{V}$ ,  
 $C_L = 15\text{pF}$ ,  $T_A = 25^\circ\text{C}$
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . .  $-55^\circ\text{C}$  to  $125^\circ\text{C}$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5\text{V}$

### Description

The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

The two modes of operation, shift right ( $Q_0$ - $Q_1$ ) and parallel load, are controlled by the state of the Parallel Enable ( $\overline{PE}$ ) input. Serial data enters the first flip-flop ( $Q_0$ ) via the J and  $\bar{K}$  inputs when the  $\overline{PE}$  input is high, and is shifted one bit in the direction  $Q_0$ - $Q_1$ - $Q_2$ - $Q_3$  following each Low to High clock transition. The J and K inputs provide the flexibility of the JK-type input for special applications and by tying the two pins together, the simple D-type input for general applications. The device appears as four common-clocked D flip-flops when the  $\overline{PE}$  input is Low. After the Low to High clock transition, data on the parallel inputs (D0-D3) is transferred to the respective  $Q_0$ - $Q_3$  outputs. Shift left operation ( $Q_3$ - $Q_2$ ) can be achieved by tying the  $Q_n$  outputs to the  $D_{n-1}$  inputs and holding the  $\overline{PE}$  input low.

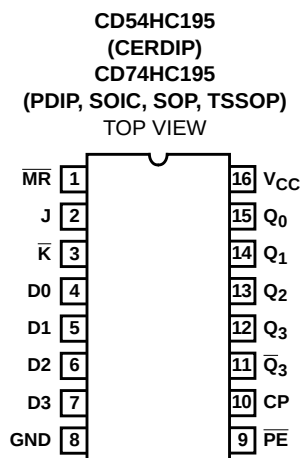
All parallel and serial data transfers are synchronous, occurring after each Low to High clock transition. The 'HC195 series utilizes edge triggering; therefore, there is no restriction on the activity of the J, K, Pn and  $\overline{PE}$  inputs for logic operations, other than set-up and hold time requirements. A Low on the asynchronous Master Reset ( $\overline{MR}$ ) input sets all Q outputs Low, independent of any other input condition.

### Ordering Information

| PART NUMBER  | TEMP. RANGE<br>( $^\circ\text{C}$ ) | PACKAGE      |
|--------------|-------------------------------------|--------------|
| CD54HC195F3A | -55 to 125                          | 16 Ld Cerdip |
| CD74HC195E   | -55 to 125                          | 16 Ld PDIP   |
| CD74HC195M   | -55 to 125                          | 16 Ld SOIC   |
| CD74HC195NSR | -55 to 125                          | 16 Ld SOP    |
| CD74HC195PW  | -55 to 125                          | 16 Ld TSSOP  |
| CD74HC195PWR | -55 to 125                          | 16 Ld TSSOP  |
| CD74HC195PWT | -55 to 125                          | 16 Ld TSSOP  |

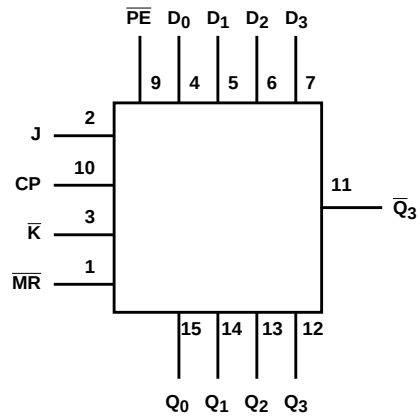
NOTE: When ordering, use the entire part number. The suffix R denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

### Pinout



# CD54HC195, CD74HC195

## Functional Diagram



TRUTH TABLE

| OPERATING MODES           | INPUTS |    |    |   |   |    | OUTPUT         |                |                |                |                |
|---------------------------|--------|----|----|---|---|----|----------------|----------------|----------------|----------------|----------------|
|                           | MR     | CP | PE | J | K | Dn | Q <sub>0</sub> | Q <sub>1</sub> | Q <sub>2</sub> | Q <sub>3</sub> | Q <sub>3</sub> |
| Asynchronous Reset        | L      | X  | X  | X | X | X  | L              | L              | L              | L              | H              |
| Shift, Set First Stage    | H      | ↑  | h  | h | h | X  | H              | q <sub>0</sub> | q <sub>1</sub> | q <sub>2</sub> | q <sub>2</sub> |
| Shift, Reset First Stage  | H      | ↑  | h  | l | l | X  | L              | q <sub>0</sub> | q <sub>1</sub> | q <sub>2</sub> | q <sub>2</sub> |
| Shift, Toggle First Stage | H      | ↑  | h  | h | l | X  | q <sub>0</sub> | q <sub>0</sub> | q <sub>1</sub> | q <sub>2</sub> | q <sub>2</sub> |
| Shift, Retain First Stage | H      | ↑  | h  | l | h | X  | q <sub>0</sub> | q <sub>0</sub> | q <sub>1</sub> | q <sub>2</sub> | q <sub>2</sub> |
| Parallel Load             | H      | ↑  | l  | X | X | dn | d <sub>0</sub> | d <sub>1</sub> | d <sub>2</sub> | d <sub>3</sub> | d <sub>2</sub> |

H = High Voltage Level

L = Low Voltage Level,

X = Don't Care

↑ = Transition from Low to High Level

l = Low Voltage Level One Set-up Time Prior to the Low to High Clock Transition

h = Low Voltage Level One Set-up Time prior to the High to Low Clock Transition,

dn (q<sub>n</sub>) = Lower Case Letters Indicate the State of the Referenced Input (or output) One Set-up Time Prior to the Low to High Clock Transition.

# CD54HC195, CD74HC195

## Absolute Maximum Ratings

DC Supply Voltage,  $V_{CC}$  ..... -0.5V to 7V  
 DC Input Diode Current,  $I_{IK}$   
     For  $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$  .....  $\pm 20mA$   
 DC Output Diode Current,  $I_{OK}$   
     For  $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$  .....  $\pm 20mA$   
 DC Output Source or Sink Current per Output Pin,  $I_O$   
     For  $V_O > -0.5V$  or  $V_O < V_{CC} + 0.5V$  .....  $\pm 25mA$   
 DC  $V_{CC}$  or Ground Current,  $I_{CC}$  or  $I_{GND}$  .....  $\pm 50mA$

## Thermal Information

Package Thermal Impedance,  $\theta_{JA}$  (see Note 1):  
     E (PDIP) Package .....  $67^{\circ}C/W$   
     M (SOIC) Package .....  $73^{\circ}C/W$   
     NS (SOP) Package .....  $64^{\circ}C/W$   
     PW (TSSOP) Package .....  $108^{\circ}C/W$   
 Maximum Junction Temperature .....  $150^{\circ}C$   
 Maximum Storage Temperature Range .....  $-65^{\circ}C$  to  $150^{\circ}C$   
 Maximum Lead Temperature (Soldering 10s) .....  $300^{\circ}C$   
     (SOIC - Lead Tips Only)

## Operating Conditions

Temperature Range ( $T_A$ ) .....  $-55^{\circ}C$  to  $125^{\circ}C$   
 Supply Voltage Range,  $V_{CC}$   
     HC Types ..... 2V to 6V  
     HCT Types ..... 4.5V to 5.5V  
 DC Input or Output Voltage,  $V_I$ ,  $V_O$  ..... 0V to  $V_{CC}$   
 Input Rise and Fall Time  
     2V ..... 1000ns (Max)  
     4.5V ..... 500ns (Max)  
     6V ..... 400ns (Max)

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

## DC Electrical Specifications

| PARAMETER                               | SYMBOL          | TEST CONDITIONS                    |                     | V <sub>CC</sub> (V) | 25°C |     |      | -40°C TO 85°C |      | -55°C TO 125°C |      | UNITS |
|-----------------------------------------|-----------------|------------------------------------|---------------------|---------------------|------|-----|------|---------------|------|----------------|------|-------|
|                                         |                 | V <sub>I</sub> (V)                 | I <sub>O</sub> (mA) |                     | MIN  | TYP | MAX  | MIN           | MAX  | MIN            | MAX  |       |
| High Level Input Voltage                | V <sub>IH</sub> | -                                  | -                   | 2                   | 1.5  | -   | -    | 1.5           | -    | 1.5            | -    | V     |
|                                         |                 |                                    |                     | 4.5                 | 3.15 | -   | -    | 3.15          | -    | 3.15           | -    | V     |
|                                         |                 |                                    |                     | 6                   | 4.2  | -   | -    | 4.2           | -    | 4.2            | -    | V     |
| Low Level Input Voltage                 | V <sub>IL</sub> | -                                  | -                   | 2                   | -    | -   | 0.5  | -             | 0.5  | -              | 0.5  | V     |
|                                         |                 |                                    |                     | 4.5                 | -    | -   | 1.35 | -             | 1.35 | -              | 1.35 | V     |
|                                         |                 |                                    |                     | 6                   | -    | -   | 1.8  | -             | 1.8  | -              | 1.8  | V     |
| High Level Output Voltage<br>CMOS Loads | V <sub>OH</sub> | V <sub>IH</sub> or V <sub>IL</sub> | -0.02               | 2                   | 1.9  | -   | -    | 1.9           | -    | 1.9            | -    | V     |
|                                         |                 |                                    | -0.02               | 4.5                 | 4.4  | -   | -    | 4.4           | -    | 4.4            | -    | V     |
|                                         |                 |                                    | -0.02               | 6                   | 5.9  | -   | -    | 5.9           | -    | 5.9            | -    | V     |
| -                                       |                 |                                    | -                   | -                   | -    | -   | -    | -             | -    | -              | V    |       |
| High Level Output Voltage<br>TTL Loads  |                 |                                    | -4                  | 4.5                 | 3.98 | -   | -    | 3.84          | -    | 3.7            | -    | V     |
|                                         |                 |                                    | -5.2                | 6                   | 5.48 | -   | -    | 5.34          | -    | 5.2            | -    | V     |
| Low Level Output Voltage<br>CMOS Loads  | V <sub>OL</sub> | V <sub>IH</sub> or V <sub>IL</sub> | 0.02                | 2                   | -    | -   | 0.1  | -             | 0.1  | -              | 0.1  | V     |
|                                         |                 |                                    | 0.02                | 4.5                 | -    | -   | 0.1  | -             | 0.1  | -              | 0.1  | V     |
|                                         |                 |                                    | 0.02                | 6                   | -    | -   | 0.1  | -             | 0.1  | -              | 0.1  | V     |
| -                                       |                 |                                    | -                   | -                   | -    | -   | -    | -             | -    | -              | V    |       |
| Low Level Output Voltage<br>TTL Loads   |                 |                                    | 4                   | 4.5                 | -    | -   | 0.26 | -             | 0.33 | -              | 0.4  | V     |
|                                         |                 |                                    | 5.2                 | 6                   | -    | -   | 0.26 | -             | 0.33 | -              | 0.4  | V     |
| Input Leakage Current                   | I <sub>I</sub>  | V <sub>CC</sub> or GND             | -                   | 6                   | -    | -   | ±0.1 | -             | ±1   | -              | ±1   | µA    |
| Quiescent Device Current                | I <sub>CC</sub> | V <sub>CC</sub> or GND             | 0                   | 6                   | -    | -   | 8    | -             | 80   | -              | 160  | µA    |

# CD54HC195, CD74HC195

## Prerequisite For Switching Function

| PARAMETER                                                   | SYMBOL           | TEST CONDITIONS | V <sub>CC</sub> (V) | 25°C |     | -40°C TO 85°C |     | -55°C TO 125°C |     | UNITS |
|-------------------------------------------------------------|------------------|-----------------|---------------------|------|-----|---------------|-----|----------------|-----|-------|
|                                                             |                  |                 |                     | MIN  | MAX | MIN           | MAX | MIN            | MAX |       |
| Clock Frequency                                             | f <sub>MAX</sub> | -               | 2                   | 6    | -   | 5             | -   | 4              | -   | MHz   |
|                                                             |                  |                 | 4.5                 | 30   | -   | 25            | -   | 20             | -   | MHz   |
|                                                             |                  |                 | 6                   | 35   | -   | 29            | -   | 23             | -   | MHz   |
| MR Pulse Width                                              | t <sub>w</sub>   | -               | 2                   | 80   | -   | 100           | -   | 120            | -   | ns    |
|                                                             |                  |                 | 4.5                 | 16   | -   | 20            | -   | 24             | -   | ns    |
|                                                             |                  |                 | 6                   | 14   | -   | 17            | -   | 20             | -   | ns    |
| Clock Pulse Width                                           | t <sub>w</sub>   | -               | 2                   | 80   | -   | 100           | -   | 120            | -   | ns    |
|                                                             |                  |                 | 4.5                 | 16   | -   | 20            | -   | 24             | -   | ns    |
|                                                             |                  |                 | 6                   | 14   | -   | 17            | -   | 20             | -   | ns    |
| Set-up Time<br>J, $\overline{K}$ , $\overline{PE}$ to Clock | t <sub>SU</sub>  | -               | 2                   | 100  | -   | 125           | -   | 150            | -   | ns    |
|                                                             |                  |                 | 4.5                 | 20   | -   | 25            | -   | 30             | -   | ns    |
|                                                             |                  |                 | 6                   | 17   | -   | 21            | -   | 26             | -   | ns    |
| Hold Time<br>J, $\overline{K}$ , $\overline{PE}$ to Clock   | t <sub>H</sub>   | -               | 2                   | 3    | -   | 3             | -   | 3              | -   | ns    |
|                                                             |                  |                 | 4.5                 | 3    | -   | 3             | -   | 3              | -   | ns    |
|                                                             |                  |                 | 6                   | 5    | -   | 3             | -   | 3              | -   | ns    |
| Removal Time,<br>MR to Clock                                | t <sub>REM</sub> | -               | 2                   | 80   | -   | 100           | -   | 120            | -   | ns    |
|                                                             |                  |                 | 4.5                 | 16   | -   | 20            | -   | 24             | -   | ns    |
|                                                             |                  |                 | 6                   | 14   | -   | 17            | -   | 20             | -   | ns    |

## Switching Specifications Input t<sub>r</sub>, t<sub>f</sub> = 6ns

| PARAMETER                                  | SYMBOL                              | TEST CONDITIONS       | V <sub>CC</sub> (V) | 25°C |     | -40°C TO 85°C | -55°C TO 125°C | UNITS |
|--------------------------------------------|-------------------------------------|-----------------------|---------------------|------|-----|---------------|----------------|-------|
|                                            |                                     |                       |                     | TYP  | MAX | MAX           | MAX            |       |
| HC TYPES                                   |                                     |                       |                     |      |     |               |                |       |
| Propagation Delay, CP to Output            | t <sub>PLH</sub> , t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | 175 | 220           | 265            | ns    |
|                                            |                                     |                       | 4.5                 | -    | 35  | 44            | 53             | ns    |
|                                            |                                     |                       | 6                   | -    | 30  | 37            | 45             | ns    |
| Propagation Delay, MR toOutput             | t <sub>PLH</sub> , t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | 150 | 190           | 225            | ns    |
|                                            |                                     |                       | 4.5                 | -    | 30  | 38            | 45             | ns    |
|                                            |                                     |                       | 6                   | -    | 26  | 33            | 38             | ns    |
| Output Transition Times (Figure 1)         | t <sub>TLH</sub> , t <sub>THL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | 75  | 95            | 110            | ns    |
|                                            |                                     |                       | 4.5                 | -    | 15  | 19            | 22             | ns    |
|                                            |                                     |                       | 6                   | -    | 13  | 16            | 19             | ns    |
| Input Capacitance                          | C <sub>IN</sub>                     | -                     | -                   | -    | 10  | 10            | 10             | pF    |
| CP to Q <sub>n</sub> Propagation Delay     | t <sub>PLH</sub> , t <sub>PHL</sub> | C <sub>L</sub> = 15pF | 5                   | 14   | -   | -             | -              | ns    |
| MR to Q <sub>n</sub>                       | t <sub>PHL</sub>                    | C <sub>L</sub> = 15pF | 5                   | 13   | -   | -             | -              | ns    |
| Maximum Clock Frequency                    | f <sub>MAX</sub>                    | C <sub>L</sub> = 15pF | 5                   | 50   | -   | -             | -              | MHz   |
| Power Dissipation Capacitance (Notes 2, 3) | C <sub>PD</sub>                     | C <sub>L</sub> = 15pF |                     | 45   | -   | -             | -              | pF    |

### NOTES:

- C<sub>PD</sub> is used to determine the dynamic power consumption, per flip-flop.
- $P_D = V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_o)$  where f<sub>i</sub> = Input Frequency, f<sub>o</sub> = Output Frequency, C<sub>L</sub> = Output Load Capacitance, V<sub>CC</sub> = Supply Voltage.

## Test Circuit and Waveforms

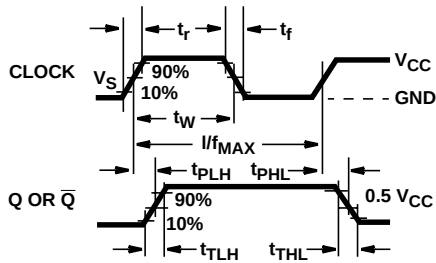


FIGURE 1. CLOCK PREREQUISITE AND PROPAGATION DELAYS AND OUTPUT TRANSITION TIMES

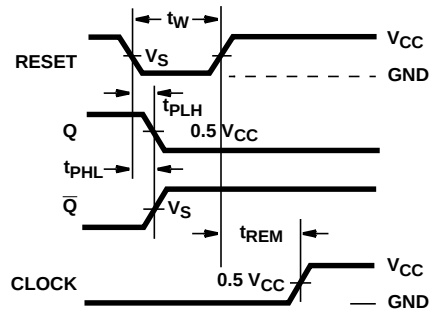


FIGURE 2. MASTER RESET PREREQUISITE AND PROPAGATION DELAYS

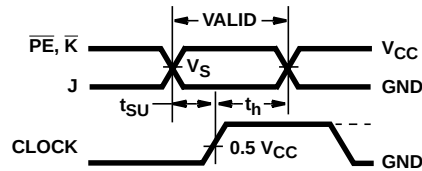


FIGURE 3. J,  $\bar{K}$ , OR PARALLEL ENABLE PREREQUISITE TIMES

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| CD74HC195E       | ACTIVE        | PDIP         | N                  | 16   | 25             | Pb-Free<br>(RoHS)          | CU NIPDAU               | N / A for Pkg Type   | -55 to 125   | CD74HC195E              | <a href="#">Samples</a> |
| CD74HC195EE4     | ACTIVE        | PDIP         | N                  | 16   | 25             | Pb-Free<br>(RoHS)          | CU NIPDAU               | N / A for Pkg Type   | -55 to 125   | CD74HC195E              | <a href="#">Samples</a> |
| CD74HC195M       | ACTIVE        | SOIC         | D                  | 16   | 40             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | HC195M                  | <a href="#">Samples</a> |
| CD74HC195M96     | ACTIVE        | SOIC         | D                  | 16   | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | HC195M                  | <a href="#">Samples</a> |
| CD74HC195M96G4   | ACTIVE        | SOIC         | D                  | 16   | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | HC195M                  | <a href="#">Samples</a> |
| CD74HC195MG4     | ACTIVE        | SOIC         | D                  | 16   | 40             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | HC195M                  | <a href="#">Samples</a> |
| CD74HC195NSR     | ACTIVE        | SO           | NS                 | 16   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | HC195M                  | <a href="#">Samples</a> |
| CD74HC195PW      | ACTIVE        | TSSOP        | PW                 | 16   | 90             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | HJ195                   | <a href="#">Samples</a> |
| CD74HC195PWG4    | ACTIVE        | TSSOP        | PW                 | 16   | 90             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | HJ195                   | <a href="#">Samples</a> |
| CD74HC195PWR     | ACTIVE        | TSSOP        | PW                 | 16   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | HJ195                   | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

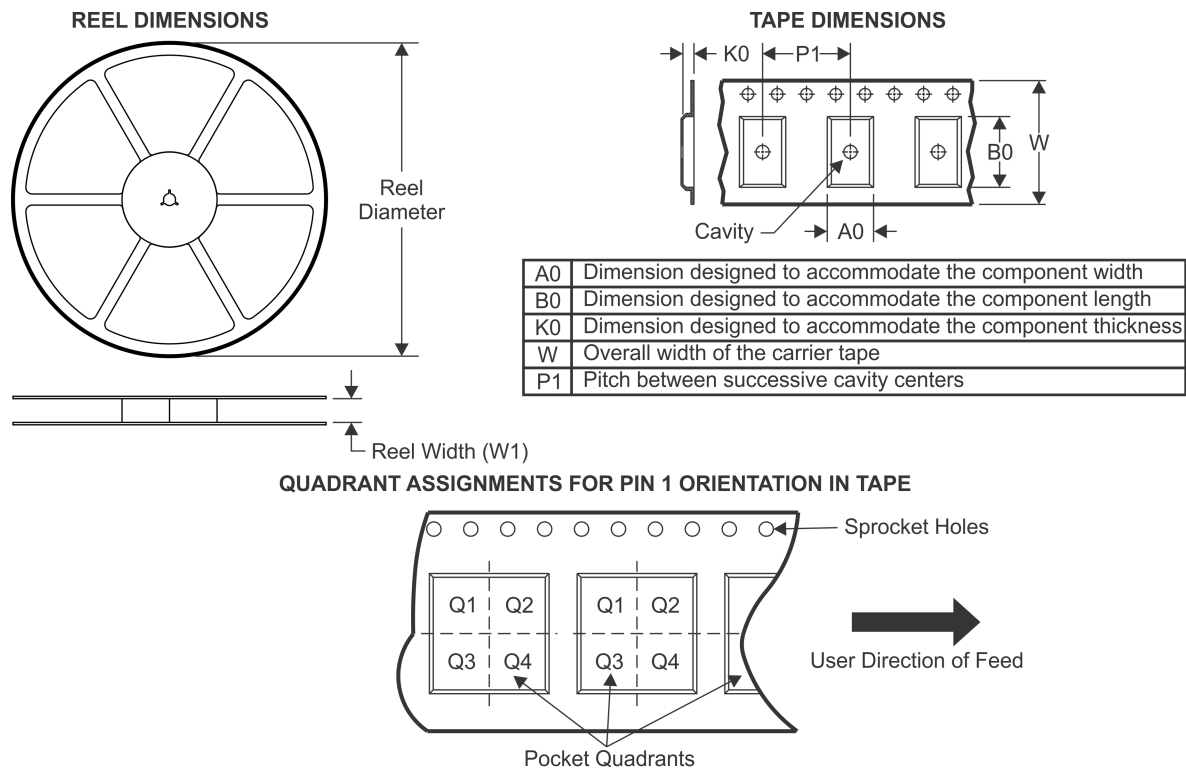
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- <sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- <sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- <sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- <sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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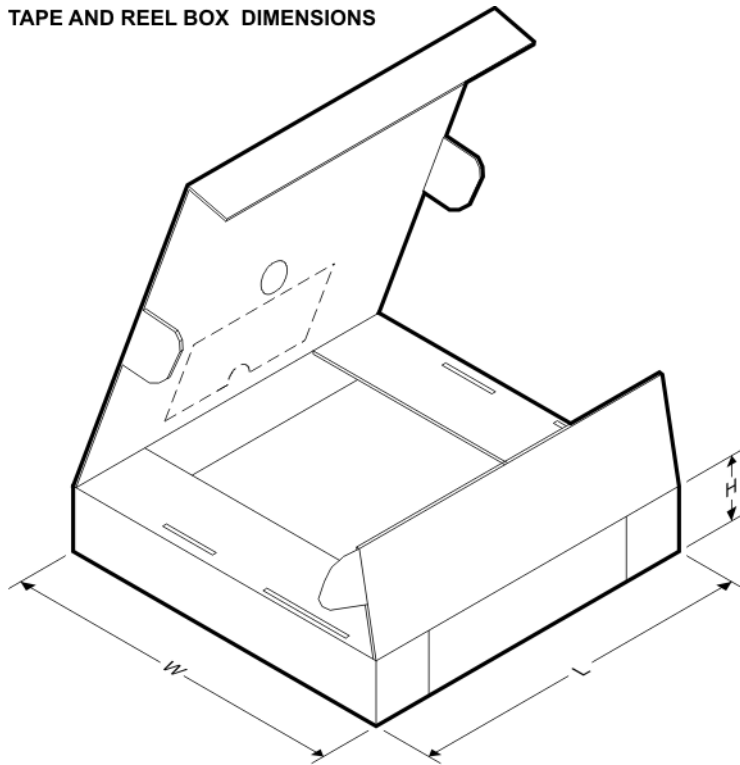
**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74HC195M96 | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| CD74HC195NSR | SO           | NS              | 16   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |
| CD74HC195PWR | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |



## TAPE AND REEL BOX DIMENSIONS



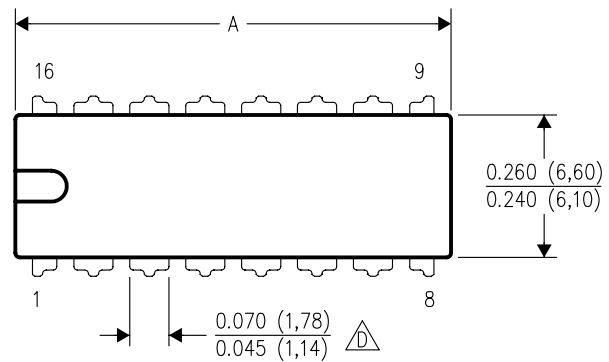
\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74HC195M96 | SOIC         | D               | 16   | 2500 | 333.2       | 345.9      | 28.6        |
| CD74HC195NSR | SO           | NS              | 16   | 2000 | 367.0       | 367.0      | 38.0        |
| CD74HC195PWR | TSSOP        | PW              | 16   | 2000 | 367.0       | 367.0      | 35.0        |

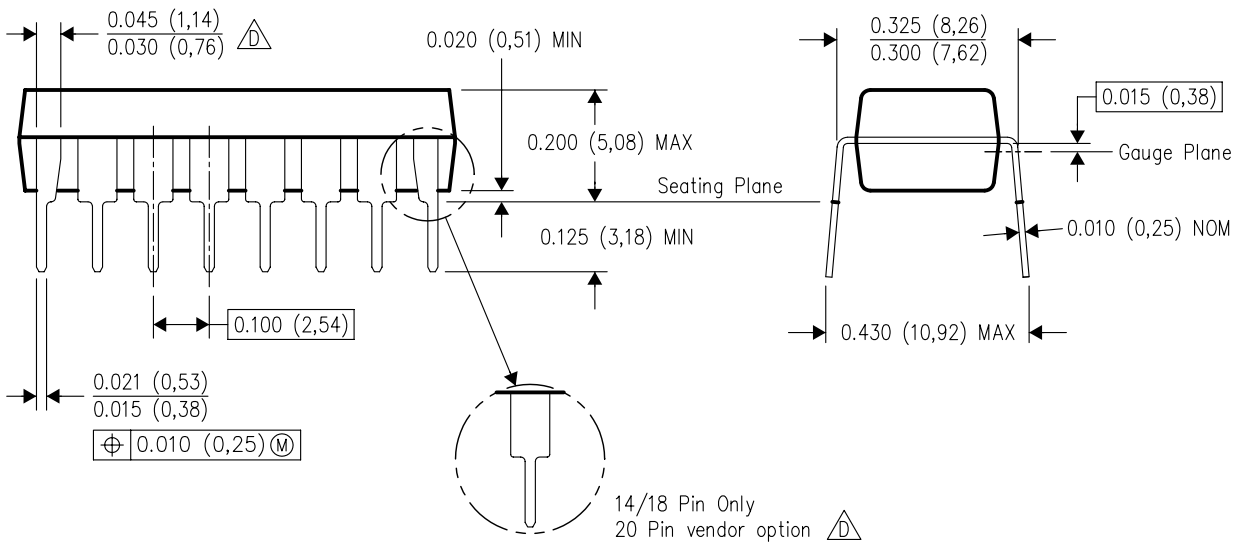
## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **             | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| DIM                 |                  |                  |                  |                  |
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |

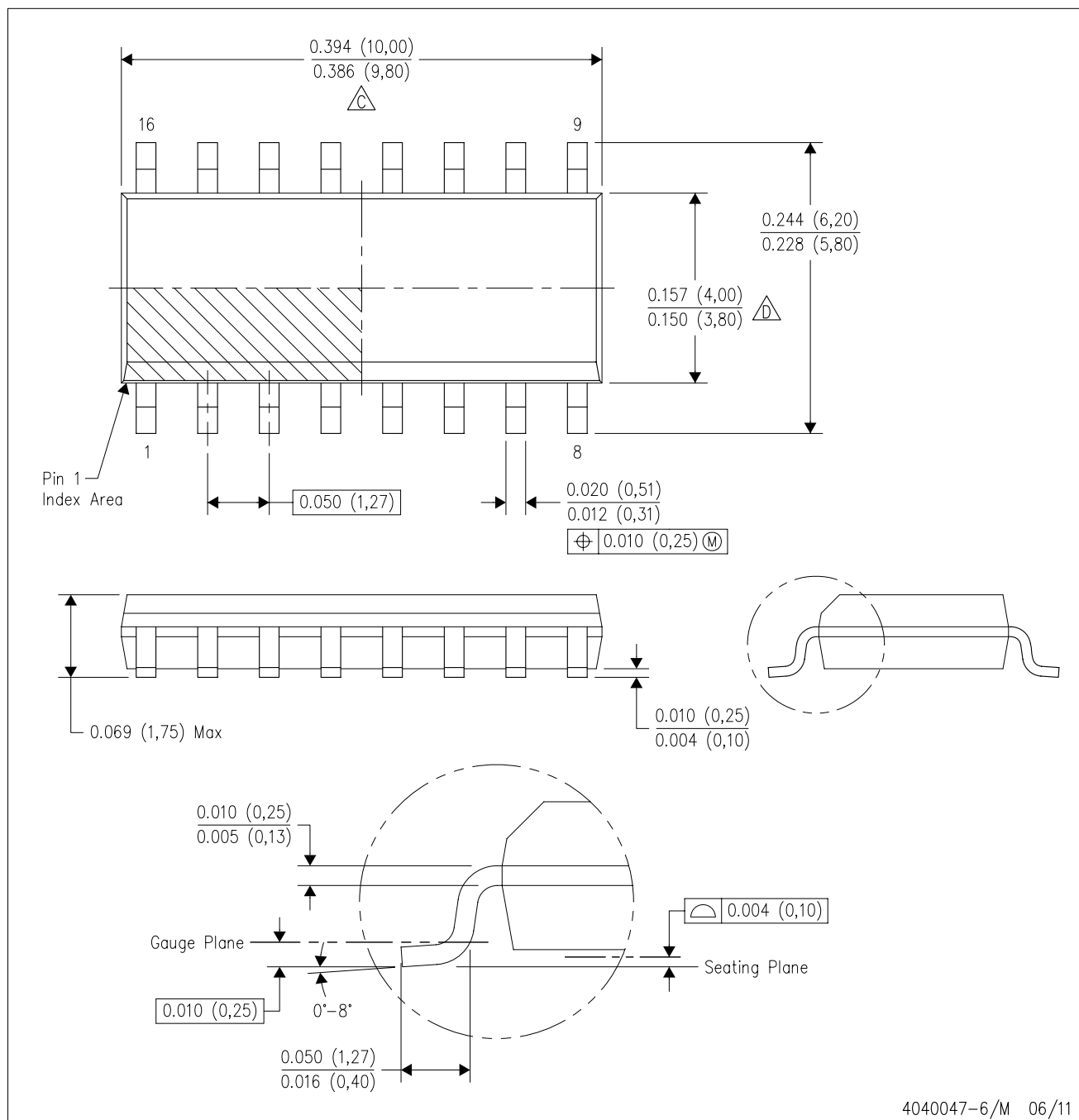


4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

## D (R-PDSO-G16)

## PLASTIC SMALL OUTLINE

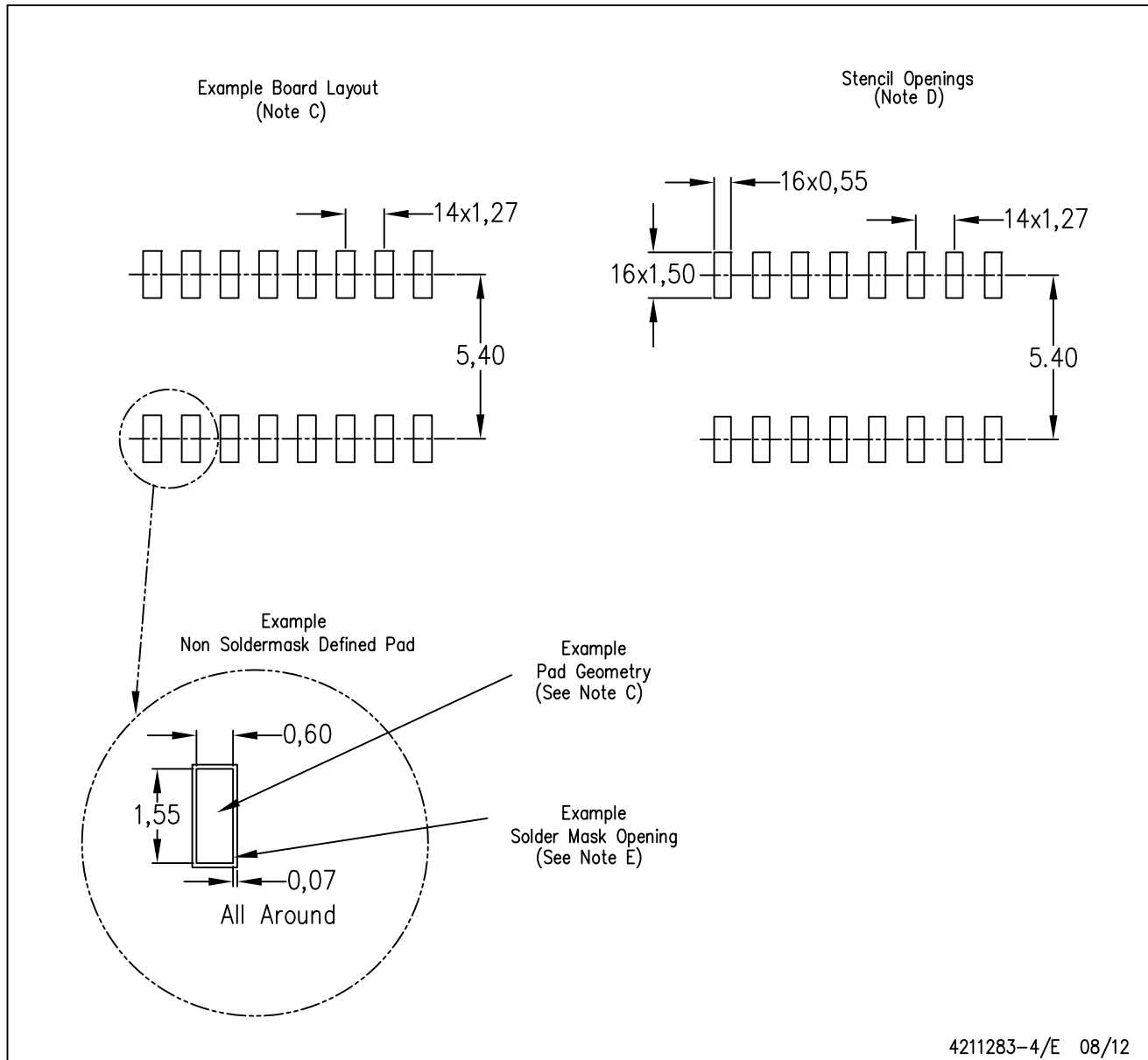


NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
**C** Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.  
**D** Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.  
E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

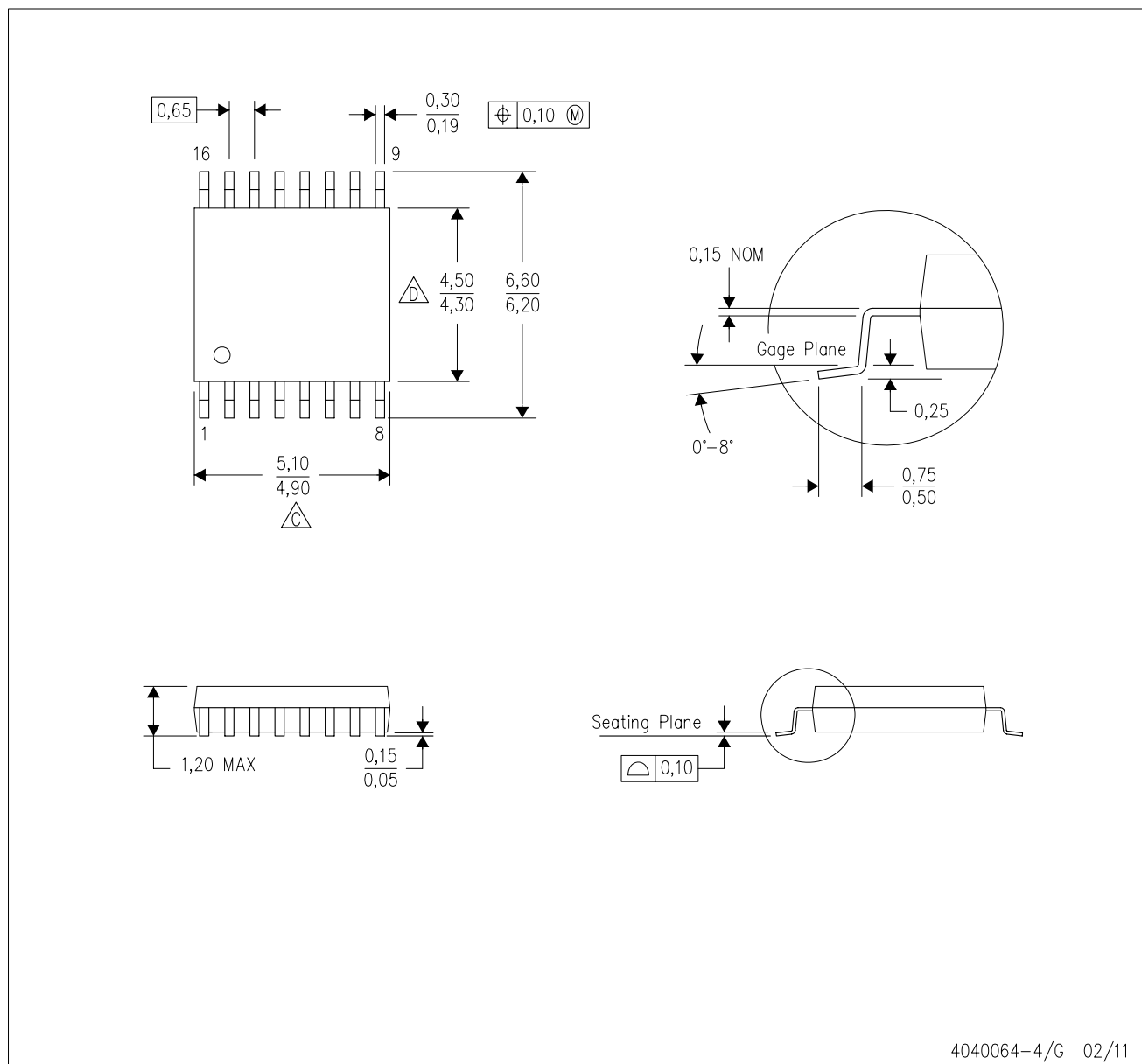
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

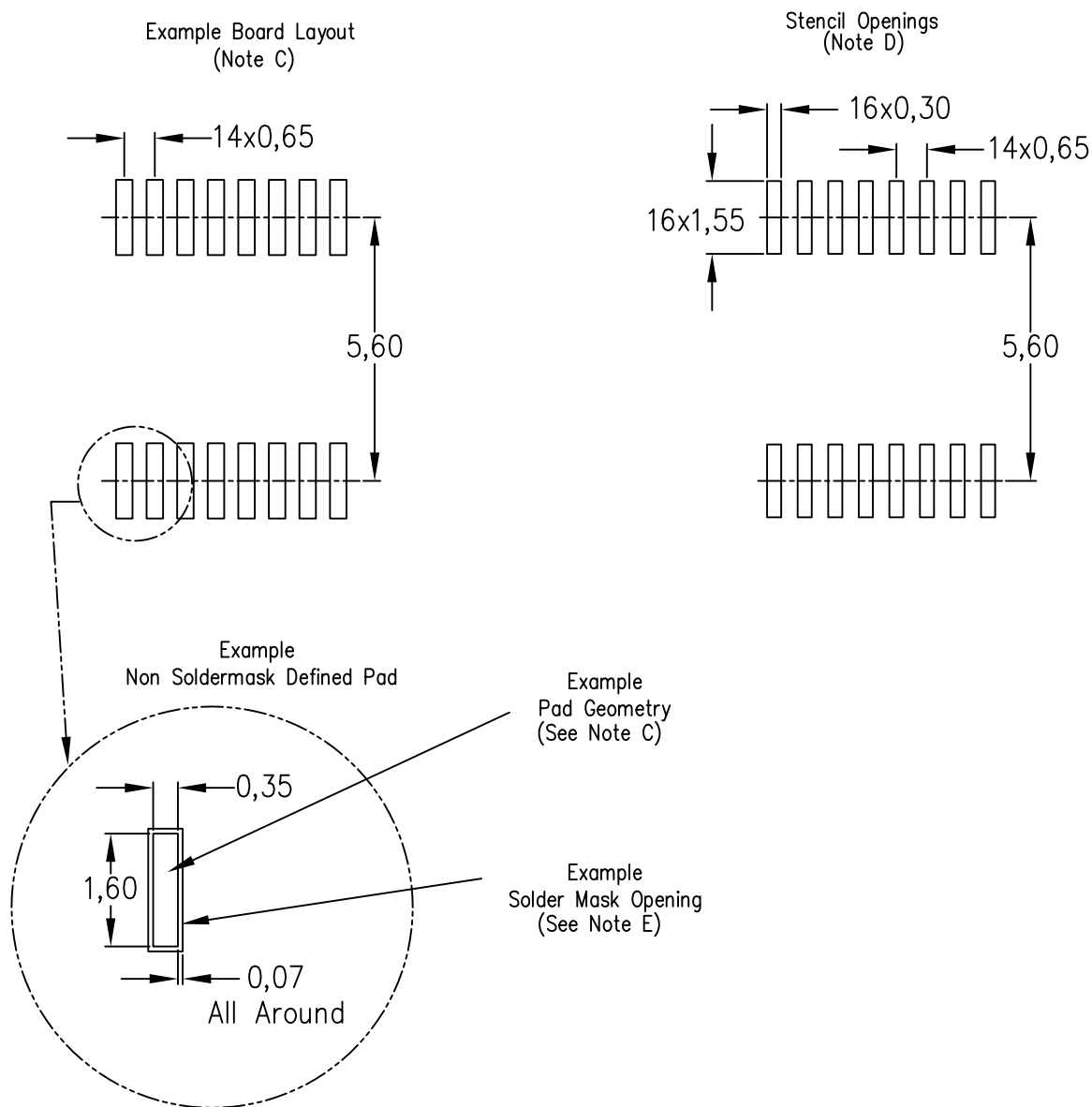


4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211284-3/F 12/12

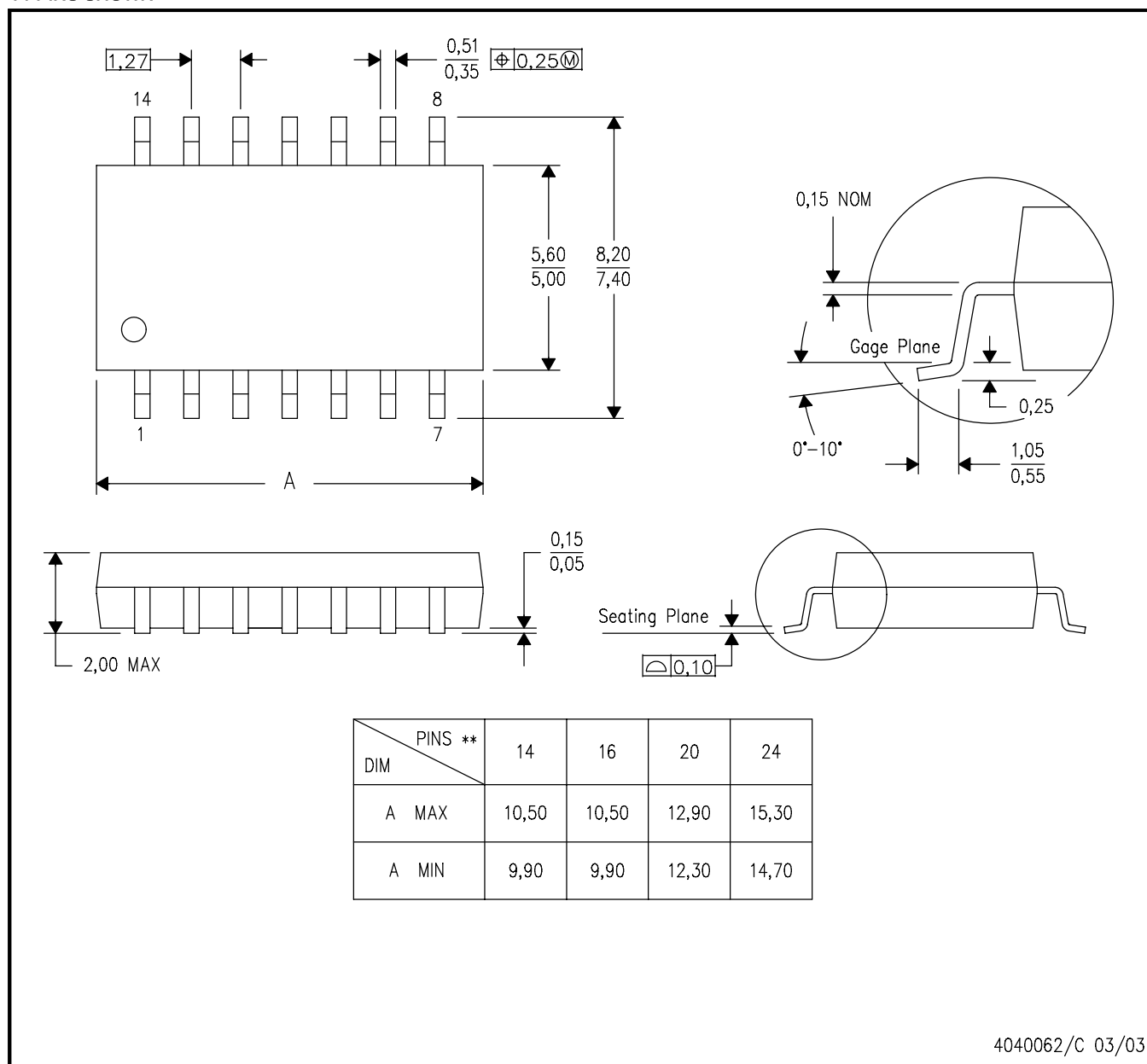
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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