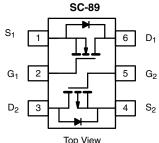




Complementary N- and P-Channel 60 V (D-S) MOSFET

PRODUCT SUMMARY						
	V _{DS} (V)	$R_{DS(on)}\left(\Omega\right)$	I _D (mA)			
N-Channel	60	1.40 at V _{GS} = 10 V	500			
		3 at V _{GS} = 4.5 V	200			
P-Channel	- 60	4 at V _{GS} = - 10 V	- 500			
		8 at V _{GS} = - 4.5 V	- 25			



Marking Code: H

Ordering Information: Si1029X-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFETs
- · Very Small Footprint
- · High-Side Switching
- Low On-Resistance: N-Channel, 1.40 Ω P-Channel, 4 Ω
- Low Threshold: ± 2 V (typ.)
- Fast Switching Speed: 15 ns (typ.)
- Gate-Source ESD Protected: 2000 V
- Compliant to RoHS Directive 2002/95/EC

BENEFITS

- · Ease in Driving Switches
- Low Offset (Error) Voltage
- Low-Voltage Operation
- · High-Speed Circuits

APPLICATIONS

- · Replace Digital Transistor, Level-Shifter
- · Battery Operated Systems
- Power Supply Converter Circuits

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)							
			N-Channel		P-Channel		
Parameter		Symbol	5 s	Steady State	5 s	Steady State	Unit
Drain-Source Voltage		V_{DS}	60		- 60		V
Gate-Source Voltage		V_{GS}	± 20]	
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 25 °C	I _D	320	305	- 200	- 190	-
	T _A = 85 °C		230	220	- 145	- 135	
Pulsed Drain Current ^b		I _{DM}	650		- 650		mA
Continuous Source Current (Diode Conduction) ^a		I _S	450	380	- 450	- 380	
Maximum Power Dissipation ^a	T _A = 25 °C	P _D	280	250	280	250	mW
	T _A = 85 °C		145	130	145	130	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150				°C
Gate-Source ESD Rating (HBM, Method 3015)		ESD	2000			V	

Notes

- a. Surface mounted on FR4 board.
- b. Pulse width limited by maximum junction temperature.

ROHS COMPLIANT HALOGEN FREE

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SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)								
Parameter	Symbol			Min.	Тур.	Max.	Unit	
Static					•	•		
Drain Course Breakdown Voltage	V	$V_{GS} = 0 \text{ V, } I_D = 10 \mu\text{A}$	N-Ch	60				
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = -10 \mu\text{A}$	P-Ch	- 60			V	
Cata Thuashald Valtage	Vaam	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	N-Ch	1		2.5		
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA	P-Ch	- 1		- 3.0		
	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{CS} = \pm 5 \text{ V}$	N-Ch			± 50	_	
Gate-Body Leakage			P-Ch			± 100		
Gale-Body Leakage		$V_{DS} = 0 \text{ V}, V_{GS} = \pm 10 \text{ V}$	N-Ch			± 150		
			P-Ch			± 200	nA	
		$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}$	N-Ch			10	- IIA	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = -50 \text{ V}, V_{GS} = 0 \text{ V}$	P-Ch			- 25		
Zero date voltage Brain ourrent	1088	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 85 ^{\circ}\text{C}$	N-Ch			100		
		$V_{DS} = -50 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 85 ^{\circ}\text{C}$	P-Ch			- 250		
		$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}$	N-Ch	500				
On State Drain Currenta	ln()	$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V}$	P-Ch	- 50			mΔ	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} = 7.5 \text{ V}, V_{GS} = -4.5 \text{ V}$	N-Ch	800			mA	
		$V_{DS} = -10 \text{ V}, V_{GS} = -10 \text{ V}$	P-Ch	- 600				
		$V_{GS} = 4.5 \text{ V}, I_D = 200 \text{ mA}$	N-Ch			3	Ω	
		$V_{GS} = -4.5 \text{ V}, I_D = -25 \text{ mA}$	P-Ch			8		
Drain-Source On-State	R _{DS(on)}	$V_{GS} = 10 \text{ V, I}_{D} = 500 \text{ mA}$	N-Ch			1.40		
Resistance ^a		V _{GS} = - 10 V, I _D = - 500 mA	P-Ch			4		
		$V_{GS} = 10 \text{ V}, I_D = 500 \text{ mA}, T_J = 125 ^{\circ}\text{C}$	N-Ch			2.50		
		$V_{GS} = -10 \text{ V}, I_D = -500 \text{ mA}, T_J = 125 ^{\circ}\text{C}$	P-Ch			6		
F	Q.	$V_{DS} = 10 \text{ V, I}_{D} = 200 \text{ mA}$	N-Ch		200		mo	
Forward Transconductance ^a	9 _{fs}	V _{DS} = - 10 V, I _D = - 100 mA	P-Ch		100		- ms	
Diede Fernand Vellere 3	V _{SD}	I _S = 200 mA, V _{GS} = 0 V	N-Ch			1.4	V	
Diode Forward Voltage ^a	V SD	I _S = - 200 mA, V _{GS} = 0 V	P-Ch			- 1.4	V	
Dynamic ^b								
Total Gate Charge	Q_{g}		N-Ch		750		pC	
Total Gate Charge	Сg	N-Channel $V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 250 \text{ mA}$	P-Ch		1700			
Gate-Source Charge	Q_{gs}	V _{DS} = 10 V, V _{GS} = 4.3 V, I _D = 230 IIIA	N-Ch		75			
Gate Course Charge	-gs	P-Channel	P-Ch		260			
Gate-Drain Charge	Q_{qd}	$V_{DS} = -30 \text{ V}, V_{GS} = -15 \text{ V}, I_{D} = -500 \text{ mA}$	N-Ch		225			
	gu		P-Ch		460			
Input Capacitance	C _{iss}	N-Channel	N-Ch		30		pF	
		$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	P-Ch		23			
Output Capacitance	Coss		N-Ch		6			
Reverse Transfer Capacitance	C _{rss}	P-Channel	P-Ch		10			
		$V_{DS} = -25 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	N-Ch P-Ch		3 5	-		
		N-Channel				 		
Turn-On Time ^c	t _{ON}	$V_{DD} = 30 \text{ V}, R_L = 150 \Omega$	N-Ch		15		<u> </u>	
TUTTI TITLE		$I_D \cong 200 \text{ mA}, V_{GEN} = 10 \text{ V}, R_g = 10 \Omega$	P-Ch		20	1	ns	
		P-Channel	N-Ch		20			
Turn-Off Time ^c	t _{OFF}	V_{DD} = - 25 V, R _L = 150 Ω $I_D \cong$ - 165 mA, V_{GEN} = - 10 V, R _g = 10 Ω				1		
		D , GEN,			1	1		

Notes:

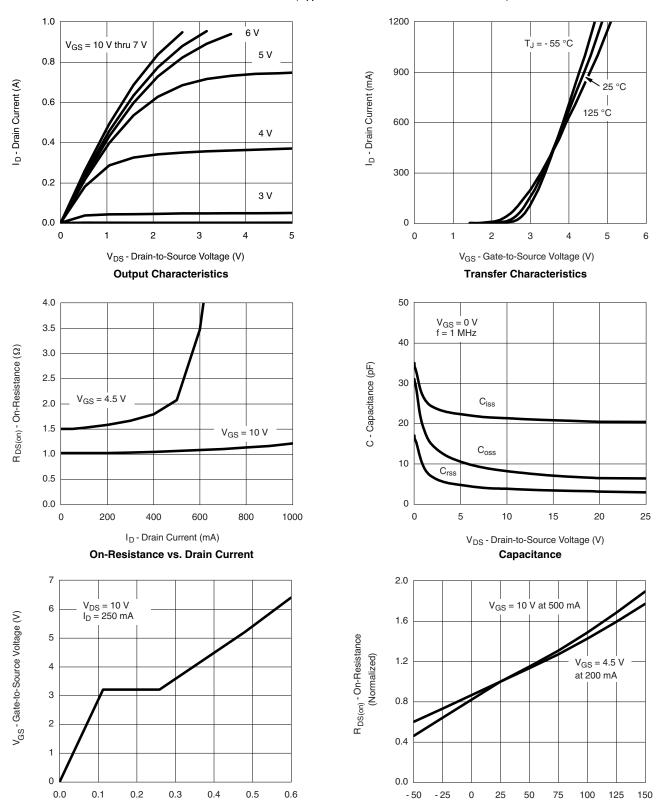
- a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %. b. Guaranteed by design, not subject to production testing.
- c. Switching time is essentially independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.





N-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25 \, ^{\circ}C$, unless otherwise noted)



Q_a - Total Gate Charge (nC)

Gate Charge

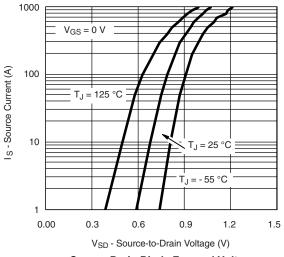
T_J - Junction Temperature (°C)

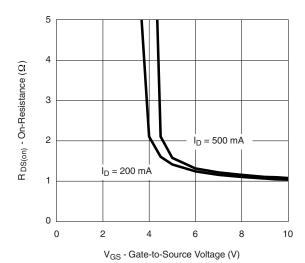
On-Resistance vs. Junction Temperature

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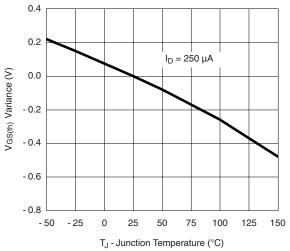
N-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25~^{\circ}C$, unless otherwise noted)



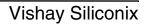


Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

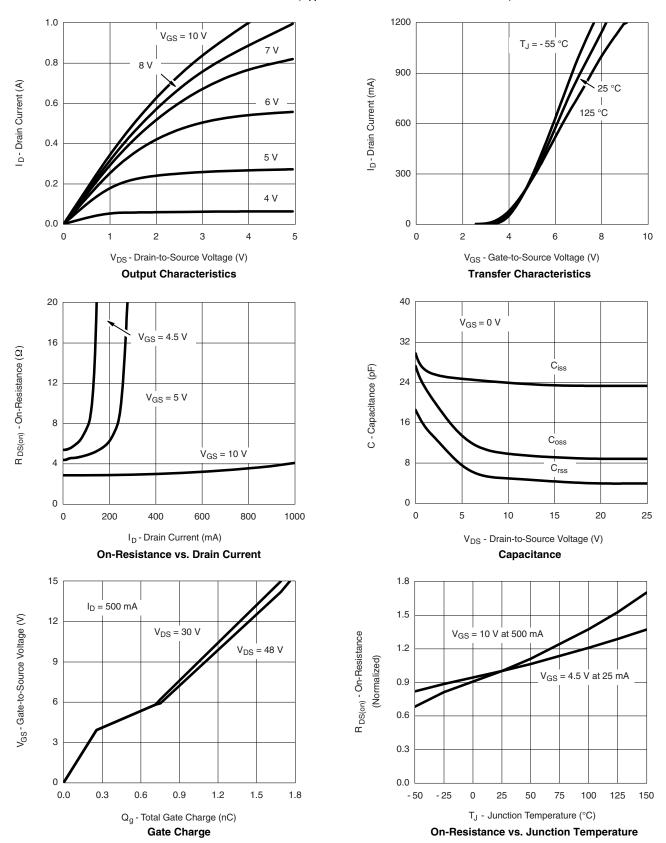


Threshold Voltage Variance Over Temperature





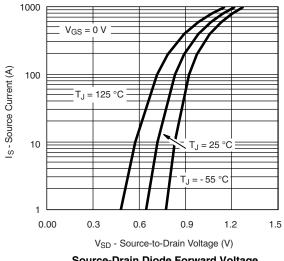
P-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25$ °C, unless otherwise noted)

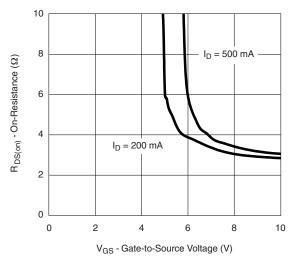


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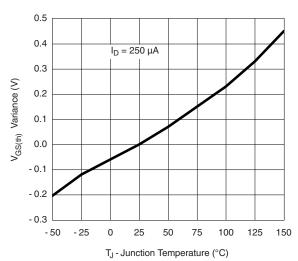
P-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25$ °C, unless otherwise noted)





Source-Drain Diode Forward Voltage

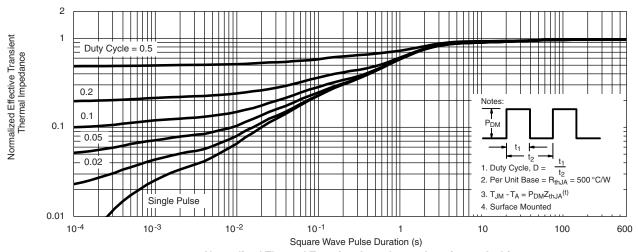
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage Variance Over Temperature



N- OR P-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25~^{\circ}C$, unless otherwise noted)

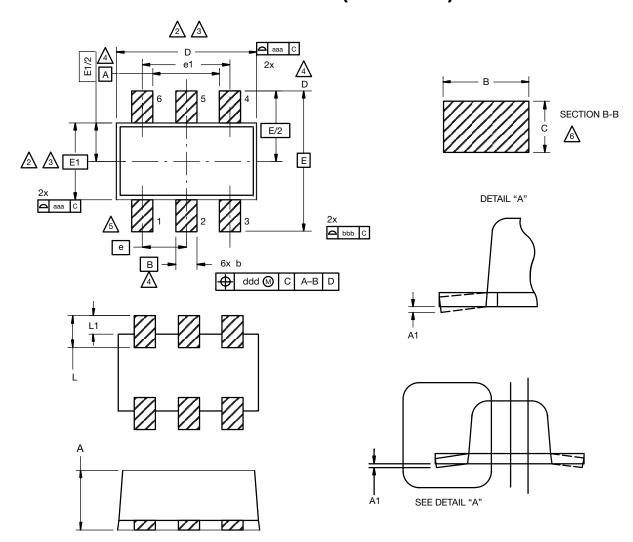


Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71435.



SC-89 6-Leads (SOT-563F)



Notes

1. Dimensions in millimeters.

Dimension D does not include mold flash, protrusions or gate burrs. Mold flush, protrusions or gate burrs shall not exceed 0.15 mm per dimension E1 does not include interlead flash or protrusion, interlead flash or protrusion shall not exceed 0.15 mm per side.

Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, the bar burrs, gate burrs and interlead flash, but including any mismatch between the top and the bottom of the plastic body.

ADatums A, B and D to be determined 0.10 mm from the lead tip.

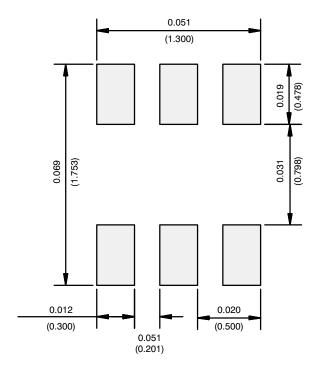
A Terminal numbers are shown for reference only.

These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.

DIM.		MILLIMETERS		
DIIVI.	MIN.	NOM.	MAX.	
Α	0.56	0.58	0.60	
A1	0	0.02	0.10	
b	0.15	0.22	0.30	
С	0.10	0.14	0.18	
D	1.50	1.60	1.70	
E	1.50	1.60	1.70	
E1	1.15	1.20	1.25	
е	0.45	0.50	0.55	
e1	0.95	1.00	1.05	
L	0.25	0.35	0.50	
L1	0.10	0.20	0.30	
C14-0439-Rev. C, 11-Aug-14 DWG: 5880				



RECOMMENDED MINIMUM PADS FOR SC-89: 6-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as RoHS-Compliant fulfill the definitions and restrictions defined under Directive 2011/65/EU of The European Parliament and of the Council of June 8, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (EEE) - recast, unless otherwise specified as non-compliant.

Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.

Revision: 02-Oct-12 Document Number: 91000

AMEYA360 Components Supply Platform

Authorized Distribution Brand:

























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