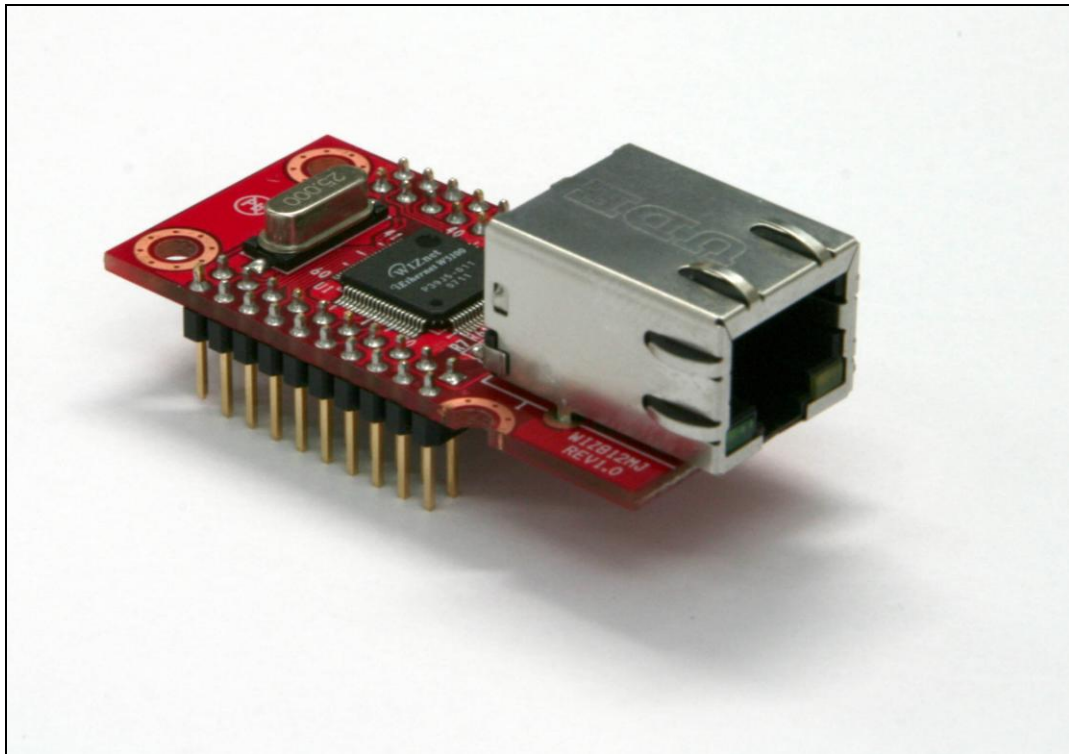


WIZ812MJ Datasheet

(Ver. 1.1)



Document History Information

| Revision | Date | Description |
|----------|--------------------|---------------------------------|
| Ver. 1.0 | September 17, 2008 | Release with WIZ812MJ Launching |
| Ver. 1.1 | January 28, 2009 | Added temperature specification |

WIZnet's Online Technical Support

If you have something to ask about WIZnet Products, Write down your question on Q&A Board in WIZnet website (www.wiznet.co.kr). WIZnet Engineer will give an answer as soon as possible.

The screenshot shows the WIZnet website interface. At the top, there is a navigation bar with links for HOME, LOGIN, JOIN, CONTACT US, and language options (ENGLISH, CHINESE, JAPANESE, KOREAN). A dropdown menu for 'On-line Mail' is also visible. The main content area includes a 'PRODUCTS' sidebar, a 'NEW PRODUCT' section for the W5300 chip (highlighted with a red box), and a 'Q&A' section. The Q&A section features a sidebar with 'Q&A', 'FAQ', and 'E-FORUM' options, and a main area with a list of questions and answers. A red box highlights the 'Q&A' link in the top navigation bar and the 'Q&A' sidebar link.

NEW PRODUCT

W5300

- Over 50 Mbps!
- 16/8 bit data bus width
- 8 independent sockets
- Also, support SWTCP/IP simultaneously thru.

WHAT'S UPDATED

- How to use PPPoE in W5300 08-05-28
- WIZ1x0SR Firmware V2.9 08-05-28
- W5300 Driver Document 08-05-28
- W5300 Driver V1.01 08-05-28
- W5300 Reference Schematic 08-05-28

Q&A

if you want to know about WIZnet we will inform you.

Total : 2315 (1/116)

| NO | SUBJECT | NAME | DATE | HIT |
|------|--|-----------------------|------------|-----|
| 2315 | How to initialization TX_WR Pointer | Andria Ginting | 2008-05-19 | 30 |
| 2314 | ASRB-US8 W3150A* | DOUG KHAN | 2008-05-17 | 23 |
| 2313 | re:ASRB-US8 W3150A* | WIZnet | 2008-05-21 | 3 |
| 2312 | W5300 - Driver (Send function) | Ari Mendes dos Santos | 2008-05-16 | 36 |
| 2311 | why RX_WR_POINTER not return to zero | harry | 2008-05-14 | 34 |
| 2310 | UDP: Sn_RX_WR bug in W3150 | Alex | 2008-05-13 | 46 |
| 2309 | UPDATE!!! UDP ERROR | Alex | 2008-05-14 | 50 |
| 2308 | recv size register does not return to .. | HARRY | 2008-05-13 | 30 |
| 2307 | re:recv size register does not return .. | WIZnet | 2008-05-21 | 4 |

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1. Introduction

WIZ812MJ is the network module that includes W5100 (TCP/IP hardwired chip, include PHY), MAG-JACK (RJ45 with X'FMR) with other glue logics. It can be used as a component and no effort is required to interface W5100 and Transformer. The WIZ812MJ is an ideal option for users who want to develop their Internet enabling systems rapidly.

For the detailed information on implementation of Hardware TCP/IP, refer to the W5100 Datasheet.

WIZ812MJ consists of W5100 and MAG-JACK.

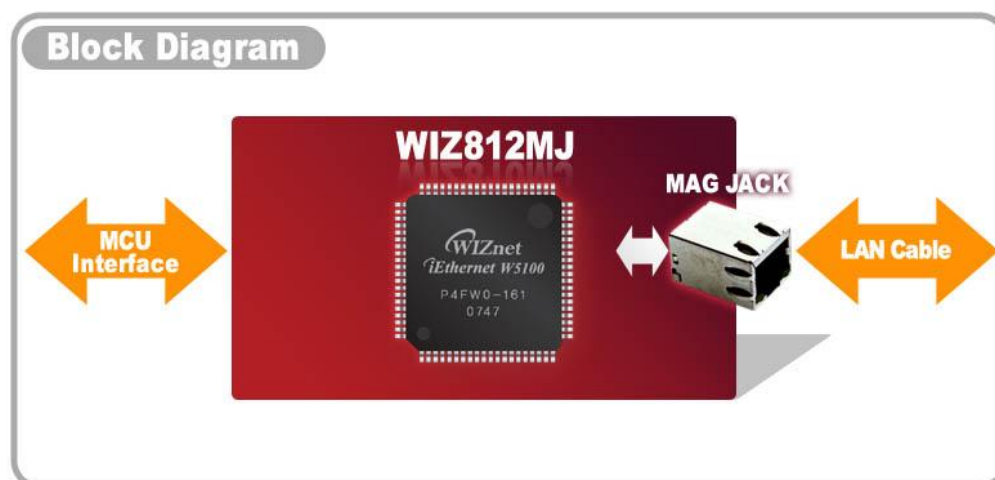
- TCP/IP, MAC protocol layer: W5100
- Physical layer: Included in W5100
- Connector: MAG-JACK(RJ45 with Transformer)

5


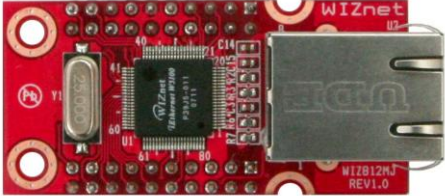
1.1. Features

- Supports 10/100 Base TX
- Supports half/full duplex operation
- Supports auto-negotiation and auto cross-over detection
- IEEE 802.3/802.3u Compliance
- Operates 3.3V with 5V I/O signal tolerance
- Supports network status indicator LEDs
- Includes Hardware Internet protocols: TCP, IP Ver.4, UDP, ICMP, ARP, PPPoE, IGMP
- Includes Hardware Ethernet protocols: DLC, MAC
- Supports 4 independent connections simultaneously
- Supports MCU bus Interface and SPI Interface
- Supports Direct/Indirect mode bus access
- Supports Socket API for easy application programming
- Interfaces with two 2.54mm pitch 2 x 10 header pin
- Temperature : 0 ~ 70°C (Operation), -40 ~ 85°C (Storage)

1.2. Block Diagram

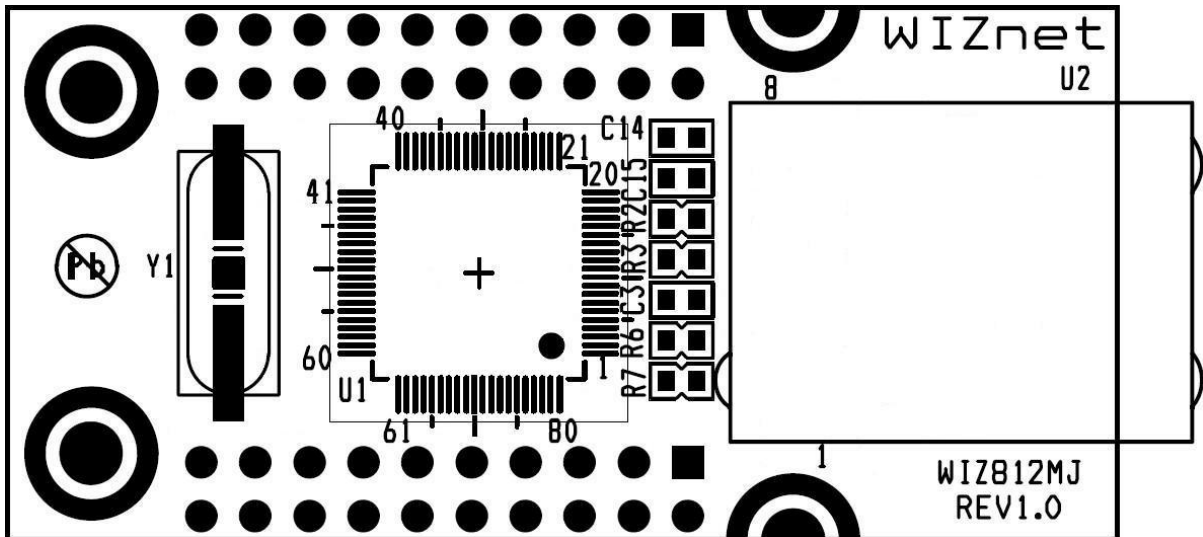


1.3. Difference between WIZ811MJ and WIZ812MJ

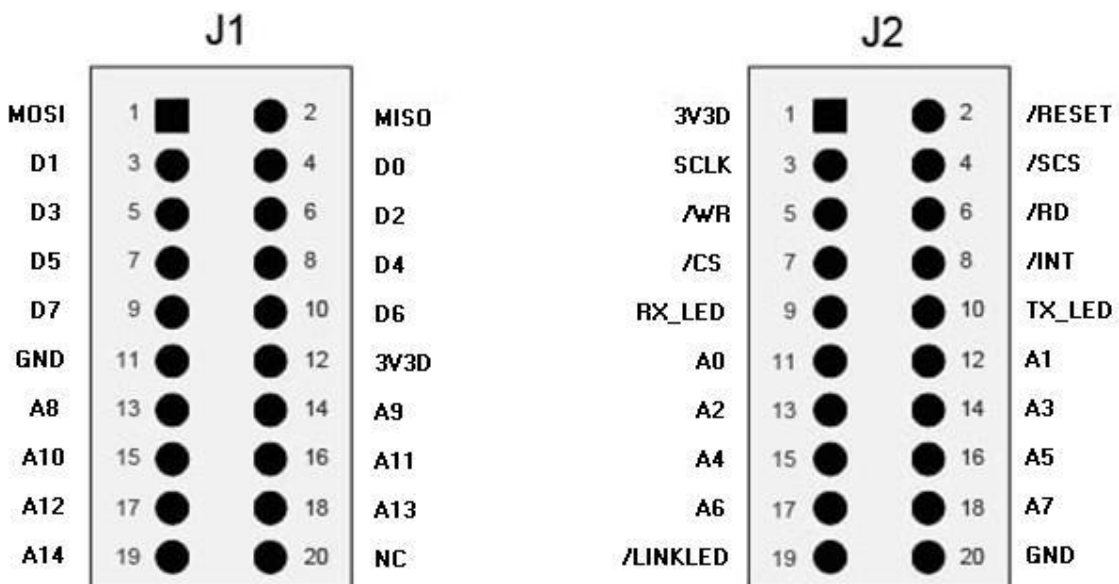
| WIZ811MJ | WIZ812MJ |
|---|---|
|  |  |
| <p>Two 2.54mm pitch 10x2 header</p> | <p>The same pin-header is mounted but pin description is different J2:9 GND -> RX_LED J2:10 GND -> TX_LED J2:19 GND -> /LINKLED</p> |
| <p>Two PCB Through Hole(Ø3.00mm)</p> | <p>Four PCB Through Hole(Ø3.00mm)</p> |
| <p>55.5 x 25 x 23.5mm (W x H x D)</p> | <p>The same size</p> |
| <p>LINKLED : Active low in link state indicates a good status for 10/100M. It is always ON when the link is OK and it flashes while in a TX or RX state.</p> | <p>/LINKLED : Active low in link state indicates a good status for 10/100M. It is always ON when the link is OK. It does not flashes while in a TX or RX state.</p> |
| | <p>ACT_LED : Active low in active state indicates a good status for 10/100M. It is always ON when the link is OK and it flashes while in a TX or RX state.</p> |

2. Pin Assignments & descriptions

2.1. Pin Assignments



7



I : Input
I/O : Bi-directional Input and output

O : Output
P : Power

2.2. Power & Ground

| Symbol | Type | Pin No. | Description |
|--------|------|--------------|----------------------------|
| 3V3D | P | J1:12 , J2:1 | Power : 3.3 V power supply |
| GND | P | J1:11, J2:20 | Ground |

8

2.3. MCU Interfaces

| Symbol | Type | Pin No. | Description |
|--------|------|---------------|--|
| SCLK | I | J2:3 | SCLK(Serial Clock) This pin is used to SPI Clock Signal pin. |
| /SCS | I | J2:4 | /SCS (Slave Select) * This pin is used to SPI Slave Select signal Pin. This pin controls SPI_EN signal of W5100. When /SCS signal assert low, W5100 drive SPI mode by SPI_EN signal toggled high. |
| MOSI | I | J1:1 | MOSI (Master Out Slave In) * This pin is used to SPI MOSI signal pin. |
| MISO | I/O | J1:2 | MISO (Master In Slave Out) * This pin is used to SPI MISO signal pin. |
| A14~A8 | I | J1:13 ~ J1:19 | Address Used as Address[14-8] pin |
| A7~A0 | I | J2:11 ~ J2:18 | Address Used as Address[7-0] pin |
| D7~D0 | I/O | J1:3 ~ J1:10 | Data 8 bit-wide data bus |
| /CS | I | J2:7 | Module Select : Active low. /CS of W5100 |
| /RD | I | J2:6 | Read Enable : Active low. /RD of W5100 |
| /WR | I | J2:5 | Write Enable : Active low /WR of W5100 |
| /INT | O | J2:8 | Interrupt : Active low After reception or transmission it indicates that the W5100 requires MCU attention. By writing values to the Interrupt Status Register of W5100 the interrupt will be cleared. All interrupts can be masked by writing values to the IMR of W5100 (Interrupt Mask Register). For more details refer to the W5100 Datasheet |

2.4. Miscellaneous Signals

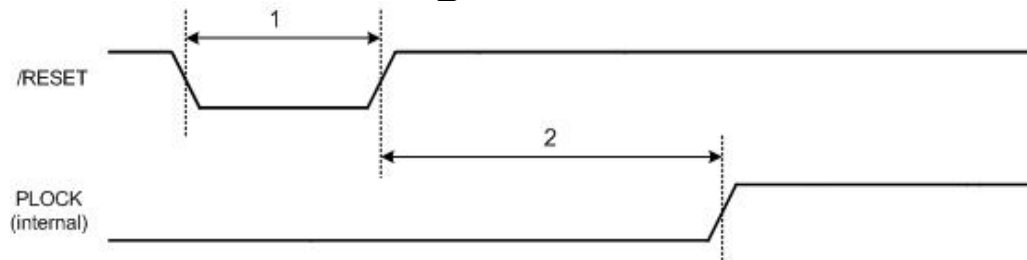
| Symbol | Type | Pin No. | Description |
|-----------------|----------|---------|---|
| /RESET | I | J2:2 | Reset : This pin is active low input to initialize or re-initialize W5100. By asserting this pin low for at least 2us, all internal registers will be re-initialized to their default states. |
| RX_LED | O | J2:9 | RX_LED : Receive activity LED Active low indicates the presence of receiving activity. |
| TX_LED | O | J2:10 | TX_LED : Transmit activity LED Active low indicates the presence of transmitting activity. |
| /LINKLED | O | J2:19 | LINKLED : Active low in link state indicates a good status for 10/100M. It is always ON when the link is OK. It does not flashes while in a TX or RX state. |
| NC | - | J1 : 20 | Not Connect |

3. Timing Diagrams

WIZ812MJ provides following interfaces of W5100.

- Direct/Indirect mode bus access
- SPI access

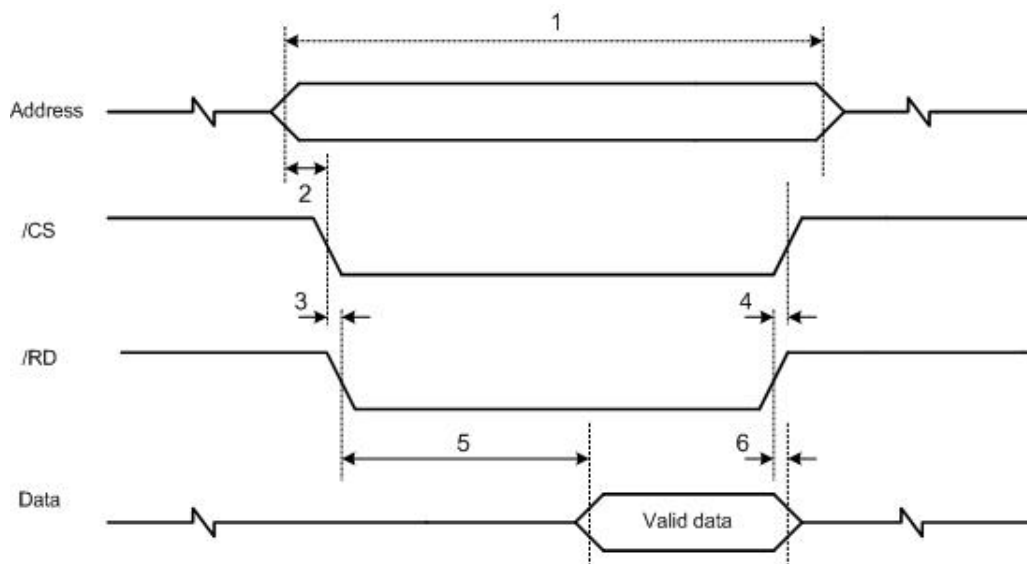
3.1. Reset Timing



| Description | | Min | Max |
|-------------|--------------------------|------|-------|
| 1 | Reset Cycle Time | 2 us | - |
| 2 | /RESET to internal PLOCK | - | 10 ms |

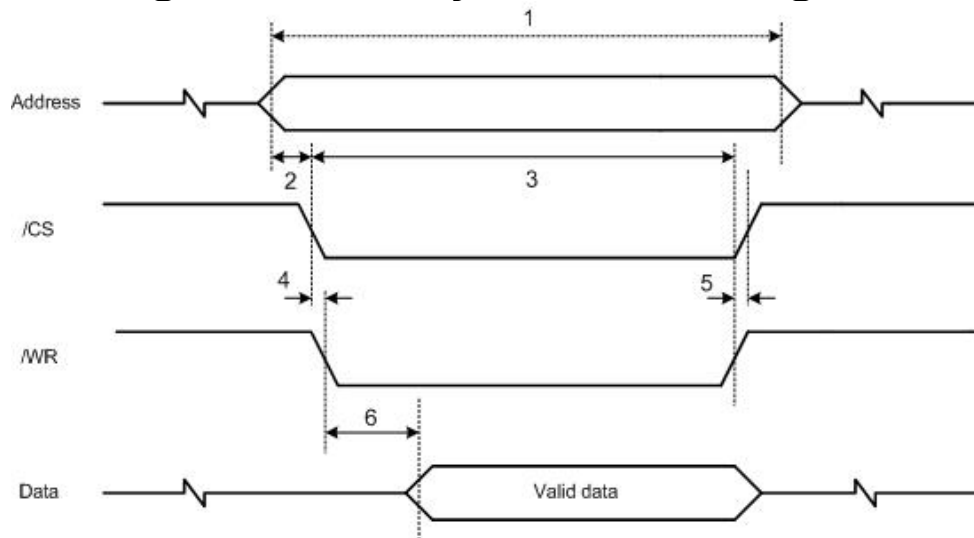
10

3.2. Register/Memory READ Timing



| Description | | Min | Max |
|-------------|-------------------------------------|-------|-------|
| 1 | Read Cycle Time | 80 ns | - |
| 2 | Valid Address to /CS low time | 8 ns | - |
| 3 | /CS low to /RD low time | - | 1 ns |
| 4 | /RD high to /CS high time | - | 1 ns |
| 5 | /RD low to Valid Data Output time | - | 80 ns |
| 6 | /RD high to Data High-Z Output time | - | 1 ns |

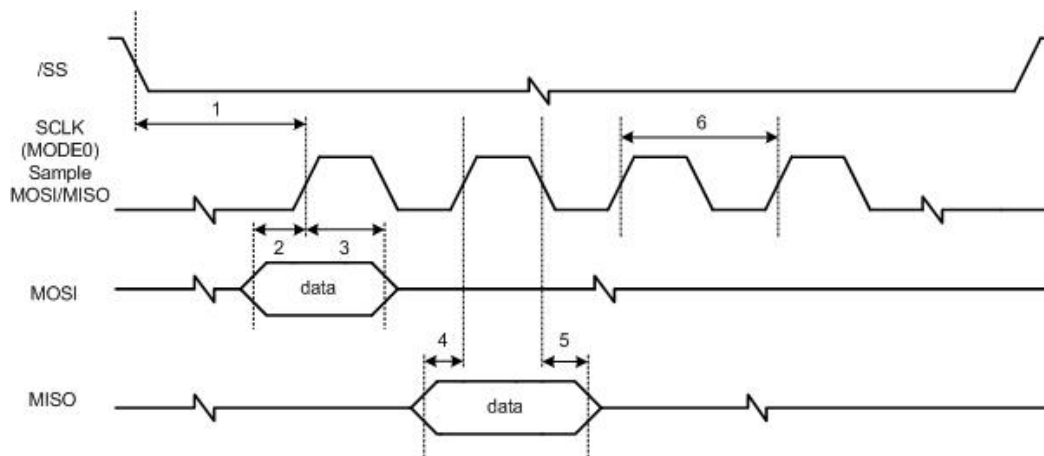
3.3. Register/Memory WRITE Timing



11

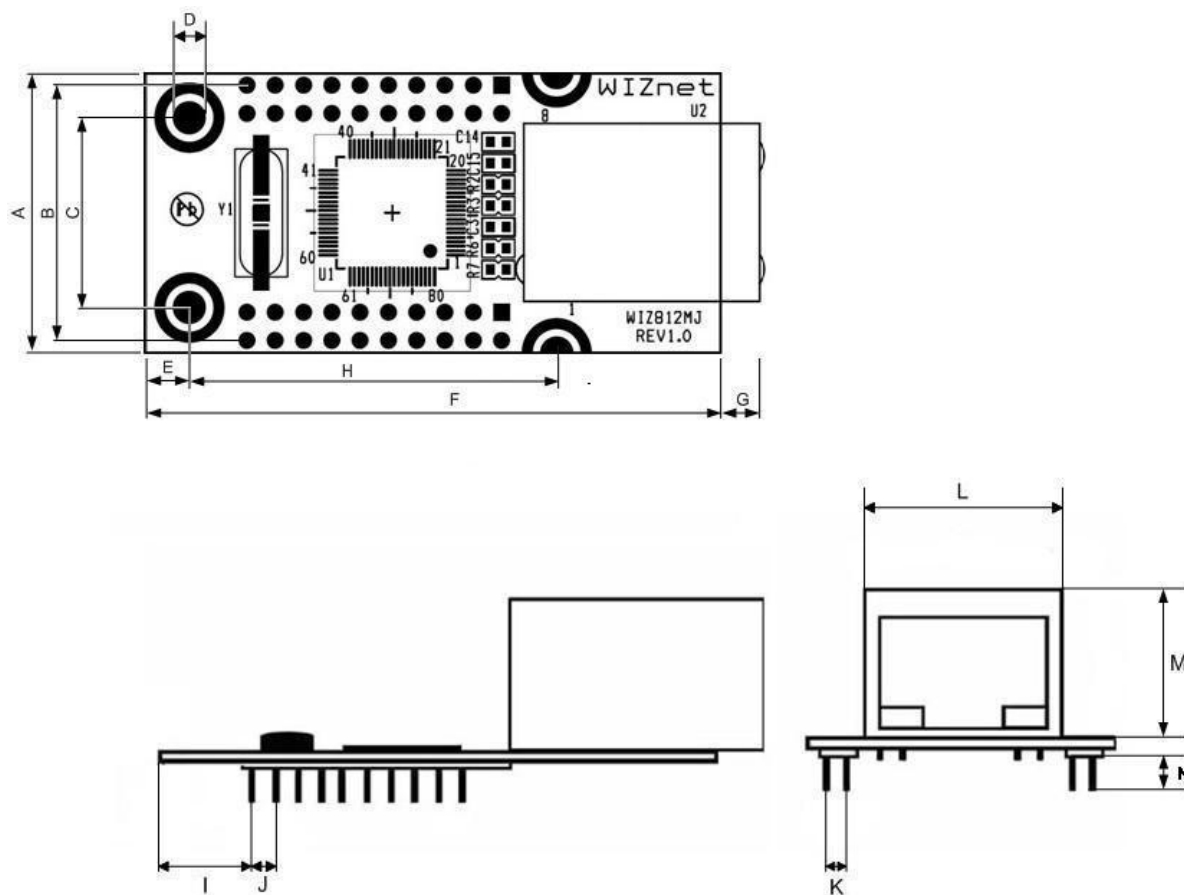
| Description | | Min | Max |
|-------------|-------------------------------|-------|-------|
| 1 | Write Cycle Time | 70 ns | - |
| 2 | Valid Address to /CS low time | 7 ns | - |
| 3 | /CS low to /WR high time | 70 ns | - |
| 4 | /CS low to /WR low time | - | 1 ns |
| 5 | /WR high to /CS high time | - | 1 ns |
| 6 | /WR low to Valid Data time | - | 14 ns |

3.4. SPI Timing



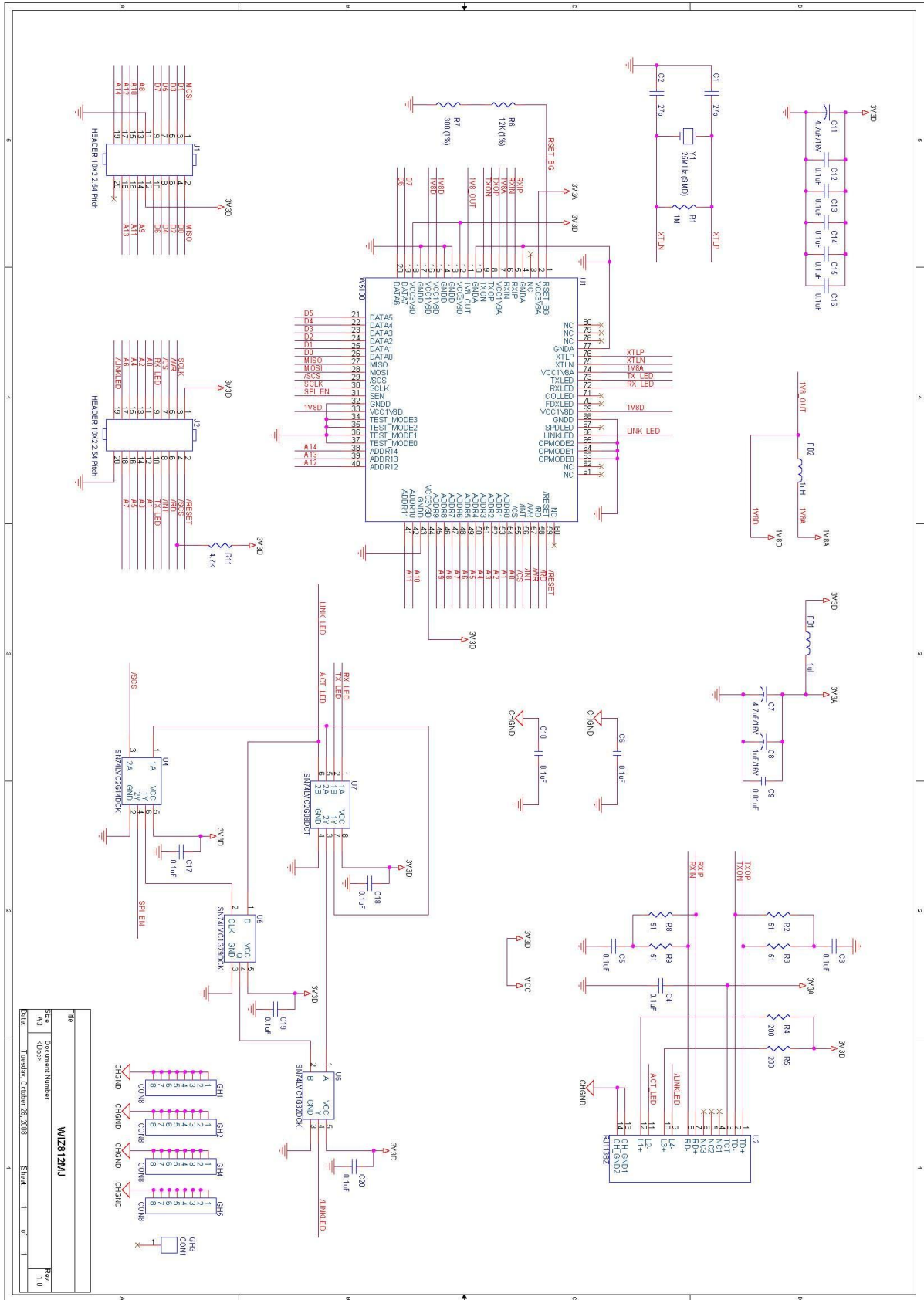
| Description | Mode | Min | Max |
|---------------------|-------|-------|-------|
| 1 /SS low to SCLK | Slave | 21 ns | - |
| 2 Input setup time | Slave | 7 ns | - |
| 3 Input hold time | Slave | 28 ns | - |
| 4 Output setup time | Slave | 7 ns | 14 ns |
| 5 Output hold time | Slave | 21 ns | - |
| 6 SCLK time | Slave | 70 ns | |

4. Dimensions



| Symbols | Dimensions (mm) |
|---------|-----------------|
| A | 25.00 |
| B | 22.86 |
| C | 17.00 |
| D | 3.00 |
| E | 4.00 |
| F | 52.00 |
| G | 3.20 |
| H | 33.02 |
| I | 9.00 |
| J | 2.54 |
| K | 2.54 |
| L | 15.90 |
| M | 13.50 |
| N | 6.00 |

5. Schematic



| Part Number | Quantity | Unit Price |
|-------------|----------|------------|
| WIZ812MJ | 1 | \$1.00 |

WIZ812MJ
Rev 1.0
January, October 26, 2008

6. Partlist

| Item | Q.ty | Reference | Part | Tech. Characteristics | Package |
|------|------|--|---------------------------------------|-------------------------------------|---------------|
| 1 | 2 | C1,C2 | 27pF | 50V-20% Ceramic | CASE 0603 |
| 2 | 14 | C3,C4,C5,C6, C10,C12,C13 ,C14,C15,16, C17,C18,C19 ,C20 | 0.1uF | 50V-20% Ceramic | CASE 0603 |
| 3 | 2 | C7,C11 | 4.7uF/16V | 16Vmin 10% | EIA/IECQ 3216 |
| 4 | 1 | C8 | 1uF/16V | 16Vmin 10% | EIA/IECQ 3216 |
| 5 | 1 | C9 | 0.01uF | 50V-20% Ceramic | CASE 0603 |
| 6 | 2 | FB2,FB1 | 1uH Chip Ferrite Inductor | 1uH, 50mA | CASE 0805 |
| 7 | 2 | J1,J2 | 2X10 20PIN 2.54mm DIP STRAIGHT Header | 2 X 10 2.54mm pitch | |
| 8 | 1 | R1 | 1M | 1/10W-5% SMD | CASE 0603 |
| 9 | 4 | R2,R3,R8,R9 | 51 1% | 1/10W-1% SMD | CASE 0603 |
| 10 | 2 | R4,R5 | 200 | 1/10W-5% SMD | CASE 0603 |
| 11 | 1 | R6 | 12K (1%) | 1/10W-1% SMD | CASE 0603 |
| 12 | 1 | R7 | 300 (1%) | 1/10W-1% SMD | CASE 0603 |
| 13 | 1 | R11 | 4.7K | 1/10W-5% SMD | CASE 0603 |
| 14 | 1 | U1 | W5100 | WIZnet Hardware TCP/IP | LQFP80 |
| 15 | 1 | U2 | RJ113BZ | Transformer + RJ45 | |
| 16 | 1 | U4 | SN74LVC2G14DCK | Dual Inverting Buffer (vendor : TI) | SC70-6 |
| 17 | 1 | U5 | SN74LVC1G79DCK | D-type Flip Flop (vendor : TI) | SC70-5 |
| 18 | 1 | U6 | SN74LVC1G32DCK | OR-Gate (vendor : TI) | SC70-5 |
| 19 | 1 | U7 | SN74LVC2G08DCT | Dual AND-Gate (vendor : TI) | SM8 |
| 20 | 1 | Y1 | 25MHz (SMD) | SMD Type | SX-1 |
| 21 | 1 | | WIZ812MJ REV1.0 1.6T 4LAYER | PRINTED CIRCUIT BOARD | |

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