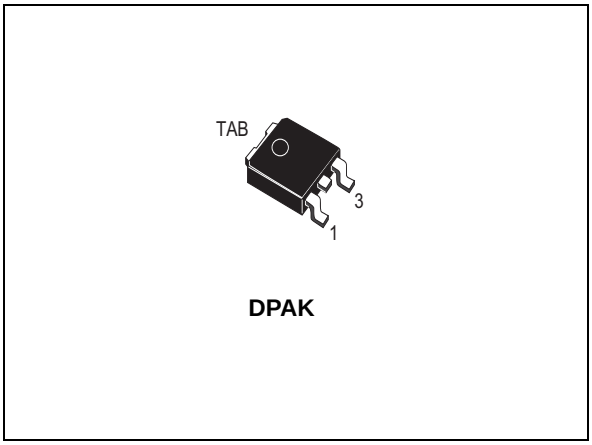
# STD12NF06LT4

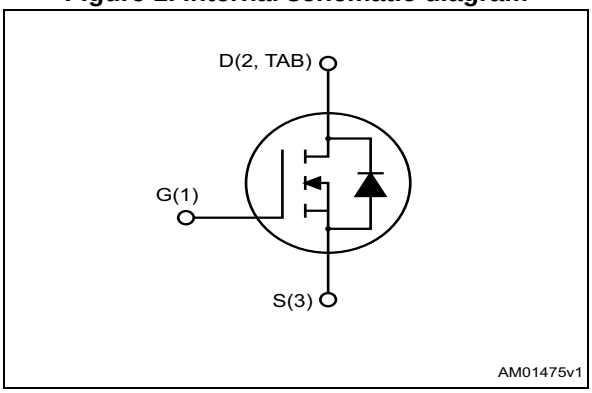
## Automotive-grade N-channel 60 V, 0.07 Ω typ., 12 A, StripFET™ II Power MOSFET in a DPAK package

**Datasheet - production data**




**DPAK**

**Figure 1. Internal schematic diagram**




## Features

| Order code | $V_{DS}$ | $R_{DS(on)}$ max. | $I_D$ |
|---|---|---|---|
| STD12NF06LT4 | 60 V | 0.09 Ω | 12 A |

- Designed for automotive applications and AEC-Q101 qualified
- Exceptional dv/dt capability
- Low gate charge

## Applications

- Switching applications

## Description

This Power MOSFET has been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

**Table 1. Device summary**

| Order code | Marking | Package | Packaging |
|---|---|---|---|
| STD12NF06LT4 | D12NF06L | DPAK | Tape and reel |

# Contents

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain-source voltage | 60 | V |
| $V_{GS}$ | Gate-source voltage | ± 16 | V |
| $I_D$ | Drain current (continuous) at $T_C$ = 25 °C | 12 | A |
| $I_D$ | Drain current (continuous) at $T_C$= 100 °C | 8.5 | A |
| $I_{DM}$(1) | Drain current (pulsed) | 48 | A |
| $P_{TOT}$ | Total dissipation at $T_C$ = 25 °C | 30 | W |
| | Derating factor | 0.2 | W/°C |
| dv/dt(2) | Peak diode recovery voltage slope | 15 | V/ns |
| $E_{AS}$(3) | Single pulse avalanche energy | 100 | mJ |
| $T_{stg}$ | Storage temperature | -55 to 175 | °C |
| $T_J$ | Max. operating junction temperature | | |

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 12$ A, di/dt $\leq 200$ A/µs, $V_{DS} \leq 40$ V, $T_J \leq T_{JMAX}$
3. Starting $T_J$ = 25 °C, $I_D$ = 6 A, $V_{DD}$ = 30 V

**Table 3. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thj\text{-}case}$ | Thermal resistance junction-case max. | 5 | °C/W |
| $R_{thj\text{-}pcb}$(1) | Thermal resistance junction-pcb max. | 50 | °C/W |

1. When mounted on FR-4 board of 1 inch², 2 oz Cu.

# 2 Electrical characteristics

($T_{CASE}$ = 25 °C unless otherwise specified)

**Table 4. On/off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS}$ = 0, $I_D$ = 250 µA, | 60 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current | $V_{GS}$ = 0, $V_{DS}$ = 60 | | | 1 | µA |
| | | $V_{GS}$ = 0, $V_{DS}$ = 60<br>$T_C$ = 125 °C | | | 10 | µA |
| $I_{GSS}$ | Gate body leakage current | $V_{DS}$ = 0<br>$V_{GS}$ = ± 16 V | | | ±100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 1 | | 2 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS}$ = 10 V, $I_D$ = 6 A | | 0.07 | 0.09 | Ω |
| | | $V_{GS}$ = 5 V, $I_D$ = 6 A | | 0.08 | 0.1 | Ω |

**Table 5. Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input capacitance | $V_{DS}$ = 25 V, f = 1 MHz,<br>$V_{GS}$ = 0 | | 350 | | pF |
| $C_{oss}$ | Output capacitance | | | 75 | | pF |
| $C_{rss}$ | Reverse transfer capacitance | | | 30 | | pF |
| $Q_g$ | Total gate charge | $V_{DD}$ = 48 V, $I_D$ = 12 A<br>$V_{GS}$ = 5 V<br>see *Figure 14* | | 7.5 | 10 | nC |
| $Q_{gs}$ | Gate-source charge | | | 2.5 | | nC |
| $Q_{gd}$ | Gate-drain charge | | | 3.0 | | nC |

**Table 6. Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}$ = 30 V, $I_D$ = 6 A,<br>$R_G$ = 4.7 Ω, $V_{GS}$ = 4.5 V<br>see *Figure 13* | | 10 | | ns |
| $t_r$ | Rise time | | | 35 | | ns |
| $t_{d(off)}$ | Turn-off delay time | | | 20 | | ns |
| $t_f$ | Fall time | | | 13 | | ns |

**Table 7. Source-drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain current | | | | 12 | A |
| $I_{SDM}$ (1) | Source-drain current (pulsed) | | | | 48 | A |
| $V_{SD}$ (2) | Forward on voltage | $I_{SD}$ = 12 A, $V_{GS}$ = 0 | | | 1.5 | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 12 A, di/dt = 100 A/µs, $V_{DD}$ = 16 V, $T_J$ = 150 °C see *Figure 15* | | 50 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | | 65 | | nC |
| $I_{RRM}$ | Reverse recovery current | | | 2.5 | | A |

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

**Figure 2. Safe operating area**

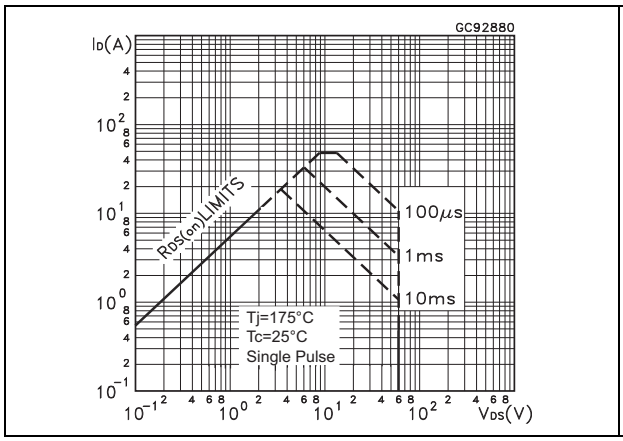



**Figure 3. Thermal impedance**

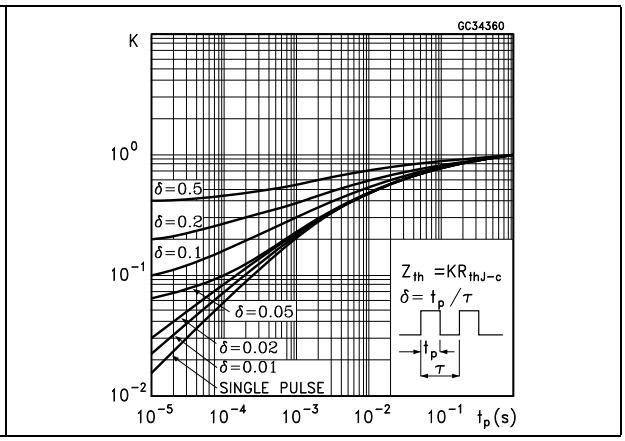



**Figure 4. Output characteristics**

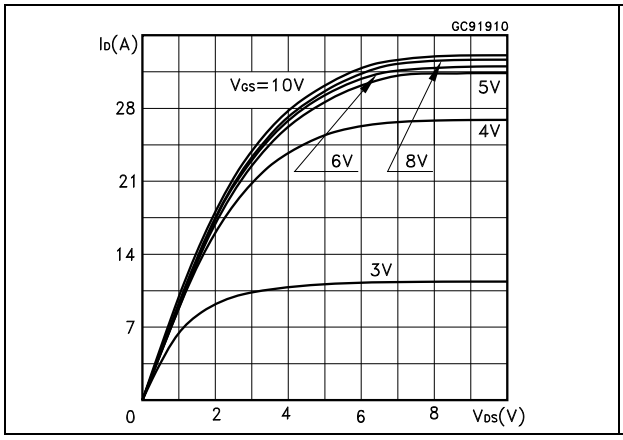



**Figure 5. Transfer characteristics**

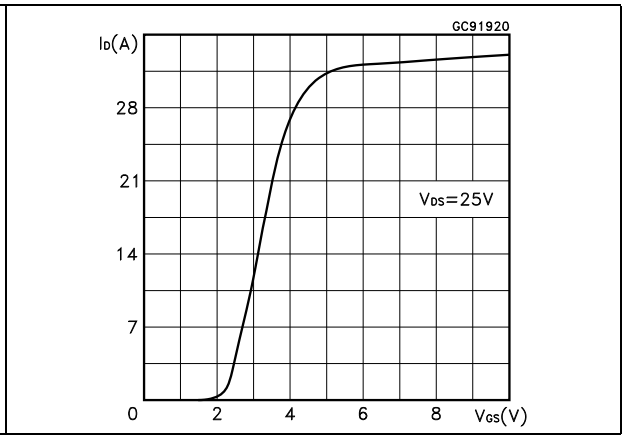



**Figure 6. Normalized $V_{(BR)DSS}$ vs. temperature**

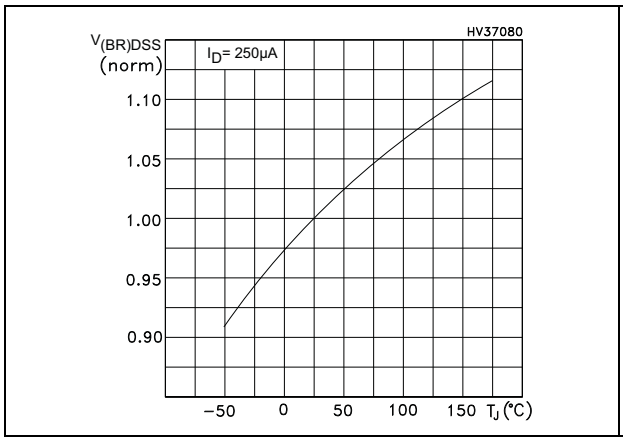



**Figure 7. Static drain-source on-resistance**

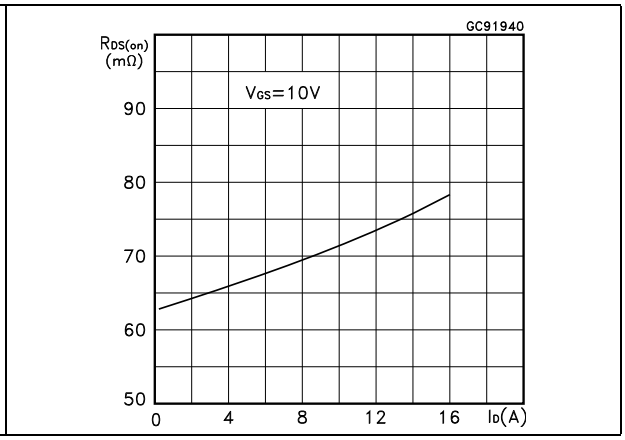


**Figure 8. Gate charge vs. gate-source voltage**

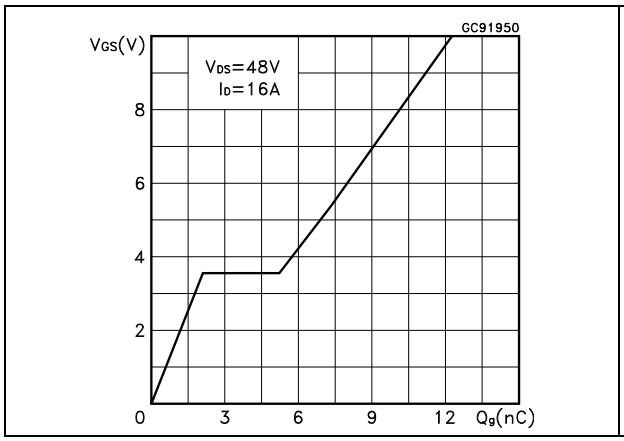



**Figure 9. Capacitance variations**

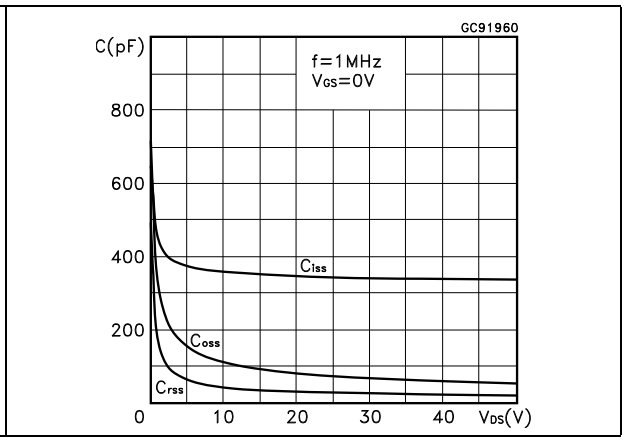



**Figure 10. Normalized gate threshold voltage vs. temperature**

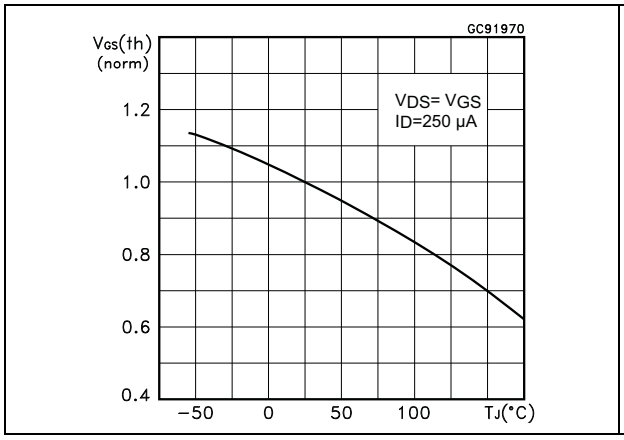



**Figure 11. Normalized on-resistance vs. temperature**

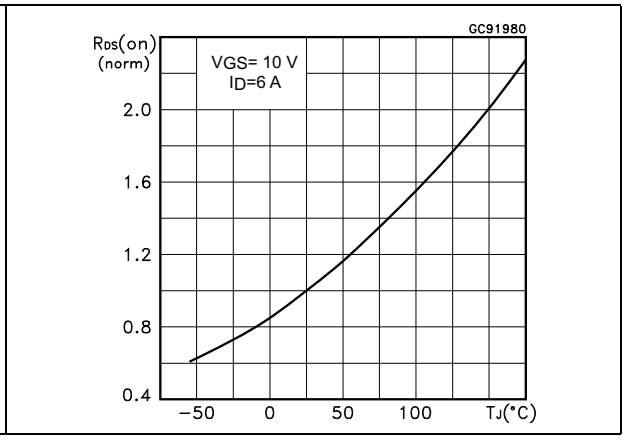
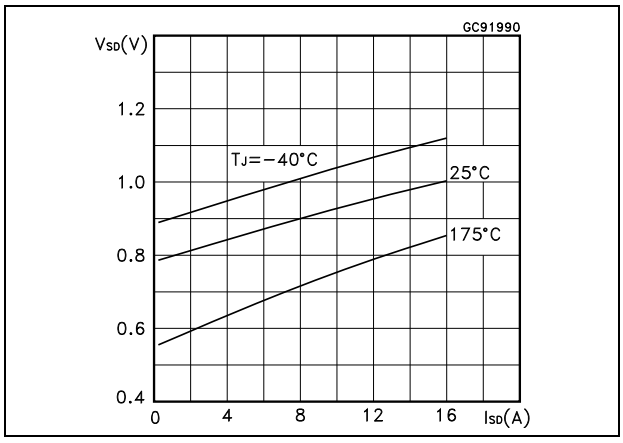



**Figure 12. Source-drain diode forward characteristics**



# 3 Test circuit

**Figure 13. Switching times test circuit for resistive load**

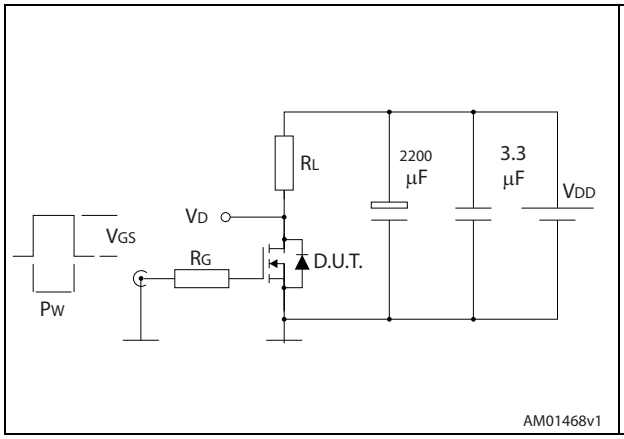



**Figure 14. Gate charge test circuit**

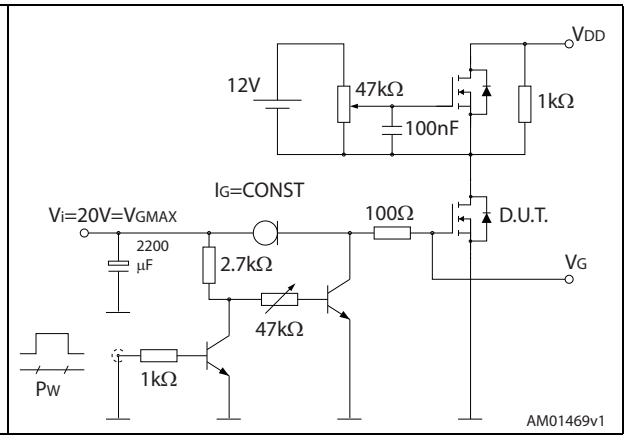



**Figure 15. Test circuit for inductive load switching and diode recovery times**

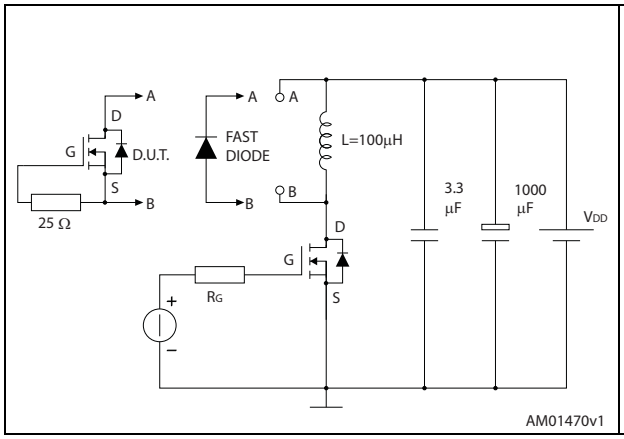



**Figure 16. Unclamped inductive load test circuit**

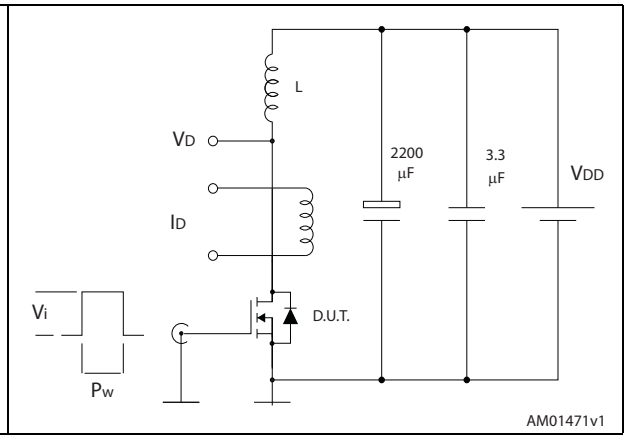



**Figure 17. Unclamped inductive waveform**

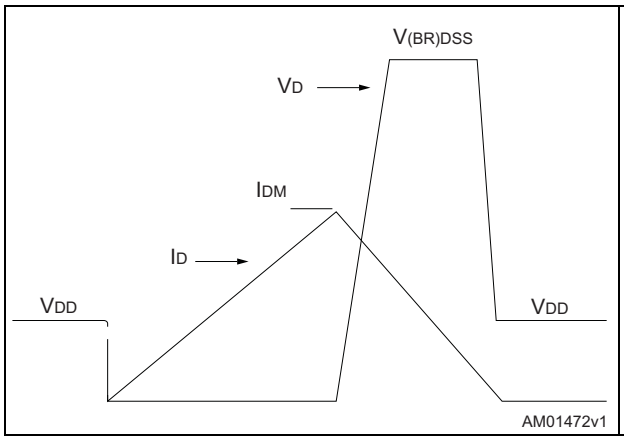
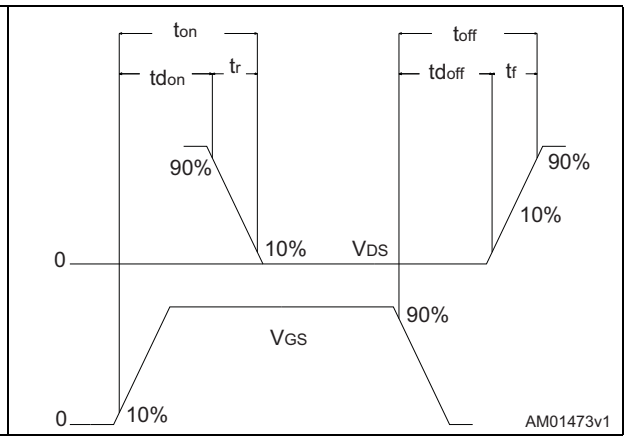



**Figure 18. Switching time waveform**



# 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 19. DPAK (TO-252) type A drawings

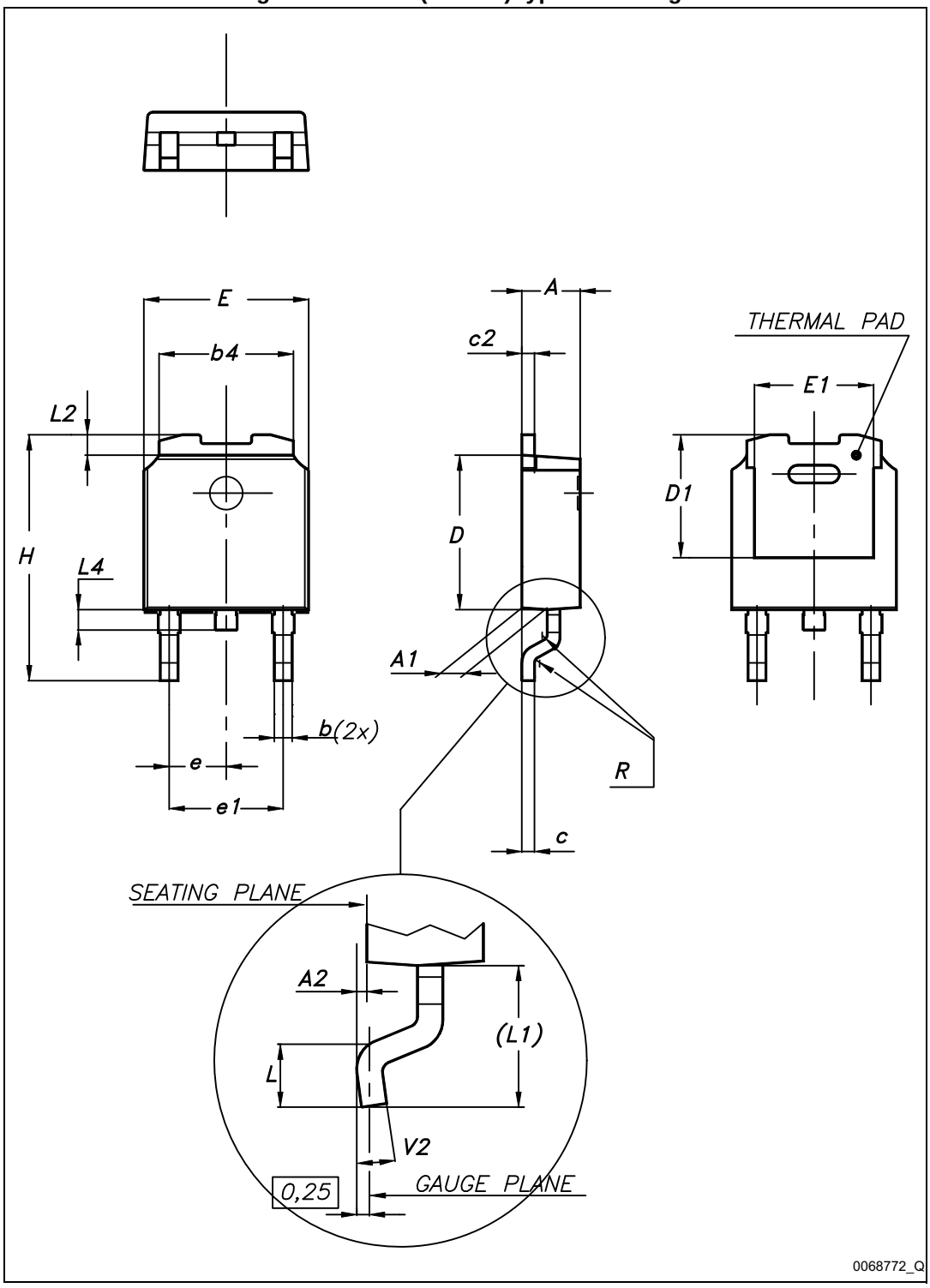
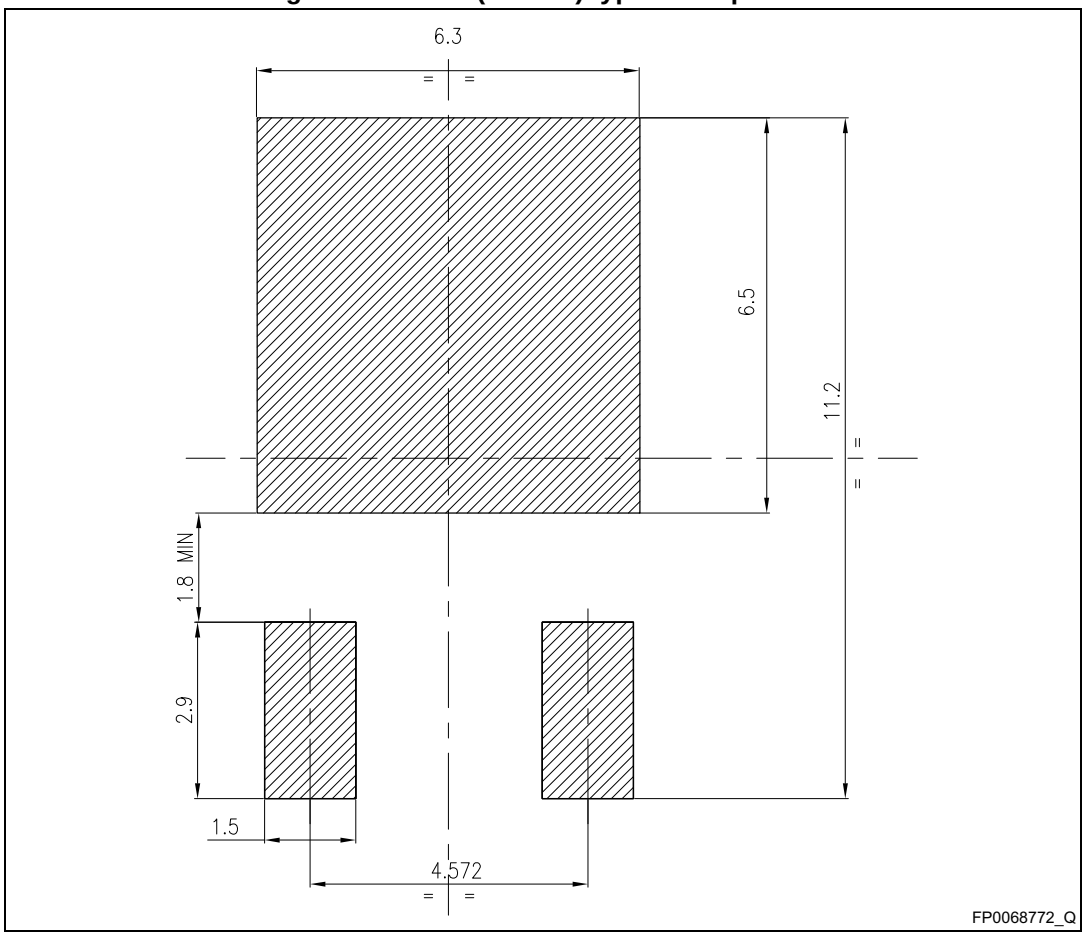


Table 8. DPAK (TO-252) type A mechanical data

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 2.20 | | 2.40 |
| A1 | 0.90 | | 1.10 |
| A2 | 0.03 | | 0.23 |
| b | 0.64 | | 0.90 |
| b4 | 5.20 | | 5.40 |
| c | 0.45 | | 0.60 |
| c2 | 0.48 | | 0.60 |
| D | 6.00 | | 6.20 |
| D1 | | 5.10 | |
| E | 6.40 | | 6.60 |
| E1 | | 4.70 | |
| e | | 2.28 | |
| e1 | 4.40 | | 4.60 |
| H | 9.35 | | 10.10 |
| L | 1.00 | | 1.50 |
| L1 | | 2.80 | |
| L2 | | 0.80 | |
| L4 | 0.60 | | 1.00 |
| R | | 0.20 | |
| V2 | 0° | | 8° |

**Figure 20. DPAK (TO-252) type A footprint [(a)]**




a. All dimensions are in millimeters

# 5 Packaging mechanical data

**Figure 21. Tape**

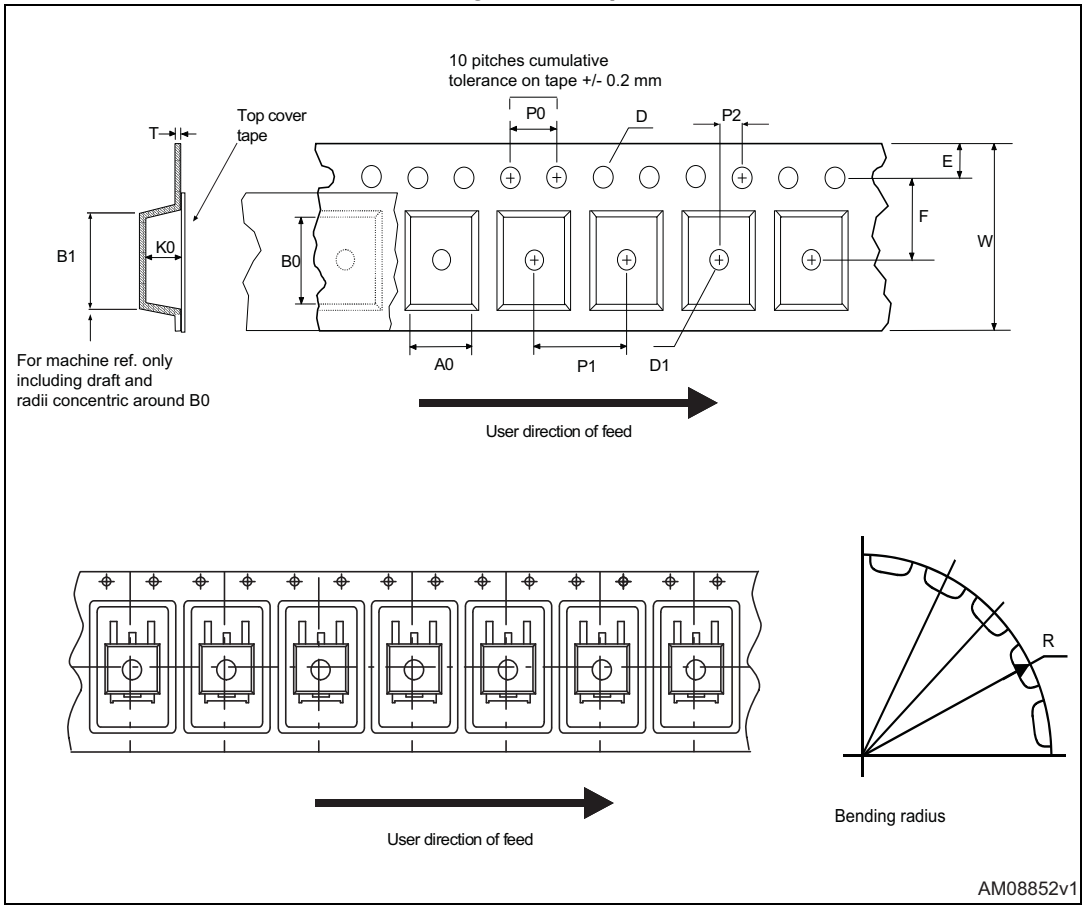


**Figure 22. Reel**

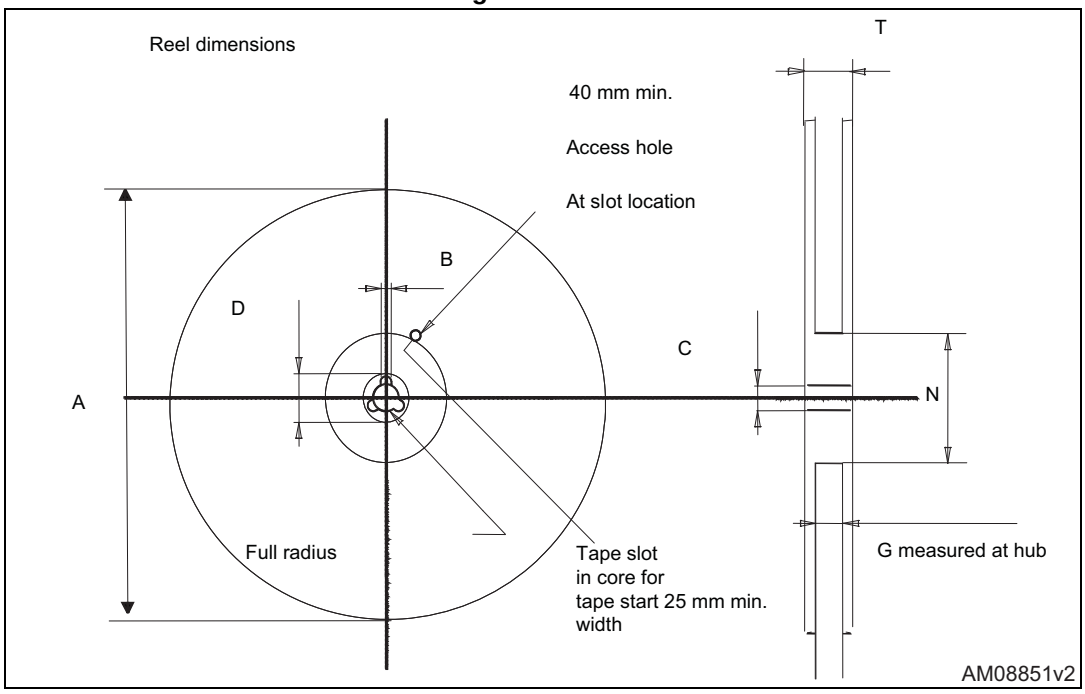



**Table 9. DPAK (TO-252) tape and reel mechanical data**

| Tape | | | Reel | | |
|---|---|---|---|---|---|
| Dim. | mm | | Dim. | mm | |
| | Min. | Max. | | Min. | Max. |
| A0 | 6.8 | 7 | A | | 330 |
| B0 | 10.4 | 10.6 | B | 1.5 | |
| B1 | | 12.1 | C | 12.8 | 13.2 |
| D | 1.5 | 1.6 | D | 20.2 | |
| D1 | 1.5 | | G | 16.4 | 18.4 |
| E | 1.65 | 1.85 | N | 50 | |
| F | 7.4 | 7.6 | T | | 22.4 |
| K0 | 2.55 | 2.75 | | | |
| P0 | 3.9 | 4.1 | Base qty. | | 2500 |
| P1 | 7.9 | 8.1 | Bulk qty. | | 2500 |
| P2 | 1.9 | 2.1 | | | |
| R | 40 | | | | |
| T | 0.25 | 0.35 | | | |
| W | 15.7 | 16.3 | | | |

# 6 Revision history

**Table 10. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 26-Jun-2014 | 1 | First release. |
| 14-Nov-2014 | 2 | Updated title and features in cover page<br>Updated *Table 3.: Thermal data*, *Table 4.: On/off states* and *Table 5.: Dynamic*<br>Updated *Figure 2: Safe operating area* ,*Figure 3: Thermal impedance*,*Figure 6.: Normalized $V_{(BR)DSS}$ vs. temperature*,*Figure 10.*,*Figure 11.: Normalized on-resistance vs. temperature* and *Section 4: Package mechanical data*. |

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