Power MOSFET

30 V, 7.0 A, Single N-Channel, TSOP-6

Features

- Low R_{DS(on)}
- Low Gate Charge
- NV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- Pb-Free Package is Available

Applications

- Load Switch
- Notebook PC
- Desktop PC

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	30	V
Gate-to-Source Voltage			V _{GS}	±20	V
Continuous Drain	Steady	T _A = 25°C	I _D	5.0	Α
Current (Note 1)	State	T _A = 85°C		3.6	
	t ≤ 10 s	T _A = 25°C		7.0	
Power Dissipation (Note 1)	Steady State	T _A = 25°C	P _D	1.0	W
	t ≤ 10 s			2.0	
Continuous Drain	Steady	T _A = 25°C	Ι _D	3.5	Α
Current (Note 2)	State	T _A = 85°C	1	2.5	
Power Dissipation (Note 2)		T _A = 25°C	P _D	0.5	W
Pulsed Drain Current	t _p = 10 μs	t _p = 10 μs, V _{GS} =10V		45	Α
Pulsed Drain Current	t _p = 30 μ	t _p = 30 μs, V _{GS} =5V		30	Α
Operating Junction and Storage Temperature		T _J , T _{STG}	–55 to 150	°C	
Source Current (Body Diode)		Is	2.0	Α	
	Single Pulse Drain–to–Source Avalanche Energy (V_{DD} = 30 V, I_{L} = 10.4 A, V_{GS} = 10 V, L = 1.0 mH, R_{G} = 25 Ω)		EAS	54	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		TL	260	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE RATINGS

Rating	Symbol	Max	Unit
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	125	°C/W
Junction-to-Ambient – t ≤ 10 s (Note 1)	$R_{\theta JA}$	62.5	
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	248	

- 1. Surface-mounted on FR4 board using 1 inch sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
- Surface-mounted on FR4 board using the minimum recommended pad size (Cu area = 0.0773 in sq).

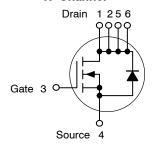


ON Semiconductor®

http://onsemi.com

V _{(BR)DSS}	R _{DS(on)} TYP	I _D MAX
20.1/	21.5 mΩ @ 10 V	7.0.4
30 V	30 mΩ @ 4.5 V	7.0 A

N-Channel





TSOP-6 CASE 318G STYLE 1



MARKING

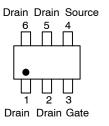
XX = Device Code

M = Date Code

Pb-Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information ion page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

OFF CHARACTERISTICS V(BRIDSS IT J) V(SR = 0 V. ID = 250 µA 30 Image: Control of the control o	Unit	Max	Тур	Min	Test Condition		Symbol	Characteristic
Drain-to-Source Breakdown Voltage Temperature Coefficient					•			OFF CHARACTERISTICS
Temperature Coefficient Poss Voss = 0 V, Voss = 0 V, Voss = 24 V T_J = 25°C 1.0	V			30	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		V _{(BR)DSS}	Drain-to-Source Breakdown Voltage
Section	mV/°C		18.4				V _{(BR)DSS} /T _J	
Gate-to-Source Leakage Current Igas VDS = 0 V, VGS = ±20 V 100 ±100 ON CHARACTERISTICS (Note 3) STATE (Note 3) Gate Threshold Voltage VGS(TH) VGS = VDS, ID = 250 μA 1.0 3.0 Negative Threshold Temperature Coefficient VGS(TH)/TJ VGS = 10 V, ID = 7.0 A 1.0 5.7 Drain-to-Source On Resistance PBS(on) VGS = 10 V, ID = 7.0 A 3.0 3.0 Forward Transconductance GFS VGS = 10 V, ID = 7.0 A 3.0 3.0 Forward Transconductance GFS VGS = 10 V, ID = 7.0 A 3.0 3.0 CHARGES, CAPACITANCES AND GATE RESISTANCE Input Capacitance CIBS VGS = 0 V, I = 1.0 MHz, VDS = 24 V 1115 560 Output Capacitance COSS COSS VGS = 10 V, VDS = 24 V 115	μΑ	1.0			$T_J = 25^{\circ}C$	$V_{GS} = 0 V$	I _{DSS}	Zero Gate Voltage Drain Current
Gate-to-Source Leakage Current Igas VDS = 0 V, VGS = ±20 V 100 ±100 ON CHARACTERISTICS (Note 3) STATE (Note 3) Gate Threshold Voltage VGS(TH) VGS = VDS, ID = 250 μA 1.0 3.0 Negative Threshold Temperature Coefficient VGS(TH)/TJ VGS = 10 V, ID = 7.0 A 1.0 5.7 Drain-to-Source On Resistance PBS(on) VGS = 10 V, ID = 7.0 A 3.0 3.0 Forward Transconductance GFS VGS = 10 V, ID = 7.0 A 3.0 3.0 Forward Transconductance GFS VGS = 10 V, ID = 7.0 A 3.0 3.0 CHARGES, CAPACITANCES AND GATE RESISTANCE Input Capacitance CIBS VGS = 0 V, I = 1.0 MHz, VDS = 24 V 1115 560 Output Capacitance COSS COSS VGS = 10 V, VDS = 24 V 115	1	10			T _J = 125°C	$V_{DS} = 24 \text{ V}$		
State Threshold Voltage VGS(TH) VGS(TH)/TJ 5.7	nA	±100			•		I _{GSS}	Gate-to-Source Leakage Current
Negative Threshold Temperature Coefficient V _{GS(TH)} /T _J								ON CHARACTERISTICS (Note 3)
Drain-to-Source On Resistance RDs(on) Vos = 10 V, ID = 7.0 A 21.5 25 Forward Transconductance gFs VDs = 10 V, ID = 6.0 A 30 35 Forward Transconductance gFs VDs = 10 V, ID = 7.0 A 30 35 CHARGES, CAPACITANCES AND GATE RESISTANCE Input Capacitance CISS VGS = 0 V, I = 1.0 MHz, VDS = 15 V, ID = 7.0 A 115 560 115<	V	3.0		1.0	ο = 250 μΑ	$V_{GS} = V_{DS}, I_{DS}$	V _{GS(TH)}	Gate Threshold Voltage
V _{GS} = 4.5 V, I _D = 6.0 A 30 35	mV/°C		5.7				V _{GS(TH)} /T _J	Negative Threshold Temperature Coefficient
Forward Transconductance	mΩ	25	21.5		I _D = 7.0 A	V _{GS} = 10 V, I	R _{DS(on)}	Drain-to-Source On Resistance
CHARGES, CAPACITANCES AND GATE RESISTANCE Input Capacitance C _{ISS} Output Capacitance C _{OSS} Reverse Transfer Capacitance C _{RSS} Total Gate Charge Q _{G(TOT)} Threshold Gate Charge Q _{G(TOT)} Gate-to-Source Charge Q _{GS} Gate-to-Drain Charge Q _{G(TOT)} Threshold Gate Charge Q _{G(TOT)} Threshold Gate Charge Q _{G(TOT)} Threshold Gate Charge Q _{G(TOT)} Gate-to-Drain Charge Q _{G(TOT)} Gate-to-Drain Charge Q _{GS} Gate-to-Drain Charge Q _{GS} Gate Resistance R _G SWITCHING CHARACTERISTICS (Note 4) Turn-On Delay Time t _d (ON) Rise Time t _f Turn-Off Delay Time t _d (OFF) Fall Time t _f DRAIN - SOURCE DIODE CHARACTERISTICS Forward Diode Voltage V _{SD} V _{SS} = 0 V, I _S = 0 V, I _S = 2 C 0.78 T _J = 125°C 0.63 Reverse Recovery Time t _A Charge Time	7	35	30		I _D = 6.0 A	$V_{GS} = 4.5 V,$		
$ \begin{array}{ c c c c c } \hline \mbox{Input Capacitance} & C_{ISS} \\ \hline \mbox{Output Capacitance} & C_{OSS} \\ \hline \mbox{Reverse Transfer Capacitance} & C_{RSS} \\ \hline \mbox{Total Gate Charge} & Q_{G(TOT)} \\ \hline \mbox{Total Gate Charge} & Q_{G(TOT)} \\ \hline \mbox{Gate-to-Source Charge} & Q_{GS} \\ \hline \mbox{Gate-to-Drain Charge} & Q_{G} \\ \hline \mbox{Total Gate Charge} & Q_{GS} \\ \hline \mbox{Gate-to-Drain Charge} & Q_{G} \\ \hline \mbox{Total Gate Charge} & Q_{G} \\ \hline \mbox{Total Gate Charge} & Q_{G} \\ \hline \mbox{Total Gate Charge} & Q_{G(TOT)} \\ \hline \mbox{Total Gate Charge} & Q_{G(TOT)} \\ \hline \mbox{Threshold Gate Charge} & Q_{G} \\ \hline \mbox{Gate-to-Drain Charge} & Q_{G} \\ \hline \mbox{SWITCHING CHARACTERISTICS (Note 4)} \\ \hline \mbox{Turn-On Delay Time} & t_{d(OFF)} \\ \hline \mbox{Turn-Off Delay Time} & t_{d(OFF)} \\ \hline \mbox{Fall Time} & t_{t} \\ \hline \mbox{DRAIN - SOURCE DIODE CHARACTERISTICS} \\ \hline \mbox{Forward Diode Voltage} & V_{SD} & V_{GS} = 0 \ V_{IS} = 0 \ $	S		30		I _D = 7.0 A	V _{DS} = 10 V, I	9FS	Forward Transconductance
Output Capacitance Coss Reverse Transfer Capacitance Coss Vps = 24 V VGs = 0 V, f = 1.0 MHz, Vps = 24 V 115 12 Total Gate Charge QG(TOT) VGS = 10 V, Vps = 15 V, Ip = 7.0 Å 12 0.85 12 Threshold Gate Charge QG(TH) VGS = 10 V, Vps = 15 V, Ip = 7.0 Å 0.85 0.85 0.85 Gate-to-Drain Charge QGD 3.0 0.85 0.80							SISTANCE	CHARGES, CAPACITANCES AND GATE RE
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	pF		560				C _{ISS}	Input Capacitance
Reverse Transfer Capacitance CRSS Total Gate Security 75 12 Total Gate Charge QG(TOT) VGS = 10 V, VDS = 15 V, ID = 7.0 Å 0.85 0.85 Gate-to-Source Charge QGS 1.9 0.85 0.85 Gate-to-Drain Charge QGD 3.0 0.85 0.85 Total Gate Charge QGD 3.0 0.8	1		115		1.0 MHz, 24 V	$V_{GS} = 0 \text{ V, f} = V_{DS} = 2$	C _{OSS}	Output Capacitance
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	1		75			v _{DS} = 24 v		Reverse Transfer Capacitance
Gate - to - Source Charge Q _{GS} Gate - to - Drain Charge Q _{GD} Total Gate Charge Q _{G(TOT)} Threshold Gate Charge Q _{G(TOT)} Gate - to - Source Charge Q _{GS} Gate - to - Source Charge Q _{GS} Gate - to - Drain Charge Q _{GS} Gate Resistance R _G SWITCHING CHARACTERISTICS (Note 4) Turn - On Delay Time t _d (ON) Rise Time t _f Turn - Off Delay Time t _d (OFF) Fall Time t _f DRAIN - SOURCE DIODE CHARACTERISTICS Forward Diode Voltage V _{SD} V _{GS} = 0 V, Reverse Recovery Time t _{RR} Charge Time t _d V _{GS} = 10 V, V _{DS} = 15 V, V _{GS} = 15 V, V _{DS} = 15 V, V _{GS} = 10 V, V _{DS} = 24 V, 15	nC		12				Q _{G(TOT)}	Total Gate Charge
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$			0.85		_{DS} = 15 V,	V _{GS} = 10 V, V	Q _{G(TH)}	Threshold Gate Charge
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$			1.9		0 A	$I_D = 7.0$	Q_{GS}	Gate-to-Source Charge
			3.0		Ī		Q_{GD}	Gate-to-Drain Charge
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	nC		6.0					Total Gate Charge
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	1		0.8		_{'ns} = 15 V,	V _{GS} = 4.5 V, V	Q _{G(TH)}	Threshold Gate Charge
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	1		1.85		0 A	$I_D = 7.0$	Q_{GS}	Gate-to-Source Charge
	1		3.0		Ī		Q_{GD}	Gate-to-Drain Charge
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Ω		2.8				R_{G}	Gate Resistance
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$					•			SWITCHING CHARACTERISTICS (Note 4)
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	ns		6.0				t _{d(ON)}	Turn-On Delay Time
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	7		15		V_{GS} = 10 V, V_{DS} = 24 V, I_{D} = 7.0 A, R_{G} = 3.0 Ω		t _r	Rise Time
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	1		18				t _{d(OFF)}	Turn-Off Delay Time
Forward Diode Voltage V_{SD} $V_{GS} = 0 \text{ V}, \\ I_S = 2.0 \text{ A}$ $T_J = 25^{\circ}\text{C}$ 0.78 1.0 Reverse Recovery Time t_{RR} 15 15 Charge Time t_a $V_{GS} = 0 \text{ V}$ 9.0	1		4.0				t _f	Fall Time
$I_{S} = 2.0 \text{ A} \qquad T_{J} = 125^{\circ}\text{C} \qquad 0.63$ Reverse Recovery Time $t_{RR} \qquad \qquad 15$ Charge Time $t_{a} \qquad V_{GS} = 0 \text{ V} \qquad 9.0$					•		cs	DRAIN - SOURCE DIODE CHARACTERISTI
$I_{S} = 2.0 \text{ A} \qquad T_{J} = 125 ^{\circ}\text{C} \qquad 0.63$ Reverse Recovery Time $t_{RR} \qquad \qquad 15$ Charge Time $t_{a} \qquad V_{GS} = 0 \text{ V} \qquad 9.0$	V	1.0	0.78		VGS = 0 V,		V _{SD}	Forward Diode Voltage
Charge Time t _a V _{GS} = 0 V 9.0	1		0.63					
# 100 A A A A A A A A A A A A A A A A A A	ns		15		$V_{GS} = 0 \text{ V}$ $dI_{S}/dt = 100 \text{ A/}\mu\text{s}, I_{S} = 2.0 \text{ A}$		t _{RR}	Reverse Recovery Time
dl /dk 400 A/ a 1 00 A	1		9.0				t _a	Charge Time
	1		6.0				t _b	Discharge Time
Reverse Recovery Charge Q _{RR} 8.0	nC		8.0				Q _{RR}	Reverse Recovery Charge

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: pulse width $\leq 300~\mu$ s, duty cycle $\leq 2\%$.

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

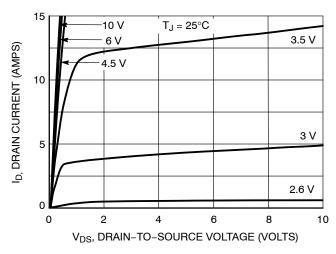
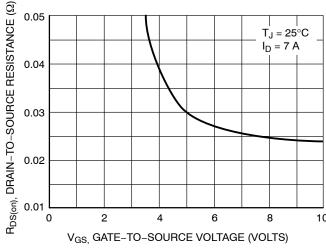


Figure 1. On-Region Characteristics

Figure 2. Transfer Characteristics



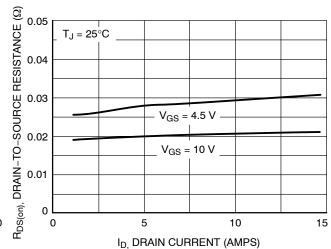
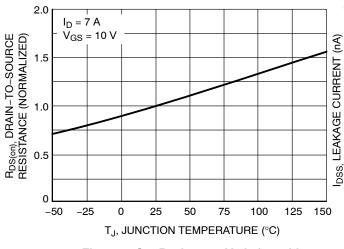


Figure 3. On-Resistance vs. Gate-to-Source Voltage

Figure 4. On-Resistance vs. Drain Current and Gate Voltage



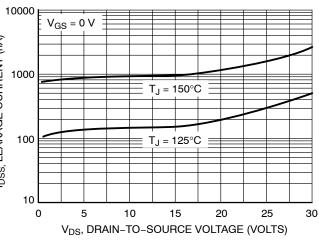
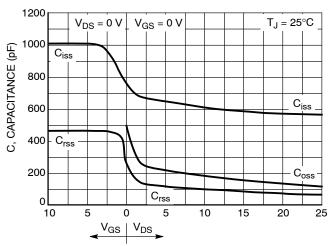


Figure 5. On–Resistance Variation with Temperature

Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

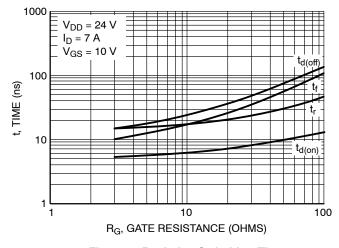


GATE-TO-SOURCE VOLTAGE (V) QT 6 Q_{GS}→ Q_{GD} I_D = 7 A 2 $V_{DD} = 15 V$ Vgs ($T_J = 25^{\circ}C$ 0 0 2 4 6 8 10 12 QG, TOTAL GATE CHARGE (nC)

GATE-TO-SOURCE OR DRAIN-TO-SOURCE VOLTAGE (VOLTS)

Figure 8. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge





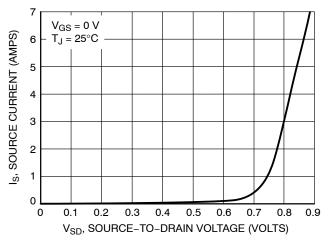
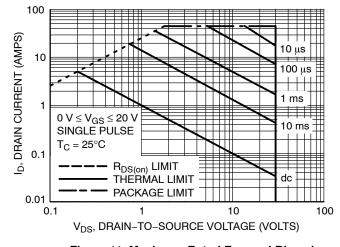


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

Figure 10. Diode Forward Voltage vs. Current



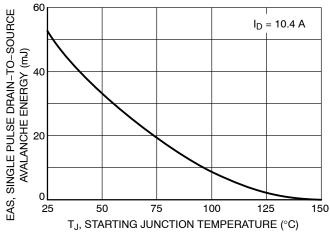


Figure 11. Maximum Rated Forward Biased Safe Operating Area

Figure 12. Maximum Avalanche Energy vs. **Starting Junction Temperature**

TYPICAL PERFORMANCE CURVES

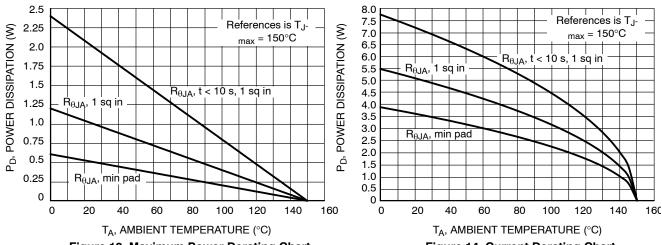


Figure 13. Maximum Power Derating Chart

Figure 14. Current Derating Chart

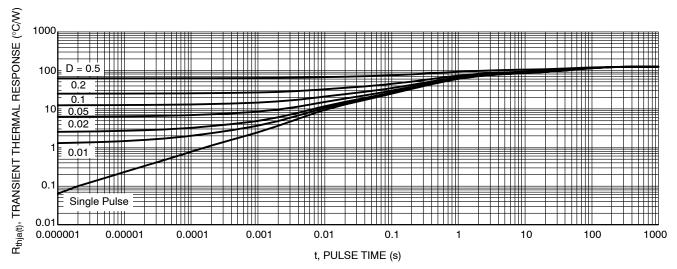


Figure 15. Thermal Response

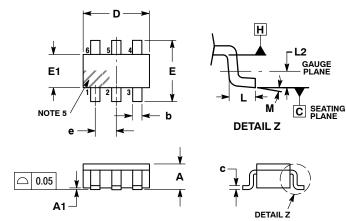
Table 1. ORDERING INFORMATION

Part Number	Marking (XX)	Package	Shipping [†]
NTGS4141NT1	S4	TSOP-6	3000 / Tape & Reel
NTGS4141NT1G	S4	TSOP-6 (Pb-Free)	3000 / Tape & Reel
NVGS4141NT1G	VS4	TSOP-6 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

TSOP-6 CASE 318G-02 ISSUE V



NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: MILLIMETERS.
 MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM
- MEATING MEAD THICKNESS INCLUES LEAD THISH. MINIMUM THICKNESS OF BASE MATERIAL. LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL. DIMENSIONS OF AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS, MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D
- AND E1 ARE DETERMINED AT DATUM H.

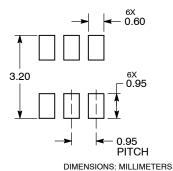
 5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

	MILLIMETERS				
DIM	MIN	NOM	MAX		
Α	0.90	1.00	1.10		
A1	0.01	0.06	0.10		
b	0.25	0.38	0.50		
С	0.10	0.18	0.26		
D	2.90	3.00	3.10		
E	2.50	2.75	3.00		
E1	1.30	1.50	1.70		
ø	0.85	0.95	1.05		
Ĺ	0.20	0.40	0.60		
L2	0.25 BSC				
М	0°	-	10°		

STYLE 1: PIN 1. DRAIN 2. DRAIN 3. GATE 4. SOURCE 5. DRAIN

6. DRAIN

RECOMMENDED **SOLDERING FOOTPRINT***



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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