



STGB14NC60K STGD14NC60K

N-channel 14A - 600V -DPAK - D²PAK
Short circuit rated PowerMESH™ IGBT

General features

Type	V _{CES}	V _{CE(sat)} (Max)@ 25°C	I _C @100°C
STGB14NC60K	600V	<2.5V	14A
STGD14NC60K	600V	<2.5V	14A

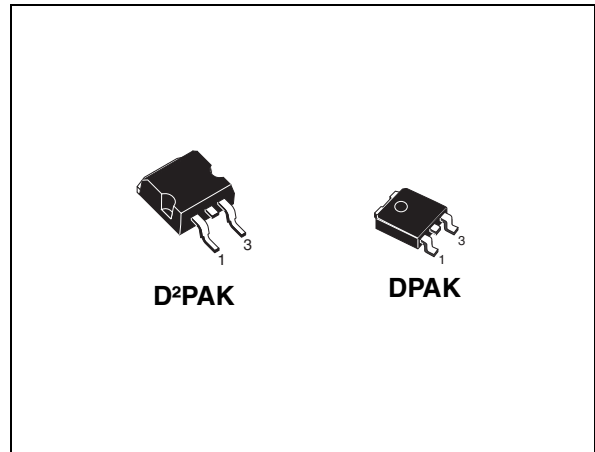
- Low on-voltage drop (V_{cesat})
- Low C_{res} / C_{ies} ratio (no cross conduction susceptibility)
- Short circuit withstand time 10μs

Description

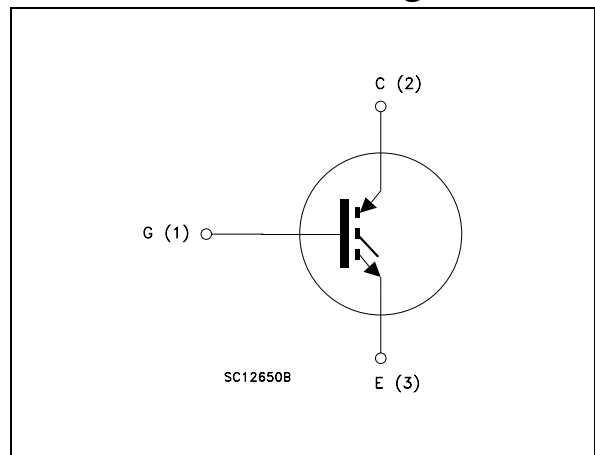
Using the latest high voltage technology based on a patented strip layout, STMicroelectronics has designed an advanced family of IGBTs, the Power MESH™ IGBTs, with outstanding performances. The suffix "K" identifies a family optimized for high frequency motor control applications with short circuit withstand capability.

Applications

- High frequency inverters
- Motor drivers with short circuit protection



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STGB14NC60KT4	GB14NC60K	D ² PAK	Tape & reel
STGD14NC60KT4	GD14NC60K	DPAK	Tape & reel

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage ($V_{GS} = 0$)	600	V
$I_C^{(1)}$	Collector current (continuous) at $T_C = 25^\circ\text{C}$	25	A
$I_C^{(1)}$	Collector current (continuous) at $T_C = 100^\circ\text{C}$	14	A
$I_{CL}^{(2)}$	Collector current (pulsed)	50	A
V_{GE}	Gate-emitter voltage	± 20	V
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	80	W
t_{scw}	Short circuit withstand time, $V_{CE} = 0.5V_{BR(CES)}$, $T_J = 125^\circ\text{C}$, $R_G = 10\Omega$, $V_{GE} = 12\text{V}$	10	μs
T_{stg}	Storage temperature	– 55 to 150	$^\circ\text{C}$
T_J	Operating junction temperature		

1. Calculated according to the iterative formula:

$$I_C(T_C) = \frac{T_{JMAX} - T_C}{R_{THJ-C} \times V_{CESAT(MAX)}(T_C, I_C)}$$

2. $V_{clamp} = 480\text{V}$, $T_J = 150^\circ\text{C}$, $R_G = 10\Omega$, $V_{GE} = 15\text{V}$

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	1.25	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	$^\circ\text{C/W}$

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 3. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{BR(CES)}$	Collector-emitter breakdown voltage	$I_C = 1\text{mA}$, $V_{GE} = 0$	600			V
I_{GES}	Gate-emitter leakage current ($V_{CE} = 0$)	$V_{GE} = \pm 20\text{V}$, $V_{CE} = 0$			± 100	nA
I_{CES}	Collector cut-off current ($V_{GE} = 0$)	$V_{CE} = \text{Max rating}$, $T_C = 25^{\circ}\text{C}$ $V_{CE} = \text{Max rating}$, $T_C = 125^{\circ}\text{C}$			150 1	μA mA
$V_{GE(th)}$	Gate threshold voltage	$V_{CE} = V_{GE}$, $I_C = 250\mu\text{A}$	4.5		6.5	V
$V_{CE(SAT)}$	Collector-emitter saturation voltage	$V_{GE} = 15\text{V}$, $I_C = 7\text{A}$ $V_{GE} = 15\text{V}$, $I_C = 7\text{A}$, $T_C = 125^{\circ}\text{C}$		2.0 1.8	2.5	V V
$g_{fs}^{(1)}$	Forward transconductance	$V_{CE} = 15\text{V}$, $I_C = 7\text{A}$		3		S

1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ies} C_{oes} C_{res}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{CE} = 25\text{V}$, $f = 1\text{MHz}$, $V_{GE} = 0$		760 86 15.5		pF pF pF
Q_g Q_{ge} Q_{gc}	Total gate charge Gate-emitter charge Gate-collector charge	$V_{CE} = 390\text{V}$, $I_C = 7\text{A}$, $V_{GE} = 15\text{V}$ (see Figure 17)		34.4 8.1 16.4		nC nC nC

Table 5. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 390V, I_C = 7A$		22.5		ns
t_r	Current rise time	$R_G = 10\Omega, V_{GE} = 15V,$		8.5		ns
$(di/dt)_{on}$	Turn-on current slope	$T_J = 25^\circ C$ (see Figure 16)		700		A/ μs
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 390V, I_C = 7A$		22		ns
t_r	Current rise time	$R_G = 10\Omega, V_{GE} = 15V,$		9.5		ns
$(di/dt)_{on}$	Turn-on current slope	$T_J = 125^\circ C$ (see Figure 16)		680		A/ μs
$t_r(V_{off})$	Off voltage rise time	$V_{CC} = 390V, I_C = 7A,$		60		ns
$t_{d(off)}$	Turn-off delay time	$R_{GE} = 10\Omega, V_{GE} = 15V$		116		ns
t_f	Current fall time	$T_J = 25^\circ C$ (see Figure 16)		75		ns
$t_r(V_{off})$	Off voltage rise time	$V_{CC} = 390V, I_C = 7A,$		24		ns
$t_{d(off)}$	Turn-off delay time	$R_{GE} = 10\Omega, V_{GE} = 15V$		196		ns
t_f	Current fall time	$T_J = 125^\circ C$ (see Figure 16)		144		ns

Table 6. Switching energy (inductive load)

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$E_{on}^{(1)}$	Turn-on switching losses	$V_{CC} = 390V, I_C = 7A$		82		μJ
$E_{off}^{(2)}$	Turn-off switching losses	$R_G = 10\Omega, V_{GE} = 15V,$		155		μJ
E_{ts}	Total switching losses	$T_J = 25^\circ C$ (see Figure 16)		237		μJ
$E_{on}^{(1)}$	Turn-on switching losses	$V_{CC} = 390V, I_C = 7A$		131		μJ
$E_{off}^{(2)}$	Turn-off switching losses	$R_G = 10\Omega, V_{GE} = 15V,$		370		μJ
E_{ts}	Total switching losses	$T_J = 125^\circ C$ (see Figure 16)		501		μJ

1. E_{on} is the turn-on losses when a typical diode is used in the test circuit in figure 2. If the IGBT is offered in a package with a co-pack diode, the co-pack diode is used as external diode. IGBTs & DIODE are at the same temperature (25°C and 125°C)
2. Turn-off losses include also the tail of the collector current.

2.1 Electrical characteristics (curves)

Figure 1. Output characteristics

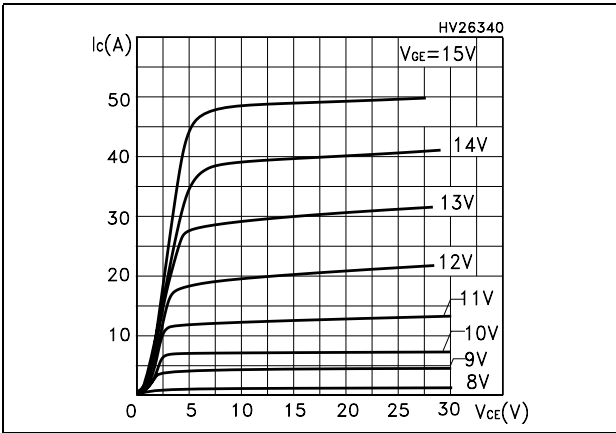


Figure 2. Transfer characteristics

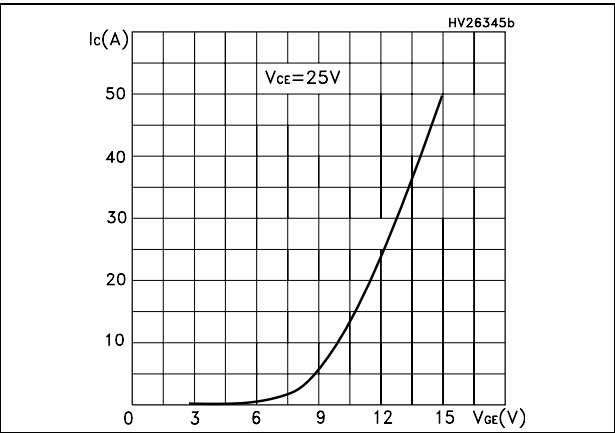


Figure 3. Transconductance

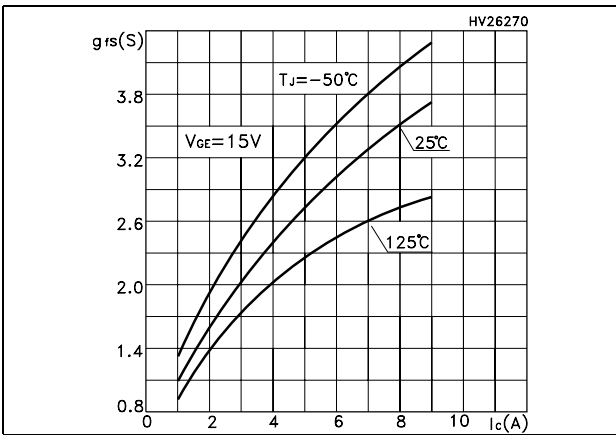


Figure 4. Collector-emitter on voltage vs temperature

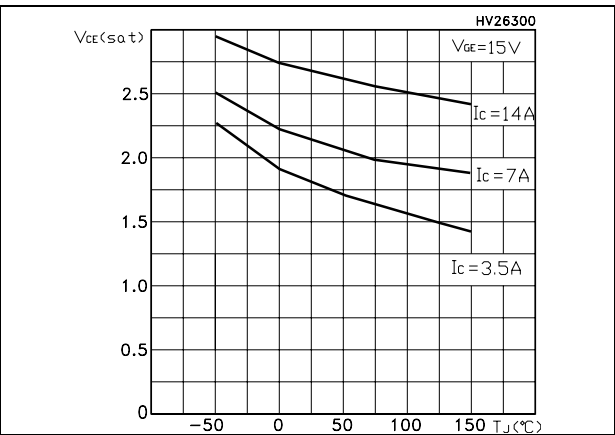


Figure 5. Collector-emitter on voltage vs collector current

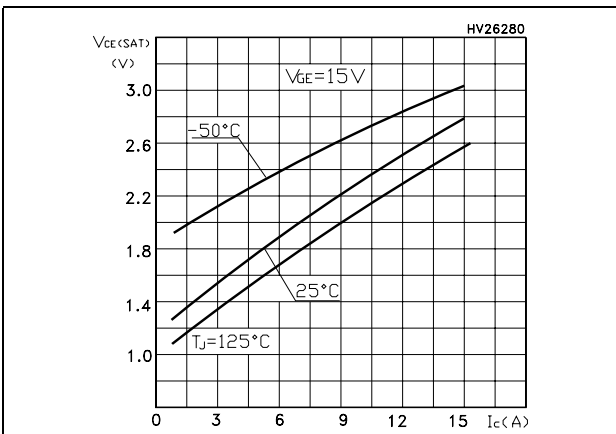


Figure 6. Normalized gate threshold vs temperature

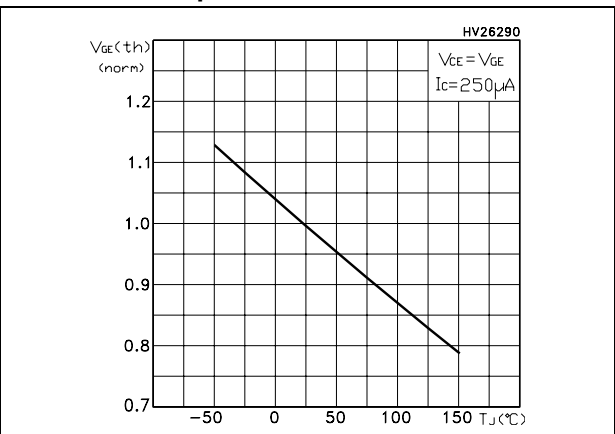


Figure 7. Normalized breakdown voltage vs temperature

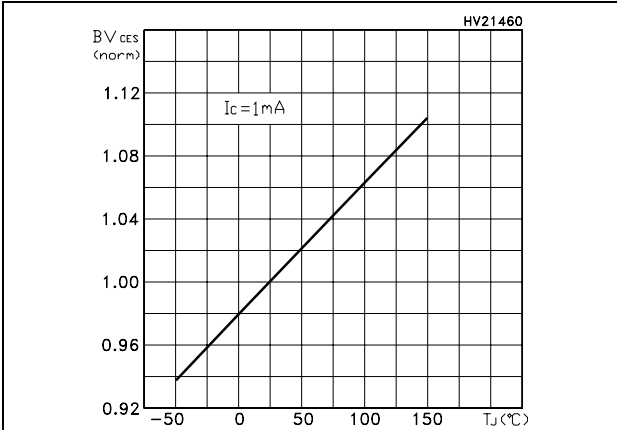


Figure 8. Gate charge vs gate-emitter voltage

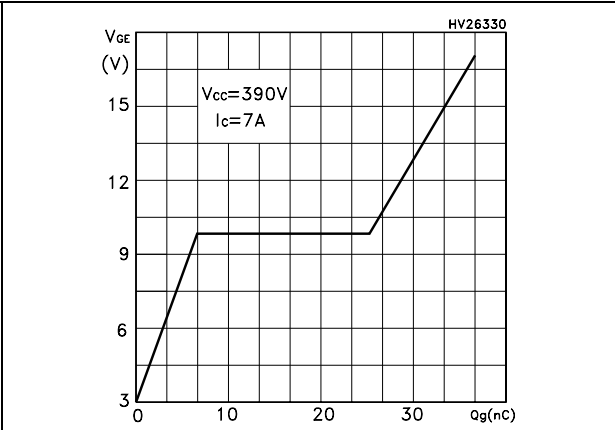


Figure 9. Capacitance variations

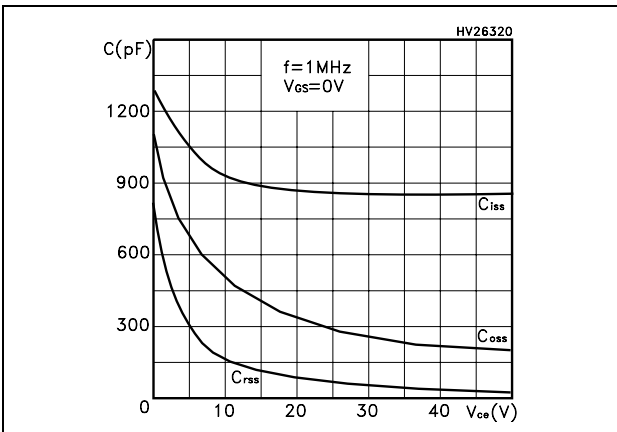


Figure 10. Switching losses vs temperature

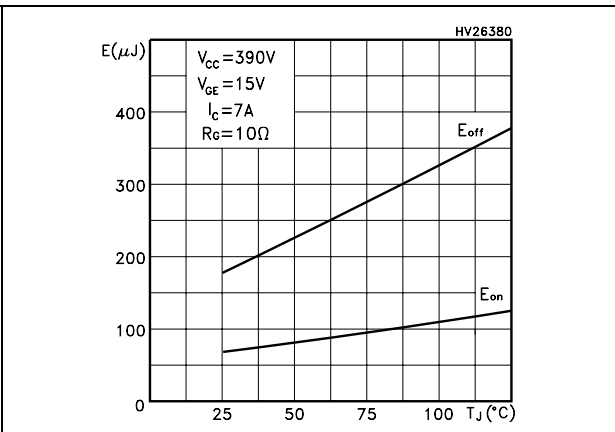


Figure 11. Switching losses vs gate resistance

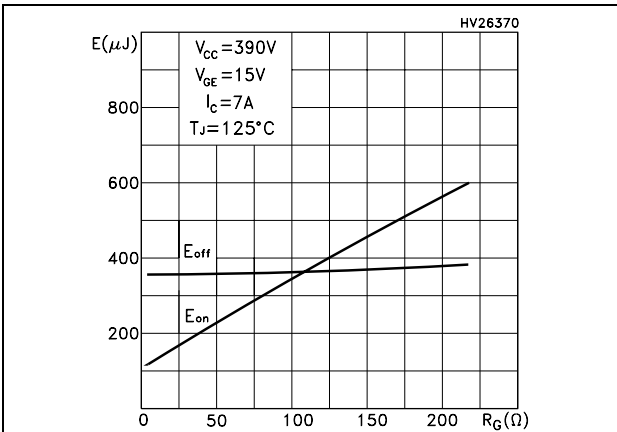


Figure 12. Switching losses vs collector current

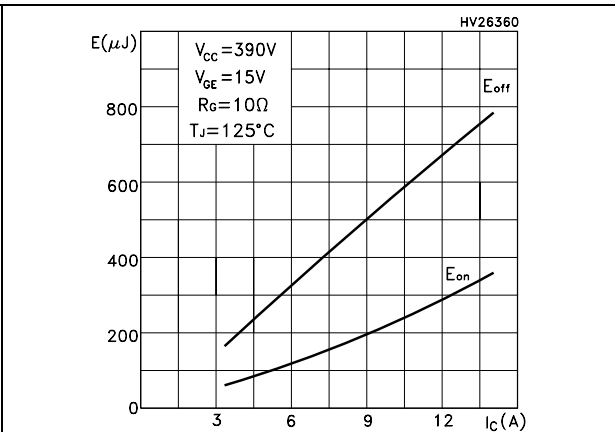


Figure 13. Thermal impedance

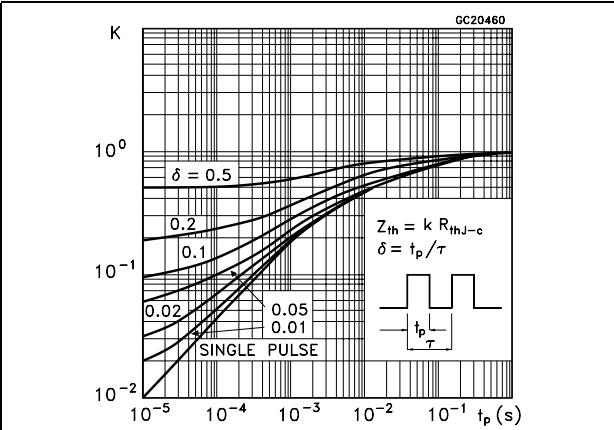


Figure 14. Turn-off SOA

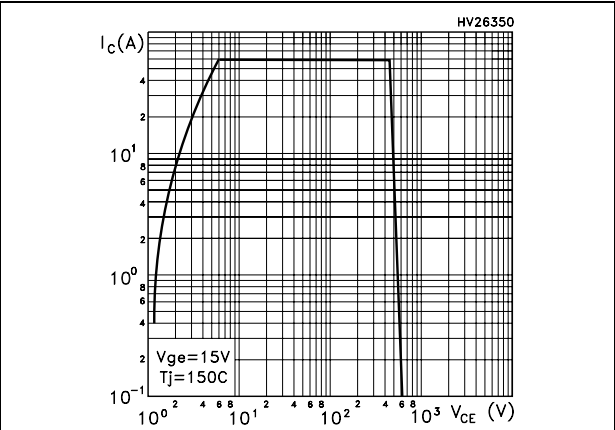
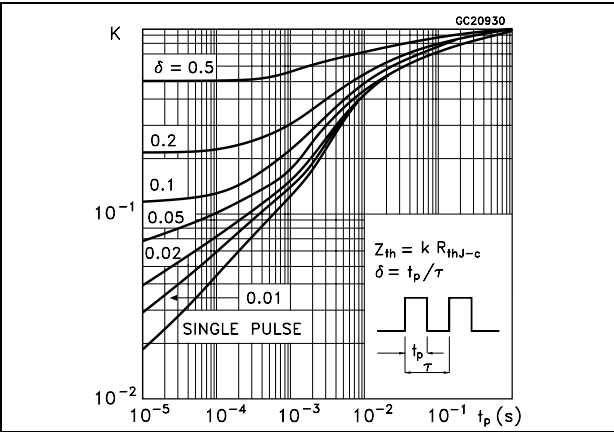


Figure 15. Thermal impedance for D²PAK



3 Test circuit

Figure 16. Test circuit for inductive load switching

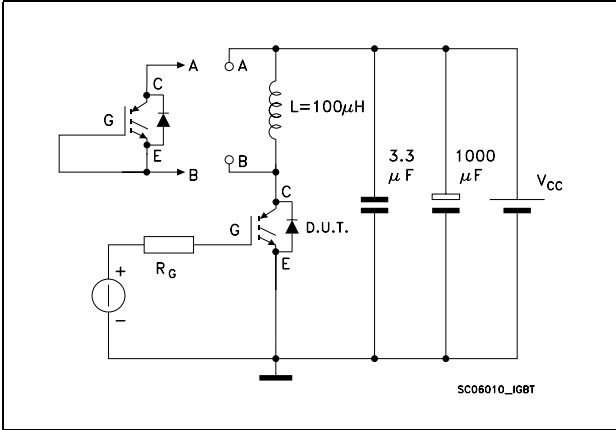


Figure 17. Gate charge test circuit

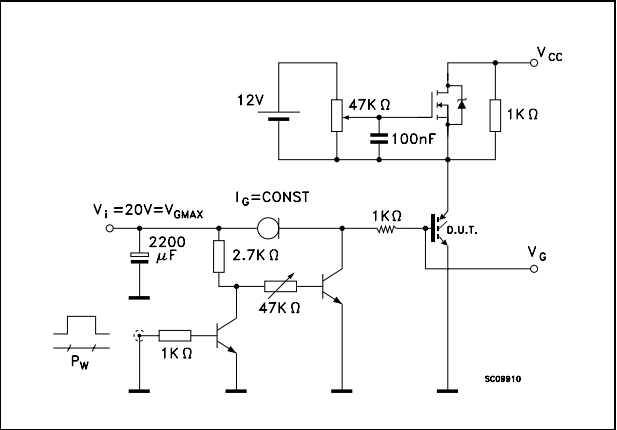


Figure 18. Switching waveforms

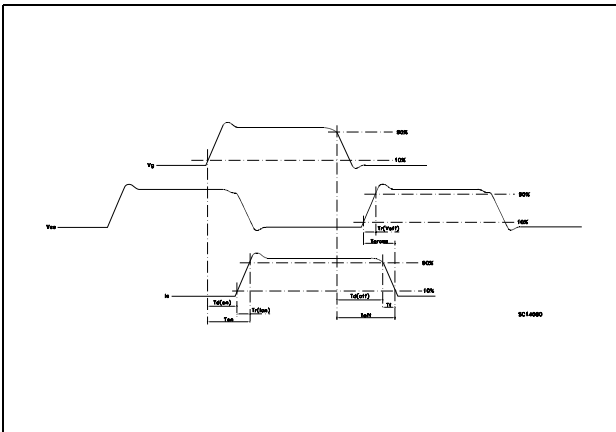
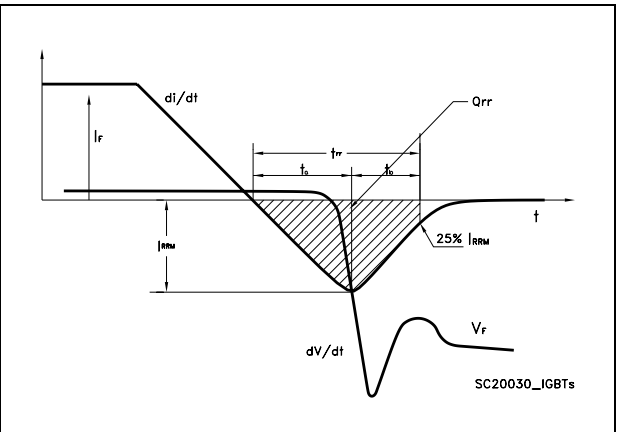


Figure 19. Diode recovery times waveform

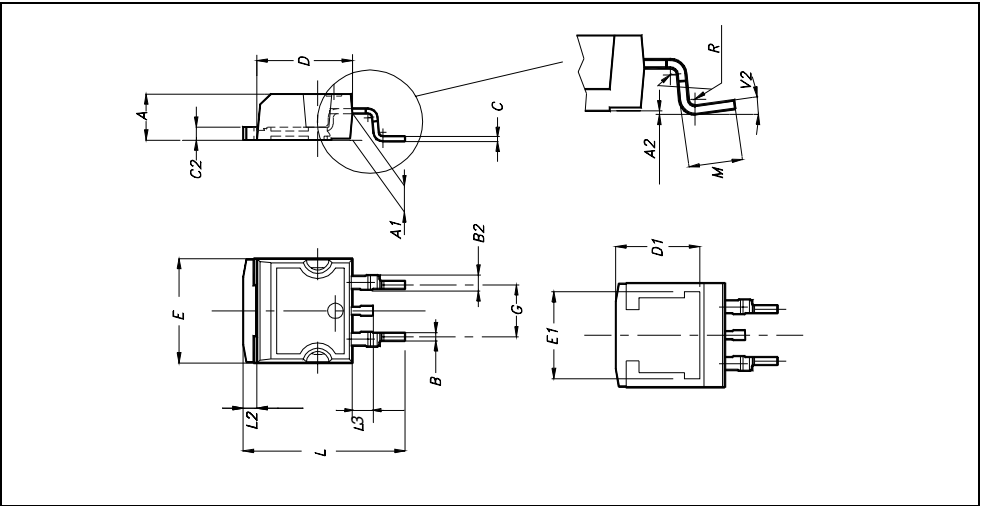


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			



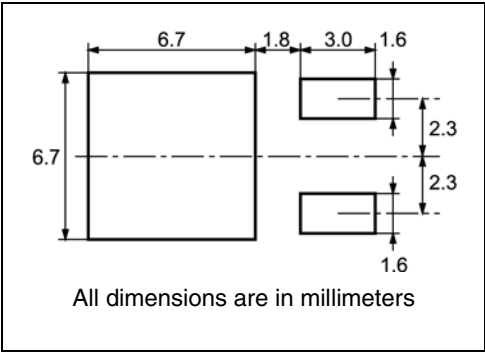
DPAK MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°

The mechanical drawing illustrates the DPAK package geometry. It includes a top view showing dimensions E, b4, L2, L4, H, e, e1, and L. A side view shows dimensions A, A1, A2, C2, D, D1, E1, and C. A detail view of the lead shows dimensions L1, L, V2, and a 0.25 gauge plane. The thermal pad is also indicated.

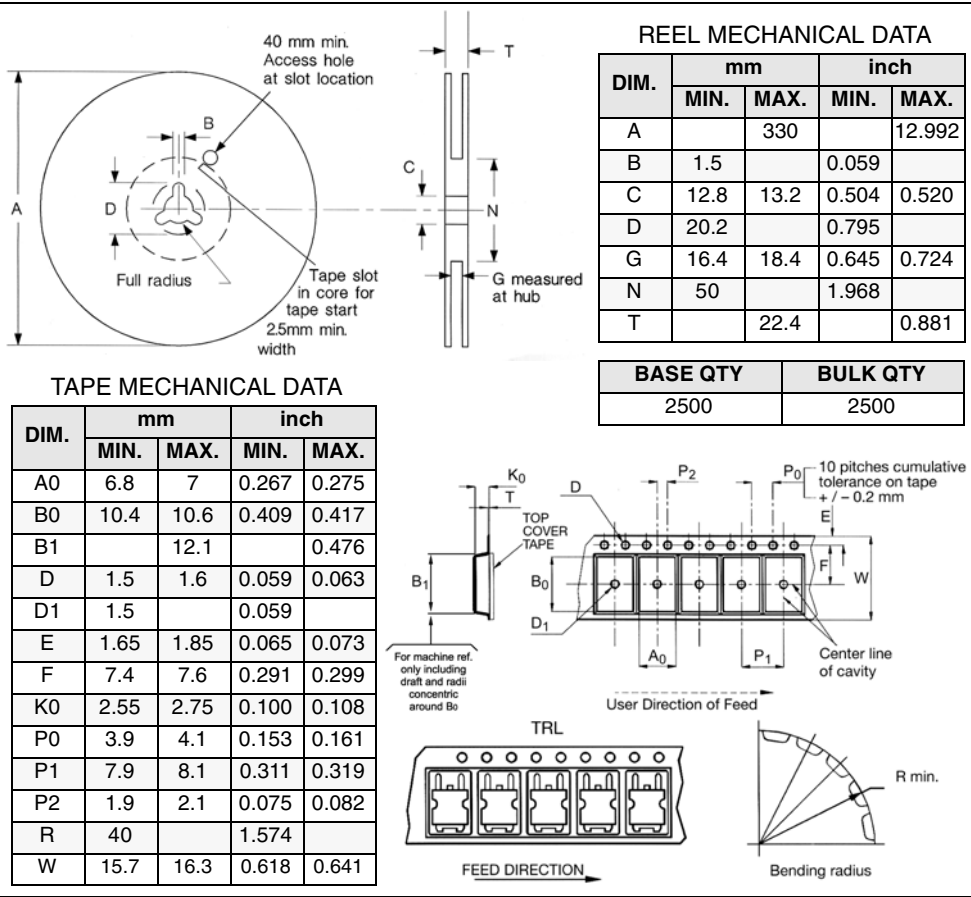
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5 Packaging mechanical data

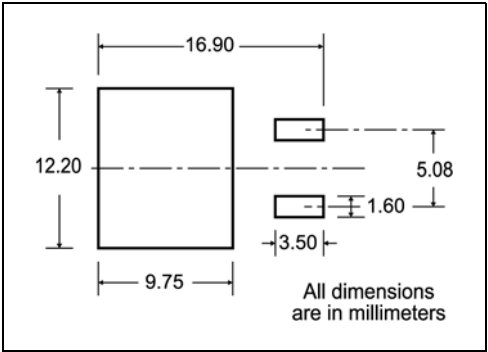
DPAK FOOTPRINT



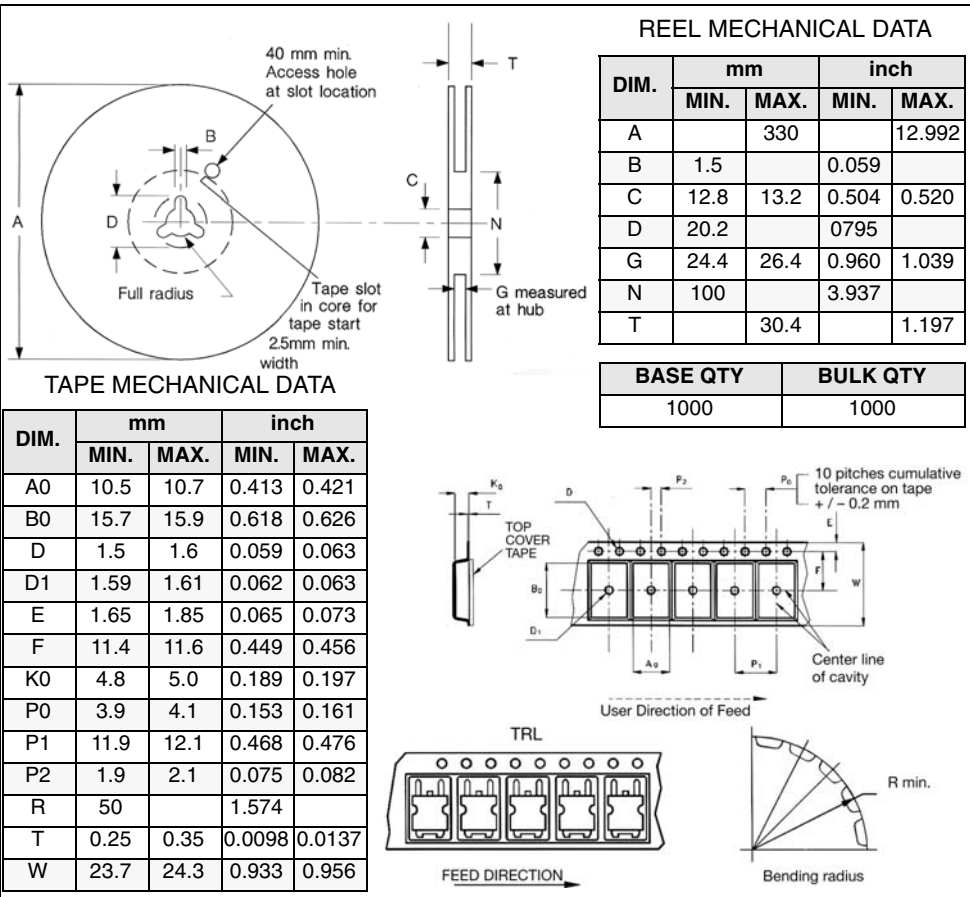
TAPE AND REEL SHIPMENT



D²PAK FOOTPRINT



TAPE AND REEL SHIPMENT



* on sales type

6 Revision history

Table 7. Revision history

Date	Revision	Changes
12-Jul-2006	1	New release

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