Data Sheet | September 1, 2005 | FN9161.6

# Bridge Controller with Precision Dead Time Control

The ISL6745 is a low-cost double-ended voltage-mode PWM controller designed for half-bridge and full-bridge power supplies and line-regulated bus converters. It provides precise control of switching frequency, adjustable soft-start, and overcurrent shutdown. In addition, the ISL6745 allows for accurate adjustment of MOSFET non-overlap time (“deadtime”) with deadtimes as low as 35ns, allowing power engineers to optimize the efficiency of open-loop bus converters. The ISL6745 also includes a control voltage input for closed-loop PWM and line voltage feed-forward functions.

Low start-up and operating currents allow for easy biasing in both AC/DC and DC/DC applications. This advanced BiCMOS design also features adjustable switching frequency up to 1MHz, 1A FET drivers, and very low propagation delays for a fast response to overcurrent faults. The ISL6745 is available in a space-saving MSOP-10 package and is guaranteed to meet rated specifications over a wide -40°C to 105°C temperature range.

## Ordering Information

| PART NUMBER | TEMP. RANGE (°C) | PACKAGE | PKG. DWG. # |
|---|---|---|---|
| ISL6745AU | -40 to 105 | 10 Ld MSOP | M10.118 |
| ISL6745AUZ (See Note) | -40 to 105 | 10 Ld MSOP (Pb-free) | M10.118 |

Add -T suffix to part number for tape and reel packaging

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

## Features

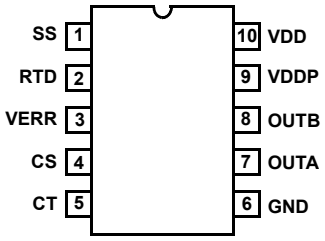
- Precision Duty Cycle and Deadtime Control
- 100μA Start-up Current
- Adjustable Delayed Overcurrent Shutdown and Re-Start
- Adjustable Oscillator Frequency Up to 2MHz
- 1A MOSFET Gate Drivers
- Adjustable Soft-Start
- Internal Over Temperature Protection
- 35ns Control to Output Propagation Delay
- Small Size and Minimal External Component Count
- Input Undervoltage Protection
- Pb-Free Plus Anneal Available (RoHS Compliant)

## Applications

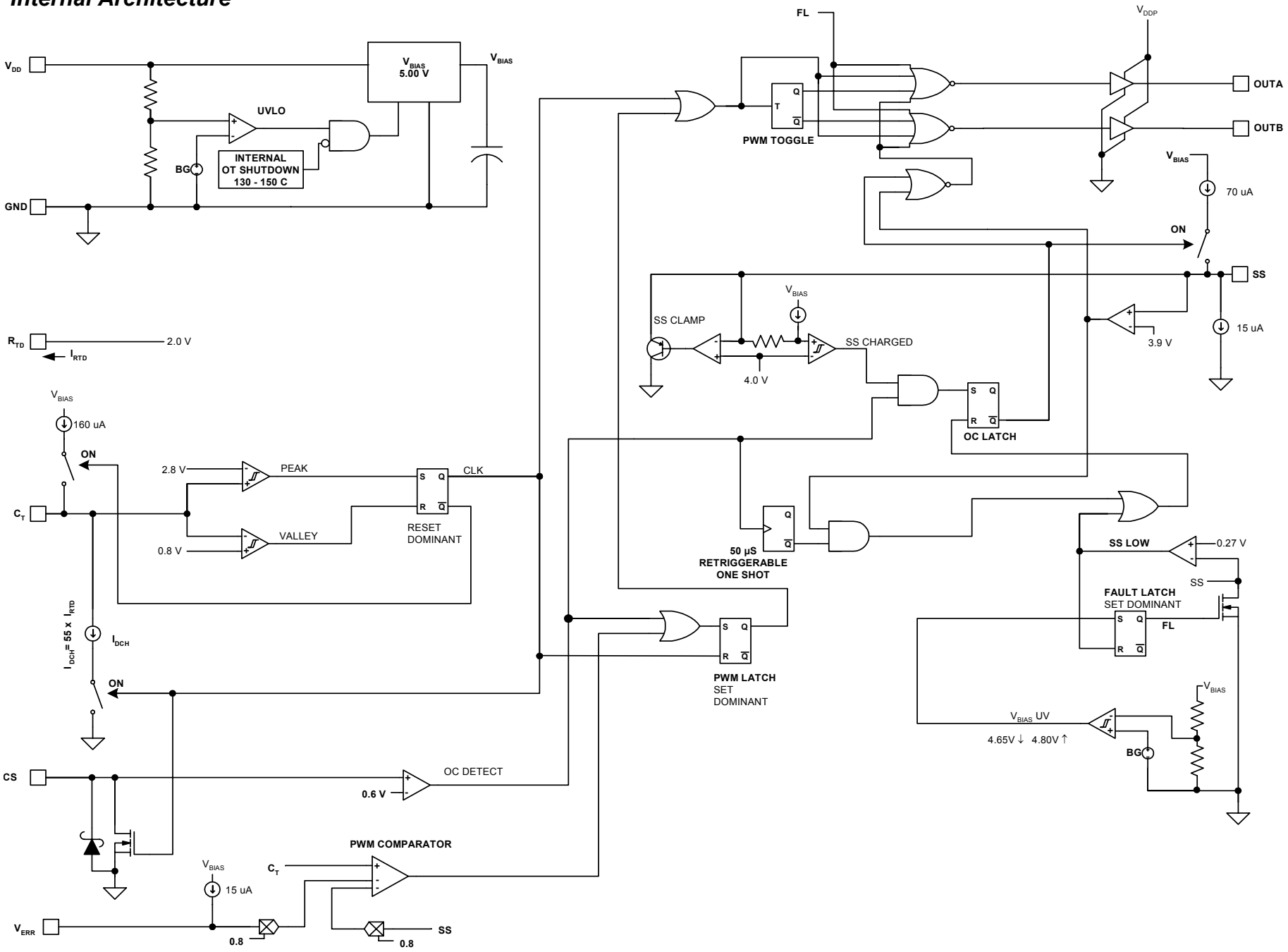
- Half-bridge Converters
- Full-bridge Converters
- Line-regulated Bus Converters
- AC/DC Power Supplies
- Telecom, Datacom, and File Server Power

## Pinout

**ISL6745 (MSOP)**
TOP VIEW



## Internal Architecture



## Absolute Maximum Ratings

Supply Voltage, $V_{DD}$ . . . . . GND - 0.3V to +20.0V
OUTA, OUTB . . . . . GND - 0.3V to $V_{DD}$
Signal Pins . . . . . GND - 0.3V to 5V
Peak GATE Current . . . . . 1A
ESD Classification
Human Body Model (Per JEDEC22 std. Method A114-B) . Class 2
Machine Model (Per JEDEC22 std. Method A115-A). . . . .Class A

## Thermal Information

| Thermal Resistance (Typical, Note 1) | $\theta_{JA}$ (°C/W) |
|---|---|
| 10 Lead MSOP | 128 |

Maximum Junction Temperature . . . . . -55°C to 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

## Operating Conditions

Temperature Range
ISL6745AU . . . . . -40°C to 105°C
Supply Voltage Range (Typical). . . . . 9-16 VDC

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTES:

1. $\theta_{JA}$ is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. All voltages are to be measured with respect to GND, unless otherwise specified.

## Electrical Specifications

Recommended operating conditions unless otherwise noted. Refer to Block Diagram and Typical Application schematic. 9V < $V_{DD}$< 16V, $R_{TD}$ = 51.1kΩ, $C_T$ = 470pF, $T_A$ = -40°C to 105°C (Note 4), Typical values are at $T_A$ = 25°C

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **SUPPLY VOLTAGE** | | | | | |
| Start-Up Current, $I_{DD}$ | $V_{DD}$< START Threshold | - | - | 175 | µA |
| Operating Current, $I_{DD}$ | $C_{OUTA,B}$ = 1nF | - | 5 | 8.5 | mA |
| UVLO START Threshold | | 5.9 | 6.3 | 6.6 | V |
| UVLO STOP Threshold | | 5.3 | 5.7 | 6.3 | V |
| Hysteresis | | - | 0.6 | - | V |
| **CURRENT SENSE** | | | | | |
| Current Limit Threshold | | 0.55 | 0.6 | 0.65 | V |
| CS to OUT Delay | (Note 4) | - | 35 | - | ns |
| CS Sink Current | | 8 | 10 | - | mA |
| Input Bias Current | | -1 | - | 1 | µA |
| **PULSE WIDTH MODULATOR** | | | | | |
| Minimum Duty Cycle | $V_{ERROR}$ < $C_T$ Offset | - | - | 0 | % |
| Maximum Duty Cycle | $C_T$ = 470pF, $R_{TD}$ = 51.1kΩ | - | 94 | - | % |
| | $C_T$ = 470pF, $R_{TD}$ = 1.1kΩ (Note 4) | - | 99 | - | % |
| $V_{ERR}$ to PWM Comparator Input Gain | | - | 0.8 | - | V/V |
| $C_T$ to PWM Comparator Input Gain | (Note 4) | - | 1 | - | V/V |
| SS to PWM Comparator Input Gain | (Note 4) | - | 0.8 | - | V/V |

**Electrical Specifications** Recommended operating conditions unless otherwise noted. Refer to Block Diagram and Typical Application schematic. 9V < $V_{DD}$< 16V, $R_{TD}$ = 51.1kΩ, $C_T$ = 470pF, $T_A$ = -40°C to 105°C (Note 4), Typical values are at $T_A$ = 25°C **(Continued)**

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **OSCILLATOR** | | | | | |
| Charge Current | $T_A$ = 25°C | 143 | 156 | 170 | µA |
| $R_{TD}$ Voltage | | 1.925 | 2 | 2.075 | V |
| Discharge Current Gain | | 45 | - | 65 | µA/µA |
| $C_T$ Valley Voltage | | 0.75 | 0.8 | 0.85 | V |
| $C_T$ Peak Voltage | | 2.70 | 2.80 | 2.90 | V |
| **SOFT-START** | | | | | |
| Net Charging Current | | 45 | - | 68 | µA |
| SS Clamp Voltage | | 3.8 | 4.0 | 4.2 | V |
| Overcurrent Shutdown Threshold Voltage | (Note 4) | - | 3.9 | - | V |
| Overcurrent Discharge Current | | 12 | 15 | 23 | µA |
| Reset Threshold Voltage | (Note 4) | 0.25 | 0.27 | 0.30 | V |
| **OUTPUT** | | | | | |
| High Level Output Voltage (VOH) | $V_{DD}$ - $V_{OUTA}$ or $V_{OUTB}$, $I_{OUT}$ = -100mA | - | 0.5 | 2.0 | V |
| Low Level Output Voltage (VOL) | $I_{OUT}$ = 100mA | - | 0.5 | 1.0 | V |
| Rise Time | $C_{GATE}$ = 1nF, $V_{DD}$ = 12V | - | 17 | 60 | ns |
| Fall Time | $C_{GATE}$ = 1nF, $V_{DD}$ = 12V | - | 20 | 60 | ns |
| **THERMAL PROTECTION** | | | | | |
| Thermal Shutdown | (Note 4) | - | 145 | - | °C |
| Thermal Shutdown Clear | (Note 4) | - | 130 | - | °C |
| Hysteresis, Internal Protection | (Note 4) | - | 15 | - | °C |

NOTES:

3. Specifications at -40°C are guaranteed by design, not production tested.
4. Guaranteed by design, not 100% tested in production.

## Typical Performance Curves

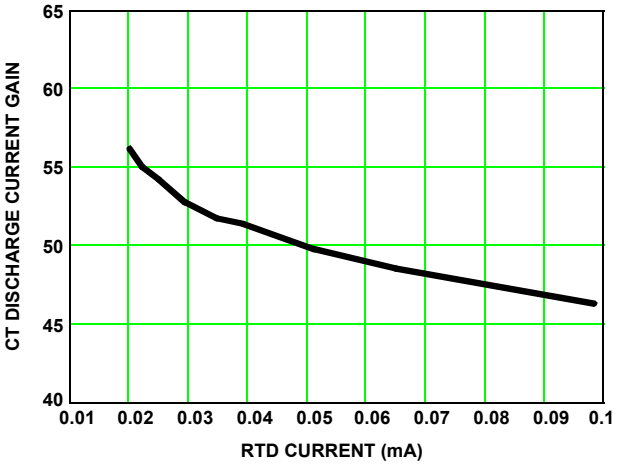



FIGURE 1. OSCILLATOR CT DISCHARGE CURRENT GAIN

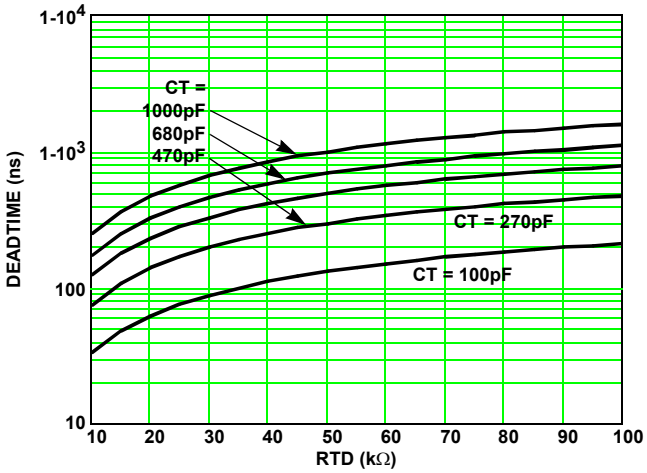



FIGURE 2. DEADTIME vs CAPACITANCE

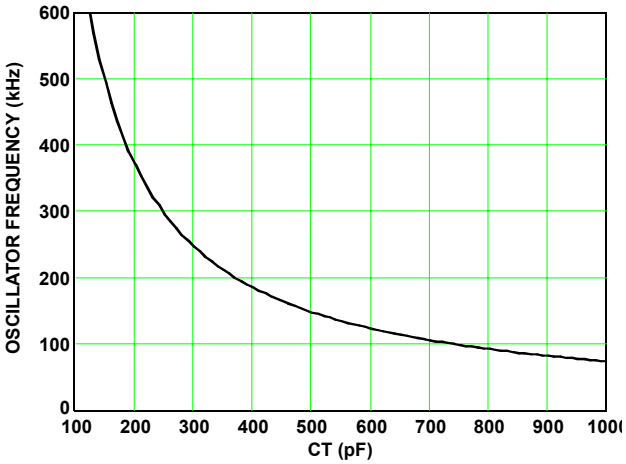



FIGURE 3. CAPACITANCE vs OSCILLATOR FREQUENCY (RTD = 49.9kΩ)

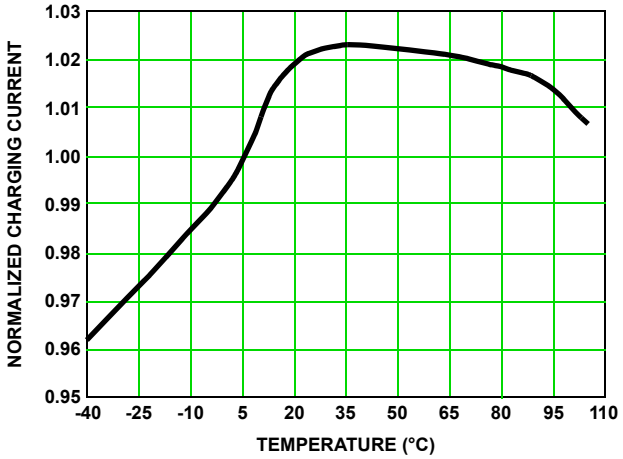



FIGURE 4. CHARGE CURRENT vs TEMPERATURE

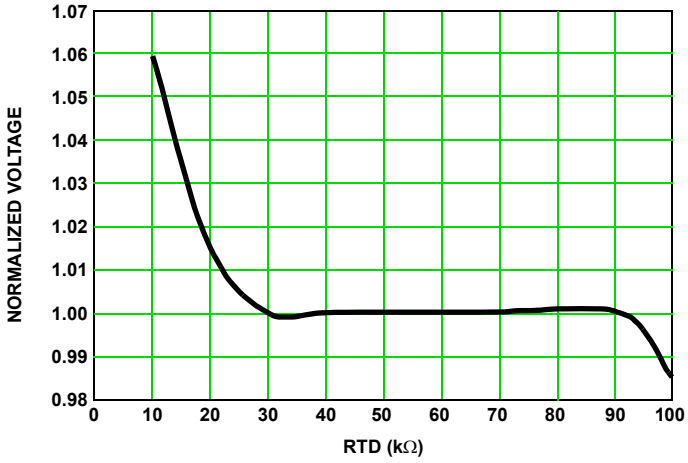



FIGURE 5. TIMING CAPACITOR VOLTAGE vs RTD

## Pin Descriptions

**$V_{DD}$ -** $V_{DD}$ is the power connection for the IC. To optimize noise immunity, bypass $V_{DD}$ to GND with a ceramic capacitor as close to the $V_{DD}$ and GND pins as possible.

The total supply current, $I_{DD}$, will be dependent on the load applied to outputs OUTA and OUTB. Total $I_{DD}$ current is the sum of the quiescent current and the average output current. Knowing the operating frequency, $F_{SW}$, and the output loading capacitance charge, Q, per output, the average output current can be calculated from:

$$I_{OUT} = 2 \bullet Q \bullet F_{SW} \quad A \qquad \text{(EQ. 1)}$$

**$R_{TD}$ -** This is the oscillator timing capacitor discharge current control pin. A resistor is connected between this pin and GND. The current flowing through the resistor determines the magnitude of the discharge current. The discharge current is nominally 55x this current. The PWM deadtime is determined by the timing capacitor discharge duration.

**$C_T$ -** The oscillator timing capacitor is connected between this pin and GND.

**CS -** This is the input to the overcurrent protection comparator. The overcurrent comparator threshold is set at 0.600V nominal. The CS pin is shorted to GND at the end of each switching cycle. Depending on the current sensing source impedance, a series input resistor may be required due to the delay between the internal clock and the external power switch.

Exceeding the overcurrent threshold will start a delayed shutdown sequence. Once an overcurrent condition is detected, the soft-start charge current source is disabled. The soft-start capacitor begins discharging through a 15µA current source, and if it discharges to less than 3.9V (Sustained Overcurrent Threshold), a shutdown condition occurs and the OUTA and OUTB outputs are forced low. When the soft-start voltage reaches 0.27V (Reset Threshold) a soft-start cycle begins.

If the overcurrent condition ceases, and then an additional 50µs period elapses before the shutdown threshold is reached, no shutdown occurs. The SS charging current is re-enabled and the soft-start voltage is allowed to recover.

**GND -** Reference and power ground for all functions on this device. Due to high peak currents and high frequency operation, a low impedance layout is necessary. Ground planes and short traces are highly recommended.

**OUTA and OUTB -** Alternate half cycle output stages. Each output is capable of 1A peak currents for driving power MOSFETs or MOSFET drivers. Each output provides very low impedance to overshoot and undershoot.

**SS -** Connect the soft-start timing capacitor between this pin and GND to control the duration of soft-start. The value of the capacitor determines the rate of increase of the duty cycle during start-up, controls the overcurrent shutdown delay, and the overcurrent and short circuit hiccup restart period.

**$V_{ERR}$** - The inverting input of the PWM comparator. The error voltage is applied to this pin to control the duty cycle. Increasing the signal level increases the duty cycle. The node may be driven with an external error amplifier or an opto-coupler.

**$V_{DDP}$ -** $V_{DDP}$ is the separate collector supply to the gate drive. Having a separate $V_{DDP}$ pin helps isolate the analog circuitry from the high power gate drive noise.

## Functional Description

### Features

The ISL6745 PWM is an excellent choice for low cost bridge topologies for applications requiring accurate frequency and deadtime control. Among its many features are 1A FET drivers, adjustable soft-start, overcurrent protection and internal thermal protection, allowing a highly flexible design with minimal external components.

### Oscillator

The ISL6745 has an oscillator with a frequency range to 2MHz, programmable using a resistor $R_{TD}$ and capacitor $C_T$.

The switching period may be considered to be the sum of the timing capacitor charge and discharge durations. The charge duration is determined by $C_T$ and the internal current source (assumed to be 160µA in the formula). The discharge duration is determined by $R_{TD}$ and $C_T$.

$$T_C \approx 1.25 \times 10^4 \bullet C_T \quad s \qquad \text{(EQ. 2)}$$

$$T_D \approx \frac{1}{CTDischargeCurrentGain} \bullet R_{TD} \bullet C_T \quad s \qquad \text{(EQ. 3)}$$

$$T_{OSC} = T_C + T_D = \frac{1}{F_{OSC}} \quad s \qquad \text{(EQ. 4)}$$

where $T_C$ and $T_D$ are the approximate charge and discharge times, respectively, $T_{OSC}$ is the oscillator free running period, and $F_{OSC}$ is the oscillator frequency. One output switching cycle requires two oscillator cycles. The actual times will be slightly longer than calculated due to internal propagation delays of approximately 5ns/transition. This delay adds directly to the switching duration, and also causes overshoot of the timing capacitor peak and valley voltage thresholds, effectively increasing the peak-to-peak voltage on the timing capacitor. Additionally, if very low charge and discharge currents are used, there will be an increased error due to the input impedance at the $C_T$ pin.

The above formulae help with the estimation of the frequency. Practically, effects like stray capacitances that affect the overall $C_T$ capacitance, variation in $R_{TD}$ voltage and charge current over temperature, etc. exist, and are best evaluated in-circuit. Equation 2 follows from the basic capacitor current equation, $i = C \times \frac{dV}{dt}$. In this case, with

variation in dV with $R_{TD}$ (Figure 5), and in charge current (Figure 4), results from Equation 2 would differ from the calculated frequency. The typical performance curves may be used as a tool along with the previous equations as a more accurate tool to estimate the operating frequency more accurately.

The maximum duty cycle, D, and deadtime, DT, can be calculated from:

$$D = T_C / T_{OSC} \quad \text{(EQ. 5)}$$

$$DT = (1 - D) \cdot T_{OSC} \quad s \quad \text{(EQ. 6)}$$

### Soft-Start Operation

The ISL6745 features a soft-start using an external capacitor in conjunction with an internal current source. Soft-start reduces stresses and surge currents during start-up.

The oscillator capacitor signal, $C_T$, is compared to the soft-start voltage, SS, in the SS comparator which drives the PWM latch. While the SS voltage is less than 3.5V, duty cycle is limited. The output pulse width increases as the soft-start capacitor voltage increases up to 3.5V. This has the effect of increasing the duty cycle from zero to the maximum pulse width during the soft-start period. When the soft-start voltage exceeds 3.5V, soft-start is completed. Soft-start occurs during start-up and after recovery from an overcurrent shutdown. The soft-start voltage is clamped to 4V.

### Gate Drive

The ISL6745 is capable of sourcing and sinking 1A peak current, and may also be used in conjunction with a MOSFET driver such as the ISL6700 for level shifting. To limit the peak current through the IC, an external resistor may be placed between the totem-pole output of the IC (OUTA or OUTB pin) and the gate of the MOSFET. This small series resistor also damps any oscillations caused by the resonant tank of the parasitic inductances in the traces of the board and the FET's input capacitance.

### Overcurrent Operation

Overcurrent delayed shutdown is enabled once the soft-start cycle is complete. If an overcurrent condition is detected, the soft-start charging current source is disabled and the soft-start capacitor is allowed to discharge through a 15µA source. At the same time a 50µs retriggerable one-shot timer is activated. It remains active for 50µs after the overcurrent condition ceases. If the soft-start capacitor discharges to 3.9V, the output is disabled. This state continues until the soft-start voltage reaches 270mV, at which time a new soft-start cycle is initiated. If the overcurrent condition stops at least 50µs prior to the soft-start voltage reaching 3.9V, the soft-start charging currents revert to normal operation and the soft-start voltage is allowed to recover.

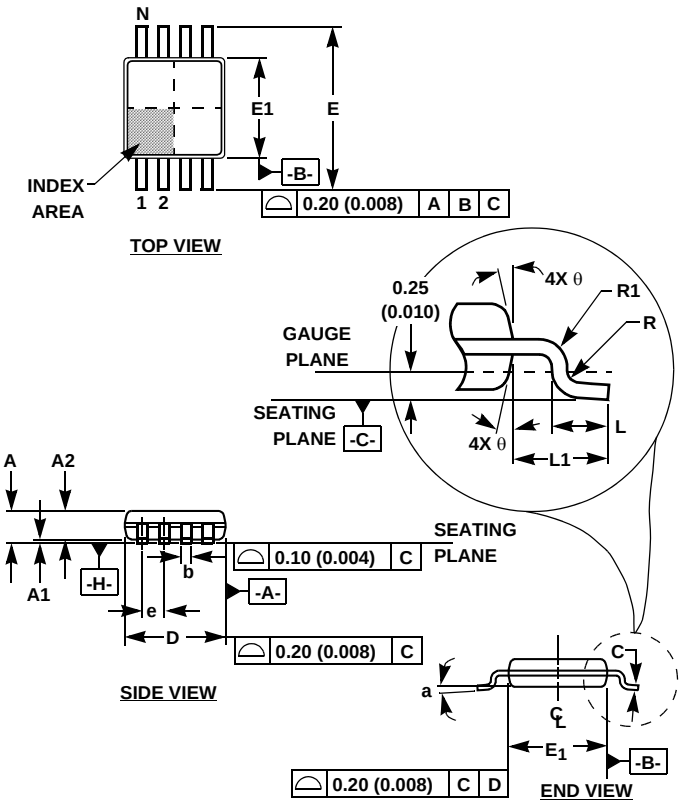
### Thermal Protection

An internal temperature sensor protects the device should the junction temperature exceed 145°C. There is approximately 15°C of hysteresis.

### Ground Plane Requirements

Careful layout is essential for satisfactory operation of the device. A good ground plane must be employed. $V_{DD}$ should be bypassed directly to GND with good high frequency capacitance.

## Mini Small Outline Plastic Packages (MSOP)




### M10.118 (JEDEC MO-187BA)

**10 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | 0.037 | 0.043 | 0.94 | 1.10 | - |
| A1 | 0.002 | 0.006 | 0.05 | 0.15 | - |
| A2 | 0.030 | 0.037 | 0.75 | 0.95 | - |
| b | 0.007 | 0.011 | 0.18 | 0.27 | 9 |
| c | 0.004 | 0.008 | 0.09 | 0.20 | - |
| D | 0.116 | 0.120 | 2.95 | 3.05 | 3 |
| E1 | 0.116 | 0.120 | 2.95 | 3.05 | 4 |
| e | 0.020 BSC | | 0.50 BSC | | - |
| E | 0.187 | 0.199 | 4.75 | 5.05 | - |
| L | 0.016 | 0.028 | 0.40 | 0.70 | 6 |
| L1 | 0.037 REF | | 0.95 REF | | - |
| N | 10 | | 10 | | 7 |
| R | 0.003 | - | 0.07 | - | - |
| R1 | 0.003 | - | 0.07 | - | - |
| θ | $5^o$ | $15^o$ | $5^o$ | $15^o$ | - |
| α | $0^o$ | $6^o$ | $0^o$ | $6^o$ | - |

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NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-187BA.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Dimension “D” does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions and are measured at Datum Plane. [ - H - ] Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. Formed leads shall be planar with respect to one another within 0.10mm (.004) at seating Plane.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Datums [ -A - ] and [ - B - ] to be determined at Datum plane [ - H - ].
11. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only

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