



PSMN034-100BS

N-channel 100 V 34.5 mΩ standard level MOSFET in D2PAK.

Rev. 2 — 2 March 2012

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel MOSFET in D2PAK package qualified to 175°C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive

1.3 Applications

- DC-to-DC converters
- Motor control
- Load switching
- Server power supplies

1.4 Quick reference data

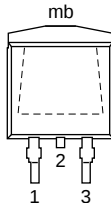
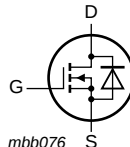
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	-	100	V
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 10 V; see Figure 1	-	-	32	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	-	86	W
T _j	junction temperature		-55	-	175	°C
Static characteristics						
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 15 A; T _j = 100 °C; see Figure 12	-	-	62	mΩ
		V _{GS} = 10 V; I _D = 15 A; T _j = 25 °C; see Figure 13	-	29.3	34.5	mΩ
Dynamic characteristics						
Q _{GD}	gate-drain charge	V _{GS} = 10 V; I _D = 15 A; V _{DS} = 50 V; see Figure 14 ; see Figure 15	-	6.9	-	nC
Q _{G(tot)}	total gate charge		-	23.8	-	nC
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(init)} = 25 °C; I _D = 32 A; V _{sup} ≤ 100 V; unclamped; R _{GS} = 50 Ω	-	-	42	mJ



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain ^[1]		
3	S	source		
mb	D	mounting base; connected to drain		
SOT404 (D2PAK)				

[1] It is not possible to make connection to pin 2

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN034-100BS	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	100	V
V_{DGR}	drain-gate voltage	$T_j \leq 175\text{ °C}$; $T_j \geq 25\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	100	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; see Figure 1	-	22	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1	-	32	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; see Figure 3	-	127	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	86	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	32	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$	-	127	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; $I_D = 32\text{ A}$; $V_{sup} \leq 100\text{ V}$; unclamped; $R_{GS} = 50\text{ }\Omega$	-	42	mJ

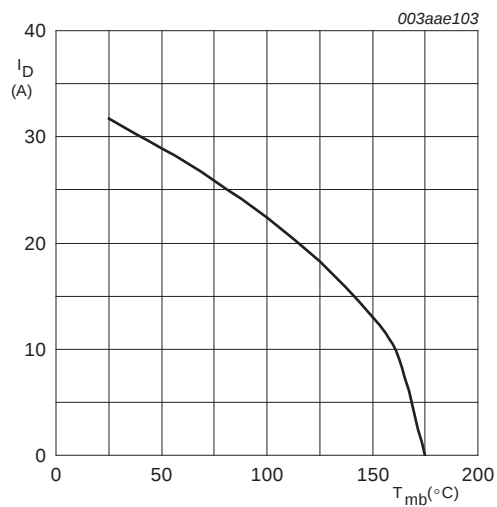


Fig 1. Continuous drain current as a function of mounting base temperature

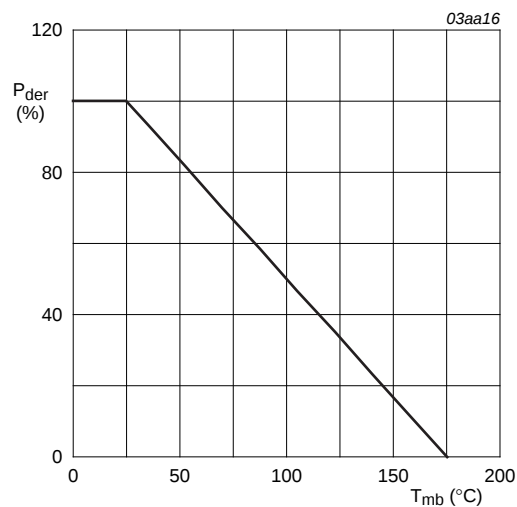


Fig 2. Normalized total power dissipation as a function of mounting base temperature

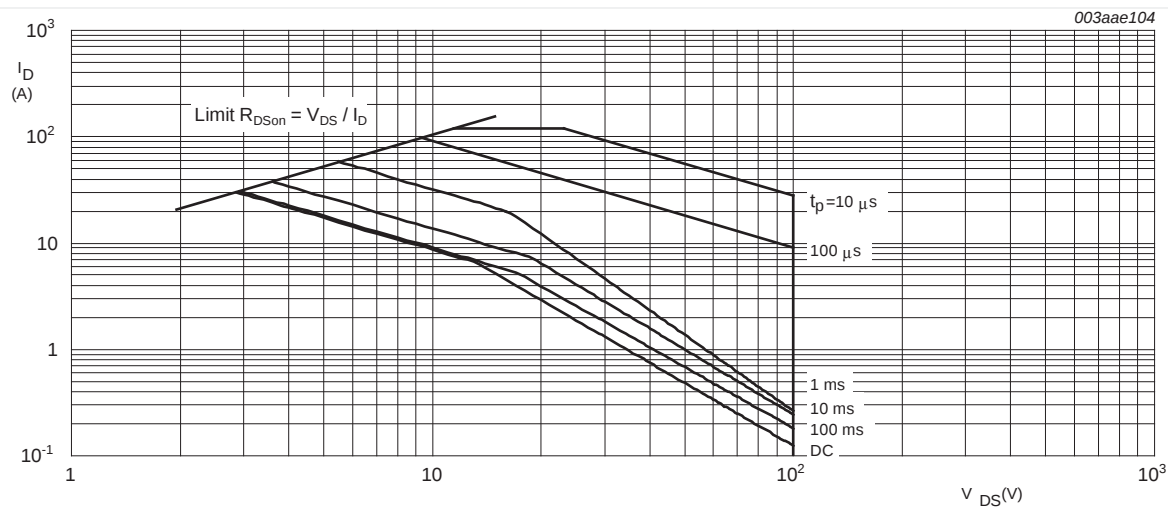
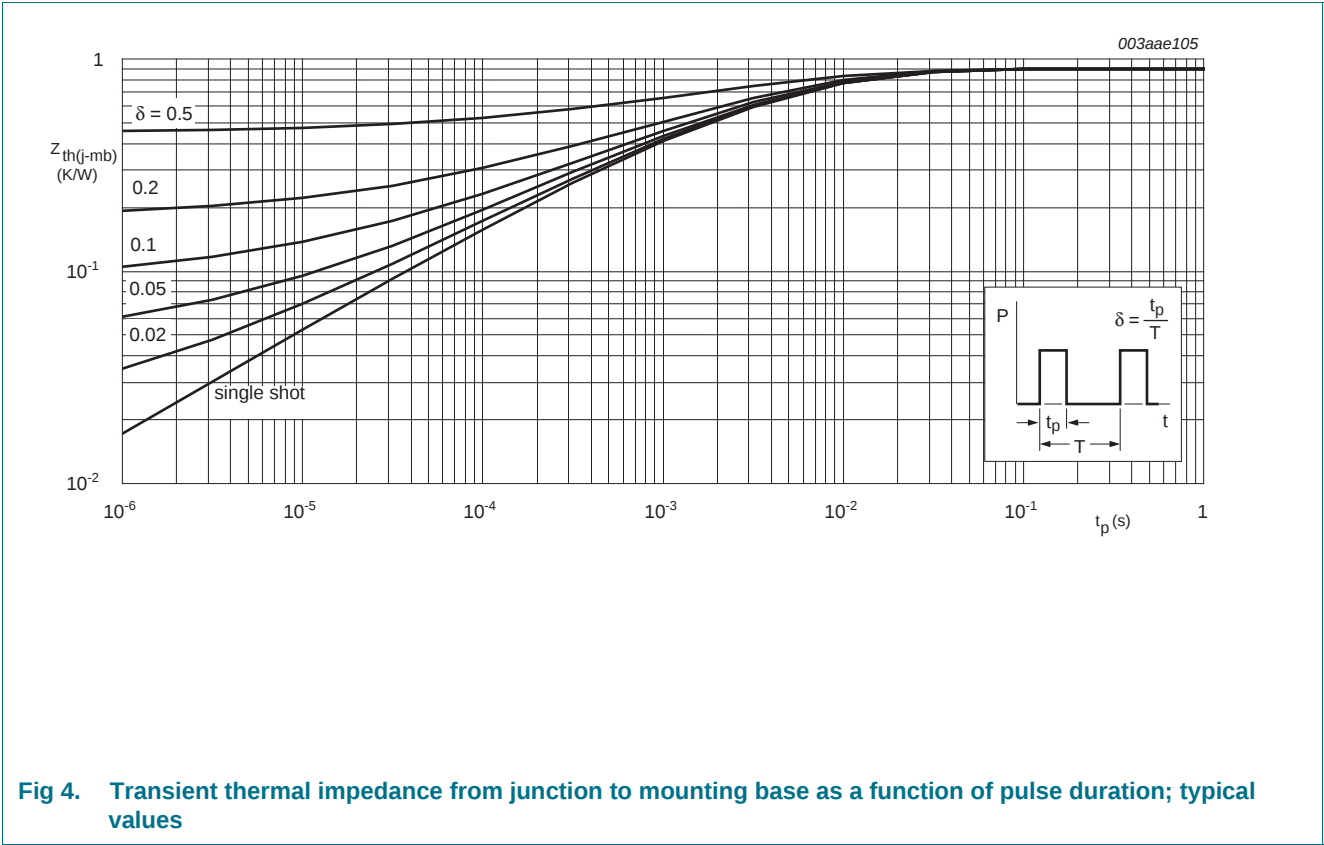


Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	0.9	1.7	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	50	-	K/W



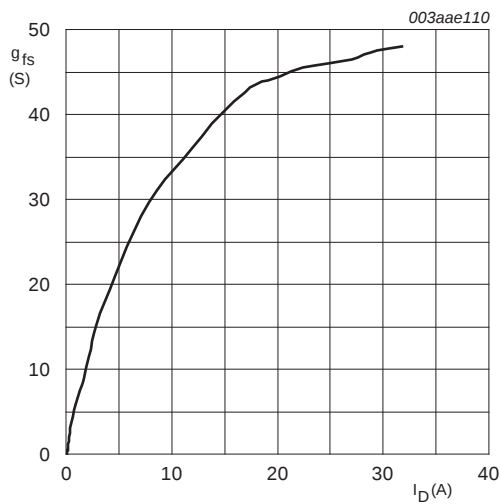
6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^{\circ}\text{C}$	90	-	-	V
		$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^{\circ}\text{C}$	100	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^{\circ}\text{C};$ see Figure 10	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^{\circ}\text{C};$ see Figure 11 ; see Figure 10	2	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^{\circ}\text{C};$ see Figure 10 ; see Figure 11	-	-	4.8	V
I_{DSS}	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^{\circ}\text{C}$	-	-	50	μA
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^{\circ}\text{C}$	-	0.02	1	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^{\circ}\text{C}$	-	10	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^{\circ}\text{C}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 100 \text{ }^{\circ}\text{C};$ see Figure 12	-	-	62	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 175 \text{ }^{\circ}\text{C};$ see Figure 12	-	82.1	96	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ }^{\circ}\text{C};$ see Figure 13	-	29.3	34.5	mΩ
R_G	internal gate resistance (AC)	$f = 1 \text{ MHz}$	-	1	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 15 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V};$ see Figure 14 ; see Figure 15	-	23.8	-	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	19	-	nC
Q_{GS}	gate-source charge	$I_D = 15 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V};$ see Figure 14 ; see Figure 15	-	5.5	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge	$I_D = 15 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V};$ see Figure 14	-	3.6	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	1.9	-	nC
Q_{GD}	gate-drain charge	$I_D = 15 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V};$ see Figure 14 ; see Figure 15	-	6.9	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$V_{DS} = 50 \text{ V};$ see Figure 14 ; see Figure 15	-	4.4	-	V
C_{iss}	input capacitance	$V_{DS} = 50 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$	-	1201	-	pF
C_{oss}	output capacitance	$T_j = 25 \text{ }^{\circ}\text{C};$ see Figure 16	-	94	-	pF
C_{rss}	reverse transfer capacitance		-	61	-	pF

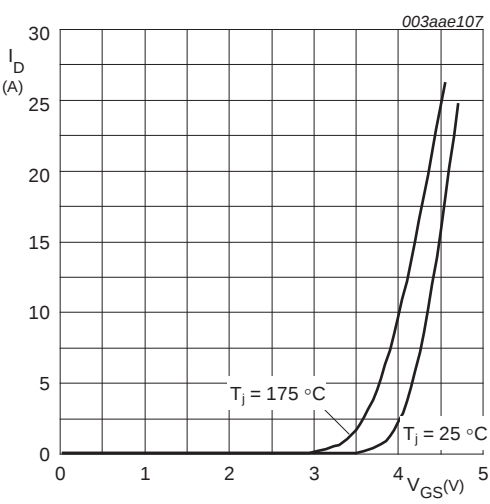
Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t _{d(on)}	turn-on delay time	V _{DS} = 50 V; R _L = 3.3 Ω; V _{GS} = 10 V; R _{G(ext)} = 4.7 Ω; T _j = 25 °C	-	12	-	ns
t _r	rise time		-	10	-	ns
t _{d(off)}	turn-off delay time		-	28	-	ns
t _f	fall time		-	9	-	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 15 A; V _{GS} = 0 V; T _j = 25 °C; see Figure 17	-	0.85	1.2	V
t _{rr}	reverse recovery time	I _S = 5 A; dI _S /dt = 100 A/μs; V _{GS} = 0 V;	-	38	-	ns
Q _r	recovered charge	V _{DS} = 50 V	-	59	-	nC



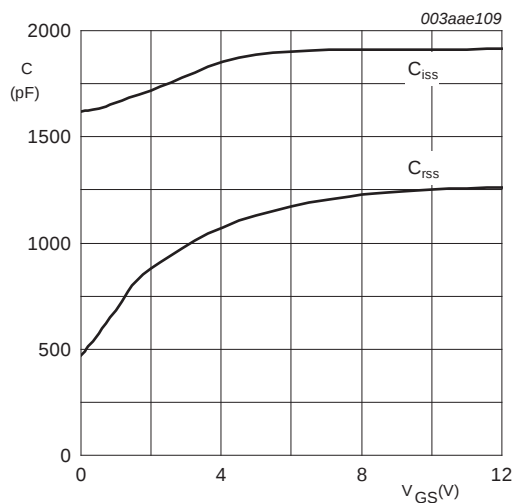
$T_j = 25^\circ\text{C}; V_{DS} = 10\text{ V}$

Fig 5. Forward transconductance as a function of drain current; typical values



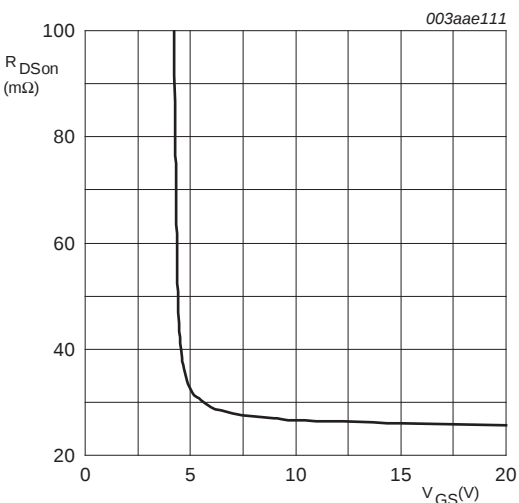
$T_j = 25^\circ\text{C}; V_{DS} = 15\text{ V}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



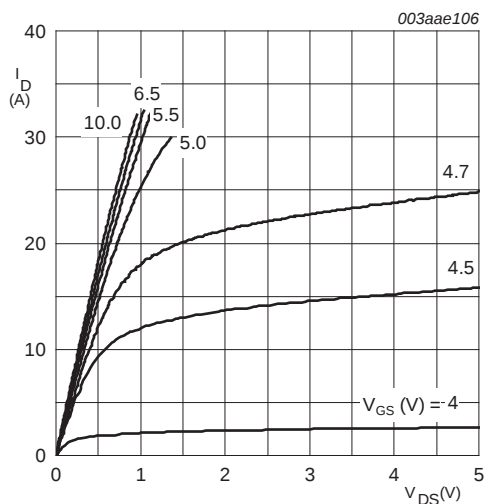
$V_{DS} = 0V; f = 1MHz$

Fig 7. Input and reverse capacitances as a function of gate-source voltage; typical values



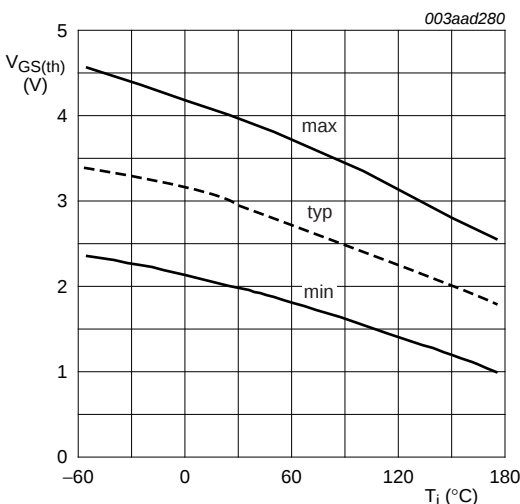
$T_j = 25^{\circ}C; I_D = 5A$

Fig 8. Drain-source on-state resistance as a function of gate-source voltage; typical values



$T_j = 25^{\circ}C; t_p = 300\mu s$

Fig 9. Output characteristics: drain current as a function of drain-source voltage; typical values



$I_D = 1mA; V_{DS} = V_{GS}$

Fig 10. Gate-source threshold voltage as a function of junction temperature

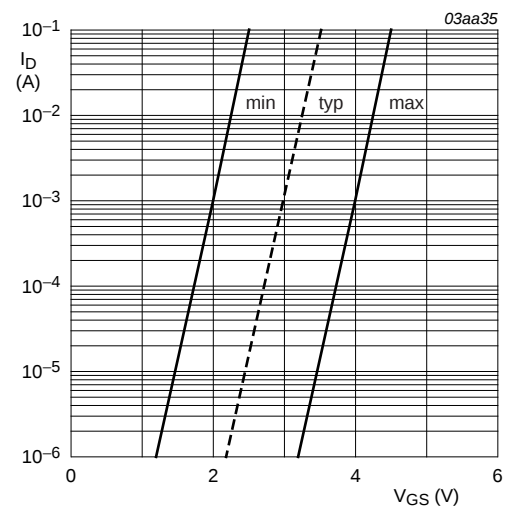


Fig 11. Sub-threshold drain current as a function of gate-source voltage

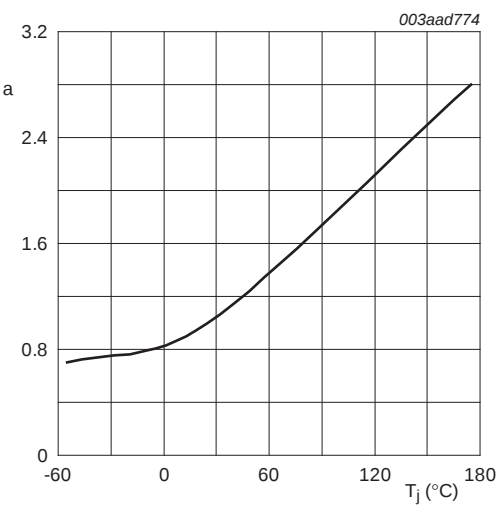


Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature

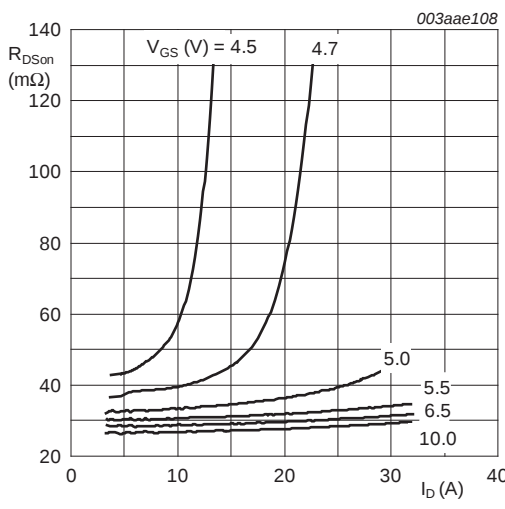


Fig 13. Drain-source on-state resistance as a function of drain current; typical values

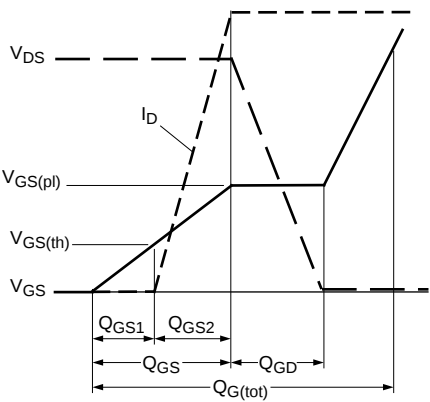


Fig 14. Gate charge waveform definitions

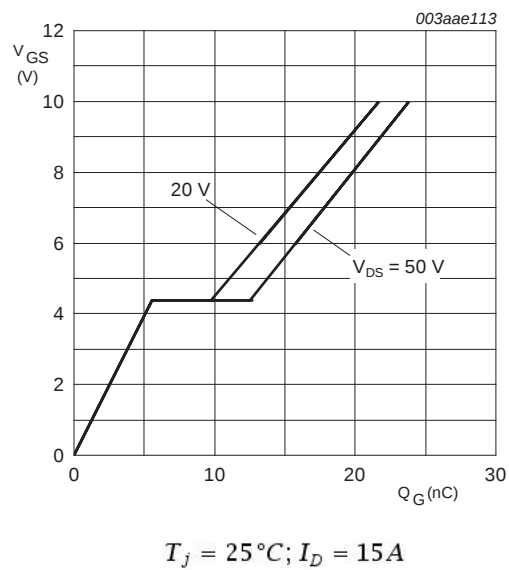


Fig 15. Gate-source voltage as a function of gate charge; typical values

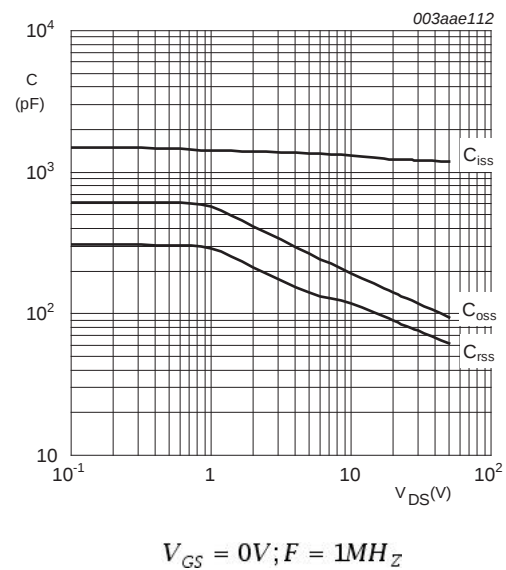


Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

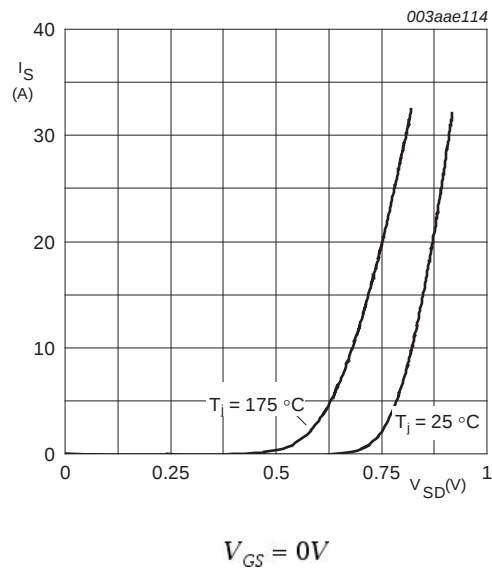


Fig 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404

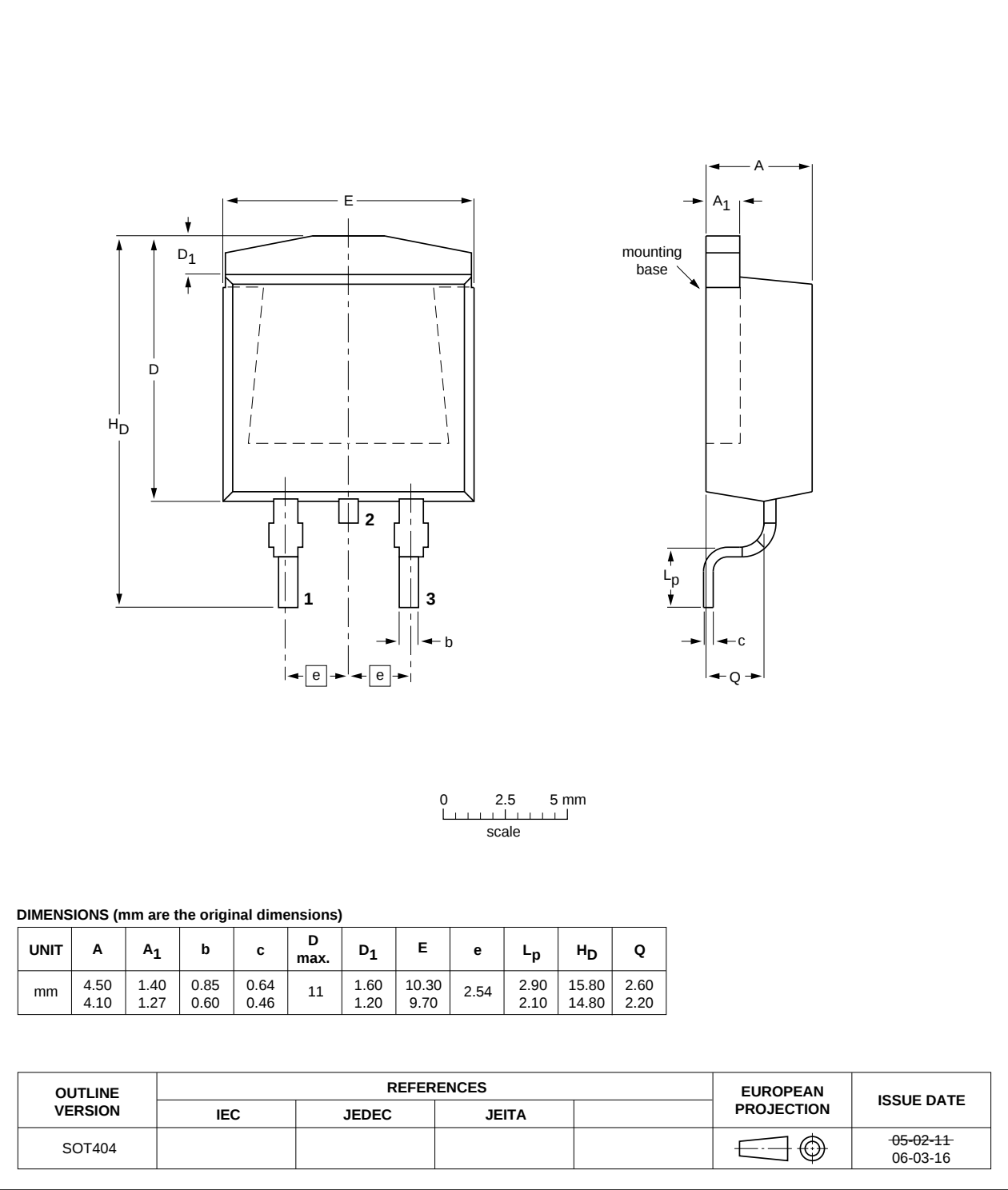


Fig 18. Package outline SOT404 (D2PAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN034-100BS v.2	20120302	Product data sheet	-	PSMN034-100BS v.1
Modifications:	• Status changed from objective to product. • Various changes to content.			
PSMN034-100BS v.1	20111027	Objective data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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