19-1210; Rev 3; 3/07

EVALUATION KIT AVAILABLE

+3.3V, 622Mbps, SDH/SONET 1:8 Deserializer with TTL Outputs

General Description

The MAX3680/MAX3680A deserializer is ideal for converting 622Mbps serial data to 8-bit-wide, 77Mbps parallel data in ATM and SDH/SONET applications. Operating from a single +3.3V supply, this device accepts PECL serial clock and data inputs, and delivers TTL clock and data outputs. The MAX3680 also provides a TTL synchronization input that enables data realignment and reframing.

The MAX3680/MAX3680A is available in the extended-industrial temperature range (-40°C to +85°C), in a 28-pin SSOP package.

Applications

622Mbps SDH/SONET Transmission Systems

622Mbps ATM/SONET Access Nodes

Add/Drop Multiplexers

Digital Cross-Connects

Pin Configuration appears at end of data sheet.

Features

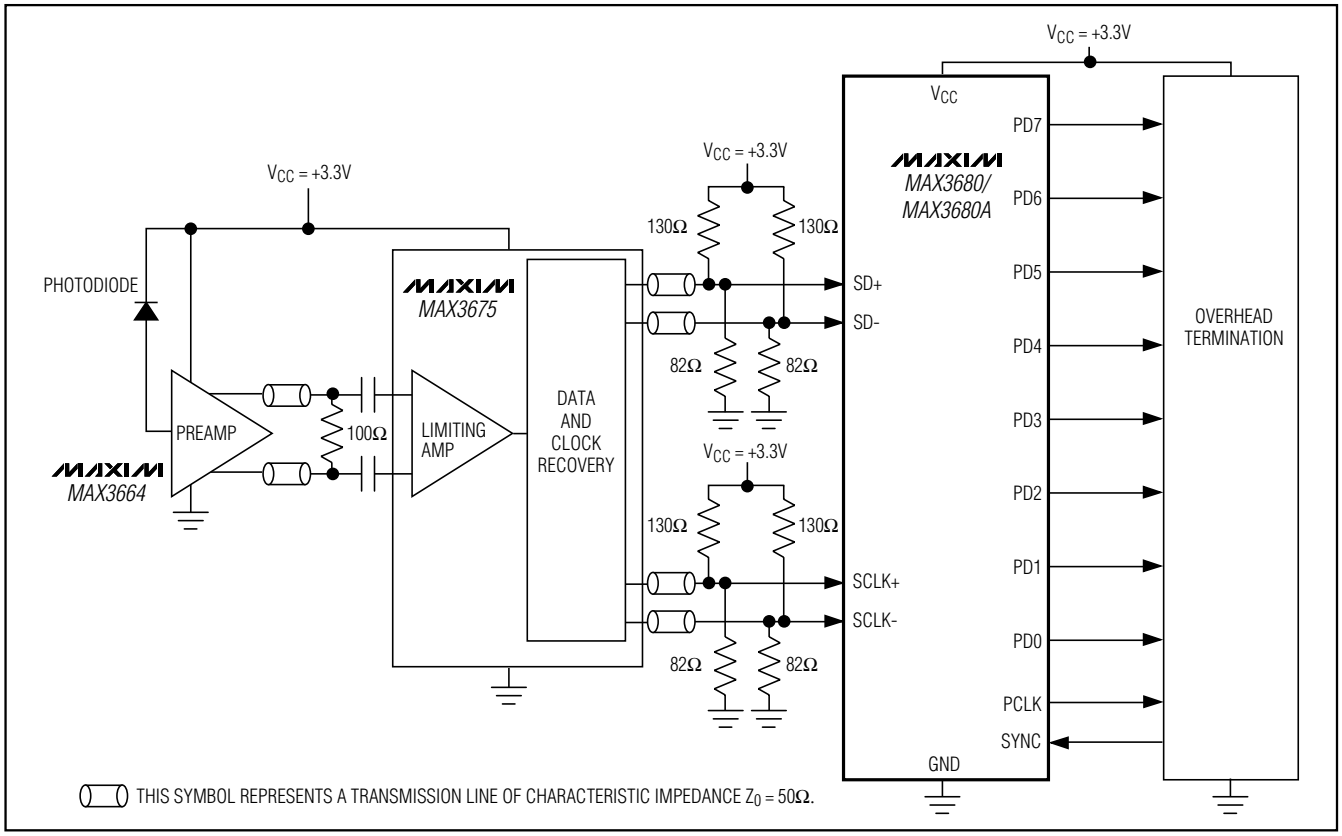
- **Single +3.3V Supply**
- **622Mbps Serial to 77Mbps Parallel Conversion**
- **165mW Power**
- **Synchronization Input for Data Realignment and Reframing (MAX3680)**
- **Differential 3.3V PECL Clock and Data Inputs**
- **TTL Data Outputs**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3680EAI	-40°C to +85°C	28 SSOP
MAX3680EAI+	-40°C to +85°C	28 SSOP
MAX3680AEAI	-40°C to +85°C	28 SSOP

+Denotes lead-free package.

Typical Operating Circuit



+3.3V, 622Mbps, SDH/SONET 1:8 Deserializer with TTL Outputs

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)
- V_{CC} .....-0.5V to +5V
- PECL Inputs (SD+/-, SCLK+/-) .....-0.5V to (V_{CC} + 0.5V)
- TTL Input (SYNC) .....-0.5V to (V_{CC} + 0.5V)
- TTL Outputs (PCLK, PD_).....-0.5V to (V_{CC} + 0.5V)

Continuous Power Dissipation (T_A = +85°C)
- SSOP (derate 9.52mW/°C above +85°C) 619mW

Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	TTL outputs = high	25	50	90	mA
PECL INPUTS (SD+/-, SCLK+/-)						
Input High Voltage	V_{IH}		V_{CC} - 1.16		V_{CC} - 0.88	V
Input Low Voltage	V_{IL}		V_{CC} - 1.81		V_{CC} - 1.48	V
Input High Current	I_{IH}	$V_{IN} = V_{IH(MAX)}$	-10		10	µA
Input Low Current	I_{IL}	$V_{IN} = V_{IL(MAX)}$	-10		10	µA
TTL INPUT AND OUTPUTS (SYNC, PCLK, PD_) (Note 1)						
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{IH(MAX)}$	-10		10	µA
Input Low Current	I_{IL}	$V_{IN} = V_{IL(MAX)}$	-10		10	µA
Output High Voltage	V_{OH}	Output sourcing = 400µA	2.4		V_{CC}	V
Output Low Voltage	V_{OL}	Output sinking = 400µA	0		0.44	V

Note 1: The SYNC input is available only on the MAX3680.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = +25°C, unless otherwise noted.) (Note 2)

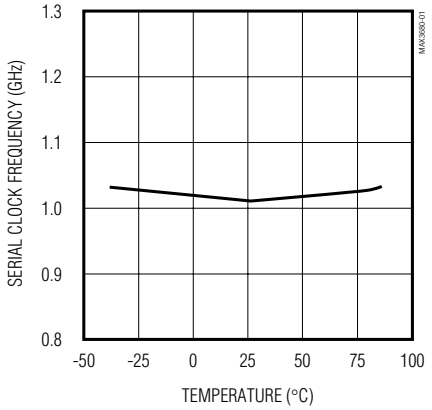
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Serial Clock Frequency	f_{SCLK}		622			MHz
Serial Data Setup Time	t_{SU}		800			ps
Serial Data Hold Time	t_H		50			ps
Parallel Clock to Data Output Delay	t_{CLK-Q}	V_{CC} = +3.3V, C_L = 18pF	-200	500	2000	ps

Note 2: AC characteristics guaranteed by design and characterization.

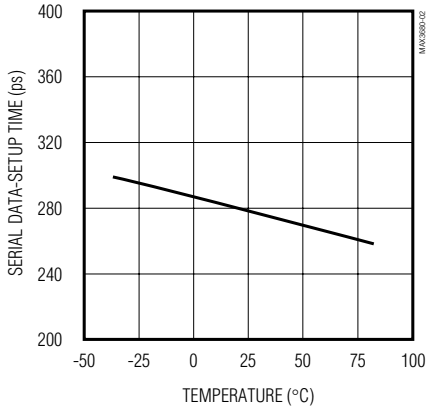
Typical Operating Characteristics

(V_{CC} = +3.0V to +3.6V, unless otherwise noted.)

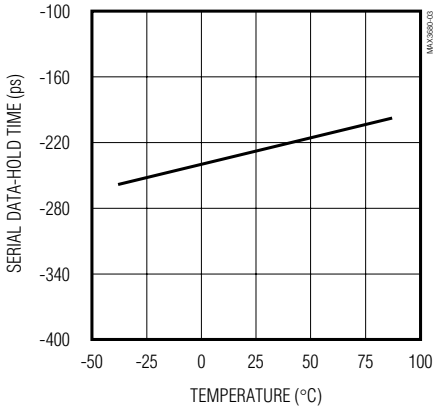
MAXIMUM SERIAL-CLOCK FREQUENCY vs. TEMPERATURE



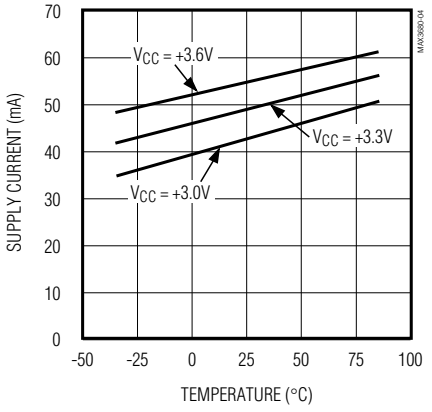
SERIAL DATA SETUP TIME vs. TEMPERATURE



SERIAL DATA HOLD TIME vs. TEMPERATURE



SUPPLY CURRENT vs. TEMPERATURE



+3.3V, 622Mbps, SDH/SONET 1:8 Deserializer with TTL Outputs

Pin Description

PIN		NAME	FUNCTION
MAX3680	MAX3680A		
1, 2, 5, 8, 14, 18, 25	1, 2, 5, 8, 14, 18, 25	V_{CC}	+3.3V Supply Voltage
3	3	SD+	Noninverting PECL Serial Data Input. Data is clocked on the SCLK signal's positive transition.
4	4	SD-	Inverting PECL Serial Data Input. Data is clocked on the SCLK signal's positive transition.
6	6	SCLK+	Noninverting PECL Serial Clock Input
7	7	SCLK-	Inverting PECL Serial Clock Input
9, 11, 12, 16, 20, 23, 27	11, 12, 16, 20, 23, 27	GND	Ground
10	—	SYNC	TTL Synchronization Pulse Input. Pulse high for at least two SCLK periods to shift the data alignment by dropping one bit in the serial input data stream.
—	9, 10	N.C.	No Connection
13	13	PCLK	TTL Parallel Clock Output
15, 17, 19, 21, 22, 24, 26, 28	15, 17, 19, 21, 22, 24, 26, 28	PD0–PD7	TTL Parallel Data Outputs. Data is updated on the falling edge of PCLK. See Figure 2 for the relationship between serial-data-bit position and output-data-bit assignment.

Detailed Description

The MAX3680/MAX3680A deserializer uses an 8-bit shift register, 8-bit parallel output register, 3-bit counter, PECL input buffers, and TTL input/output buffers to convert 622Mbps serial data to 8-bit-wide, 77Mbps parallel data (Figure 1).

The input shift register continuously clocks incoming data on the positive transition of the serial clock (SCLK) input signal. The 3-bit counter generates a parallel output clock (PCLK) by dividing down the serial clock frequency. The PCLK signal is used to clock the parallel output register. During normal operation, the counter divides the SCLK frequency by eight, causing the output register to latch every eight bits of incoming serial data.

The MAX3680 synchronization input (SYNC) is used for data realignment and reframing. When the SYNC signal is pulsed high for at least two SCLK cycles, PCLK is delayed by one SCLK cycle, causing the first incoming bit of the serial input data stream to be dropped. This realignment is guaranteed to occur within two PCLK cycles of the SYNC rising edge.

See Figure 2 for the functional timing diagrams and Figure 3 for the timing parameters diagram.

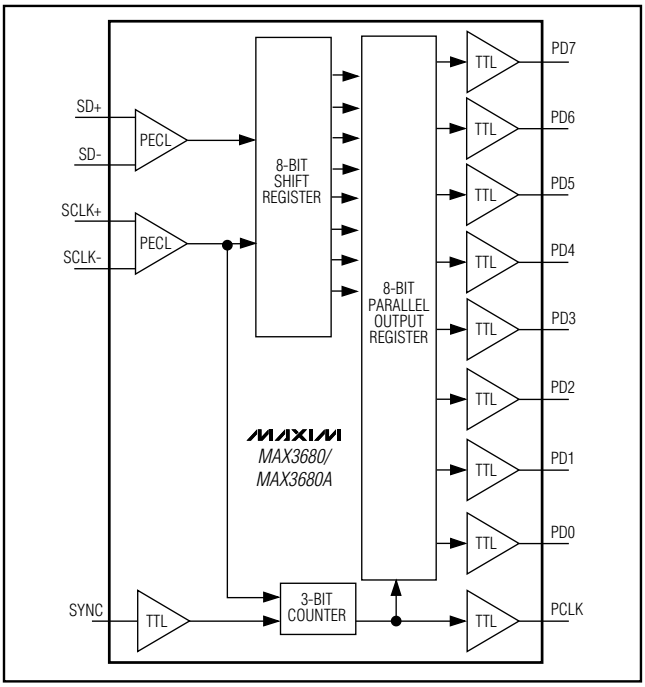


Figure 1. Functional Diagram

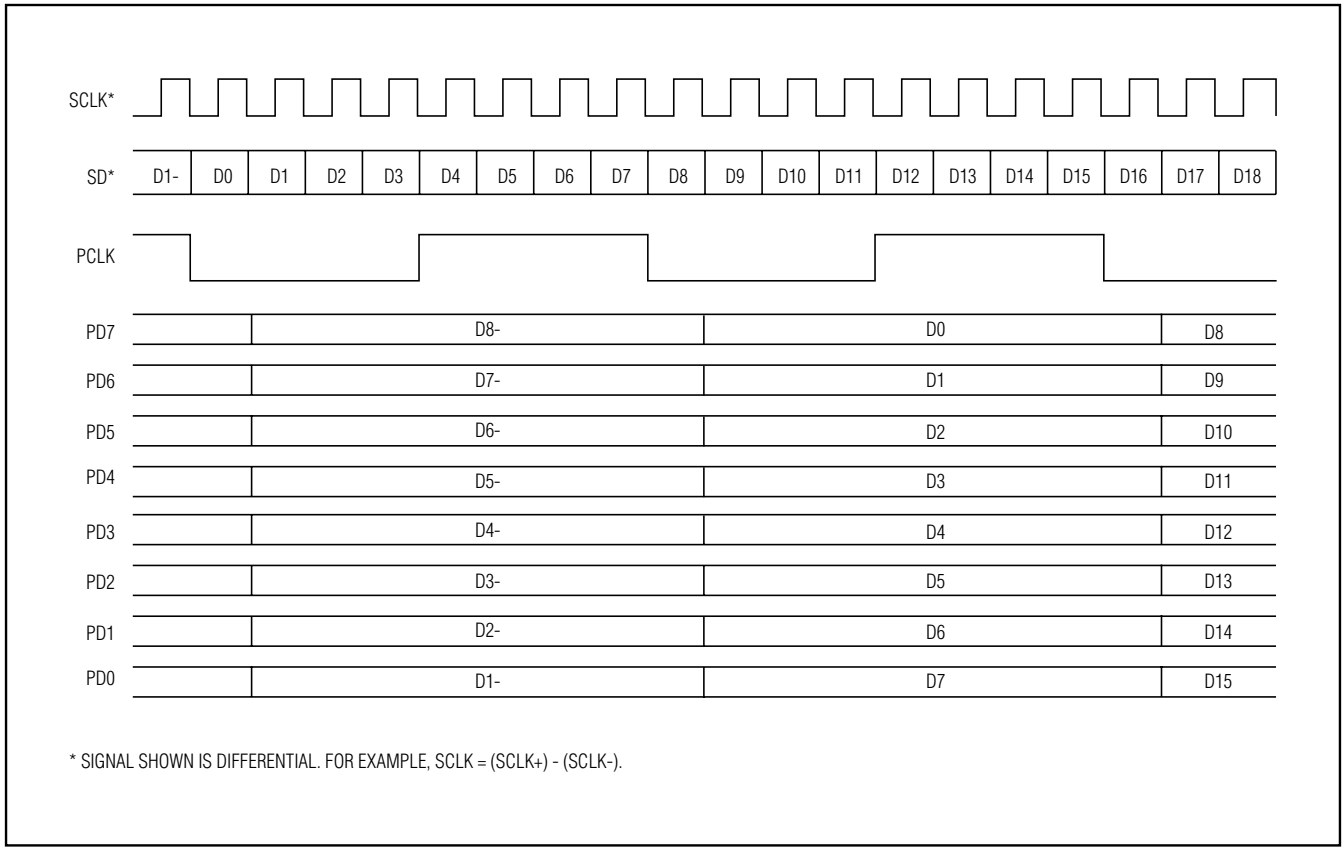


Figure 2a. Functional Timing Diagram—Normal Operation

+3.3V, 622Mbps, SDH/SONET 1:8 Deserializer with TTL Outputs

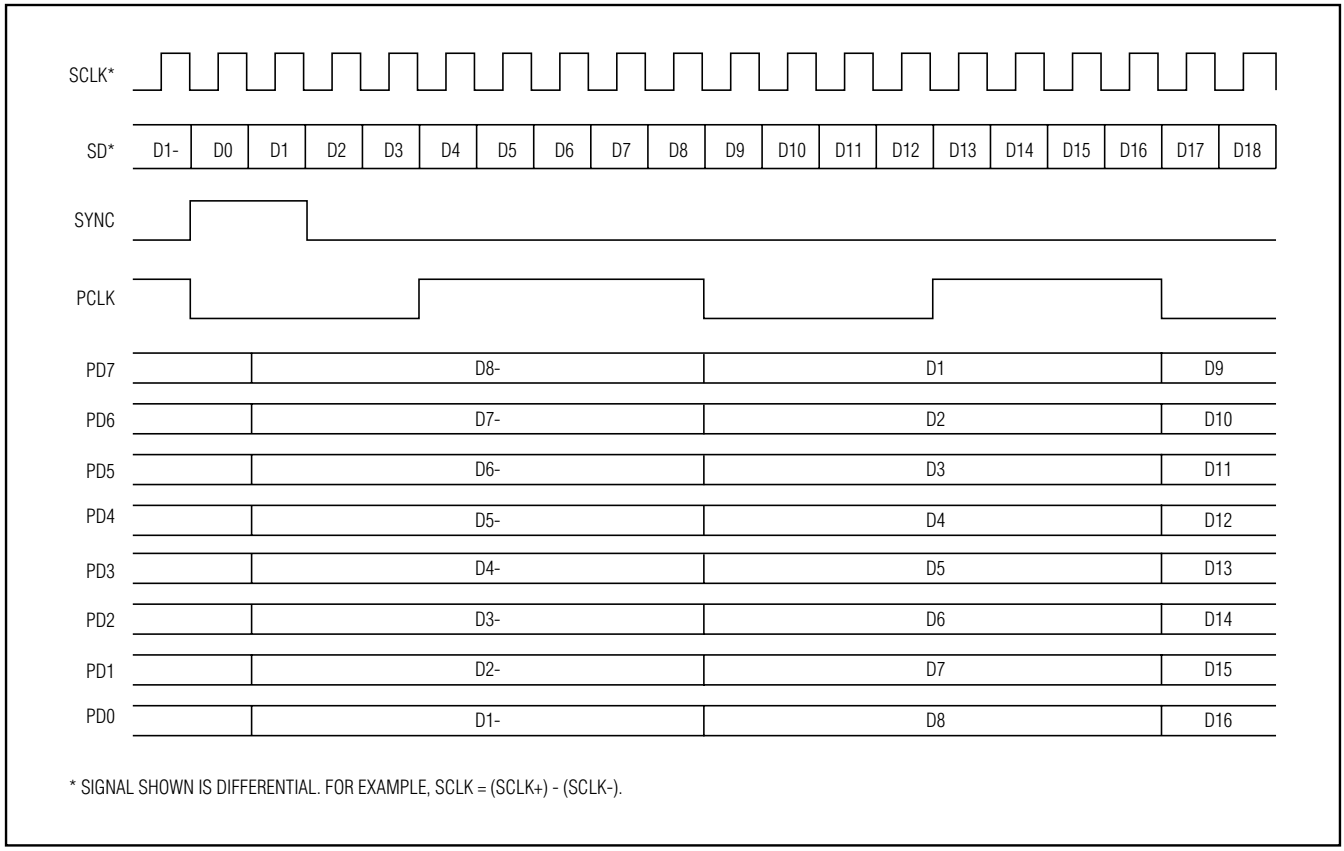


Figure 2b. Functional Timing Diagram—SYNC Operation (MAX3680)

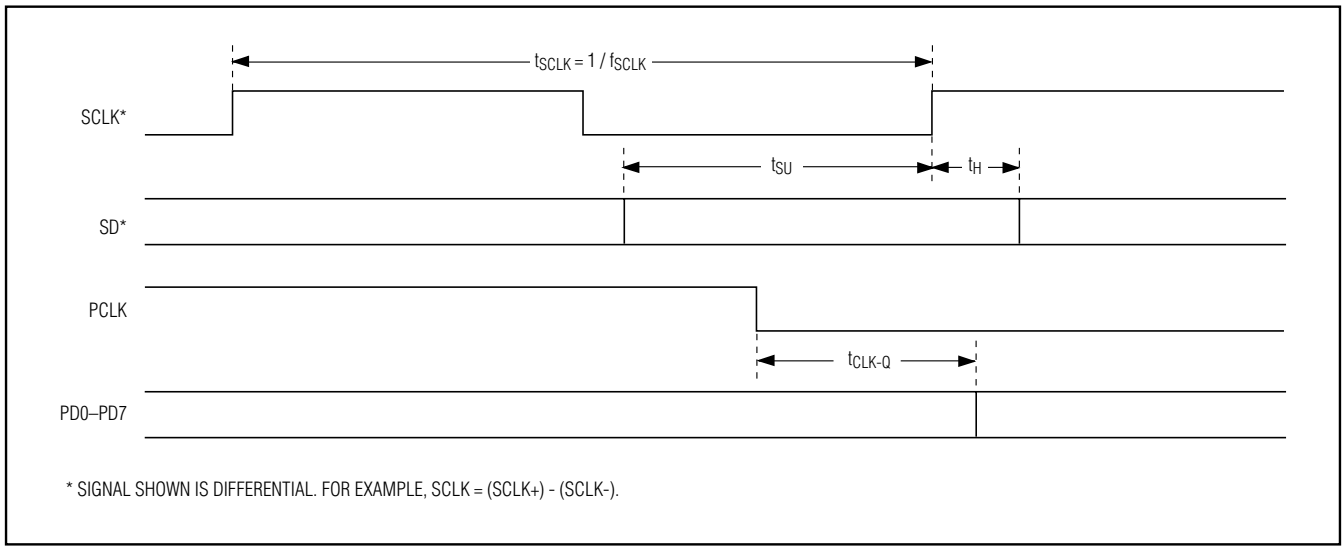


Figure 3. Timing Parameters

PECL Inputs

The serial data and clock PECL inputs (SD+, SD-, SCLK+, SCLK-) require 50Ω termination to (V_{CC} - 2V) when interfacing with a PECL source (see *Alternative PECL Input Termination*).

Applications Information

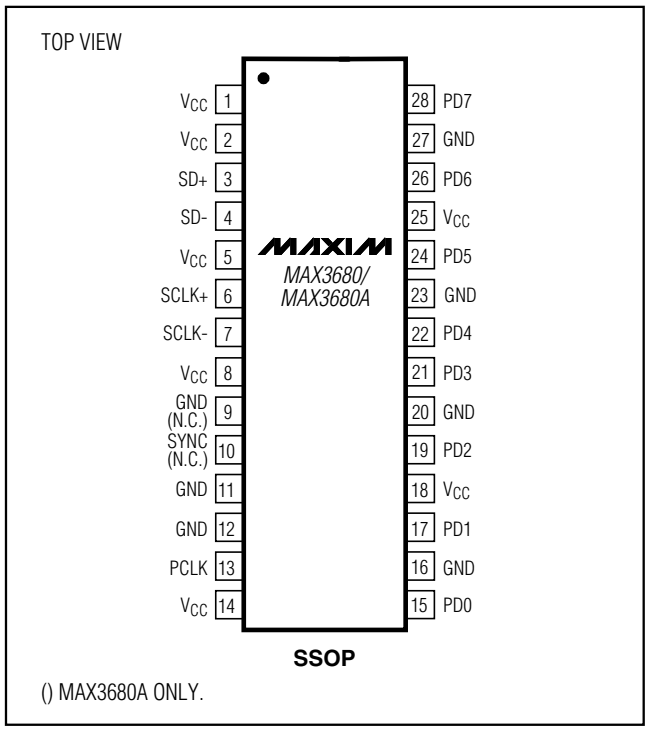
Alternative PECL Input Termination

Figure 4 shows alternative PECL input-termination methods. Use Thevenin-equivalent termination when a (V_{CC} - 2V) termination voltage is not available. If AC coupling is necessary, such as when interfacing with an ECL-output device, use the ECL AC-coupling termination.

Layout Techniques

For best performance, use good high-frequency layout techniques. Filter voltage supplies and keep ground connections short. Use multiple vias where possible. Also, use controlled impedance transmission lines to interface with the MAX3680 data inputs.

Pin Configuration



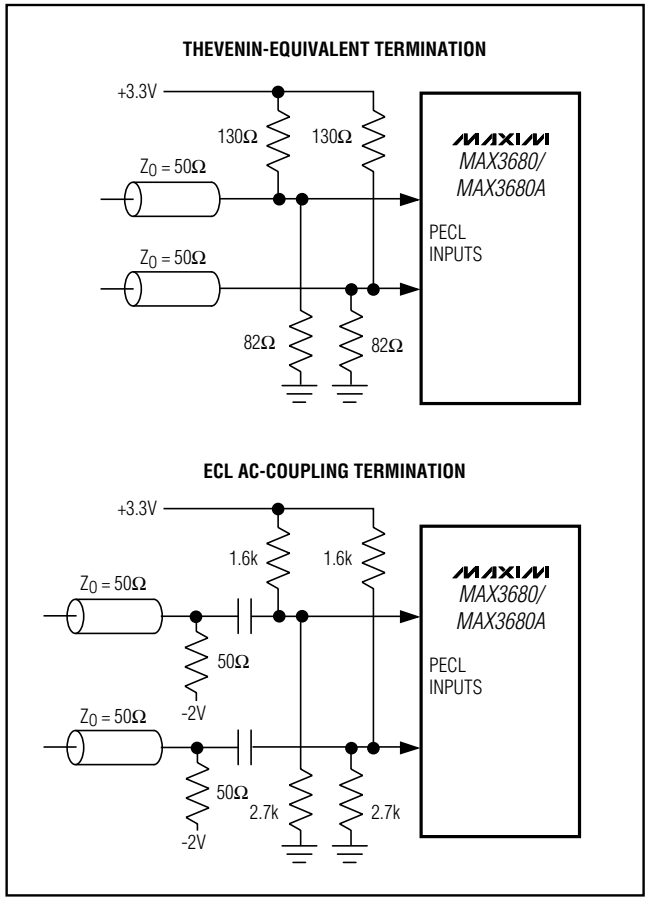


Figure 4. Alternative PECL Input Termination

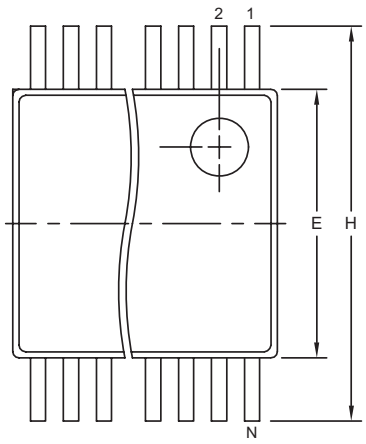
Chip Information

TRANSISTOR COUNT: 1346

+3.3V, 622Mbps, SDH/SONET 1:8 Deserializer with TTL Outputs

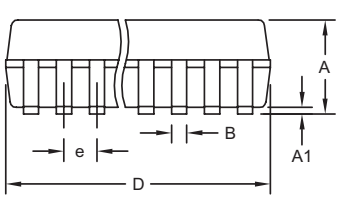
Package Information

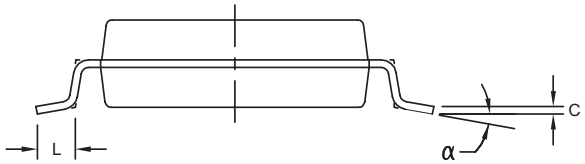
SSOP.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.212	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0∞	8∞	0∞	8∞

	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	N
D	0.239	0.249	6.07	6.33	14L
D	0.239	0.249	6.07	6.33	16L
D	0.278	0.289	7.07	7.33	20L
D	0.317	0.328	8.07	8.33	24L
D	0.397	0.407	10.07	10.33	28L





NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15 MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO150.
5. LEADS TO BE COPLANAR WITHIN 0.10 MM.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, SSOP, 5.3 MM
APPROVAL | DOCUMENT CONTROL NO. 21-0056 | REV. C | 1/1

Revision History

Rev 0; 3/97: Initial MAX3680 release.

Rev 1; 11/00: Changed t_{CLK-Q} max from 1300ps to 2000ps (page 2); replaced TOC3 (page 3).

Rev 2; 7/04: Added lead-free package to Ordering Information table (page 1).

Rev 3; 3/07: Added MAX3680A (pages 1, 2, 4, 6, 7).

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