

## 0.9-Ω SPST ANALOG SWITCH

Check for Samples: [TS5A3166](#)

### FEATURES

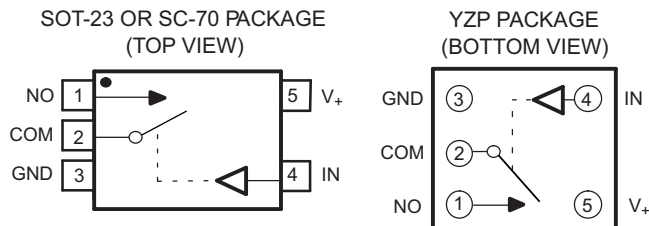
- Isolation in Powered-Off Mode,  $V_+ = 0$
- Low ON-State Resistance (0.9 Ω)
- Control Inputs Are 5.5-V Tolerant
- Low Charge Injection
- Low Total Harmonic Distortion (THD)
- 1.65-V to 5.5-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

### APPLICATIONS

- Cell Phones
- PDAs
- Portable Instrumentation
- Audio and Video Signal Routing
- Low-Voltage Data-Acquisition Systems
- Communication Circuits
- Modems
- Hard Drives
- Computer Peripherals
- Wireless Terminals and Peripherals
- Microphone Switching – Notebook Docking

### DESCRIPTION

The TS5A3166 is a single-pole single-throw (SPST) analog switch that is designed to operate from 1.65 V to 5.5 V. The device offers a low ON-state resistance. The device has excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications.



### ORDERING INFORMATION

For package and ordering information, see the Package Option Addendum at the end of this document.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**Summary Of Characteristics<sup>(1)</sup>**

Configuration	Single Pole Single Throw (SPST)
Number of channels	1
ON-state resistance ( $r_{on}$ )	0.9 $\Omega$
ON-state resistance flatness ( $r_{on(flat)}$ )	0.15 $\Omega$
Turn-on/turn-off time ( $t_{ON}/t_{OFF}$ )	7.5 ns/12.5 ns
Charge injection ( $Q_C$ )	1 pC
Bandwidth (BW)	200 MHz
OFF isolation ( $O_{ISO}$ )	-64 dB at 1 MHz
Total harmonic distortion (THD)	0.005%
Leakage current ( $I_{COM(OFF)}$ )	$\pm 20$ nA
Power-supply current ( $I_+$ )	0.5 $\mu$ A
Package option	5-pin DSBGA, SOT-23, or SC-70

(1)  $V_+ = 5$  V,  $T_A = 25^\circ$ C

**FUNCTION TABLE**

IN	NO TO COM, COM TO NO
L	OFF
H	ON

**Table 1. PIN DESCRIPTION**

PIN NUMBER	NAME	DESCRIPTION
1	NO	Normally closed
2	COM	Common
3	GND	Digital ground
4	IN	Digital control pin to connect COM to NO
5	$V_+$	Power Supply

**PARAMETER DESCRIPTION**

SYMBOL	DESCRIPTION
$V_{COM}$	Voltage at COM
$V_{NO}$	Voltage at NO
$r_{on}$	Resistance between COM and NO ports when the channel is ON
$r_{peak}$	Peak on-state resistance over a specified voltage range
$r_{on(flat)}$	Difference between the maximum and minimum value of $r_{on}$ in a channel over the specified range of conditions
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state under worst-case input and output conditions
$I_{NO(PWROFF)}$	Leakage current measured at the NO port during the power-down condition, $V_+ = 0$
$I_{COM(OFF)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO) in the OFF state under worst-case input and output conditions
$I_{COM(PWROFF)}$	Leakage current measured at the COM port during the power-down condition, $V_+ = 0$
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open

**PARAMETER DESCRIPTION (continued)**

SYMBOL	DESCRIPTION
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO) in the ON state and the output (NO) open
$V_{IH}$	Minimum input voltage for logic high for the control input (IN)
$V_{IL}$	Maximum input voltage for logic low for the control input (IN)
$V_I$	Voltage at the control input (IN)
$I_{IH}, I_{IL}$	Leakage current measured at the control input (IN)
$t_{ON}$	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning ON.
$t_{OFF}$	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning OFF.
$Q_C$	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NO or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$ , $C_L$ is the load capacitance, and $\Delta V_{COM}$ is the change in analog output voltage.
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
$C_{COM(OFF)}$	Capacitance at the COM port when the corresponding channel (COM to NO) is OFF
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NO) is ON
$C_I$	Capacitance of control input (IN)
$O_{ISO}$	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NO to COM) in the OFF state.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic.
$I_+$	Static power-supply current with the control (IN) pin at $V_+$ or GND

**Absolute Maximum Ratings<sup>(1) (2)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_+$	Supply voltage range <sup>(3)</sup>	–0.5	6.5	V
$V_{NO}$ $V_{COM}$	Analog voltage range <sup>(3) (4) (5)</sup>	–0.5	$V_+ + 0.5$	V
$I_K$	Analog port diode current	$V_{NO}, V_{COM} < 0$		mA
$I_{NO}$ $I_{COM}$	On-state switch current On-state peak switch current <sup>(6)</sup>	$V_{NO}, V_{COM} = 0$ to $V_+$		mA
$V_I$	Digital input voltage range <sup>(3) (4)</sup>	–0.5	6.5	V
$I_{IK}$	Digital clamp current	$V_I < 0$		mA
$I_+$	Continuous current through $V_+$			100 mA
$I_{GND}$	Continuous current through GND			–100 mA
$\theta_{JA}$	Package thermal impedance <sup>(7)</sup>	DBV package		206
		DCK package		252
		YZP package		132
$T_{stg}$	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (5) This value is limited to 5.5 V maximum.
- (6) Pulse at 1-ms duration < 10% duty cycle.
- (7) The package thermal impedance is calculated in accordance with JESD 51-7.

**Electrical Characteristics for 5-V Supply<sup>(1)</sup>**

$V_+ = 4.5\text{ V to }5.5\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Analog Switch</b>									
Analog signal range	$V_{COM}, V_{NO}$				0		$V_+$	V	
Peak ON resistance	$r_{peak}$	$0 \leq V_{NO} \leq V_+$ , $I_{COM} = -100\text{ mA}$ ,	Switch ON, See Figure 13	25°C	4.5 V	0.8	1.1	$\Omega$	
				Full			1.2		
ON-state resistance	$r_{on}$	$V_{NO} = 2.5\text{ V}$ , $I_{COM} = -100\text{ mA}$ ,	Switch ON, See Figure 13	25°C	4.5 V	0.7	0.9	$\Omega$	
				Full			1		
ON-state resistance flatness	$r_{on(Flat)}$	$0 \leq V_{NO} \leq V_+$ , $I_{COM} = -100\text{ mA}$ ,	Switch ON, See Figure 13	25°C	4.5 V	0.15		$\Omega$	
				25°C		0.09 0.15			
				Full		0.15			
NO OFF leakage current	$I_{NO(OFF)}$	$V_{NO} = 1\text{ V}$ , $V_{COM} = 4.5\text{ V}$ , or $V_{NO} = 4.5\text{ V}$ , $V_{COM} = 1\text{ V}$ ,	Switch OFF, See Figure 14	25°C	5.5 V	-20	4 20	nA	
				Full			-100		100
				25°C		0 V	-5		0.4 5
Full		-15	15						
COM OFF leakage current	$I_{COM(OFF)}$	$V_{COM} = 1\text{ V}$ , $V_{NO} = 4.5\text{ V}$ , or $V_{COM} = 4.5\text{ V}$ , $V_{NO} = 1\text{ V}$ ,	Switch OFF, See Figure 14	25°C	5.5 V	-20	4 20	nA	
				Full			-100		100
				25°C		0 V	-5		0.4 5
Full		-15	15						
NO ON leakage current	$I_{NO(ON)}$	$V_{NO} = 1\text{ V}$ , $V_{COM} = \text{Open}$ , or $V_{NO} = 4.5\text{ V}$ , $V_{COM} = \text{Open}$ ,	Switch ON, See Figure 15	25°C	5.5 V	-2	0.3 2	nA	
				Full			-20		20
COM ON leakage current	$I_{COM(ON)}$	$V_{COM} = 1\text{ V}$ , $V_{NO} = \text{Open}$ , or $V_{COM} = 4.5\text{ V}$ , $V_{NO} = \text{Open}$ ,	Switch ON, See Figure 15	25°C	5.5 V	-2	0.3 2	nA	
				Full			-20		20
<b>Digital Control Inputs (IN)</b>									
Input logic high	$V_{IH}$		Full		2.4		5.5	V	
Input logic low	$V_{IL}$		Full		0		0.8	V	
Input leakage current	$I_{IH}, I_{IL}$	$V_I = 5.5\text{ V or }0$	25°C	5.5 V	-2	0.3	2	nA	
			Full			-20	20		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

**Electrical Characteristics for 5-V Supply<sup>(1)</sup> (continued)**
 $V_+ = 4.5\text{ V to }5.5\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Dynamic</b>									
Turn-on time	$t_{ON}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , See Figure 17	25°C	5 V	2.5	4.5	7	ns
				Full	4.5 V to 5.5 V	1.5		7.5	
Turn-off time	$t_{OFF}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , See Figure 17	25°C	5 V	6	9	11.5	ns
				Full	4.5 V to 5.5 V	4		12.5	
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ ,	$C_L = 1\text{ nF}$ , See Figure 20	25°C	5 V		1	pC	
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	5 V		19	pF	
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	5 V		18	pF	
NO ON capacitance	$C_{NO(ON)}$	$V_{NO} = V_+$ or GND, Switch ON,	See Figure 16	25°C	5 V		35.5	pF	
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See Figure 16	25°C	5 V		35.5	pF	
Digital input capacitance	$C_I$	$V_I = V_+$ or GND,	See Figure 16	25°C	5 V		2	pF	
Bandwidth	BW	$R_L = 50\ \Omega$ , Switch ON,	See Figure 18	25°C	5 V		200	MHz	
OFF isolation	$O_{ISO}$	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ ,	Switch OFF, See Figure 19	25°C	5 V		-64	dB	
Total harmonic distortion	THD	$R_L = 600\ \Omega$ , $C_L = 50\text{ pF}$ ,	$f = 20\text{ Hz to }20\text{ kHz}$ , See Figure 21	25°C	5 V		0.005	%	
<b>Supply</b>									
Positive supply current	$I_+$	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	5.5 V		0.01	0.1	$\mu\text{A}$
				Full				0.5	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

**Electrical Characteristics for 3.3-V Supply<sup>(1)</sup>**

V<sub>+</sub> = 3 V to 3.6 V, T<sub>A</sub> = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T <sub>A</sub>	V <sub>+</sub>	MIN	TYP	MAX	UNIT	
<b>Analog Switch</b>									
Analog signal range	V <sub>COM</sub> , V <sub>NO</sub>				0		V <sub>+</sub>	V	
Peak ON resistance	r <sub>peak</sub>	0 ≤ V <sub>NO</sub> ≤ V <sub>+</sub> , I <sub>COM</sub> = –100 mA,	Switch ON, See Figure 13	25°C	3 V	1.1	1.5	Ω	
				Full		1.7			
ON-state resistance	r <sub>on</sub>	V <sub>NO</sub> = 2 V, I <sub>COM</sub> = –100 mA,	Switch ON, See Figure 13	25°C	3 V	1	1.4	Ω	
				Full		1.5			
ON-state resistance flatness	r <sub>on(flat)</sub>	0 ≤ V <sub>NO</sub> ≤ V <sub>+</sub> , I <sub>COM</sub> = –100 mA, V <sub>NO</sub> = 2 V, 0.8 V, I <sub>COM</sub> = –100 mA,	Switch ON, See Figure 13	25°C	3 V	0.3		Ω	
				25°C		0.09 0.15			
				Full		0.15			
NO OFF leakage current	I <sub>NO(OFF)</sub>	V <sub>NO</sub> = 1 V, V <sub>COM</sub> = 3 V, or V <sub>NO</sub> = 3 V, V <sub>COM</sub> = 1 V,	Switch OFF, See Figure 14	25°C	3.6 V	–2	0.5	2	nA
				Full		–20	20		
	I <sub>NO(PWROFF)</sub>	V <sub>NO</sub> = 0 to 3.6 V, V <sub>COM</sub> = 3.6 V to 0,		25°C	0 V	–1	0.1	1	μA
				Full		–5	5		
COM OFF leakage current	I <sub>COM(OFF)</sub>	V <sub>COM</sub> = 1 V, V <sub>NO</sub> = 3 V, or V <sub>COM</sub> = 3 V, V <sub>NO</sub> = 1 V,	Switch OFF, See Figure 14	25°C	3.6 V	–2	0.5	2	nA
				Full		–20	20		
	I <sub>COM(PWROFF)</sub>	V <sub>COM</sub> = 3.6 V to 0, V <sub>NO</sub> = 0 to 3.6 V,		25°C	0 V	–1	0.1	1	μA
				Full		–5	5		
NO ON leakage current	I <sub>NO(ON)</sub>	V <sub>NO</sub> = 1 V, V <sub>COM</sub> = Open, or V <sub>NO</sub> = 3 V, V <sub>COM</sub> = Open,	Switch ON, See Figure 15	25°C	3.6 V	–2	0.2	2	nA
				Full		–20	20		
COM ON leakage current	I <sub>COM(ON)</sub>	V <sub>COM</sub> = 1 V, V <sub>NO</sub> = Open, or V <sub>COM</sub> = 3 V, V <sub>NO</sub> = Open,	Switch ON, See Figure 15	25°C	3.6 V	–2	0.2	2	nA
				Full		–20	20		
<b>Digital Control Inputs (IN)</b>									
Input logic high	V <sub>IH</sub>		Full		2		5.5	V	
Input logic low	V <sub>IL</sub>		Full		0		0.8	V	
Input leakage current	I <sub>IH</sub> , I <sub>IL</sub>	V <sub>I</sub> = 5.5 V or 0	25°C	3.6 V	–2	0.3	2	nA	
			Full		–20	20			

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

**Electrical Characteristics for 3.3-V Supply<sup>(1)</sup> (continued)**
 $V_+ = 3\text{ V to }3.6\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Dynamic</b>									
Turn-on time	$t_{ON}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , See Figure 17	25°C	3.3 V	2	5	10	ns
				Full	3 V to 3.6 V	1.5		11	
Turn-off time	$t_{OFF}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , See Figure 17	25°C	3.3 V	6.5	9	12	ns
				Full	3 V to 3.6 V	4		13	
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ ,	$C_L = 1\text{ nF}$ , See Figure 21	25°C	3.3 V		1	pC	
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	3.3 V		19	pF	
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	3.3 V		18	pF	
NO ON capacitance	$C_{NO(ON)}$	$V_{NO} = V_+$ or GND, Switch ON,	See Figure 16	25°C	3.3 V		36	pF	
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See Figure 16	25°C	3.3 V		36	pF	
Digital input capacitance	$C_I$	$V_I = V_+$ or GND,	See Figure 16	25°C	3.3 V		2	pF	
Bandwidth	BW	$R_L = 50\ \Omega$ , Switch ON,	See Figure 18	25°C	3.3 V		200	MHz	
OFF isolation	$O_{ISO}$	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ ,	Switch OFF, See Figure 19	25°C	3.3 V		-64	dB	
Total harmonic distortion	THD	$R_L = 600\ \Omega$ , $C_L = 50\text{ pF}$ ,	$f = 20\text{ Hz to }20\text{ kHz}$ , See Figure 21	25°C	3.3 V		0.01	%	
<b>Supply</b>									
Positive supply current	$I_+$	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	3.6 V	0.01	0.1	$\mu\text{A}$	
				Full			0.25		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

**Electrical Characteristics for 2.5-V Supply<sup>(1)</sup>**

$V_+ = 2.3 \text{ V to } 2.7 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT		
<b>Analog Switch</b>										
Analog signal range	$V_{COM}, V_{NO}$			2.3 V	0		$V_+$	V		
Peak ON resistance	$r_{peak}$	$0 \leq V_{NO} \leq V_+$ , $I_{COM} = -100 \text{ mA}$ ,	Switch ON, See Figure 13	25°C	2.3 V	1.8	2.4	$\Omega$		
				Full					2.6	
ON-state resistance	$r_{on}$	$V_{NO} = 2 \text{ V}$ , $I_{COM} = -100 \text{ mA}$ ,	Switch ON, See Figure 13	25°C	2.3 V	1.2	2.1	$\Omega$		
				Full					2.4	
ON-state resistance flatness	$r_{on(Flat)}$	$0 \leq V_{NO} \leq V_+$ , $I_{COM} = -100 \text{ mA}$ ,	Switch ON, See Figure 13	25°C	2.3 V	0.7		$\Omega$		
				25°C					0.4	0.6
				Full						
NO OFF leakage current	$I_{NO(OFF)}$	$V_{NO} = 1 \text{ V}$ , $V_{COM} = 3 \text{ V}$ , or $V_{NO} = 3 \text{ V}$ , $V_{COM} = 1 \text{ V}$ ,	Switch OFF, See Figure 14	25°C	2.7 V	-5	0.3	5	nA	
				Full		-50	50			
	$I_{NO(PWROFF)}$	$V_{NO} = 0 \text{ to } 3.6 \text{ V}$ , $V_{COM} = 3.6 \text{ V to } 0$ ,	25°C	0 V	-2	0.05	2	$\mu\text{A}$		
Full	-15	15								
COM OFF leakage current	$I_{COM(OFF)}$	$V_{COM} = 1 \text{ V}$ , $V_{NO} = 3 \text{ V}$ , or $V_{COM} = 3 \text{ V}$ , $V_{NO} = 1 \text{ V}$ ,	Switch OFF, See Figure 14	25°C	2.7 V	-5	0.3	5	nA	
				Full		-50	50			
	$I_{COM(PWROFF)}$	$V_{COM} = 3.6 \text{ V to } 0$ , $V_{NO} = 0 \text{ to } 3.6 \text{ V}$ ,	25°C	0 V	-2	0.05	2	$\mu\text{A}$		
Full	-15	15								
NO ON leakage current	$I_{NO(ON)}$	$V_{NO} = 1 \text{ V}$ , $V_{COM} = \text{Open}$ , or $V_{NO} = 3 \text{ V}$ , $V_{COM} = \text{Open}$ ,	Switch ON, See Figure 15	25°C	2.7 V	-2	0.3	2	nA	
				Full		-20	20			
COM ON leakage current	$I_{COM(ON)}$	$V_{COM} = 1 \text{ V}$ , $V_{NO} = \text{Open}$ , or $V_{COM} = 3 \text{ V}$ , $V_{NO} = \text{Open}$ ,	Switch ON, See Figure 15	25°C	2.7 V	-2	0.3	2	nA	
				Full		-20	20			
<b>Digital Control Inputs (IN1, IN2)</b>										
Input logic high	$V_{IH}$		Full		1.8		5.5	V		
Input logic low	$V_{IL}$		Full		0		0.6	V		
Input leakage current	$I_{IH}, I_{IL}$	$V_I = 5.5 \text{ V or } 0$	25°C	2.7 V	-2	0.3	2	nA		
			Full		-20	20				

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum



**Electrical Characteristics for 2.5-V Supply<sup>(1)</sup> (continued)**
 $V_+ = 2.3 \text{ V to } 2.7 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Dynamic</b>								
Turn-on time	$t_{ON}$	$V_{COM} = V_+$ , $R_L = 50 \Omega$ , $C_L = 35 \text{ pF}$ , See Figure 17	25°C	2.5 V	2	6	10	ns
			Full	2.3 V to 2.7 V	1		12	
Turn-off time	$t_{OFF}$	$V_{COM} = V_+$ , $R_L = 50 \Omega$ , $C_L = 35 \text{ pF}$ , See Figure 17	25°C	2.5 V	4.5	8	10.5	ns
			Full	2.3 V to 2.7 V	3		15	
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ , $C_L = 1 \text{ nF}$ , See Figure 21	25°C	2.5 V		4		pC
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF, See Figure 16	25°C	2.5 V		19.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_+$ or GND, Switch OFF, See Figure 16	25°C	2.5 V		18.5		pF
NO ON capacitance	$C_{NO(ON)}$	$V_{NO} = V_+$ or GND, Switch ON, See Figure 16	25°C	2.5 V		36.5		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON, See Figure 16	25°C	2.5 V		36.5		pF
Digital input capacitance	$C_I$	$V_I = V_+$ or GND, See Figure 16	25°C	2.5 V		2		pF
Bandwidth	BW	$R_L = 50 \Omega$ , Switch ON, See Figure 18	25°C	2.5 V		150		MHz
OFF isolation	$O_{ISO}$	$R_L = 50 \Omega$ , $f = 1 \text{ MHz}$ , Switch OFF, See Figure 19	25°C	2.5 V		-62		dB
Total harmonic distortion	THD	$R_L = 600 \Omega$ , $C_L = 50 \text{ pF}$ , $f = 20 \text{ Hz to } 20 \text{ kHz}$ , See Figure 21	25°C	2.5 V		0.02		%
<b>Supply</b>								
Positive supply current	$I_+$	$V_I = V_+$ or GND, Switch ON or OFF	25°C	2.7 V	0.001	0.02		$\mu\text{A}$
			Full			0.25		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

**Electrical Characteristics for 1.8-V Supply<sup>(1)</sup>**

V<sub>+</sub> = 1.65 V to 1.95 V, T<sub>A</sub> = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T <sub>A</sub>	V <sub>+</sub>	MIN	TYP	MAX	UNIT
<b>Analog Switch</b>								
Analog signal range	V <sub>COM</sub> , V <sub>NO</sub>				0		V <sub>+</sub>	V
Peak ON resistance	r <sub>peak</sub>	0 ≤ V <sub>NO</sub> ≤ V <sub>+</sub> , I <sub>COM</sub> = –100 mA,	Switch ON, See Figure 13	25°C	1.65 V	4.2	25	Ω
				Full			30	
ON-state resistance	r <sub>on</sub>	V <sub>NO</sub> = 2 V, I <sub>COM</sub> = –100 mA,	Switch ON, See Figure 13	25°C	1.65 V	1.6	3.9	Ω
				Full			4.0	
ON-state resistance flatness	r <sub>on(flat)</sub>	0 ≤ V <sub>NO</sub> ≤ V <sub>+</sub> , I <sub>COM</sub> = –100 mA, V <sub>NO</sub> = 2 V, 0.8 V, I <sub>COM</sub> = –100 mA,	Switch ON, See Figure 13	25°C	1.65 V	2.8		Ω
				25°C		4.1 22		
				Full		27		
NO OFF leakage current	I <sub>NO(OFF)</sub>	V <sub>NO</sub> = 1 V, V <sub>COM</sub> = 3 V, or V <sub>NO</sub> = 3 V, V <sub>COM</sub> = 1 V,	Switch OFF, See Figure 14	25°C	1.95 V	–5	5	nA
				Full			–50	
	I <sub>NO(PWROFF)</sub>	V <sub>NO</sub> = 0 to 3.6 V, V <sub>COM</sub> = 3.6 V to 0,		25°C	0 V	–2	2	μA
				Full			–10	
COM OFF leakage current	I <sub>COM(OFF)</sub>	V <sub>COM</sub> = 1 V, V <sub>NO</sub> = 3 V, or V <sub>COM</sub> = 3 V, V <sub>NO</sub> = 1 V,	Switch OFF, See Figure 14	25°C	1.95 V	–5	5	nA
				Full			–50	
	I <sub>COM(PWROFF)</sub>	V <sub>COM</sub> = 0 to 3.6 V, V <sub>NO</sub> = 3.6 V to 0,		25°C	0 V	–2	2	μA
				Full			–10	
NO ON leakage current	I <sub>NO(ON)</sub>	V <sub>NO</sub> = 1 V, V <sub>COM</sub> = Open, or V <sub>NO</sub> = 3 V, V <sub>COM</sub> = Open,	Switch ON, See Figure 15	25°C	1.95 V	–2	2	nA
				Full			–20	
COM ON leakage current	I <sub>COM(ON)</sub>	V <sub>COM</sub> = 1 V, V <sub>NO</sub> = Open, or V <sub>COM</sub> = 3 V, V <sub>NO</sub> = Open,	Switch ON, See Figure 15	25°C	1.95 V	–2	2	nA
				Full			–20	
<b>Digital Control Inputs (IN1, IN2)</b>								
Input logic high	V <sub>IH</sub>		Full		1.5		5.5	V
Input logic low	V <sub>IL</sub>		Full		0		0.6	V
Input leakage current	I <sub>IH</sub> , I <sub>IL</sub>	V <sub>I</sub> = 5.5 V or 0	25°C	1.95 V	–2	0.3	2	nA
			Full			–20	20	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

**Electrical Characteristics for 1.8-V Supply<sup>(1)</sup> (continued)**
 $V_+ = 1.65\text{ V to }1.95\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Dynamic</b>									
Turn-on time	$t_{ON}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , See Figure 17	25°C	1.8 V	3	9	18	ns
				Full	1.65 V to 1.95 V	1		20	
Turn-off time	$t_{OFF}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , See Figure 17	25°C	1.8 V	5	10	15.5	ns
				Full	1.65 V to 1.95 V	4		18.5	
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ ,	$C_L = 1\text{ nF}$ , See Figure 21	25°C	1.8 V		2	pC	
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	1.8 V		19.5	pF	
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	1.8 V		18.5	pF	
NO ON capacitance	$C_{NO(ON)}$	$V_{NO} = V_+$ or GND, Switch ON,	See Figure 16	25°C	1.8 V		36.5	pF	
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See Figure 16	25°C	1.8 V		36.5	pF	
Digital input capacitance	$C_I$	$V_I = V_+$ or GND,	See Figure 16	25°C	1.8 V		2	pF	
Bandwidth	BW	$R_L = 50\ \Omega$ , Switch ON,	See Figure 18	25°C	1.8 V		150	MHz	
OFF isolation	$O_{ISO}$	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ ,	Switch OFF, See Figure 19	25°C	1.8 V		-62	dB	
Total harmonic distortion	THD	$R_L = 600\ \Omega$ , $C_L = 50\text{ pF}$ ,	$f = 20\text{ Hz to }20\text{ kHz}$ See Figure 21	25°C	1.8 V		0.055	%	
<b>Supply</b>									
Positive supply current	$I_+$	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	1.95 V	0.001	0.01	$\mu\text{A}$	
				Full			0.15		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

TYPICAL PERFORMANCE

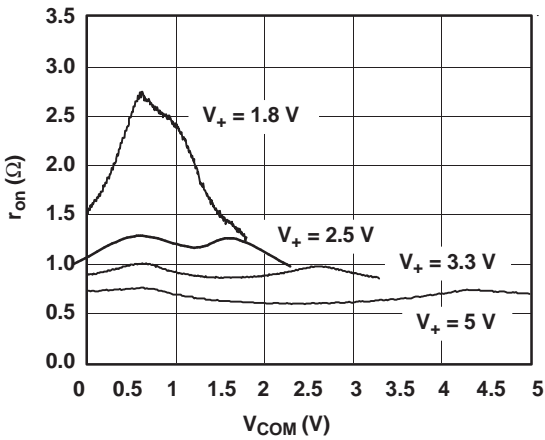


Figure 1.  $r_{on}$  vs  $V_{COM}$

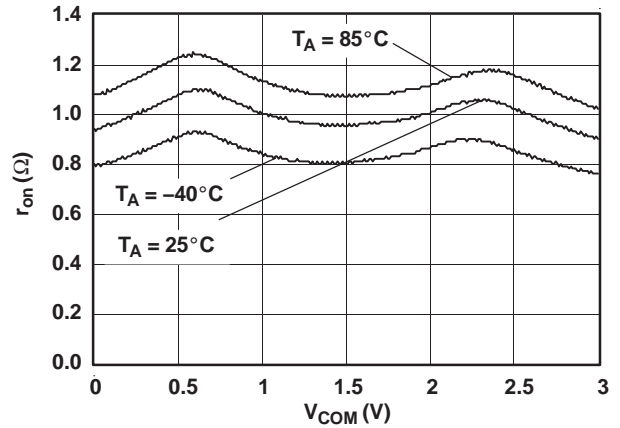


Figure 2.  $r_{on}$  vs  $V_{COM}$  ( $V_+ = 3V$ )

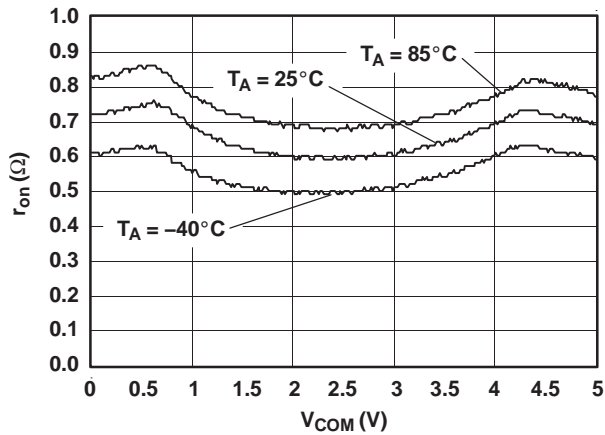


Figure 3.  $r_{on}$  vs  $V_{COM}$  ( $V_+ = 5V$ )

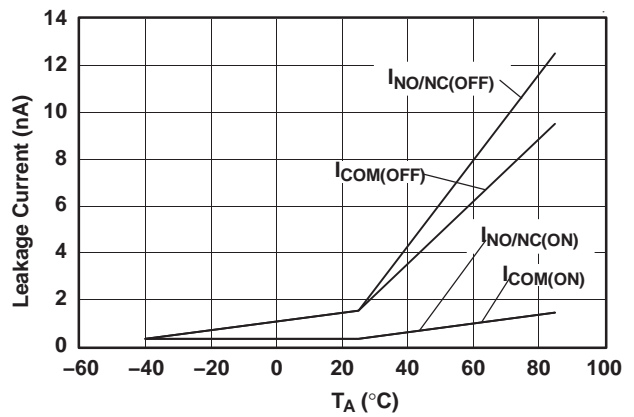


Figure 4. Leakage Current vs Temperature ( $V_+ = 5.5V$ )

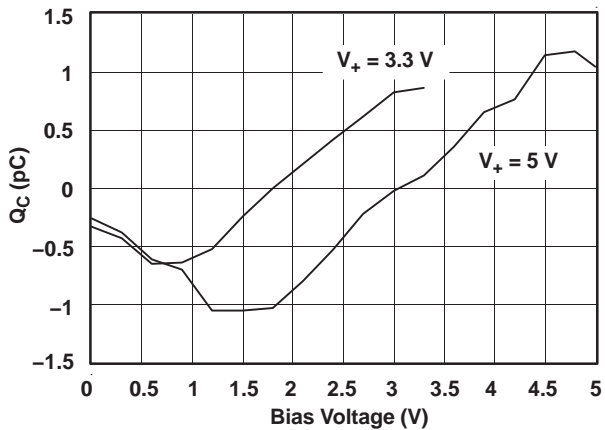


Figure 5. Charge Injection ( $Q_C$ ) vs  $V_{COM}$

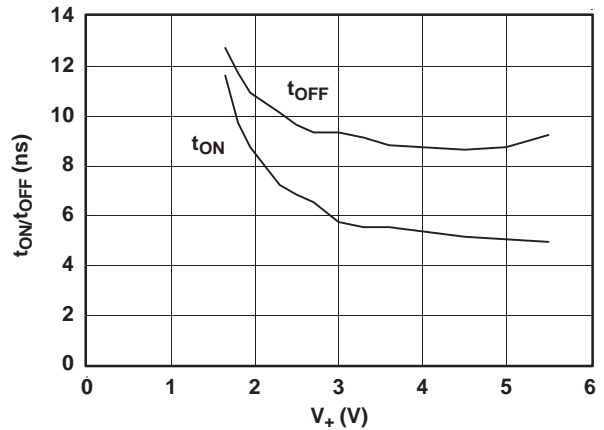


Figure 6.  $t_{ON}$  and  $t_{OFF}$  vs Supply Voltage

TYPICAL PERFORMANCE (continued)

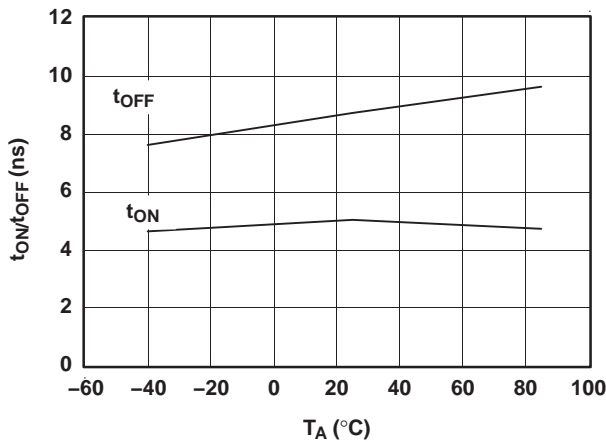


Figure 7.  $t_{ON}$  and  $t_{OFF}$  vs Temperature ( $V_+ = 5\text{ V}$ )

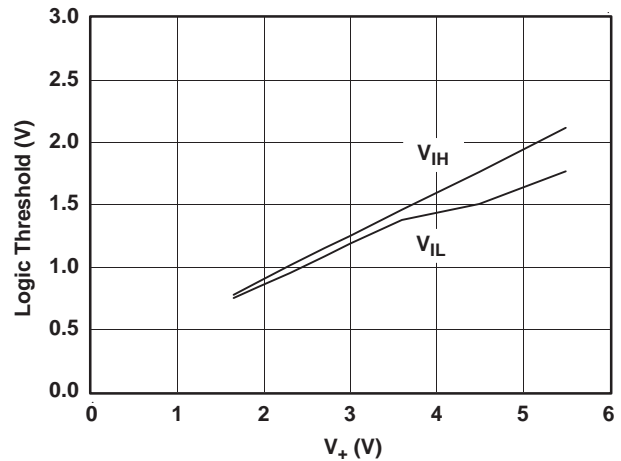


Figure 8. Logic Threshold vs  $V_+$

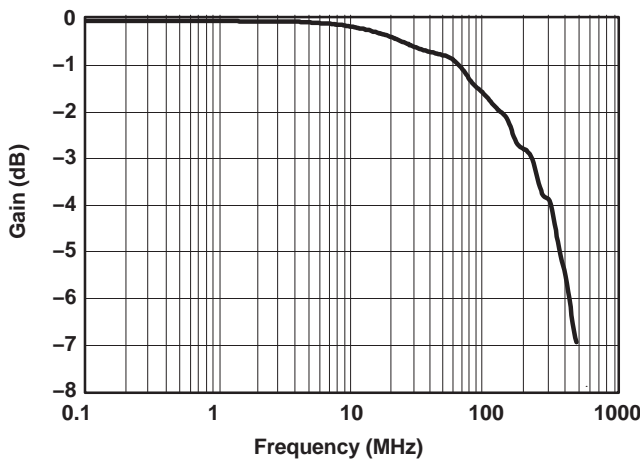


Figure 9. Gain vs Frequency ( $V_+ = 5\text{ V}$ )

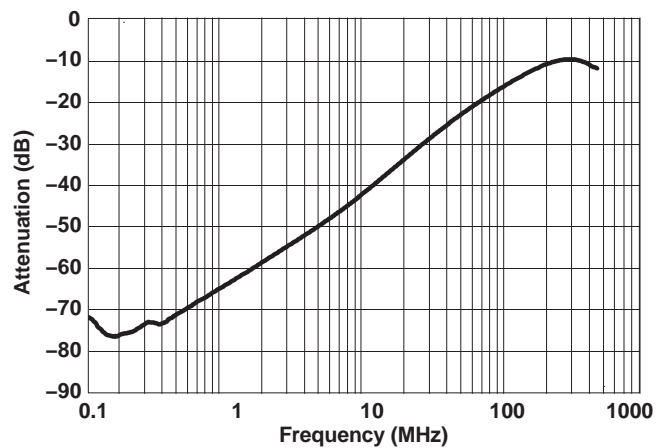


Figure 10. OFF Isolation vs Frequency ( $V_+ = 5\text{ V}$ )

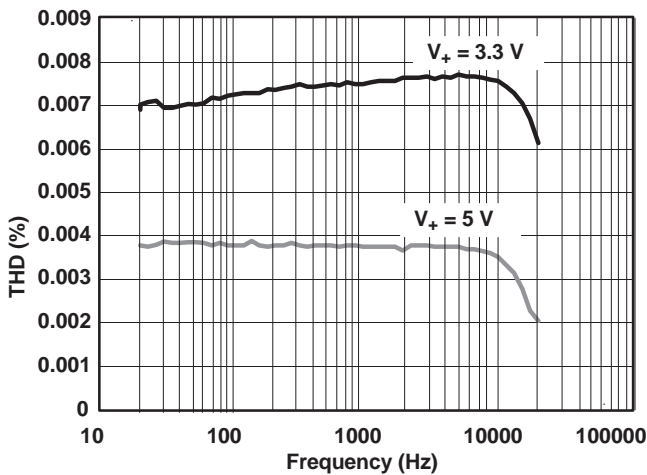


Figure 11. Total Harmonic Distortion vs Frequency ( $V_+ = 5\text{ V}$ )

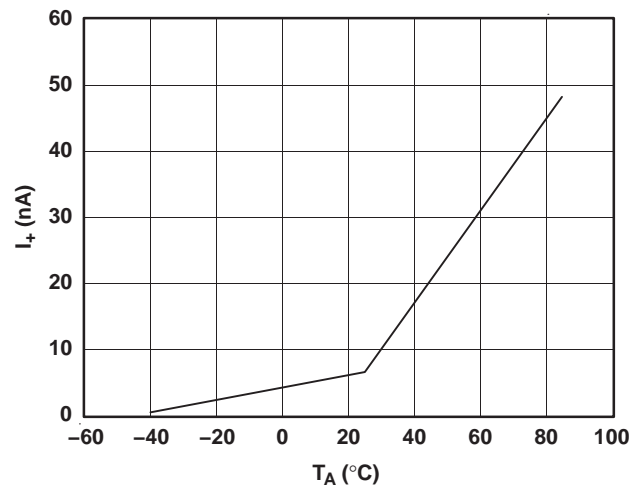


Figure 12. Power-Supply Current vs Temperature ( $V_+ = 5\text{ V}$ )

PARAMETER MEASUREMENT INFORMATION

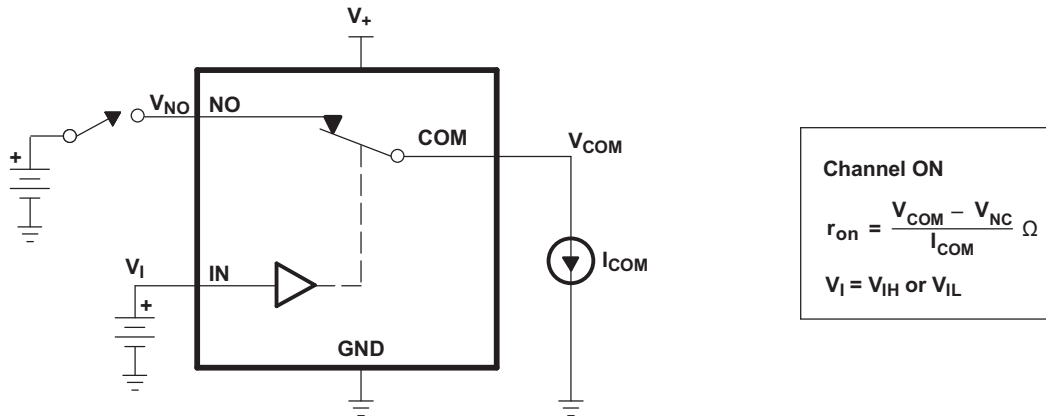


Figure 13. ON-State Resistance ( $r_{on}$ )

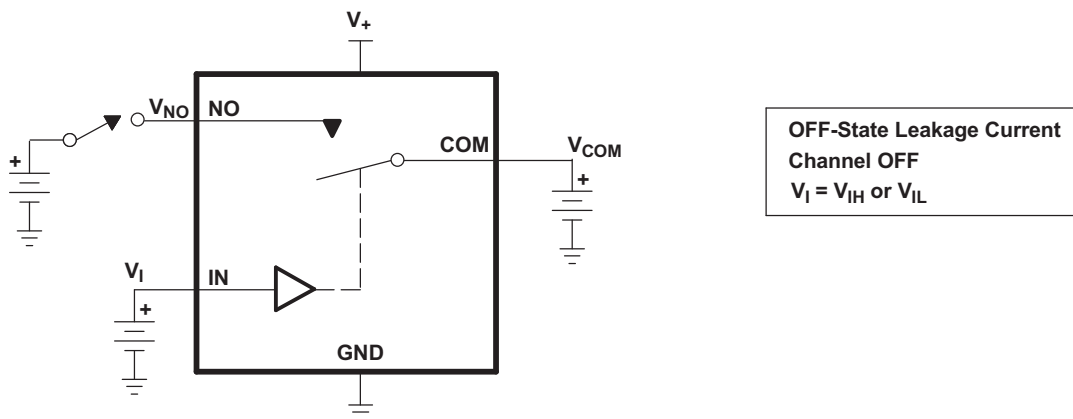


Figure 14. OFF-State Leakage Current ( $I_{COM(OFF)}$ ,  $I_{NO(OFF)}$ ,  $I_{COM(PWROFF)}$ ,  $I_{NO(PWRFF)}$ )

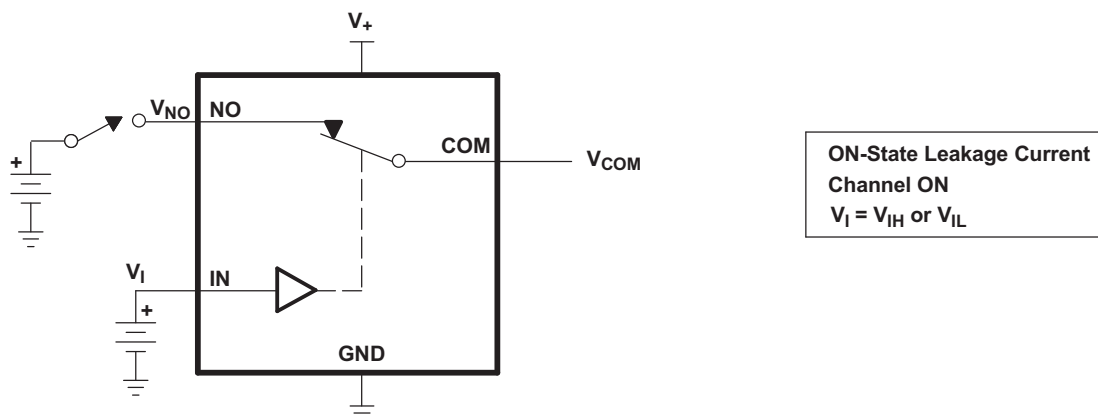


Figure 15. ON-State Leakage Current ( $I_{COM(ON)}$ ,  $I_{NO(ON)}$ )

PARAMETER MEASUREMENT INFORMATION (continued)

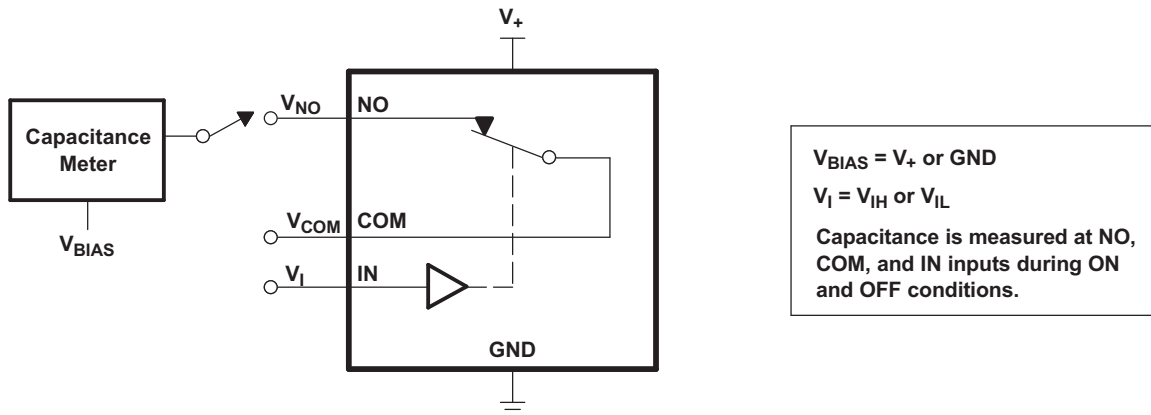
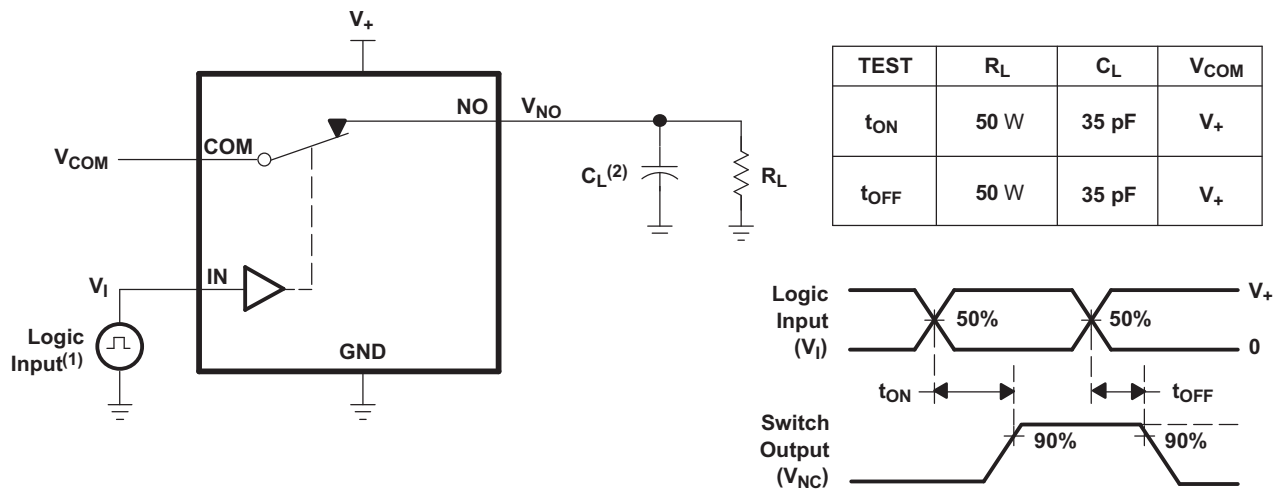


Figure 16. Capacitance ( $C_I$ ,  $C_{COM(OFF)}$ ,  $C_{COM(ON)}$ ,  $C_{NO(OFF)}$ ,  $C_{NO(ON)}$ )



- (1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> < 5 ns, t<sub>f</sub> < 5 ns.
- (2) C<sub>L</sub> includes probe and jig capacitance.

Figure 17. Turn-On (t<sub>ON</sub>) and Turn-Off Time (t<sub>OFF</sub>)

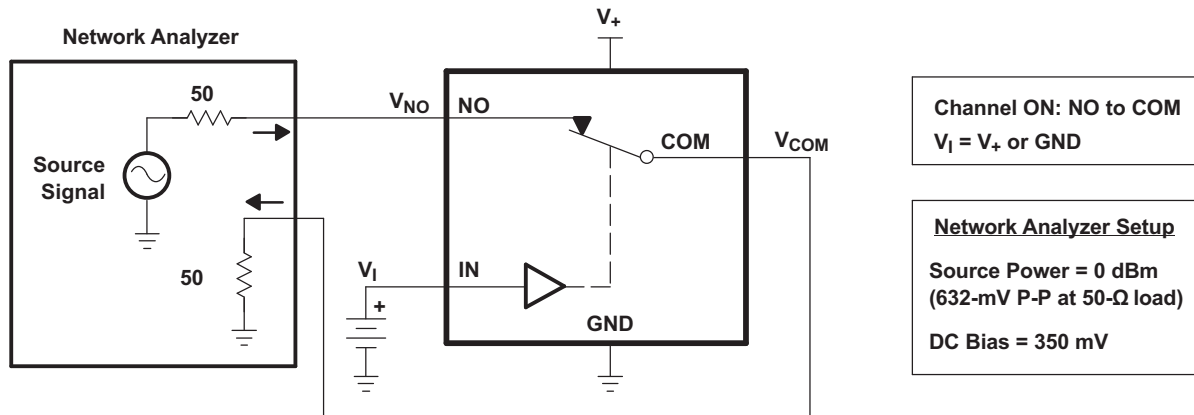


Figure 18. Bandwidth (BW)

PARAMETER MEASUREMENT INFORMATION (continued)

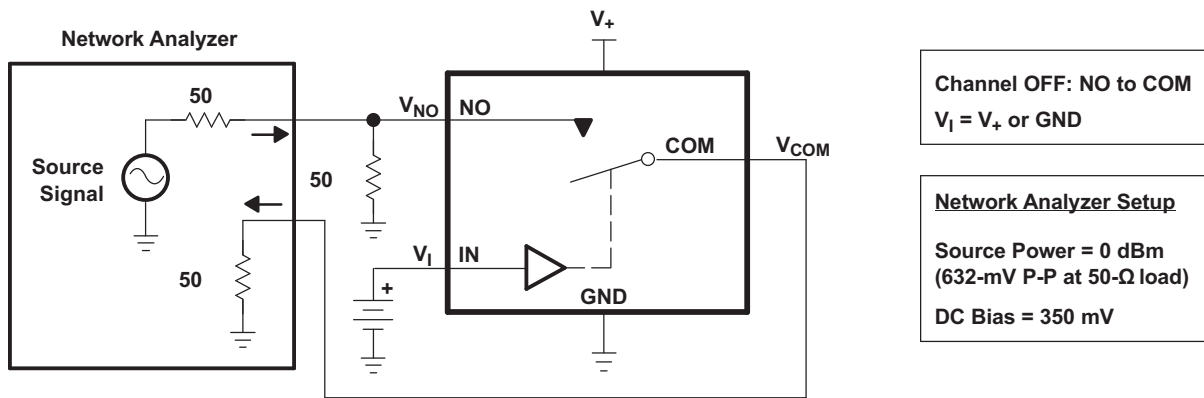
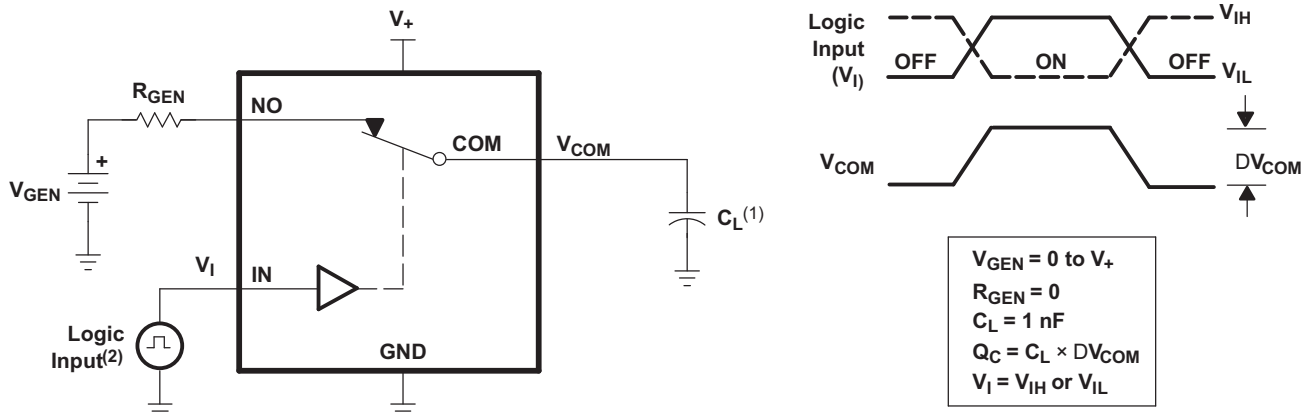
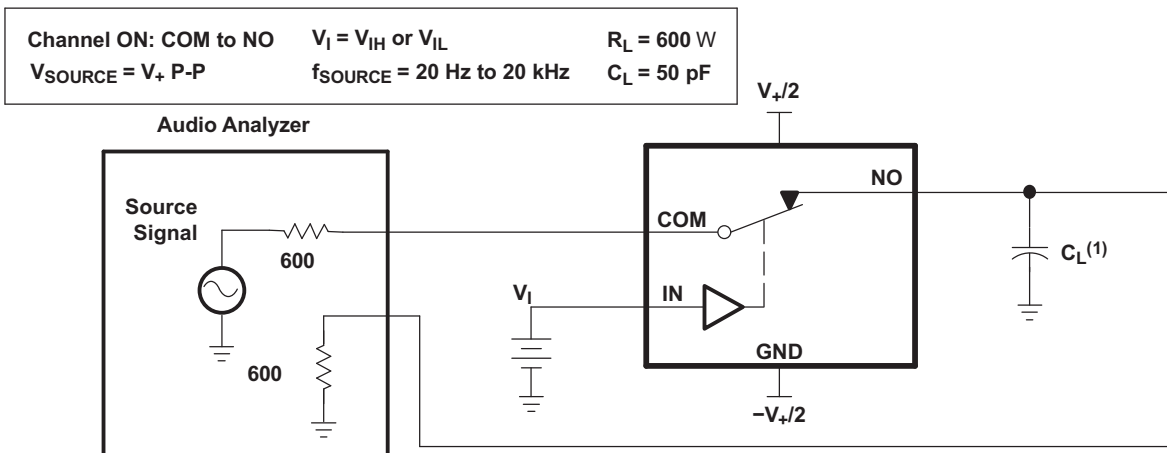


Figure 19. OFF Isolation ( $O_{ISO}$ )



- (1)  $C_L$  includes probe and jig capacitance.
- (2) All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r < 5$  ns,  $t_f < 5$  ns.

Figure 20. Charge Injection ( $Q_C$ )



- (1)  $C_L$  includes probe and jig capacitance.

Figure 21. Total Harmonic Distortion (THD)



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**REVISION HISTORY****Changes from Original (February 2005) to Revision A** **Page**

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- Updated ORDERING INFORMATION table. .... 1
- 

**Changes from Revision A (October 2012) to Revision B** **Page**

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- Changed pin name from NC to NO throughout the datasheet. .... 1
  - Removed ORDERING INFORMATION table. .... 1
-

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A3166DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JASF ~ JASR)	<a href="#">Samples</a>
TS5A3166DBVRE4	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 85	JASF	<a href="#">Samples</a>
TS5A3166DBVRG4	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 85	JASF	<a href="#">Samples</a>
TS5A3166DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JF5 ~ JFF ~ JFR)	<a href="#">Samples</a>
TS5A3166DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JF5 ~ JFF ~ JFR)	<a href="#">Samples</a>
TS5A3166DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JF5 ~ JFF ~ JFR)	<a href="#">Samples</a>
TS5A3166YZPR	ACTIVE	DSBGA	YZP	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(JF7 ~ JFN)	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF TS5A3166 :**

- Automotive: [TS5A3166-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A3166DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TS5A3166DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TS5A3166DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TS5A3166YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A3166DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TS5A3166DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
TS5A3166DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TS5A3166YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-203 variation AA.



DCK (R-PDSO-G5)

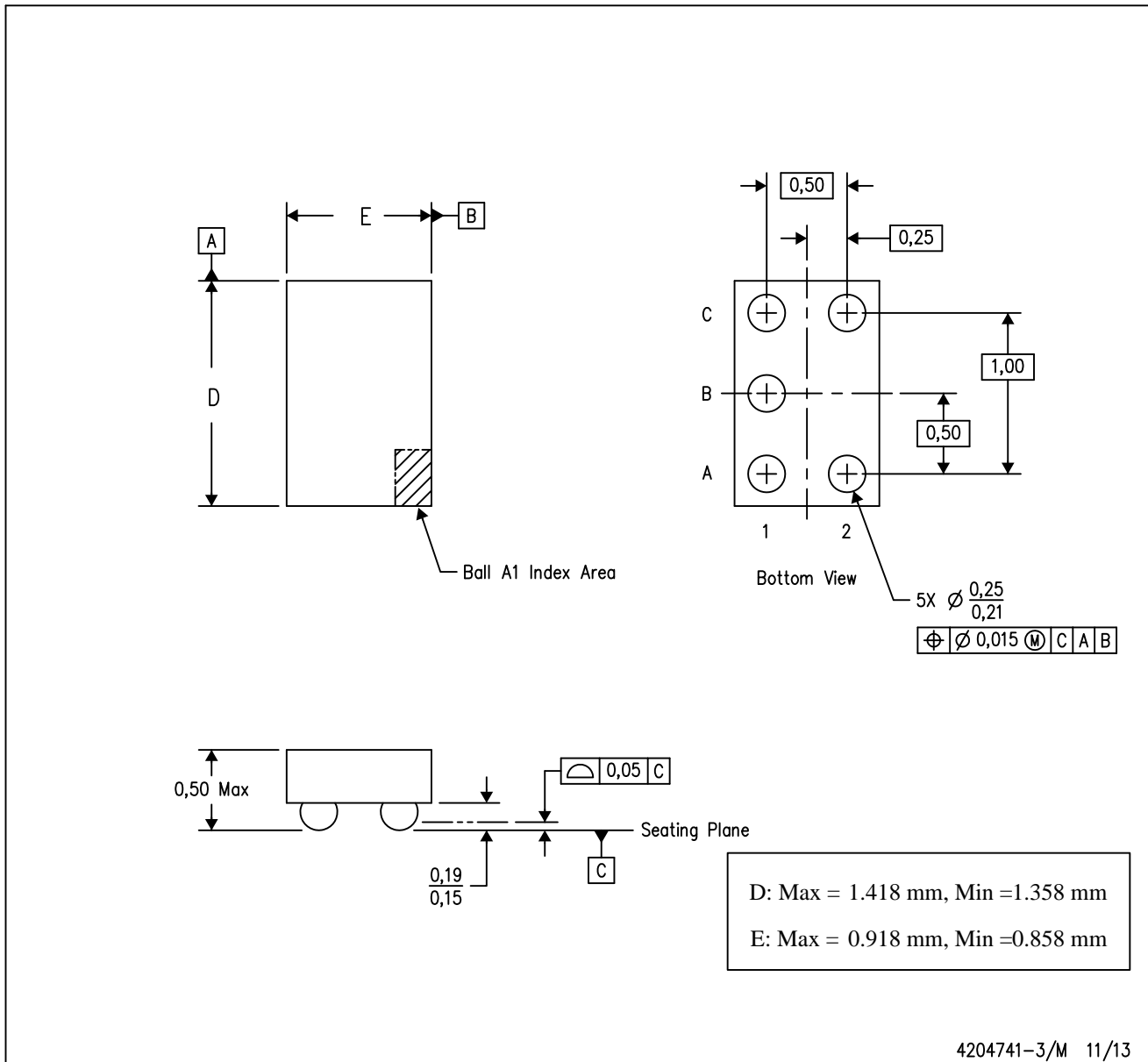
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

YZP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. NanoFree™ package configuration.

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