

PHC21025

Complementary intermediate level FET

Rev. 04 — 17 March 2011

Product data sheet

1. Product profile

1.1 General description

Intermediate level N-channel and P-channel complementary pair enhancement mode Field-Effect Transistor (FET) in a plastic package using vertical D-MOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Suitable for high frequency applications due to fast switching characteristics

1.3 Applications

- Motor and actuator drivers
- Synchronized rectification
- Power management

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$; N-channel	-	-	30	V
		$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$; P-channel	-	-	-30	V
I_D	drain current	$T_{sp} \leq 80\text{ °C}$; P-channel	-	-	-2.3	A
		$T_{sp} \leq 80\text{ °C}$; N-channel	-	-	3.5	A
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C}$	[1]	-	1	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -10\text{ V}$; $I_D = -1\text{ A}$; $T_j = 25\text{ °C}$; P-channel; see Figure 16 ; see Figure 19	-	0.22	0.25	Ω
		$V_{GS} = 10\text{ V}$; $I_D = 2.2\text{ A}$; $T_j = 25\text{ °C}$; N-channel; see Figure 15 ; see Figure 18	-	0.08	0.1	Ω



Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = -10\text{ V}$; $I_D = -2.3\text{ A}$; $V_{DS} = -15\text{ V}$; $T_J = 25\text{ }^\circ\text{C}$; P-channel; see Figure 12	-	3	-	nC
		$V_{GS} = 10\text{ V}$; $I_D = 2.3\text{ A}$; $V_{DS} = 15\text{ V}$; $T_J = 25\text{ }^\circ\text{C}$; N-channel; see Figure 11	-	2.5	-	nC

[1] Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with a thermal resistance from ambient to solder point of 90 K/W.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 SOT96-1 (SO8)	 sym114
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PHC21025	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 150 °C; N-channel	-	30	V	
		T _j ≥ 25 °C; T _j ≤ 150 °C; P-channel	-	-30	V	
V _{GS}	gate-source voltage		-	-	V	
V _{GSO}	gate-source voltage	open drain	-20	20	V	
I _D	drain current	T _{sp} ≤ 80 °C; P-channel	-	-2.3	A	
		T _{sp} ≤ 80 °C; N-channel	-	3.5	A	
I _{DM}	peak drain current	T _{sp} = 25 °C; pulsed; N-channel; see Figure 2	[1]	-	14	A
		T _{sp} = 25 °C; pulsed; P-channel; see Figure 3	[1]	-	-10	A
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	1	W
		T _{sp} = 80 °C; see Figure 1	[3]	-	2	W
		T _{amb} = 25 °C	[4]	-	1.3	W
			[5]	-	2	W
T _{stg}	storage temperature		-65	150	°C	
T _j	junction temperature		-	150	°C	
Source-drain diode						
I _S	source current	T _{sp} ≤ 80 °C; P-channel	-	-1.25	A	
		T _{sp} ≤ 80 °C; N-channel	-	1.5	A	
I _{SM}	peak source current	T _{sp} = 25 °C; pulsed; P-channel	[6]	-	-5	A
		T _{sp} = 25 °C; pulsed; N-channel	[6]	-	6	A

[1] Pulse width and duty cycle limited by maximum junction temperature.

[2] Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with a thermal resistance from ambient to solder point of 90 K/W.

[3] Maximum permissible dissipation per MOS transistor. Both devices may be loaded up to 2 W at the same time.

[4] Maximum permissible dissipation if only one MOS transistor dissipates. Device mounted on printed-circuit board with thermal resistance from ambient to solder point of 90 K/W.

[5] Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with a Thermal resistance from ambient to solder point of 27.5 K/W.

[6] Pulse width and duty cycle limited by maximum junction temperature.

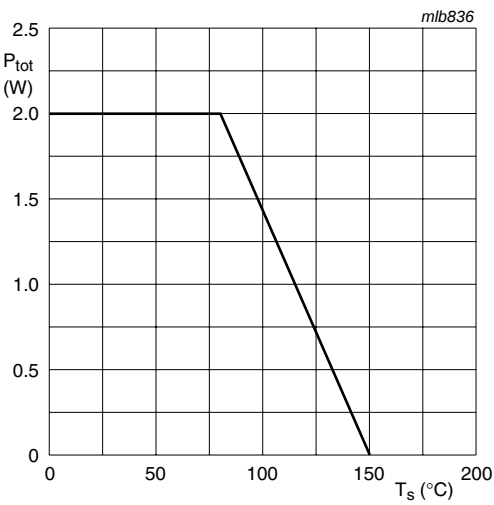
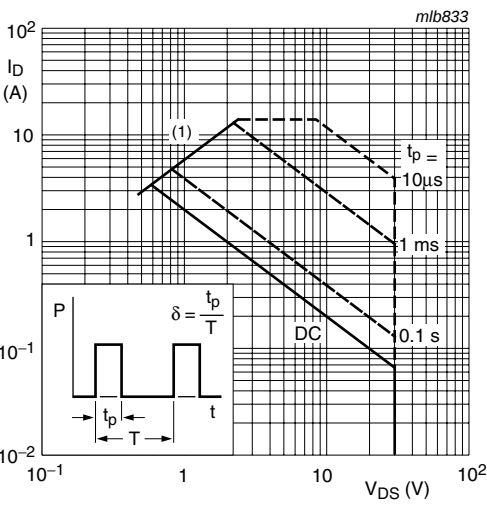
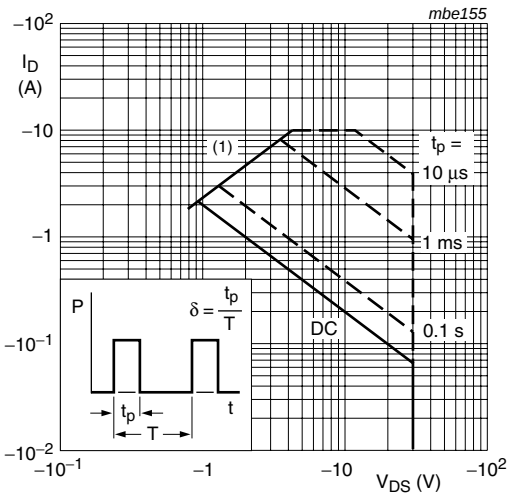


Fig 1. Power derating curve



$\delta = 0.01$.
 $T_s = 80$ °C.
(1) R_{DSon} limitation.

Fig 2. SOAR; N-channel



$\delta = 0.01$
 $T_s = 80$ °C.
(1) R_{DSon} limitation.

Fig 3. SOAR; P-channel

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	35	K/W

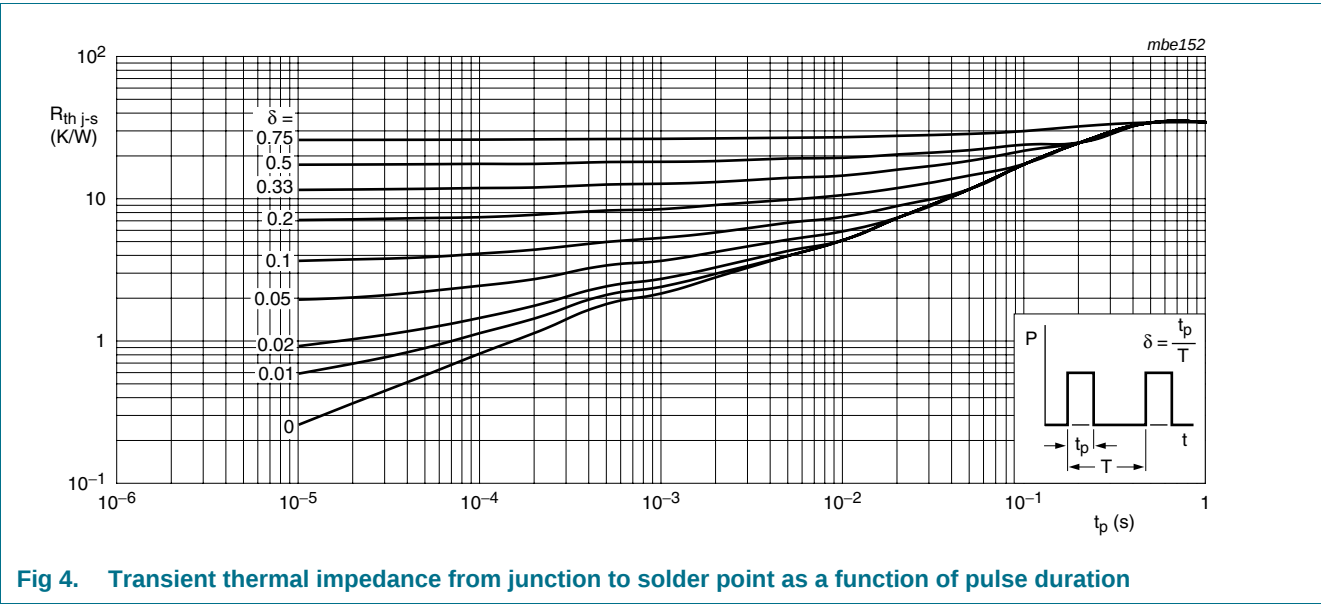


Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

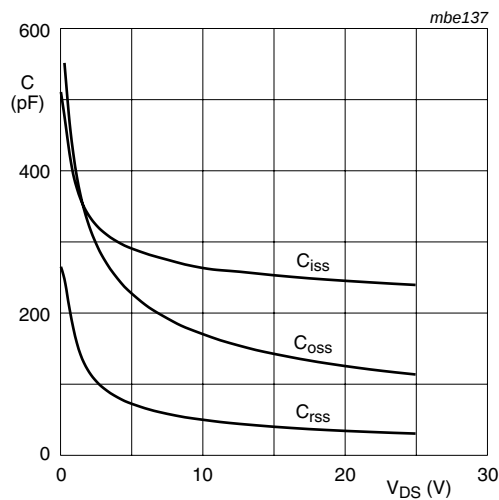
6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = -10 μA; V _{GS} = 0 V; T _j = 25 °C; P-channel	-30	-	-	V
		I _D = 10 μA; V _{GS} = 0 V; T _j = 25 °C; N-channel	30	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = -1 mA; V _{DS} = V _{GS} ; T _j = 25 °C; P-channel; see Figure 17	-1	-	-2.8	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 25 °C; N-channel; see Figure 17	1	-	2.8	V
I _{DSS}	drain leakage current	V _{DS} = -24 V; V _{GS} = 0 V; T _j = 25 °C; P-channel	-	-	-100	nA
		V _{DS} = 24 V; V _{GS} = 0 V; T _j = 25 °C; N-channel	-	-	100	nA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C; N-channel	-	-	100	nA
		V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C; P-channel	-	-	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C; P-channel	-	-	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C; N-channel	-	-	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = -10 V; I _D = -1 A; T _j = 25 °C; P-channel; see Figure 16 ; see Figure 19	-	0.22	0.25	Ω
		V _{GS} = 10 V; I _D = 2.2 A; T _j = 25 °C; N-channel; see Figure 15 ; see Figure 18	-	0.08	0.1	Ω
		V _{GS} = -4.5 V; I _D = -0.5 A; T _j = 25 °C; P-channel; see Figure 16 ; see Figure 19	-	0.33	0.4	Ω
		V _{GS} = 4.5 V; I _D = 1 A; N-channel; see Figure 15 ; see Figure 18	-	0.11	0.2	Ω
I _{DSon}	on-state drain current	V _{DS} = 5 V; V _{GS} = 4.5 V; N-channel	2	-	-	A
		V _{DS} = -5 V; V _{GS} = -4.5 V; P-channel	-1	-	-	A
		V _{DS} = -1 V; V _{GS} = -10 V; P-channel	-2.3	-	-	A
		V _{DS} = 1 V; V _{GS} = 10 V; N-channel	3.5	-	-	A
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 2.3 A; V _{DS} = 15 V; V _{GS} = 10 V; T _j = 25 °C; N-channel; see Figure 11	-	10	30	nC
		I _D = -2.3 A; V _{DS} = -15 V; V _{GS} = -10 V; T _j = 25 °C; P-channel; see Figure 12	-	10	25	nC

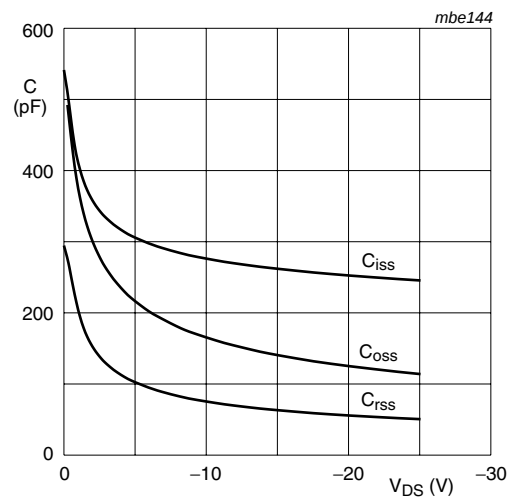
Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Q _{GS}	gate-source charge	I _D = 2.3 A; V _{DS} = 15 V; V _{GS} = 10 V; T _j = 25 °C; N-channel; see Figure 11	-	1	-	nC
		I _D = -2.3 A; V _{DS} = -15 V; V _{GS} = -10 V; T _j = 25 °C; P-channel; see Figure 12	-	1	-	nC
Q _{GD}	gate-drain charge	I _D = -2.3 A; V _{DS} = -15 V; V _{GS} = -10 V; T _j = 25 °C; P-channel; see Figure 12	-	3	-	nC
		I _D = 2.3 A; V _{DS} = 15 V; V _{GS} = 10 V; T _j = 25 °C; N-channel; see Figure 11	-	2.5	-	nC
C _{iss}	input capacitance	V _{DS} = 20 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; N-channel; see Figure 5	-	250	-	pF
		V _{DS} = -20 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; P-channel; see Figure 6	-	250	-	pF
C _{oss}	output capacitance	V _{DS} = 20 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; N-channel; see Figure 5	-	140	-	pF
		V _{DS} = -20 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; P-channel; see Figure 6	-	140	-	pF
C _{rss}	reverse transfer capacitance	V _{DS} = 20 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; N-channel; see Figure 5	-	50	-	pF
		V _{DS} = -20 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; P-channel; see Figure 6	-	50	-	pF
g _{fs}	transfer conductance	V _{DS} = -20 V; I _D = -1 A; T _j = 25 °C; P-channel	1	2	-	S
		V _{DS} = 20 V; I _D = 2.2 A; T _j = 25 °C; N-channel	2	4.5	-	S
t _{off}	turn-off time	V _{DS} = 20 V; V _{GS} = 10 V; R _{G(ext)} = 4.7 Ω; I _D = 1 A; R _L = 20 Ω; T _j = 25 °C; N-channel	-	25	140	ns
t _{on}	turn-on time	V _{DS} = -20 V; V _{GS} = -10 V; R _{G(ext)} = 4.7 Ω; I _D = -1 A; R _L = 20 Ω; T _j = 25 °C; P-channel	-	50	140	ns
		V _{DS} = -20 V; V _{GS} = -10 V; R _{G(ext)} = 4.7 Ω; I _D = -1 A; R _L = 20 Ω; T _j = 25 °C; P-channel	-	20	80	ns
		V _{DS} = 20 V; V _{GS} = 10 V; R _{G(ext)} = 4.7 Ω; I _D = 1 A; R _L = 20 Ω; T _j = 25 °C; N-channel	-	15	40	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 1.25 A; V _{GS} = 0 V; T _j = 25 °C; N-channel; see Figure 13	-	-	1.2	V
		I _S = -1.25 A; V _{GS} = 0 V; T _j = 25 °C; P-channel; see Figure 14	-	-	-1.6	V
t _{rr}	reverse recovery time	I _S = -1.25 A; dI _S /dt = 100 A/μs; V _{GS} = 0 V; V _{DS} = -25 V; T _j = 25 °C; P-channel	-	150	200	ns
		I _S = 1.25 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 25 V; T _j = 25 °C; N-channel	-	35	100	ns



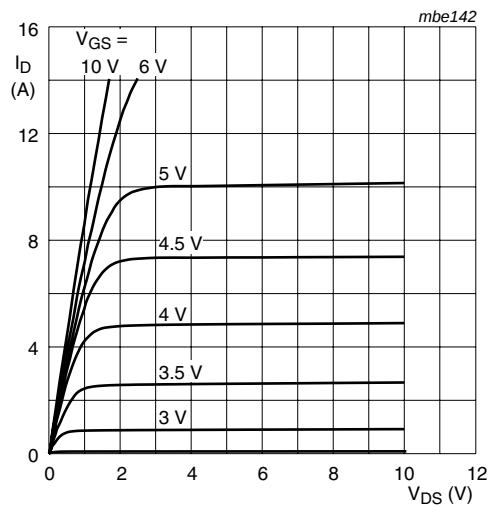
$T_j = 25^{\circ}\text{C}; V_{GS} = 0\text{V}$

Fig 5. Capacitance as a function of drain-source voltage; N-channel; typical values



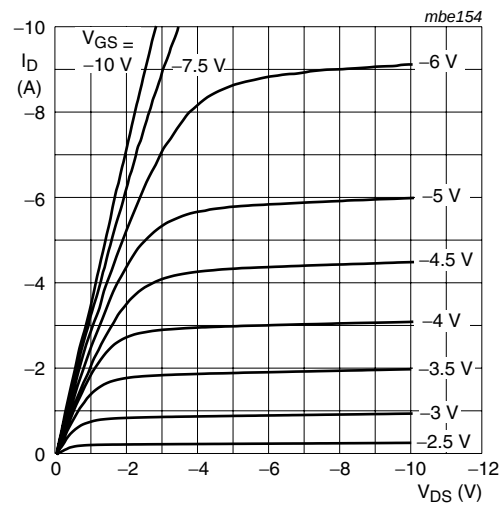
$T_j = 25^{\circ}\text{C}; V_{GS} = 0\text{V}$

Fig 6. Capacitance as a function of drain-source voltage; P-channel; typical values



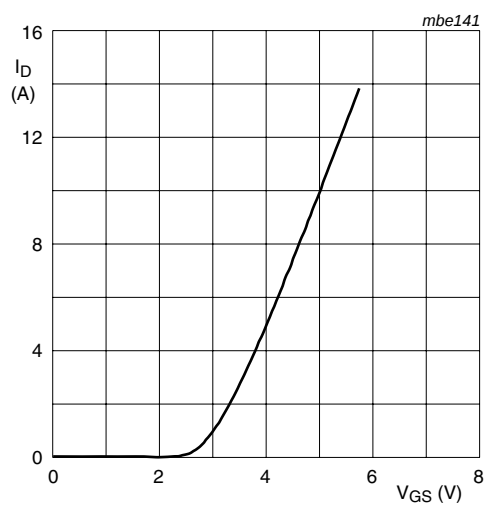
$T_j = 25^{\circ}\text{C}$

Fig 7. Output characteristics: drain current as a function of drain-source voltage; N-channel; typical values



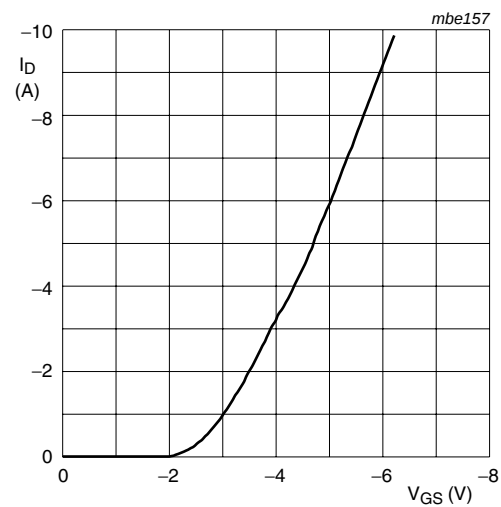
$T_j = 25^{\circ}\text{C}$

Fig 8. Output characteristics: drain current as a function of drain-source voltage; P-channel; typical values



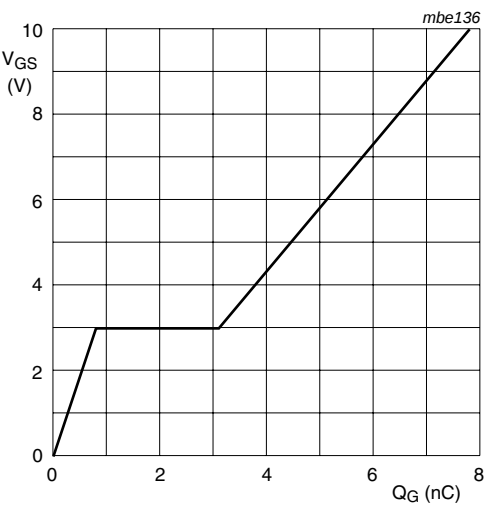
$T_j = 25^{\circ}\text{C}; V_{DS} = 10\text{V}$

Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; N-channel; typical values



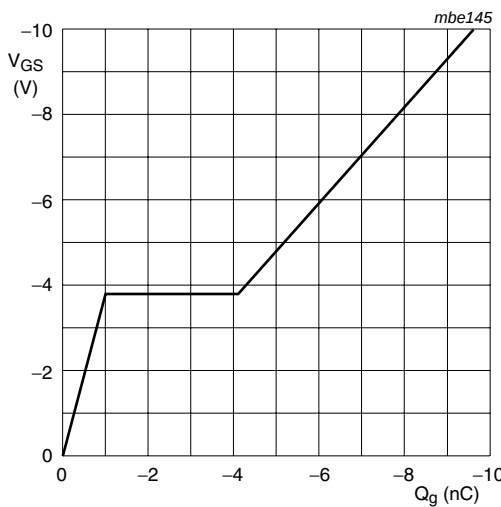
$T_j = 25^{\circ}\text{C}; V_{DS} = -10\text{V}$

Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; P-channel; typical values



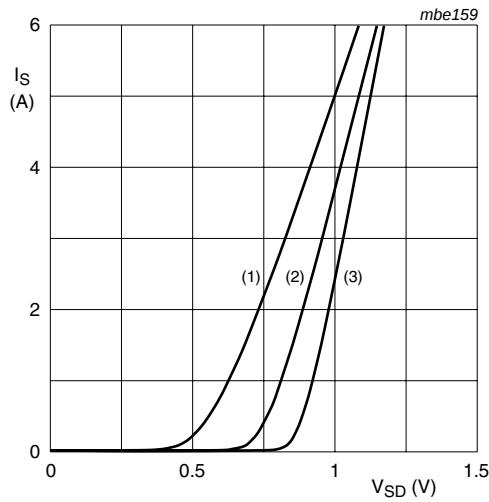
$I_D = 3.5\text{A}; V_{DS} = 15\text{V}$

Fig 11. Gate-source voltage as a function of gate charge; N-channel; typical values



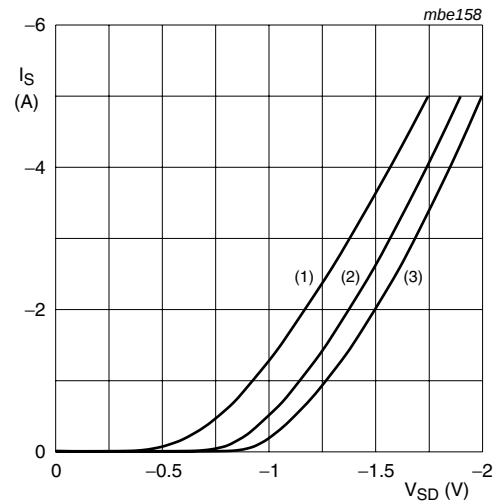
$I_D = -2.3\text{A}; V_{DS} = -15\text{V}$

Fig 12. Gate-source voltage as a function of gate charge; P-channel; typical values



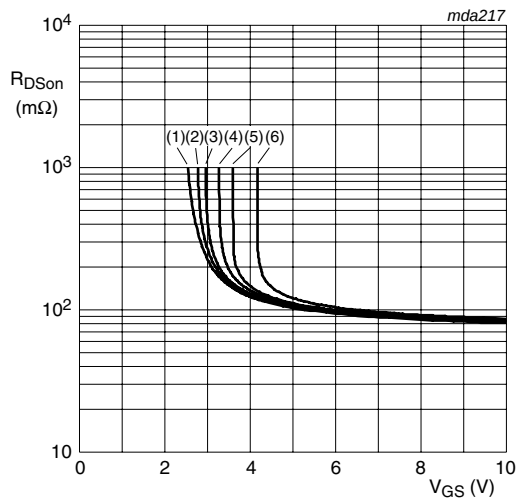
$V_{GD} = 0$.
(1) $T_j = 150\text{ }^{\circ}\text{C}$.
(2) $T_j = 25\text{ }^{\circ}\text{C}$.
(3) $T_j = -55\text{ }^{\circ}\text{C}$.

Fig 13. Source current as a function of source-drain voltage; N-channel; typical values



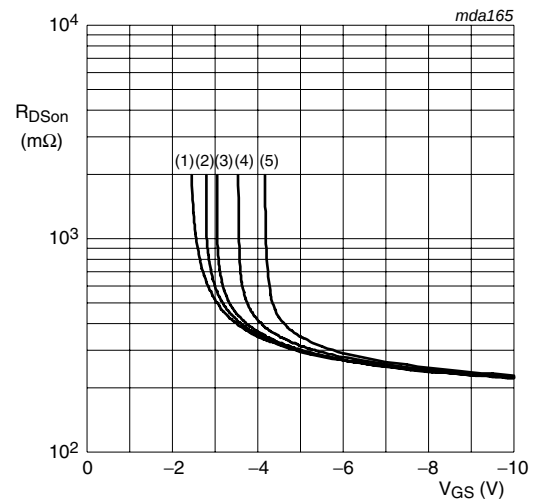
$V_{GD} = 0$.
(1) $T_j = 150\text{ }^{\circ}\text{C}$.
(2) $T_j = 25\text{ }^{\circ}\text{C}$.
(3) $T_j = -55\text{ }^{\circ}\text{C}$.

Fig 14. Source current as a function of source-drain voltage; P-channel; typical values



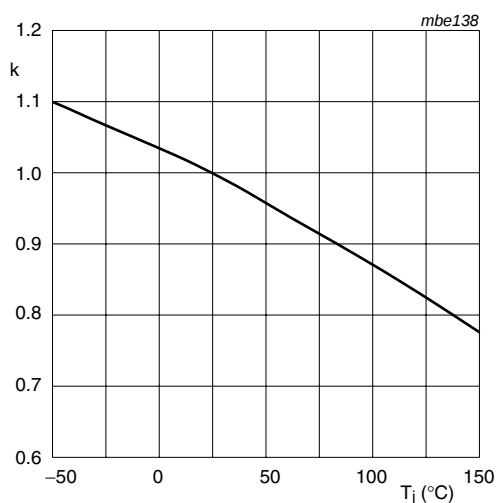
$V_{DS} \geq I_D \times R_{DSon}$; $T_j = 25\text{ }^{\circ}\text{C}$.
(1) $I_D = 0.1\text{ A}$.
(2) $I_D = 0.5\text{ A}$.
(3) $I_D = 1\text{ A}$.
(4) $I_D = 2.2\text{ A}$.
(5) $I_D = 3.5\text{ A}$.
(6) $I_D = 7\text{ A}$.

Fig 15. Drain-source on-state resistance as a function of drain current; N-channel; typical values



$-V_{DS} \geq -I_D \times R_{DSon}$; $T_j = 25\text{ }^{\circ}\text{C}$.
(1) $I_D = -0.1\text{ A}$.
(2) $I_D = -0.5\text{ A}$.
(3) $I_D = -1\text{ A}$.
(4) $I_D = -2.3\text{ A}$.
(5) $I_D = -4.5\text{ A}$.

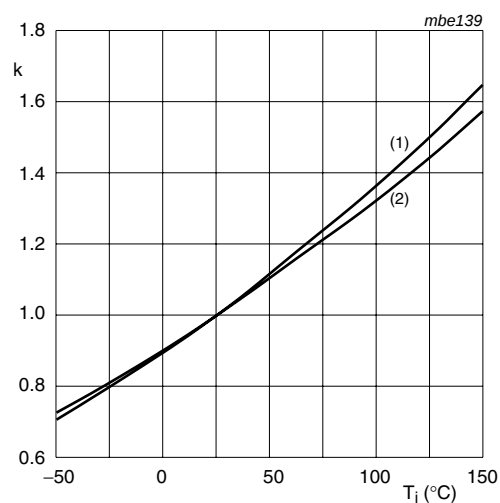
Fig 16. Drain-source on-state resistance as a function of drain current; typical values



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25^\circ\text{C}}$$

Typical V_{GSth} at $I_D = 1 \text{ mA}$; $V_{DS} = V_{GS} = V_{GSth}$.

Fig 17. Temperature coefficient of gate-source threshold voltage



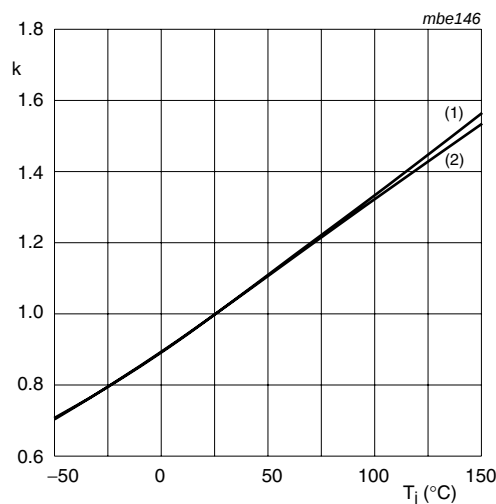
$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25^\circ\text{C}}$$

Typical R_{DSon} at:

(1) $I_D = 2.2 \text{ A}$; $V_{GS} = 10 \text{ V}$.

(2) $I_D = 1 \text{ A}$; $V_{GS} = 4.5 \text{ V}$.

Fig 18. Temperature coefficient of drain-source on-state resistance; N-channel



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25^\circ\text{C}}$$

Typical R_{DSon} at:

(1) $I_D = -1 \text{ A}$; $V_{GS} = -10 \text{ V}$.

(2) $I_D = -0.5 \text{ A}$; $V_{GS} = -4.5 \text{ V}$.

Fig 19. Temperature coefficient of drain-source on-state resistance; P-channel

7. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

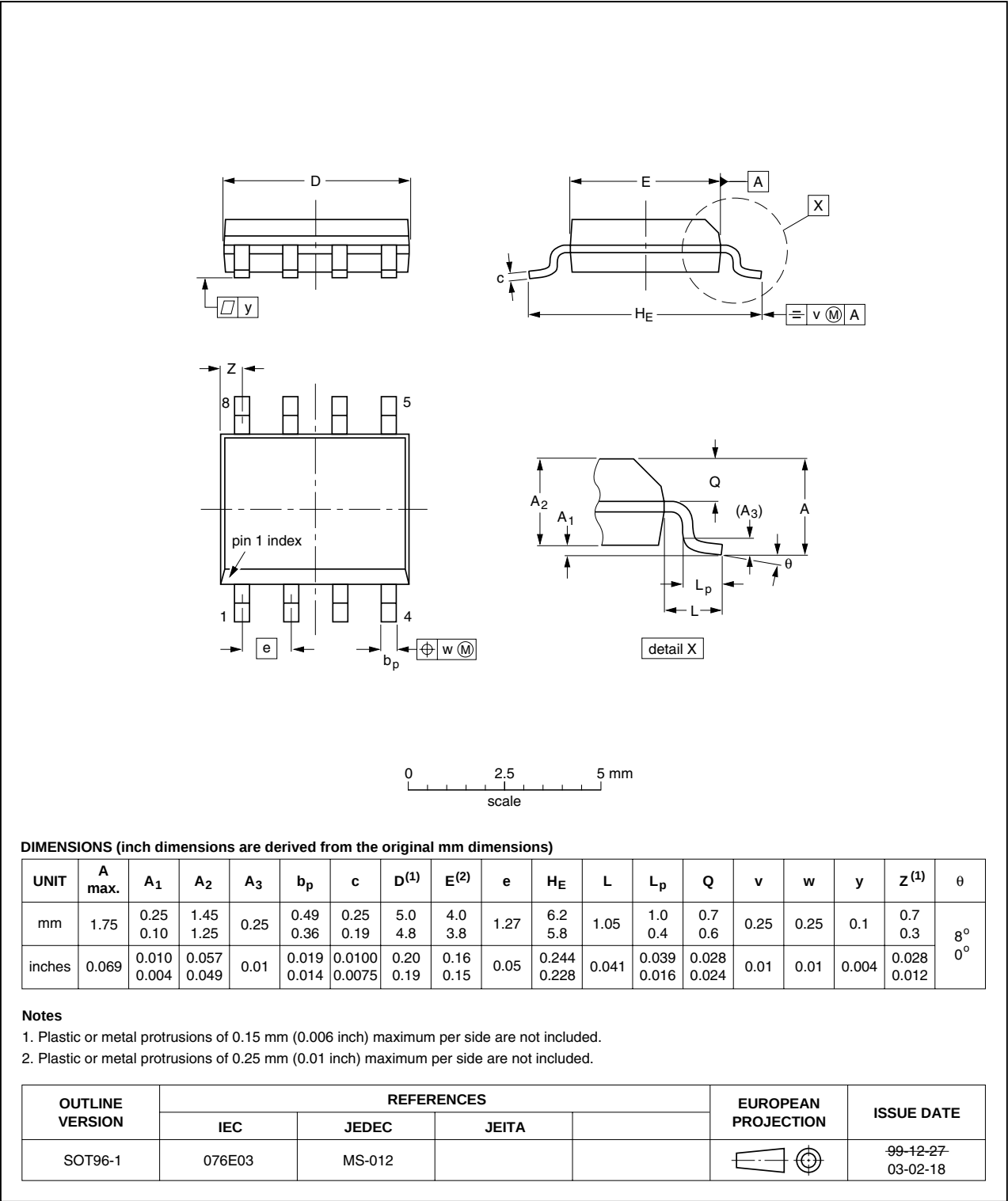


Fig 20. Package outline SOT96-1 (SO8)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHC21025 v.4	20110317	Product data sheet	-	PHC21025 v.3
Modifications:	• Various changes to content.			
PHC21025 v.3	20101217	Product data sheet	-	PHC21025 v.2

9. Legal information

9.1 Data sheet status

Document status ^{[1] [2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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10. Contact information

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