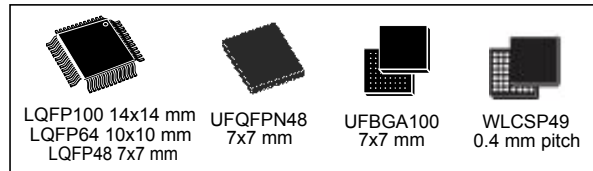


## ARM-based 32-bit MCU, up to 128 KB Flash, 12 timers, ADC, DAC & communication interfaces, 2.0 - 3.6 V

Datasheet - production data

### Features

- Core: ARM® 32-bit Cortex®-M0 CPU, frequency up to 48 MHz
- Memories
  - 64 to 128 Kbytes of Flash memory
  - 16 Kbytes of SRAM with HW parity
- CRC calculation unit
- Reset and power management
  - Digital & I/Os supply:  $V_{DD} = 2.0\text{ V to }3.6\text{ V}$
  - Analog supply:  $V_{DDA} = V_{DD}$  to 3.6 V
  - Selected I/Os:  $V_{DDIO2} = 1.65\text{ V to }3.6\text{ V}$
  - Power-on/Power down reset (POR/PDR)
  - Programmable voltage detector (PVD)
  - Low power modes: Sleep, Stop, Standby
  - $V_{BAT}$  supply for RTC and backup registers
- Clock management
  - 4 to 32 MHz crystal oscillator
  - 32 kHz oscillator for RTC with calibration
  - Internal 8 MHz RC with x6 PLL option
  - Internal 40 kHz RC oscillator
  - Internal 48 MHz oscillator with automatic trimming based on ext. synchronization
- Up to 87 fast I/Os
  - All mappable on external interrupt vectors
  - Up to 68 I/Os with 5V tolerant capability and 19 with independent supply  $V_{DDIO2}$
- 7-channel DMA controller
- One 12-bit, 1.0  $\mu\text{s}$  ADC (up to 16 channels)
  - Conversion range: 0 to 3.6 V
  - Separate analog supply: 2.4 V to 3.6 V
- One 12-bit D/A converter (with 2 channels)
- Two fast low-power analog comparators with programmable input and output
- Up to 24 capacitive sensing channels for touchkey, linear and rotary touch sensors



- Calendar RTC with alarm and periodic wakeup from Stop/Standby
- 12 timers
  - One 16-bit advanced-control timer for 6 channel PWM output
  - One 32-bit and seven 16-bit timers, with up to 4 IC/OC, OCN, usable for IR control decoding or DAC control
  - Independent and system watchdog timers
  - SysTick timer
- Communication interfaces
  - Two I<sup>2</sup>C interfaces supporting Fast Mode Plus (1 Mbit/s) with 20 mA current sink; one supporting SMBus/PMBus and wakeup
  - Four USARTs supporting master synchronous SPI and modem control; two with ISO7816 interface, LIN, IrDA, auto baud rate detection and wakeup feature
  - Two SPIs (18 Mbit/s) with 4 to 16 programmable bit frames, and with I<sup>2</sup>S interface multiplexed
- HDMI CEC, wakeup on header reception
- Serial wire debug (SWD)
- 96-bit unique ID
- All packages ECOPACK®<sub>2</sub>

**Table 1. Device summary**

Reference	Part number
STM32F071xB	STM32F071CB, STM32F071RB, STM32F071VB
STM32F071x8	STM32F071V8

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# 1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F071xx microcontrollers.

This document should be read in conjunction with the STM32F0xxxx reference manual (RM0091). The reference manual is available from the STMicroelectronics website [www.st.com](http://www.st.com).

For information on the ARM® Cortex®-M0 core, please refer to the Cortex®-M0 Technical Reference Manual, available from the [www.arm.com](http://www.arm.com) website.



## 2 Description

The STM32F071xx microcontrollers incorporate the high-performance ARM® Cortex®-M0 32-bit RISC core operating at a 48 MHz frequency, high-speed embedded memories (up to 128 Kbytes of Flash memory and 16 Kbytes of SRAM), and an extensive range of enhanced peripherals and I/Os. All devices offer standard communication interfaces (two I<sup>2</sup>Cs, two SPIs/one I2S, one HDMI CEC and four USARTs), one 12-bit ADC, one 12-bit DAC with two channels, seven general-purpose 16-bit timers, a 32-bit timer and an advanced-control PWM timer.

The STM32F071xx microcontrollers operate in the -40 to +85 °C and -40 to +105 °C temperature ranges from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

The STM32F071xx microcontrollers include devices in six different packages ranging from 48 pins to 100 pins with a die form also available upon request. Depending on the device chosen, different sets of peripherals are included. The description below provides an overview of the complete range of STM32F071xx peripherals proposed.

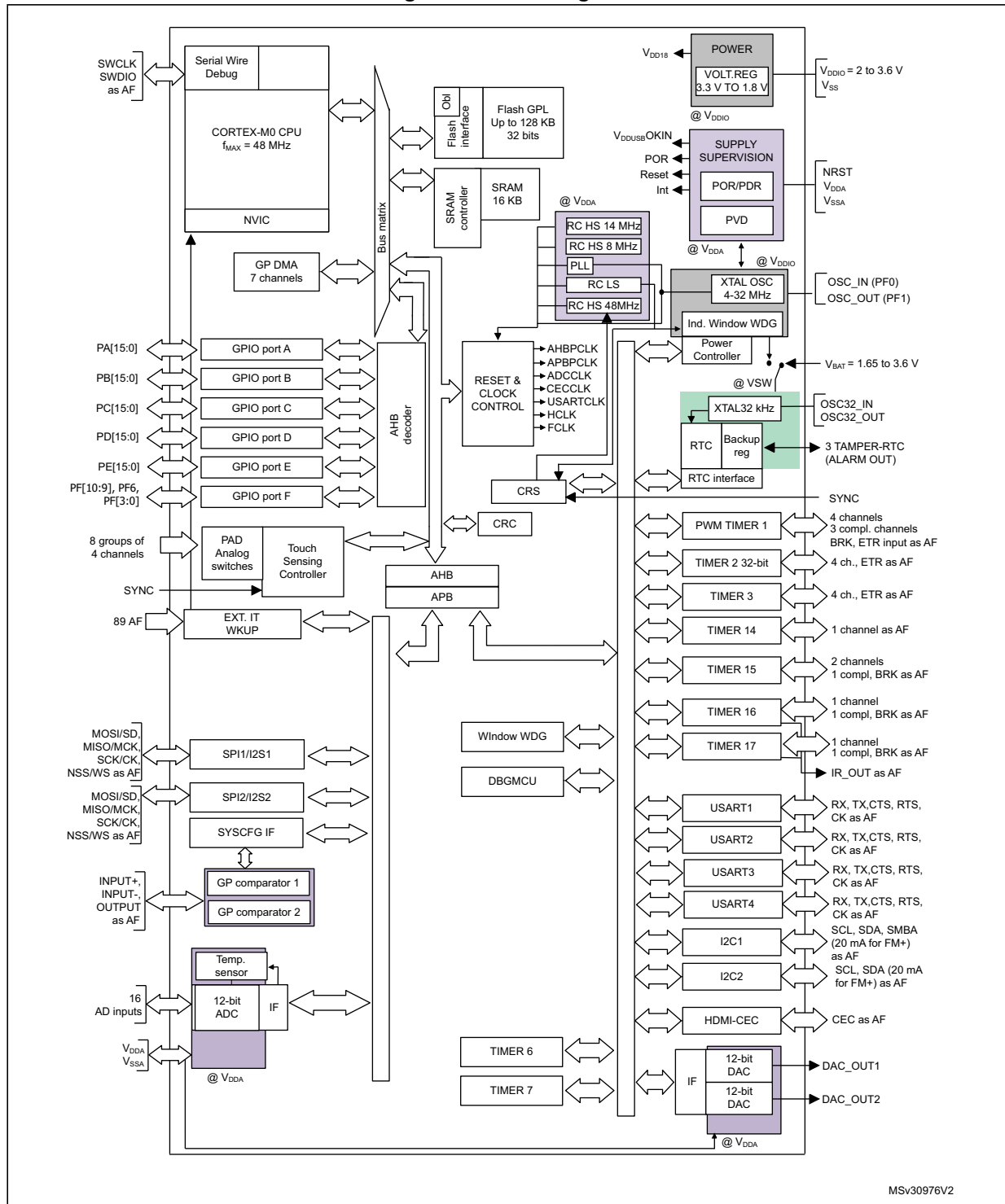
These features make the STM32F071xx microcontrollers suitable for a wide range of applications such as application control and user interfaces, handheld equipment, A/V receivers and digital TV, PC peripherals, gaming and GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms, and HVACs.

Table 2. STM32F071xx family device features and peripheral counts

Peripheral		STM32F071CB	STM32F071RB	STM32F071Vx	
Flash (Kbytes)		128	128	64	128
SRAM (Kbytes)		16	16	16	
Timers	Advanced control	1 (16-bit)			
	General purpose	5 (16-bit) 1 (32-bit)			
	Basic	2 (16-bit)			
Comm. interfaces	SPI [I2S] <sup>(1)</sup>	2 [2]			
	I <sup>2</sup> C	2			
	USART	4			
	CEC	1			
12-bit ADC (number of channels)		1 (10 ext. + 3 int.)	1 (16 ext. + 3 int.)		
GPIOs		37	51	87	
Capacitive sensing channels		17	18	24	
12-bit DAC (number of channels)		1 (2)			
Analog comparator		2			
Max. CPU frequency		48 MHz			
Operating voltage		2.0 to 3.6 V			
Operating temperature		Ambient operating temperature: -40 °C to 85 °C / -40 °C to 105 °C Junction temperature: -40 °C to 125 °C			
Packages		LQFP48 UFQFPN48 WLCSP49	LQFP64	LQFP100 UFBGA100	

1. The SPI interface can be used either in SPI mode or in I2S audio mode.

Figure 1. Block diagram



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## 3 Functional overview

### 3.1 ARM Cortex-M0 core with embedded Flash and SRAM

The ARM Cortex-M0 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex-M0 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The STM32F0xx family has an embedded ARM core and is therefore compatible with all ARM tools and software.

*Figure 1* shows the general block diagram of the device family.

### 3.2 Memories

The device has the following features:

- 16 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states and featuring embedded parity checking with exception generation for fail-critical applications.
- The non-volatile memory is divided into two arrays:
  - 64 to 128 Kbytes of embedded Flash memory for programs and data
  - Option bytes

The option bytes are used to write-protect the memory (with 4 KB granularity) and/or readout-protect the whole memory with the following options:

- Level 0: no readout protection
- Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
- Level 2: chip readout protection, debug features (Cortex-M0 serial wire) and boot in RAM selection disabled

### 3.3 Boot modes

At startup, the boot pin and boot selector option bits are used to select one of the three boot options:

- Boot from User Flash
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART on pins PA14/PA15 or PA9/PA10, I2C on pins PB6/PB7.

## 3.4 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

## 3.5 Power management

### 3.5.1 Power supply schemes

- $V_{DD} = 2.0$  to  $3.6$  V: external power supply for I/Os and the internal regulator. Provided externally through  $V_{DD}$  pins.
- $V_{DDA} = 2.0$  to  $3.6$  V: external analog power supply for ADC, Reset blocks, RCs and PLL (minimum voltage to be applied to  $V_{DDA}$  is  $2.4$  V when the ADC is used). The  $V_{DDA}$  voltage level must be always greater or equal to the  $V_{DD}$  voltage level and must be provided first.
- $V_{DDIO2} = 1.65$  to  $3.6$  V: external power supply for marked I/Os. Provided externally through the  $V_{DDIO2}$  pin. The  $V_{DDIO2}$  voltage level is completely independent from  $V_{DD}$  or  $V_{DDA}$ , but it must not be provided without a valid supply on  $V_{DD}$ . Refer to the pinout diagrams or tables for concerned I/Os list.
- $V_{BAT} = 1.65$  to  $3.6$  V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when  $V_{DD}$  is not present.

### 3.5.2 Power supply supervisors

The device has integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 2 V. The device remains in reset mode when the monitored supply voltage is below a specified threshold,  $V_{POR/PDR}$ , without the need for an external reset circuit.

- The POR monitors only the  $V_{DD}$  supply voltage. During the startup phase it is required that  $V_{DDA}$  should arrive first and be greater than or equal to  $V_{DD}$ .
- The PDR monitors both the  $V_{DD}$  and  $V_{DDA}$  supply voltages, however the  $V_{DDA}$  power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that  $V_{DDA}$  is higher than or equal to  $V_{DD}$ .

The  $V_{DDIO2}$  supply is monitored and compared with the internal reference voltage ( $V_{REFINT}$ ). When the  $V_{DDIO2}$  is below this threshold, all the I/Os supplied from this rail are disabled by hardware. The output of this comparator is connected to EXTI line 31 and it can be used to generate an interrupt.

The device features an embedded programmable voltage detector (PVD) that monitors the  $V_{DD}$  power supply and compares it to the  $V_{PVD}$  threshold. An interrupt can be generated when  $V_{DD}$  drops below the  $V_{PVD}$  threshold and/or when  $V_{DD}$  is higher than the  $V_{PVD}$  threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

### 3.5.3 Voltage regulator

The regulator has two operating modes and it is always enabled after reset.

- Main (MR) is used in normal operating mode (Run).
- Low power (LPR) can be used in Stop mode where the power demand is reduced.

In Standby mode, it is put in power down mode. In this mode, the regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost).

### 3.5.4 Low-power modes

The STM32F071xx microcontrollers support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

Stop mode achieves very low power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.

The device can be woken up from Stop mode by any of the EXTI lines. The EXTI line source can be one of the 16 external lines, the PVD output, RTC alarm, I2C1, USART1 or the CEC.

The I2C1, USART1 and the CEC can be configured to enable the HSI RC oscillator for processing incoming data. If this is used when the voltage regulator is put in low power mode, the regulator is first switched to normal mode before the clock is provided to the given peripheral.

- **Standby mode**

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the RTC domain and Standby circuitry.

The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pins, or an RTC event occurs.

*Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.*

## 3.6 Clocks and startup

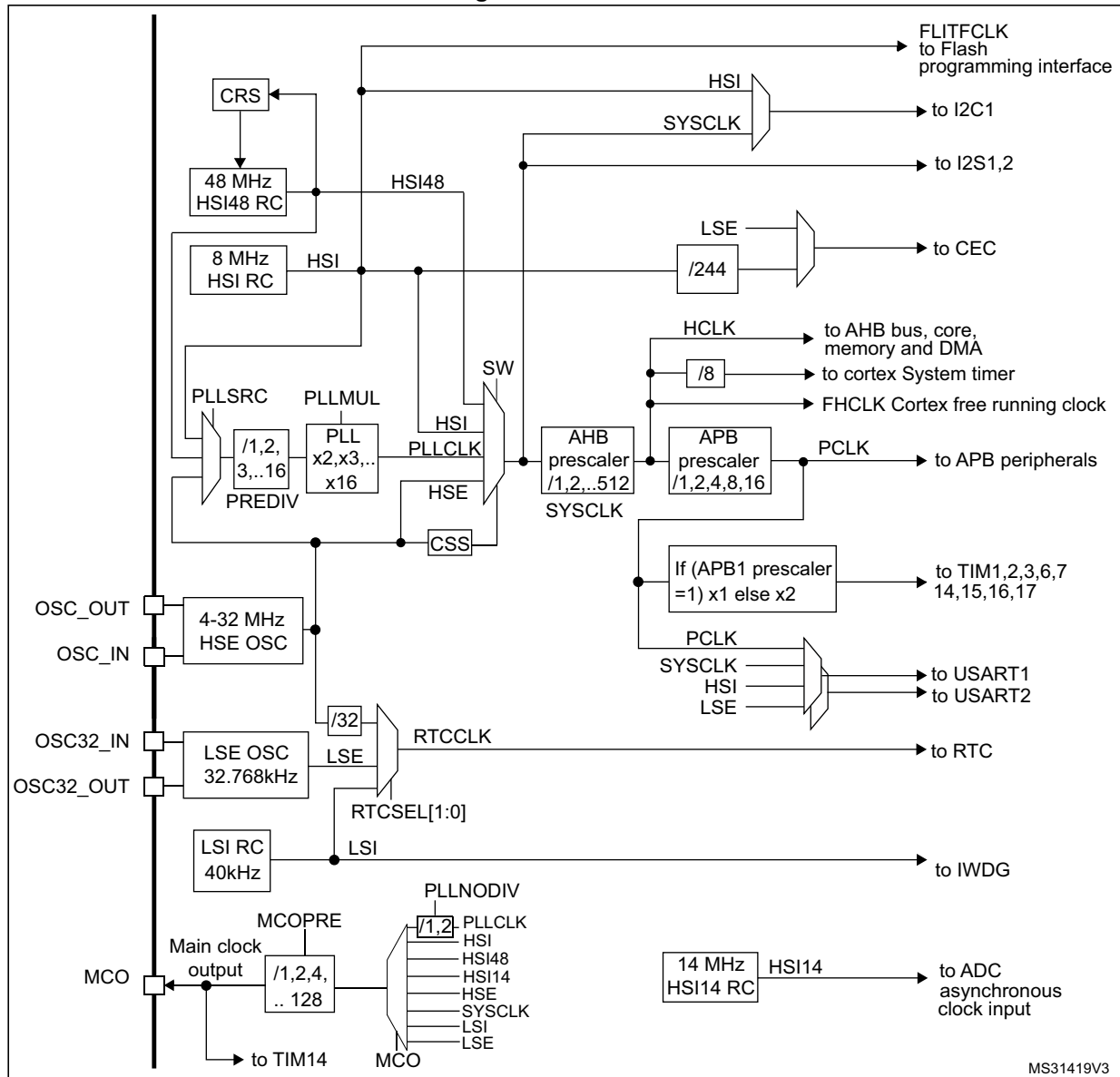
System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the application to configure the frequency of the AHB and the APB domains. The maximum frequency of the AHB and the APB domains is 48 MHz.

Additionally, also the internal RC 48 MHz oscillator can be selected for system clock or PLL input source. This oscillator can be automatically fine-trimmed by the means of the CRS peripheral using the external synchronization.



Figure 2. Clock tree



MS31419V3

### 3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

The I/O configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

## 3.8 Direct memory access controller (DMA)

The 7-channel general-purpose DMAs manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers.

The DMA supports circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

DMA can be used with the main peripherals: SPI, I2S, I2C, USART, all TIMx timers (except TIM14), DAC and ADC.

## 3.9 Interrupts and events

### 3.9.1 Nested vectored interrupt controller (NVIC)

The STM32F0xx family embeds a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels (not including the 16 interrupt lines of Cortex-M0) and 4 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

### 3.9.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 32 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 87 GPIOs can be connected to the 16 external interrupt lines.

## 3.10 Analog to digital converter (ADC)

The 12-bit analog to digital converter has up to 16 external and 3 internal (temperature sensor, voltage reference, VBAT voltage measurement) channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

### 3.10.1 Temperature sensor

The temperature sensor (TS) generates a voltage  $V_{SENSE}$  that varies linearly with temperature.

The temperature sensor is internally connected to the ADC\_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

**Table 3. Temperature sensor calibration values**

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at a temperature of 30 °C ( $\pm 5$ °C), $V_{DDA} = 3.3$ V ( $\pm 10$ mV)	0x1FFF F7B8 - 0x1FFF F7B9
TS_CAL2	TS ADC raw data acquired at a temperature of 110 °C ( $\pm 5$ °C), $V_{DDA} = 3.3$ V ( $\pm 10$ mV)	0x1FFF F7C2 - 0x1FFF F7C3

### 3.10.2 Internal voltage reference ( $V_{REFINT}$ )

The internal voltage reference ( $V_{REFINT}$ ) provides a stable (bandgap) voltage output for the ADC.  $V_{REFINT}$  is internally connected to the ADC\_IN17 input channel. The precise voltage of  $V_{REFINT}$  is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

**Table 4. Internal voltage reference calibration values**

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at a temperature of 30 °C ( $\pm 5$ °C), $V_{DDA} = 3.3$ V ( $\pm 10$ mV)	0x1FFF F7BA - 0x1FFF F7BB

### 3.10.3 $V_{BAT}$ battery voltage monitoring

This embedded hardware feature allows the application to measure the  $V_{BAT}$  battery voltage using the internal ADC channel ADC\_IN18. As the  $V_{BAT}$  voltage may be higher than  $V_{DDA}$ , and thus outside the ADC input range, the  $V_{BAT}$  pin is internally connected to a bridge divider by 2. As a consequence, the converted digital value is half the  $V_{BAT}$  voltage.

### 3.11 Digital-to-analog converter (DAC)

The two 12-bit buffered DAC channels can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in non-inverting configuration.

This digital Interface supports the following features:

- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion

Six DAC trigger inputs are used in the device. The DAC is triggered through the timer trigger outputs and the DAC interface is generating its own DMA requests.

### 3.12 Comparators (COMP)

The device embeds two fast rail-to-rail low-power comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output pins
- Internal reference voltage or submultiple (1/4, 1/2, 3/4). Refer to [Table 28: Embedded internal reference voltage](#) for the value and precision of the internal reference voltage.

Both comparators can wake up from STOP mode, generate interrupts and breaks for the timers and can be also combined into a window comparator.

### 3.13 Touch sensing controller (TSC)

The STM32F071xx devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 24 capacitive sensing channels distributed over 8 analog I/O groups.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage, this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library, which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

**Table 5. Capacitive sensing GPIOs available on STM32F071xx devices**

Group	Capacitive sensing signal name	Pin name	Group	Capacitive sensing signal name	Pin name
1	TSC_G1_IO1	PA0	5	TSC_G5_IO1	PB3
	TSC_G1_IO2	PA1		TSC_G5_IO2	PB4
	TSC_G1_IO3	PA2		TSC_G5_IO3	PB6
	TSC_G1_IO4	PA3		TSC_G5_IO4	PB7
2	TSC_G2_IO1	PA4	6	TSC_G6_IO1	PB11
	TSC_G2_IO2	PA5		TSC_G6_IO2	PB12
	TSC_G2_IO3	PA6		TSC_G6_IO3	PB13
	TSC_G2_IO4	PA7		TSC_G6_IO4	PB14
3	TSC_G3_IO1	PC5	7	TSC_G7_IO1	PE2
	TSC_G3_IO2	PB0		TSC_G7_IO2	PE3
	TSC_G3_IO3	PB1		TSC_G7_IO3	PE4
	TSC_G3_IO4	PB2		TSC_G7_IO4	PE5
4	TSC_G4_IO1	PA9	8	TSC_G8_IO1	PD12
	TSC_G4_IO2	PA10		TSC_G8_IO2	PD13
	TSC_G4_IO3	PA11		TSC_G8_IO3	PD14
	TSC_G4_IO4	PA12		TSC_G8_IO4	PD15

**Table 6. No. of capacitive sensing channels available on STM32F071xx devices**

Analog I/O group	Number of capacitive sensing channels		
	STM32F071Vx	STM32F071Rx	STM32F071Cx
G1	3	3	3
G2	3	3	3
G3	3	3	2
G4	3	3	3
G5	3	3	3
G6	3	3	3
G7	3	0	0
G8	3	0	0
Number of capacitive sensing channels	24	18	17

### 3.14 Timers and watchdogs

The STM32F071xx devices include up to six general-purpose timers, two basic timers and an advanced control timer.

*Table 7* compares the features of the advanced-control, general-purpose and basic timers.

**Table 7. Timer feature comparison**

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
Advanced control	TIM1	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	Yes
General purpose	TIM2	32-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
	TIM3	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
	TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No
	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	Yes
	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	Yes
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

### 3.14.1 Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on six channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers via the Timer Link feature for synchronization or event chaining.

### 3.14.2 General-purpose timers (TIM2..3, TIM14..17)

There are six synchronizable general-purpose timers embedded in the STM32F071xx devices (see [Table 7](#) for differences). Each general-purpose timer can be used to generate PWM outputs, or as simple time base.

#### TIM2, TIM3

STM32F071xx devices feature two synchronizable 4-channel general-purpose timers. TIM2 is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. TIM3 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM2 and TIM3 general-purpose timers can work together or with the TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining.

TIM2 and TIM3 both have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Their counters can be frozen in debug mode.

#### TIM14

This timer is based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM14 features one single channel for input capture/output compare, PWM or one-pulse mode output.

Its counter can be frozen in debug mode.

#### TIM15, TIM16 and TIM17

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM15 has two independent channels, whereas TIM16 and TIM17 feature one single

channel for input capture/output compare, PWM or one-pulse mode output.

The TIM15, TIM16 and TIM17 timers can work together, and TIM15 can also operate with TIM1 via the Timer Link feature for synchronization or event chaining.

TIM15 can be synchronized with TIM16 and TIM17.

TIM15, TIM16 and TIM17 have a complementary output with dead-time generation and independent DMA request generation.

Their counters can be frozen in debug mode.

### 3.14.3 Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

### 3.14.4 Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit downcounter with user-defined refresh window. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

### 3.14.5 System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability and the counter can be frozen in debug mode.

### 3.14.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source (HCLK or HCLK/8)

## 3.15 Real-time clock (RTC) and backup registers

The RTC and the 5 backup registers are supplied through a switch that takes power either on  $V_{DD}$  supply when present or through the  $V_{BAT}$  pin. The backup registers are five 32-bit registers used to store 20 bytes of user application data when  $V_{DD}$  power is not present. They are not reset by a system or power reset, or when the device wakes up from Standby mode.



The RTC is an independent BCD timer/counter. Its main features are the following:

- Calendar with subseconds, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatically correction for 28, 29 (leap year), 30, and 31 day of the month.
- Programmable alarm with wake up from Stop and Standby mode capability.
- Periodic wakeup unit with programmable resolution and period.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy.
- 3 anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32

### 3.16 Inter-integrated circuit interfaces (I<sup>2</sup>C)

Up to two I<sup>2</sup>C interfaces (I2C1 and I2C2) can operate in multimaster or slave modes. Both can support Standard mode (up to 100 kbit/s), Fast mode (up to 400 kbit/s) and Fast Mode Plus (up to 1 Mbit/s) with 20 mA output drive on some I/Os.

Both support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). They also include programmable analog and digital noise filters.

**Table 8. Comparison of I2C analog and digital filters**

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, I2C1 provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts

verifications and ALERT protocol management. I2C1 also has a clock domain independent from the CPU clock, allowing the I2C1 to wake up the MCU from Stop mode on address match.

The I2C interfaces can be served by the DMA controller.

Refer to [Table 9](#) for the differences between I2C1 and I2C2.

**Table 9. STM32F071xx I<sup>2</sup>C implementation**

I2C features <sup>(1)</sup>	I2C1	I2C2
7-bit addressing mode	X	X
10-bit addressing mode	X	X
Standard mode (up to 100 kbit/s)	X	X
Fast mode (up to 400 kbit/s)	X	X
Fast Mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	X	X
Independent clock	X	
SMBus	X	
Wakeup from STOP	X	

1. X = supported.

### 3.17 Universal synchronous/asynchronous receiver transmitters (USART)

The device embeds up to four universal synchronous/asynchronous receiver transmitters (USART1, USART2, USART3 and USART4), which communicate at speeds of up to 6 Mbit/s.

They provide hardware management of the CTS, RTS and RS485 DE signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. USART1 and USART2 support also SmartCard communication (ISO 7816), IrDA SIR ENDEC, LIN Master/Slave capability and auto baud rate feature, and have a clock domain independent from the CPU clock, allowing USART1 and USART2 to wake up the MCU from Stop mode.

The USART interfaces can be served by the DMA controller.

Refer to [Table 10](#) for the differences between USART1, USART2, USART3 and USART4.

**Table 10. STM32F071xx USART implementation**

USART modes/features <sup>(1)</sup>	USART1 and USART2	USART3 and USART4
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous mode	X	X

**Table 10. STM32F071xx USART implementation (continued)**

USART modes/features <sup>(1)</sup>	USART1 and USART2	USART3 and USART4
Smartcard mode	X	
Single-wire half-duplex communication	X	X
IrDA SIR ENDEC block	X	
LIN mode	X	
Dual clock domain and wakeup from Stop mode	X	
Receiver timeout interrupt	X	
Modbus communication	X	
Auto baud rate detection	X	
Driver Enable	X	X

1. X = supported.

### 3.18 Serial peripheral interface (SPI)/Inter-integrated sound interfaces (I<sup>2</sup>S)

Up to two SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

Two standard I<sup>2</sup>S interfaces (multiplexed with SPI1 and SPI2 respectively) supporting four different audio standards can operate as master or slave at half-duplex communication mode. They can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by an 8-bit programmable linear prescaler. When operating in master mode, they can output a clock for an external audio component at 256 times the sampling frequency.

Both SPI1 and SPI2 are identical and implement the set of features shown in the following table.

**Table 11. STM32F071xx SPI/I2S implementation**

SPI features <sup>(1)</sup>	SPI1 and SPI2
Hardware CRC calculation	X
Rx/Tx FIFO	X
NSS pulse mode	X
I2S mode	X
TI mode	X

1. X = supported.

### 3.19 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The device embeds a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI\_CEC controller to wakeup the MCU from Stop mode on data reception.

### 3.20 Clock recovery system (CRS)

The STM32F071xx embeds a special block which allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range. This automatic trimming is based on the external synchronization signal, which could be either derived from LSE oscillator, from an external signal on CRS\_SYNC pin or generated by user software. For faster lock-in during startup it is also possible to combine automatic trimming with manual trimming action.

### 3.21 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

# 4 Pinouts and pin descriptions

Figure 3. UFBGA100 package ballout (top view)

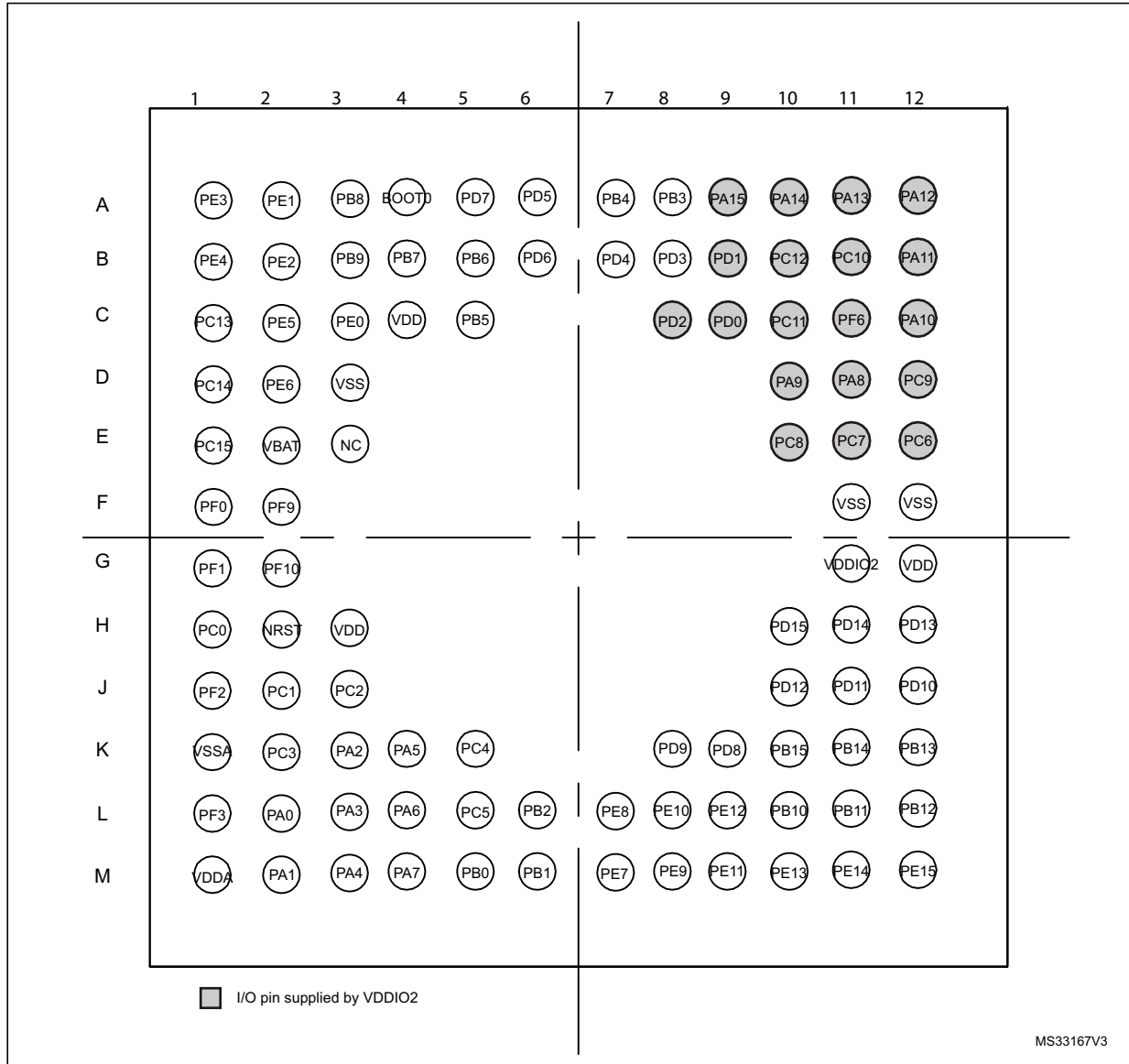


Figure 4. LQFP100 100-pin package pinout (top view)

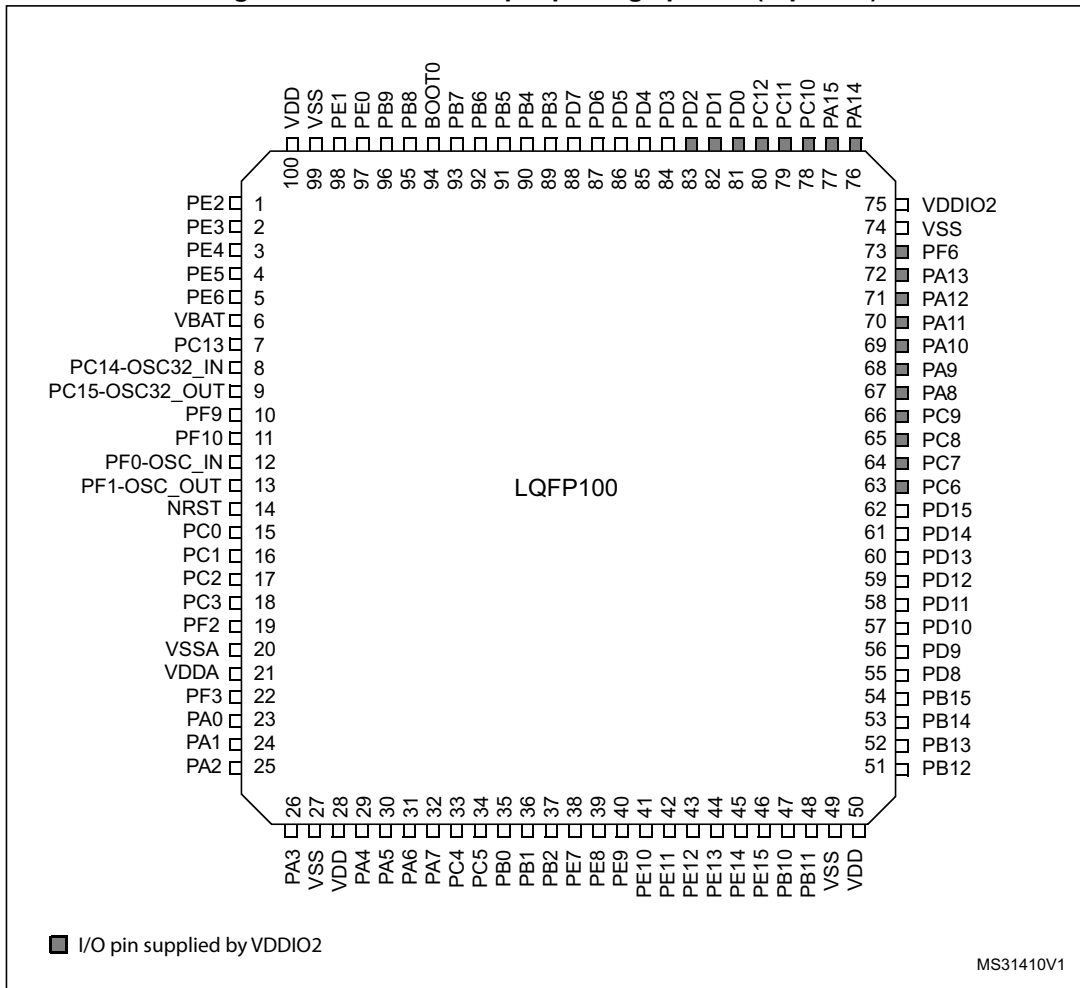


Figure 5. LQFP64 64-pin package pinout (top view)

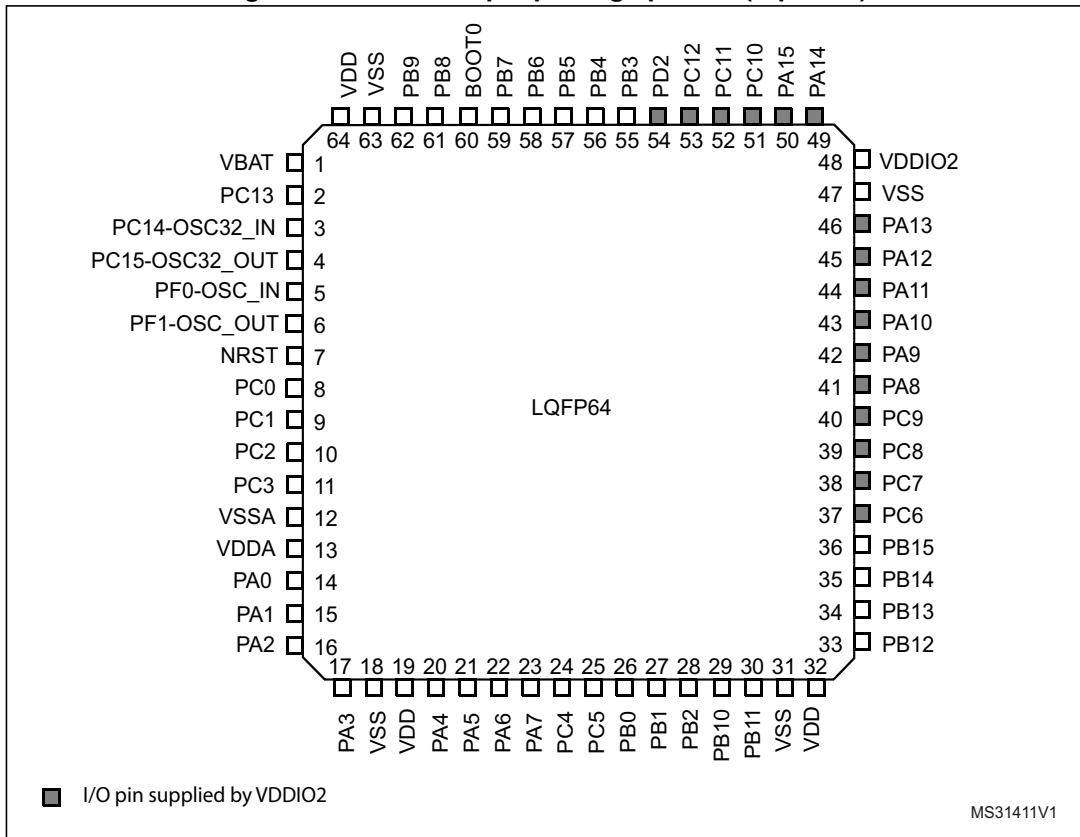


Figure 6. LQFP48 48-pin package pinout (top view)

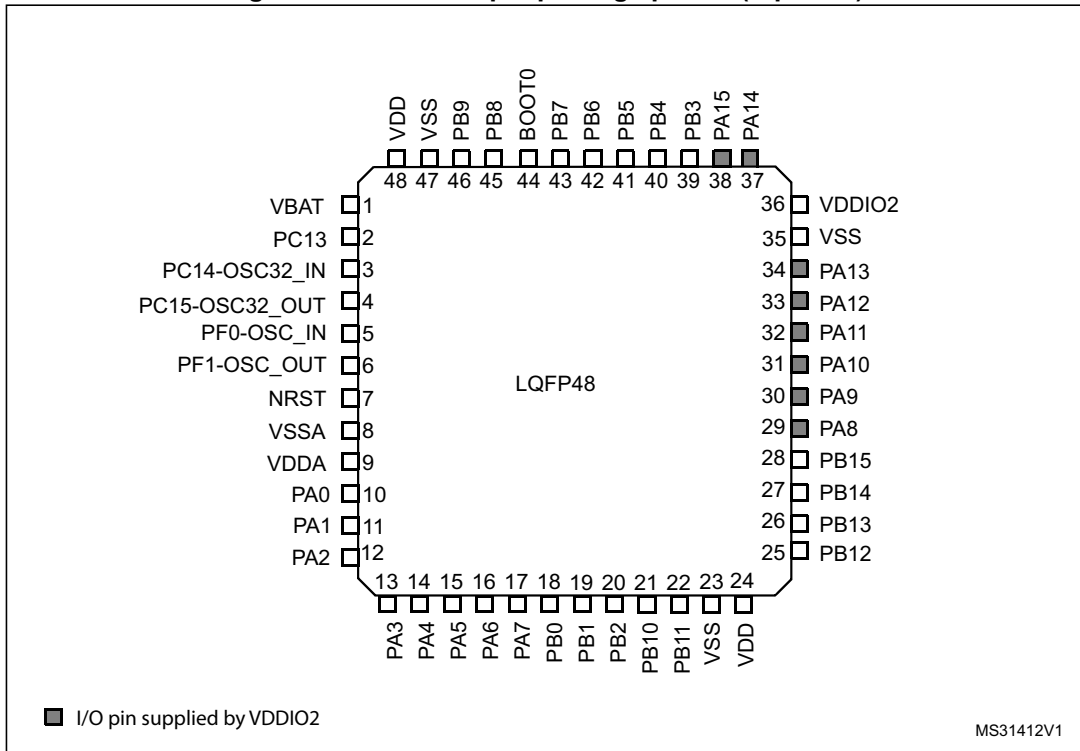


Figure 7. UFQFPN48 48-pin package pinout (top view)

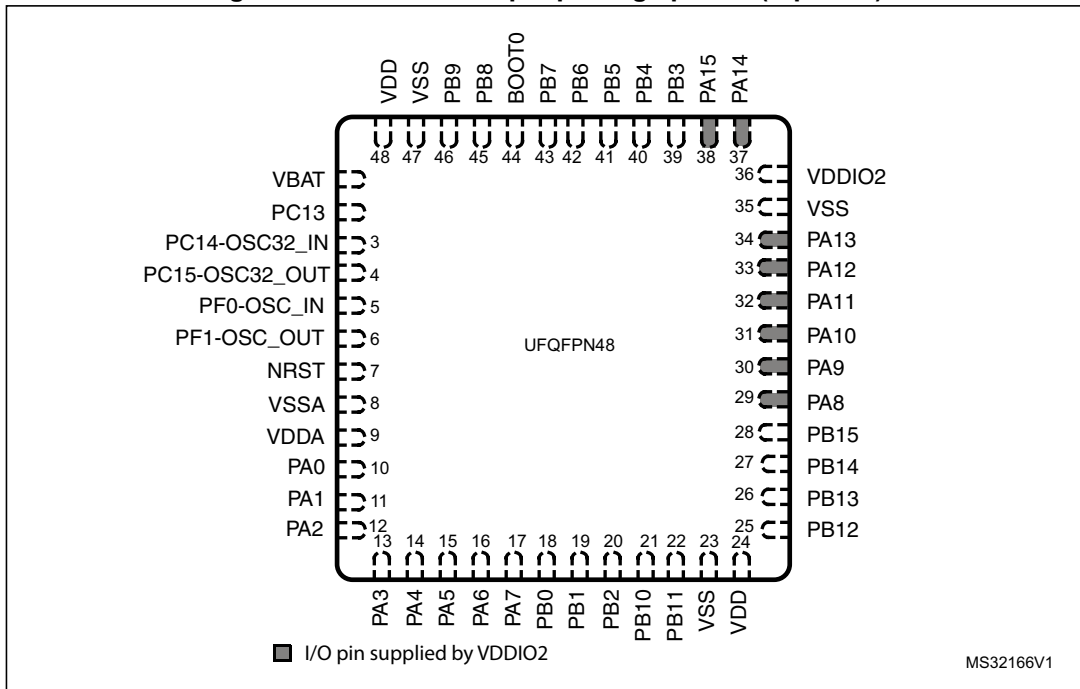
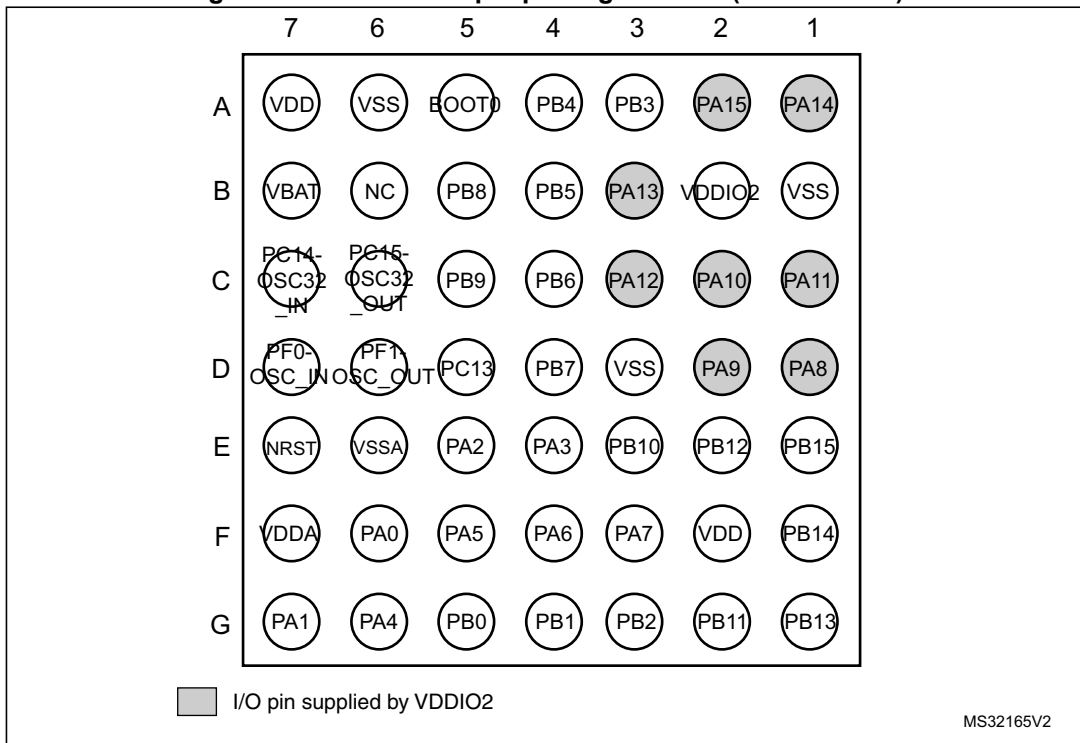


Figure 8. WLCSP49 49-pin package ballout (bottom view)





**Table 12. Legend/abbreviations used in the pinout table**

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		FTf	5 V tolerant I/O, FM+ capable
		TTa	3.3 V tolerant I/O directly connected to ADC
		TC	Standard 3.3 V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

**Table 13. STM32F071xx pin definitions**

Pin numbers					Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
UFBGA100	LQFP100	LQFP64	LQFP48/UFQFPN48	WLCSP49					Alternate functions	Additional functions
B2	1	-	-	-	PE2	I/O	FT		TSC_G7_IO1, TIM3_ETR	-
A1	2	-	-	-	PE3	I/O	FT		TSC_G7_IO2, TIM3_CH1	-
B1	3	-	-	-	PE4	I/O	FT		TSC_G7_IO3, TIM3_CH2	-
C2	4	-	-	-	PE5	I/O	FT		TSC_G7_IO4, TIM3_CH3	-
D2	5	-	-	-	PE6	I/O	FT		TIM3_CH4	WKUP3, RTC_TAMP3
E2	6	1	1	B7	VBAT	S			Backup power supply	
C1	7	2	2	D5	PC13	I/O	TC	(1) (2)	-	WKUP2, RTC_TAMP1, RTC_TS, RTC_OUT

Table 13. STM32F071xx pin definitions (continued)

Pin numbers					Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
UFBGA100	LQFP100	LQFP64	LQFP48/UFP48	WLCSP49					Alternate functions	Additional functions
D1	8	3	3	C7	PC14-OSC32_IN (PC14)	I/O	TC	(1) (2)	-	OSC32_IN
E1	9	4	4	C6	PC15- OSC32_OUT (PC15)	I/O	TC	(1) (2)	-	OSC32_OUT
F2	10	-	-	-	PF9	I/O	FT		TIM15_CH1	-
G2	11	-	-	-	PF10	I/O	FT		TIM15_CH2	-
F1	12	5	5	D7	PF0-OSC_IN (PF0)	I	FT		CRS_SYNC	OSC_IN
G1	13	6	6	D6	PF1-OSC_OUT (PF1)	O	FT		-	OSC_OUT
H2	14	7	7	E7	NRST	I/O	RST		Device reset input / internal reset output (active low)	
H1	15	8	-	-	PC0	I/O	TTa		EVENTOUT	ADC_IN10
J2	16	9	-	-	PC1	I/O	TTa		EVENTOUT	ADC_IN11
J3	17	10	-	-	PC2	I/O	TTa		SPI2_MISO, I2S2_MCK, EVENTOUT	ADC_IN12
K2	18	11	-	-	PC3	I/O	TTa		SPI2_MOSI, I2S2_SD, EVENTOUT	ADC_IN13
J1	19	-	-	-	PF2	I/O	FT		EVENTOUT	WKUP8
K1	20	12	8	E6	VSSA	S			Analog ground	
M1	21	13	9	F7	VDDA	S			Analog power supply	
L1	22	-	-	-	PF3	I/O	FT		EVENTOUT	
L2	23	14	10	F6	PA0	I/O	TTa		USART2_CTS, TIM2_CH1_ETR, TSC_G1_IO1, USART4_TX	RTC_TAMP2, WKUP1, COMP1_OUT, ADC_IN0, COMP1_INM6
M2	24	15	11	G7	PA1	I/O	TTa		USART2_RTS, TIM2_CH2, TIM15_CH1N, TSC_G1_IO2, USART4_RX, EVENTOUT	ADC_IN1, COMP1_INP

Table 13. STM32F071xx pin definitions (continued)

Pin numbers					Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
UFBGA100	LQFP100	LQFP64	LQFP48/JUFQFPN48	WLCSP49					Alternate functions	Additional functions
K3	25	16	12	E5	PA2	I/O	TTa	USART2_TX, TIM2_CH3, TIM15_CH1, TSC_G1_IO3	ADC_IN2, COMP2_OUT, COMP2_INM6, WKUP4	
L3	26	17	13	E4	PA3	I/O	TTa	USART2_RX, TIM2_CH4, TIM15_CH2, TSC_G1_IO4	ADC_IN3, COMP2_INP	
D3	27	18	-	-	VSS	S		Ground		
H3	28	19	-	-	VDD	S		Digital power supply		
M3	29	20	14	G6	PA4	I/O	TTa	SPI1_NSS, I2S1_WS, TIM14_CH1, TSC_G2_IO1, USART2_CK	COMP1_INM4, COMP2_INM4, ADC_IN4, DAC_OUT1	
K4	30	21	15	F5	PA5	I/O	TTa	SPI1_SCK, I2S1_CK, CEC, TIM2_CH1_ETR, TSC_G2_IO2	COMP1_INM5, COMP2_INM5, ADC_IN5, DAC_OUT2	
L4	31	22	16	F4	PA6	I/O	TTa	SPI1_MISO, I2S1_MCK, TIM3_CH1, TIM1_BKIN, TIM16_CH1, COMP1_OUT, TSC_G2_IO3, EVENTOUT, USART3_CTS	ADC_IN6	
M4	32	23	17	F3	PA7	I/O	TTa	SPI1_MOSI, I2S1_SD, TIM3_CH2, TIM14_CH1, TIM1_CH1N, TIM17_CH1, COMP2_OUT, TSC_G2_IO4, EVENTOUT	ADC_IN7	
K5	33	24	-	-	PC4	I/O	TTa	EVENTOUT, USART3_TX	ADC_IN14	
L5	34	25	-	-	PC5	I/O	TTa	TSC_G3_IO1, USART3_RX	ADC_IN15, WKUP5	
M5	35	26	18	G5	PB0	I/O	TTa	TIM3_CH3, TIM1_CH2N, TSC_G3_IO2, EVENTOUT, USART3_CK	ADC_IN8	
M6	36	27	19	G4	PB1	I/O	TTa	TIM3_CH4, USART3_RTS, TIM14_CH1, TIM1_CH3N, TSC_G3_IO3	ADC_IN9	
L6	37	28	20	G3	PB2	I/O	FT	TSC_G3_IO4	-	

Table 13. STM32F071xx pin definitions (continued)

Pin numbers					Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
UFBGA100	LQFP100	LQFP64	LQFP48/UQFPN48	WLCSP49					Alternate functions	Additional functions
M7	38	-	-	-	PE7	I/O	FT		TIM1_ETR	-
L7	39	-	-	-	PE8	I/O	FT		TIM1_CH1N	-
M8	40	-	-	-	PE9	I/O	FT		TIM1_CH1	-
L8	41	-	-	-	PE10	I/O	FT		TIM1_CH2N	-
M9	42	-	-	-	PE11	I/O	FT		TIM1_CH2	-
L9	43	-	-	-	PE12	I/O	FT		SPI1_NSS, I2S1_WS, TIM1_CH3N	-
M10	44	-	-	-	PE13	I/O	FT		SPI1_SCK, I2S1_CK, TIM1_CH3	-
M11	45	-	-	-	PE14	I/O	FT		SPI1_MISO, I2S1_MCK, TIM1_CH4	-
M12	46	-	-	-	PE15	I/O	FT		SPI1_MOSI, I2S1_SD, TIM1_BKIN	-
L10	47	29	21	E3	PB10	I/O	FT		SPI2_SCK, I2C2_SCL, USART3_TX, CEC, TSC_SYNC, TIM2_CH3	-
L11	48	30	22	G2	PB11	I/O	FT		USART3_RX, TIM2_CH4, EVENTOUT, TSC_G6_IO1, I2C2_SDA	-
F12	49	31	23	D3	VSS	S			Ground	
G12	50	32	24	F2	VDD	S			Digital power supply	
L12	51	33	25	E2	PB12	I/O	FT		TIM1_BKIN, TIM15_BKIN, SPI2_NSS, I2S2_WS, USART3_CK, TSC_G6_IO2, EVENTOUT	-
K12	52	34	26	G1	PB13	I/O	FTf		SPI2_SCK, I2S2_CK, I2C2_SCL, USART3_CTS, TIM1_CH1N, TSC_G6_IO3	-
K11	53	35	27	F1	PB14	I/O	FTf		SPI2_MISO, I2S2_MCK, I2C2_SDA, USART3_RTS, TIM1_CH2N, TIM15_CH1, TSC_G6_IO4	-

Table 13. STM32F071xx pin definitions (continued)

Pin numbers					Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
UFBGA100	LQFP100	LQFP64	LQFP48/UQFPN48	WLCSP49					Alternate functions	Additional functions
K10	54	36	28	E1	PB15	I/O	FT		SPI2_MOSI, I2S2_SD, TIM1_CH3N, TIM15_CH1N, TIM15_CH2	WKUP7, RTC_REFIN
K9	55	-	-	-	PD8	I/O	FT		USART3_TX	-
K8	56	-	-	-	PD9	I/O	FT		USART3_RX	-
J12	57	-	-	-	PD10	I/O	FT		USART3_CK	-
J11	58	-	-	-	PD11	I/O	FT		USART3_CTS	-
J10	59	-	-	-	PD12	I/O	FT		USART3_RTS, TSC_G8_IO1	-
H12	60	-	-	-	PD13	I/O	FT		TSC_G8_IO2	-
H11	61	-	-	-	PD14	I/O	FT		TSC_G8_IO3	-
H10	62	-	-	-	PD15	I/O	FT		TSC_G8_IO4, CRS_SYNC	-
E12	63	37	-	-	PC6	I/O	FT	(3)	TIM3_CH1	-
E11	64	38	-	-	PC7	I/O	FT	(3)	TIM3_CH2	-
E10	65	39	-	-	PC8	I/O	FT	(3)	TIM3_CH3	-
D12	66	40	-	-	PC9	I/O	FT	(3)	TIM3_CH4	-
D11	67	41	29	D1	PA8	I/O	FT	(3)	USART1_CK, TIM1_CH1, EVENTOUT, MCO, CRS_SYNC	-
D10	68	42	30	D2	PA9	I/O	FT	(3)	USART1_TX, TIM1_CH2, TIM15_BKIN, TSC_G4_IO1	-
C12	69	43	31	C2	PA10	I/O	FT	(3)	USART1_RX, TIM1_CH3, TIM17_BKIN, TSC_G4_IO2	-
B12	70	44	32	C1	PA11	I/O	FT	(3)	USART1_CTS, TIM1_CH4, COMP1_OUT, TSC_G4_IO3, EVENTOUT	-
A12	71	45	33	C3	PA12	I/O	FT	(3)	USART1_RTS, TIM1_ETR, COMP2_OUT, TSC_G4_IO4, EVENTOUT	-
A11	72	46	34	B3	PA13	I/O	FT	(3) (4)	IR_OUT, SWDIO	-

Table 13. STM32F071xx pin definitions (continued)

Pin numbers					Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
UFBGA100	LQFP100	LQFP64	LQFP48/JUFQFPN48	WLCSP49					Alternate functions	Additional functions
C11	73	-	-	-	PF6	I/O	FT	(3)	-	-
F11	74	47	35	B1	VSS	S			Ground	
G11	75	48	36	B2	VDDIO2	S			Digital power supply	
A10	76	49	37	A1	PA14	I/O	FT	(3) (4)	USART2_TX, SWCLK	-
A9	77	50	38	A2	PA15	I/O	FT	(3)	SPI1_NSS, I2S1_WS, USART2_RX, USART4_RTS, TIM2_CH1_ETR, EVENTOUT	-
B11	78	51	-	-	PC10	I/O	FT	(3)	USART3_TX, USART4_TX	-
C10	79	52	-	-	PC11	I/O	FT	(3)	USART3_RX, USART4_RX	-
B10	80	53	-	-	PC12	I/O	FT	(3)	USART3_CK, USART4_CK	-
C9	81	-	-	-	PD0	I/O	FT	(3)	SPI2_NSS, I2S2_WS	-
B9	82	-	-	-	PD1	I/O	FT	(3)	SPI2_SCK, I2S2_CK	-
C8	83	54	-	-	PD2	I/O	FT	(3)	USART3_RTS, TIM3_ETR	-
B8	84	-	-	-	PD3	I/O	FT		SPI2_MISO, I2S2_MCK, USART2_CTS	-
B7	85	-	-	-	PD4	I/O	FT		SPI2_MOSI, I2S2_SD, USART2_RTS	-
A6	86	-	-	-	PD5	I/O	FT		USART2_TX	-
B6	87	-	-	-	PD6	I/O	FT		USART2_RX	-
A5	88	-	-	-	PD7	I/O	FT		USART2_CK	-
A8	89	55	39	A3	PB3	I/O	FT		SPI1_SCK, I2S1_CK, TIM2_CH2, TSC_G5_IO1, EVENTOUT	-
A7	90	56	40	A4	PB4	I/O	FT		SPI1_MISO, I2S1_MCK, TIM17_BKIN, TIM3_CH1, TSC_G5_IO2, EVENTOUT	-
C5	91	57	41	B4	PB5	I/O	FT		SPI1_MOSI, I2S1_SD, I2C1_SMBA, TIM16_BKIN, TIM3_CH2	WKUP6

Table 13. STM32F071xx pin definitions (continued)

Pin numbers					Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
UFBGA100	LQFP100	LQFP64	LQFP48/JUFQFPN48	WLCSP49					Alternate functions	Additional functions
B5	92	58	42	C4	PB6	I/O	FTf		I2C1_SCL, USART1_TX, TIM16_CH1N, TSC_G5_I03	-
B4	93	59	43	D4	PB7	I/O	FTf		I2C1_SDA, USART1_RX, USART4_CTS, TIM17_CH1N, TSC_G5_I04	-
A4	94	60	44	A5	BOOT0	I	B		Boot memory selection	
A3	95	61	45	B5	PB8	I/O	FTf		I2C1_SCL, CEC, TIM16_CH1, TSC_SYNC	-
B3	96	62	46	C5	PB9	I/O	FTf		SPI2_NSS, I2S2_WS, I2C1_SDA, IR_OUT, TIM17_CH1, EVENTOUT	-
C3	97	-	-	-	PE0	I/O	FT		EVENTOUT, TIM16_CH1	-
A2	98	-	-	-	PE1	I/O	FT		EVENTOUT, TIM17_CH1	-
D3	99	63	47	A6	VSS	S			Ground	
C4	100	64	48	A7	VDD	S			Digital power supply	

- PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
  - The speed should not exceed 2 MHz with a maximum load of 30 pF.
  - These GPIOs must not be used as current sources (e.g. to drive an LED).
- After the first RTC domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers which are not reset by the system reset. For details on how to manage these GPIOs, refer to the RTC domain and RTC register descriptions in the reference manual.
- PC6, PC7, PC8, PC9, PA8, PA9, PA10, PA11, PA12, PA13, PF6, PA14, PA15, PC10, PC11, PC12, PD0, PD1 and PD2 I/Os are supplied by VDDIO2.
- After reset, these pins are configured as SWDIO and SWCLK alternate functions, and the internal pull-up on the SWDIO pin and the internal pull-down on the SWCLK pin are activated.



**Table 14. Alternate functions selected through GPIOA\_AFR registers for port A**

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0		USART2_CTS	TIM2_CH1_ETR	TSC_G1_IO1	USART4_TX			COMP1_OUT
PA1	EVENTOUT	USART2_RTS	TIM2_CH2	TSC_G1_IO2	USART4_RX	TIM15_CH1N		
PA2	TIM15_CH1	USART2_TX	TIM2_CH3	TSC_G1_IO3				COMP2_OUT
PA3	TIM15_CH2	USART2_RX	TIM2_CH4	TSC_G1_IO4				
PA4	SPI1_NSS, I2S1_WS	USART2_CK		TSC_G2_IO1	TIM14_CH1			
PA5	SPI1_SCK, I2S1_CK	CEC	TIM2_CH1_ETR	TSC_G2_IO2				
PA6	SPI1_MISO, I2S1_MCK	TIM3_CH1	TIM1_BKIN	TSC_G2_IO3	USART3_CTS	TIM16_CH1	EVENTOUT	COMP1_OUT
PA7	SPI1_MOSI, I2S1_SD	TIM3_CH2	TIM1_CH1N	TSC_G2_IO4	TIM14_CH1	TIM17_CH1	EVENTOUT	COMP2_OUT
PA8	MCO	USART1_CK	TIM1_CH1	EVENTOUT	CRS_SYNC			
PA9	TIM15_BKIN	USART1_TX	TIM1_CH2	TSC_G4_IO1				
PA10	TIM17_BKIN	USART1_RX	TIM1_CH3	TSC_G4_IO2				
PA11	EVENTOUT	USART1_CTS	TIM1_CH4	TSC_G4_IO3				COMP1_OUT
PA12	EVENTOUT	USART1_RTS	TIM1_ETR	TSC_G4_IO4				COMP2_OUT
PA13	SWDIO	IR_OUT						
PA14	SWCLK	USART2_TX						
PA15	SPI1_NSS, I2S1_WS	USART2_RX	TIM2_CH1_ETR	EVENTOUT	USART4_RTS			



**Table 15. Alternate functions selected through GPIOB\_AFR registers for port B**

Pin name	AF0	AF1	AF2	AF3	AF4	AF5
PB0	EVENTOUT	TIM3_CH3	TIM1_CH2N	TSC_G3_IO2	USART3_CK	
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	TSC_G3_IO3	USART3_RTS	
PB2				TSC_G3_IO4		
PB3	SPI1_SCK, I2S1_CK	EVENTOUT	TIM2_CH2	TSC_G5_IO1		
PB4	SPI1_MISO, I2S1_MCK	TIM3_CH1	EVENTOUT	TSC_G5_IO2		TIM17_BKIN
PB5	SPI1_MOSI, I2S1_SD	TIM3_CH2	TIM16_BKIN	I2C1_SMBA		
PB6	USART1_TX	I2C1_SCL	TIM16_CH1N	TSC_G5_IO3		
PB7	USART1_RX	I2C1_SDA	TIM17_CH1N	TSC_G5_IO4	USART4_CTS	
PB8	CEC	I2C1_SCL	TIM16_CH1	TSC_SYNC		
PB9	IR_OUT	I2C1_SDA	TIM17_CH1	EVENTOUT		SPI2_NSS, I2S2_WS
PB10	CEC	I2C2_SCL	TIM2_CH3	TSC_SYNC	USART3_TX	SPI2_SCK, I2S2_CK
PB11	EVENTOUT	I2C2_SDA	TIM2_CH4	TSC_G6_IO1	USART3_RX	
PB12	SPI2_NSS, I2S2_WS	EVENTOUT	TIM1_BKIN	TSC_G6_IO2	USART3_CK	TIM15_BKIN
PB13	SPI2_SCK, I2S2_CK		TIM1_CH1N	TSC_G6_IO3	USART3_CTS	I2C2_SCL
PB14	SPI2_MISO, I2S2_MCK	TIM15_CH1	TIM1_CH2N	TSC_G6_IO4	USART3_RTS	I2C2_SDA
PB15	SPI2_MOSI, I2S2_SD	TIM15_CH2	TIM1_CH3N	TIM15_CH1N		

**Table 16. Alternate functions selected through GPIOC\_AFR registers for port C**

Pin name	AF0	AF1
PC0	EVENTOUT	-
PC1	EVENTOUT	-
PC2	EVENTOUT	SPI2_MISO, I2S2_MCK
PC3	EVENTOUT	SPI2_MOSI, I2S2_SD
PC4	EVENTOUT	USART3_TX
PC5	TSC_G3_IO1	USART3_RX
PC6	TIM3_CH1	-
PC7	TIM3_CH2	-
PC8	TIM3_CH3	-
PC9	TIM3_CH4	-
PC10	USART4_TX	USART3_TX
PC11	USART4_RX	USART3_RX
PC12	USART4_CK	USART3_CK
PC13	-	-
PC14	-	-
PC15	-	-

**Table 17. Alternate functions selected through GPIOD\_AFR registers for port D**

Pin name	AF0	AF1
PD0	-	SPI2_NSS, I2S2_WS
PD1	-	SPI2_SCK, I2S2_CK
PD2	TIM3_ETR	USART3_RTS
PD3	USART2_CTS	SPI2_MISO, I2S2_MCK
PD4	USART2_RTS	SPI2_MOSI, I2S2_SD
PD5	USART2_TX	-
PD6	USART2_RX	-
PD7	USART2_CK	-
PD8	USART3_TX	-
PD9	USART3_RX	-
PD10	USART3_CK	-
PD11	USART3_CTS	-
PD12	USART3_RTS	TSC_G8_IO1
PD13	-	TSC_G8_IO2
PD14	-	TSC_G8_IO3
PD15	CRS_SYNC	TSC_G8_IO4

**Table 18. Alternate functions selected through GPIOE\_AFR registers for port E**

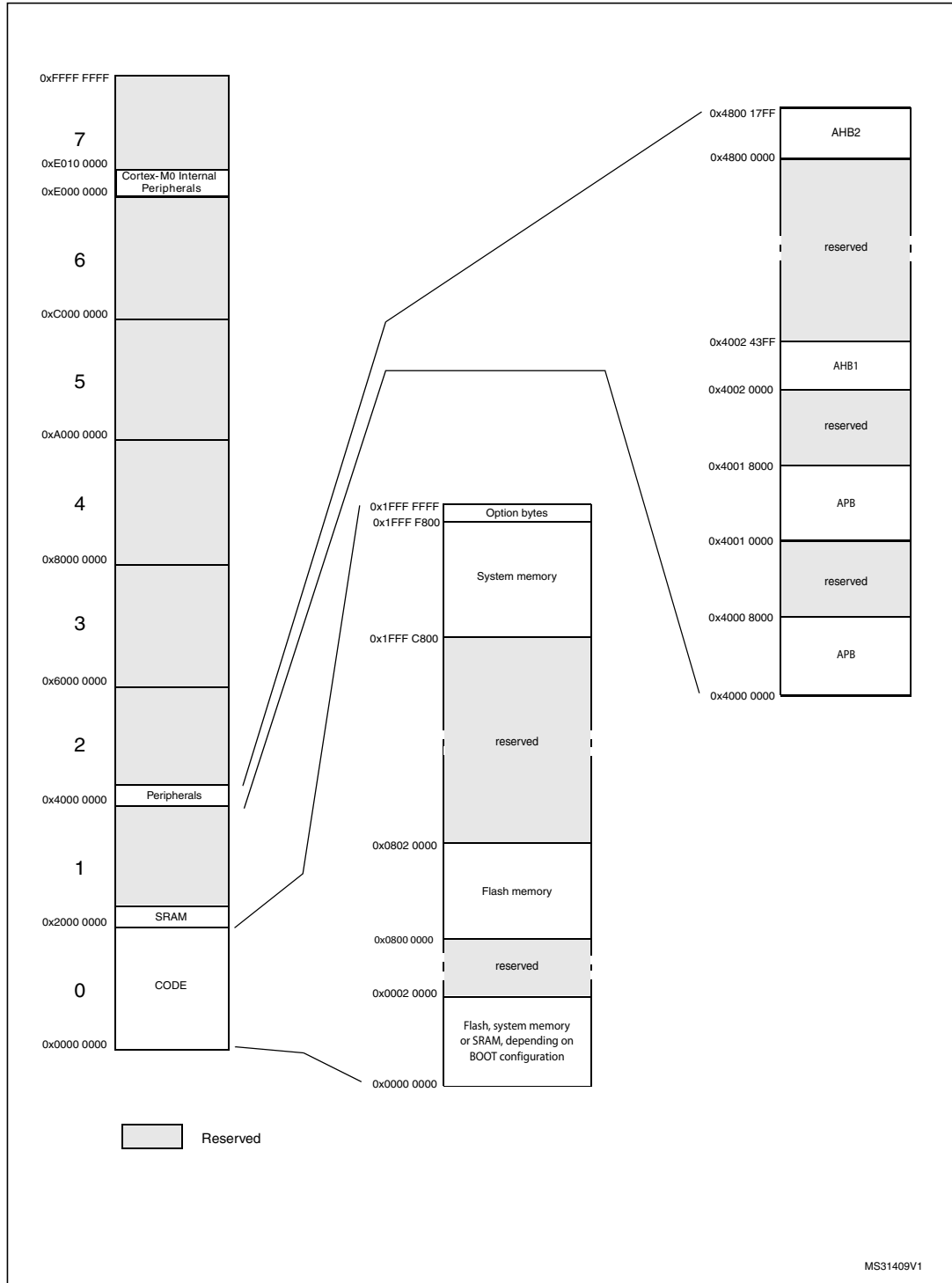
Pin name	AF0	AF1
PE0	TIM16_CH1	EVENTOUT
PE1	TIM17_CH1	EVENTOUT
PE2	TIM3_ETR	TSC_G7_IO1
PE3	TIM3_CH1	TSC_G7_IO2
PE4	TIM3_CH2	TSC_G7_IO3
PE5	TIM3_CH3	TSC_G7_IO4
PE6	TIM3_CH4	-
PE7	TIM1_ETR	-
PE8	TIM1_CH1N	-
PE9	TIM1_CH1	-
PE10	TIM1_CH2N	-
PE11	TIM1_CH2	-
PE12	TIM1_CH3N	SPI1_NSS, I2S1_WS
PE13	TIM1_CH3	SPI1_SCK, I2S1_CK
PE14	TIM1_CH4	SPI1_MISO, I2S1_MCK
PE15	TIM1_BKIN	SPI1_MOSI, I2S1_SD

**Table 19. Alternate functions available on port F**

Pin name	AF
PF0	CRS_SYNC
PF1	-
PF2	EVENTOUT
PF3	EVENTOUT
PF6	-
PF9	TIM15_CH1
PF10	TIM15_CH2

# 5 Memory mapping

Figure 9. STM32F071xx memory map



**Table 20. STM32F071xx peripheral register boundary addresses**

Bus	Boundary address	Size	Peripheral
	0x4800 1800 - 0x5FFF FFFF	~384 MB	Reserved
AHB2	0x4800 1400 - 0x4800 17FF	1 KB	GPIOF
	0x4800 1000 - 0x4800 13FF	1 KB	GPIOE
	0x4800 0C00 - 0x4800 0FFF	1 KB	GPIOD
	0x4800 0800 - 0x4800 0BFF	1 KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1 KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1 KB	GPIOA
	0x4002 4400 - 0x47FF FFFF	~128 MB	Reserved
AHB1	0x4002 4000 - 0x4002 43FF	1 KB	TSC
	0x4002 3400 - 0x4002 3FFF	3 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
	0x4002 2000 - 0x4002 23FF	1 KB	FLASH Interface
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 0400 - 0x4002 0FFF	3 KB	Reserved
	0x4002 0000 - 0x4002 03FF	1 KB	DMA
	0x4001 8000 - 0x4001 FFFF	32 KB	Reserved
APB	0x4001 5C00 - 0x4001 7FFF	9 KB	Reserved
	0x4001 5800 - 0x4001 5BFF	1 KB	DBGMCU
	0x4001 4C00 - 0x4001 57FF	3 KB	Reserved
	0x4001 4800 - 0x4001 4BFF	1 KB	TIM17
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16
	0x4001 4000 - 0x4001 43FF	1 KB	TIM15
	0x4001 3C00 - 0x4001 3FFF	1 KB	Reserved
	0x4001 3800 - 0x4001 3BFF	1 KB	USART1
	0x4001 3400 - 0x4001 37FF	1 KB	Reserved
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1/I2S1
	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1
	0x4001 2800 - 0x4001 2BFF	1 KB	Reserved
	0x4001 2400 - 0x4001 27FF	1 KB	ADC
	0x4001 0800 - 0x4001 23FF	7 KB	Reserved
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI
	0x4001 0000 - 0x4001 03FF	1 KB	SYSCFG + COMP
	0x4000 8000 - 0x4000 FFFF	32 KB	Reserved

Table 20. STM32F071xx peripheral register boundary addresses (continued)

Bus	Boundary address	Size	Peripheral
APB	0x4000 7C00 - 0x4000 7FFF	1 KB	Reserved
	0x4000 7800 - 0x4000 7BFF	1 KB	CEC
	0x4000 7400 - 0x4000 77FF	1 KB	DAC
	0x4000 7000 - 0x4000 73FF	1 KB	PWR
	0x4000 6C00 - 0x4000 6FFF	1 KB	CRS
	0x4000 5C00 - 0x4000 6BFF	4 KB	Reserved
	0x4000 5800 - 0x4000 5BFF	1 KB	I2C2
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 5000 - 0x4000 53FF	1 KB	Reserved
	0x4000 4C00 - 0x4000 4FFF	1 KB	USART4
	0x4000 4800 - 0x4000 4BFF	1 KB	USART3
	0x4000 4400 - 0x4000 47FF	1 KB	USART2
	0x4000 3C00 - 0x4000 43FF	2 KB	Reserved
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC
	0x4000 2400 - 0x4000 27FF	1 KB	Reserved
	0x4000 2000 - 0x4000 23FF	1 KB	TIM14
	0x4000 1800 - 0x4000 1FFF	2 KB	Reserved
	0x4000 1400 - 0x4000 17FF	1 KB	TIM7
	0x4000 1000 - 0x4000 13FF	1 KB	TIM6
	0x4000 0800 - 0x4000 0FFF	2 KB	Reserved
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3
	0x4000 0000 - 0x4000 03FF	1 KB	TIM2

## 6 Electrical characteristics

### 6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to  $V_{SS}$ .

#### 6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at  $T_A = 25\text{ }^\circ\text{C}$  and  $T_A = T_{Amax}$  (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean  $\pm 3\sigma$ ).

#### 6.1.2 Typical values

Unless otherwise specified, typical data are based on  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{DD} = V_{DDA} = 3.3\text{ V}$ . They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean  $\pm 2\sigma$ ).

#### 6.1.3 Typical curves

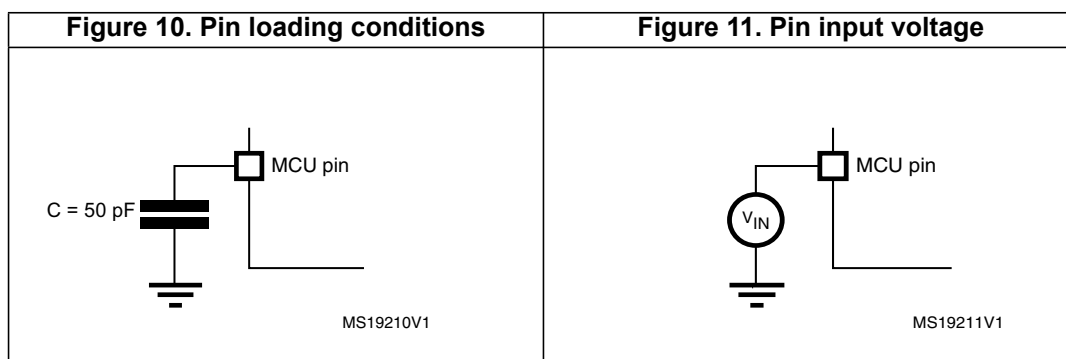
Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

#### 6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 10](#).

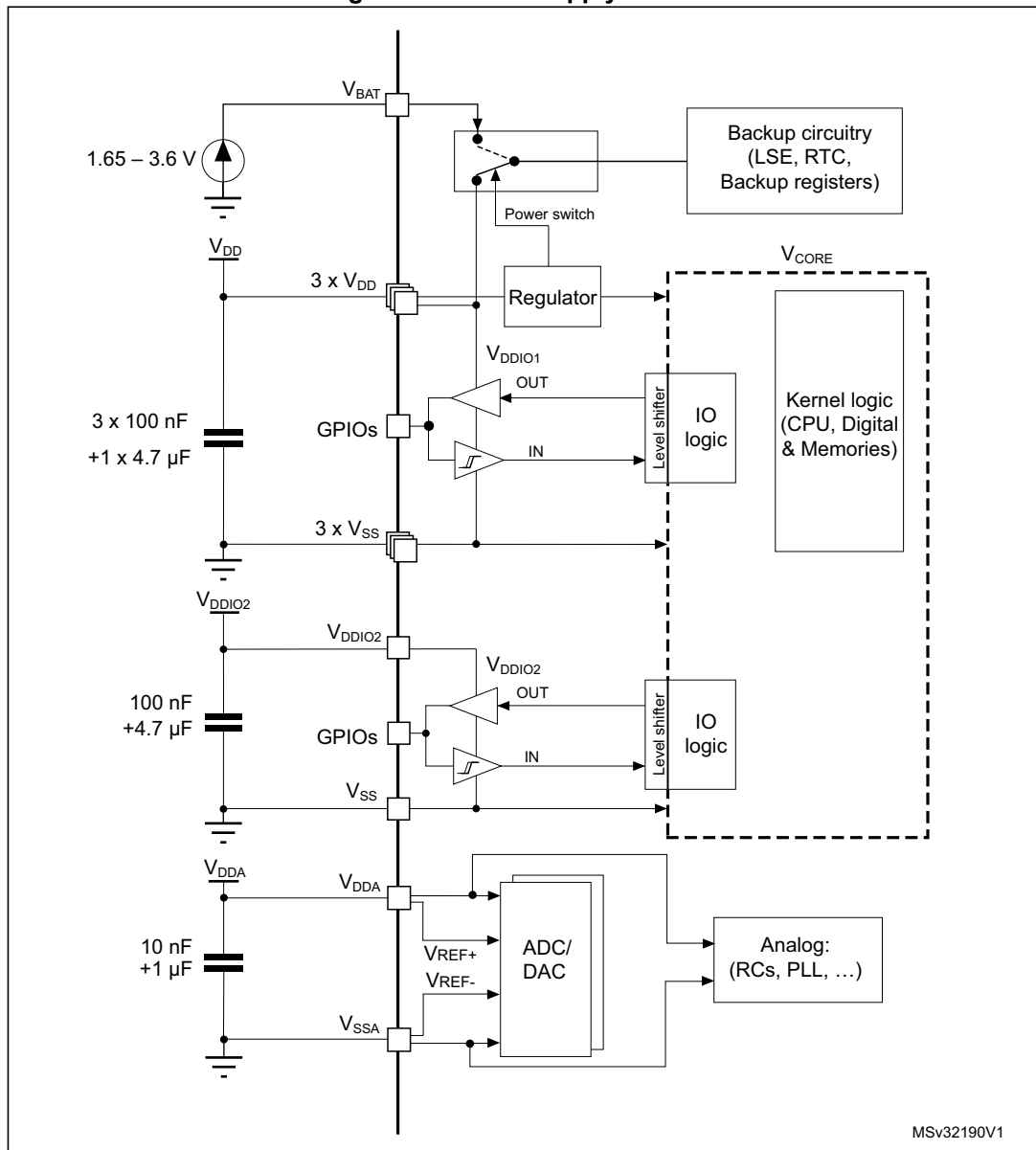
#### 6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in [Figure 11](#).



### 6.1.6 Power supply scheme

Figure 12. Power supply scheme

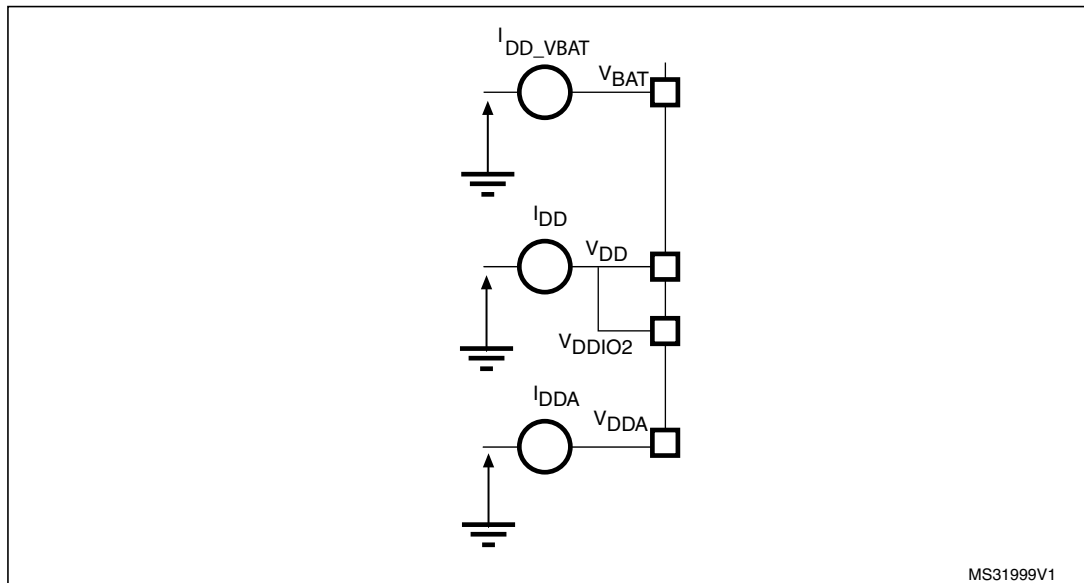


**Caution:** Each power supply pair ( $V_{DD}/V_{SS}$ ,  $V_{DDA}/V_{SSA}$  etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.



### 6.1.7 Current consumption measurement

Figure 13. Current consumption measurement scheme



## 6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 21: Voltage characteristics](#), [Table 22: Current characteristics](#) and [Table 23: Thermal characteristics](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 21. Voltage characteristics<sup>(1)</sup>

Symbol	Ratings	Min	Max	Unit
$V_{DDx}-V_{SS}$	External main supply voltage (including $V_{DDA}$ , $V_{DD}$ , $V_{DDIO2}$ and $V_{BAT}$ )	-0.3	4.0	V
$V_{DD}-V_{DDA}$	Allowed voltage difference for $V_{DD} > V_{DDA}$	-	0.4	V
$V_{IN}^{(2)}$	Input voltage on FT and FTf pins	$V_{SS} - 0.3$	$V_{DDIOx} + 4.0$	V
	Input voltage on TTa pins	$V_{SS} - 0.3$	4.0	V
	Input voltage on any other pin	$V_{SS} - 0.3$	4.0	V
$ \Delta V_{DDx} $	Variations between different $V_{DD}$ power pins	-	50	mV
$ V_{SSx} - V_{SS} $	Variations between all the different ground pins	-	50	mV
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see <a href="#">Section 6.3.12: Electrical sensitivity characteristics</a>		

1. All main power ( $V_{DD}$ ,  $V_{DDA}$ ) and ground ( $V_{SS}$ ,  $V_{SSA}$ ) pins must always be connected to the external power supply, in the permitted range.
2.  $V_{IN}$  maximum must always be respected. Refer to [Table 22: Current characteristics](#) for the maximum allowed injected current values.

**Table 22. Current characteristics**

Symbol	Ratings	Max.	Unit
$\Sigma I_{VDD}$	Total current into sum of all VDD power lines (source) <sup>(1)</sup>	120	mA
$\Sigma I_{VSS}$	Total current out of sum of all VSS ground lines (sink) <sup>(1)</sup>	-120	
$I_{VDD(PIN)}$	Maximum current into each VDD power pin (source) <sup>(1)</sup>	100	
$I_{VSS(PIN)}$	Maximum current out of each VSS ground pin (sink) <sup>(1)</sup>	-100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	25	
	Output current source by any I/O and control pin	-25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all IOs and control pins <sup>(2)</sup>	80	
	Total output current sourced by sum of all IOs and control pins <sup>(2)</sup>	-80	
	Total output current sourced by sum of all IOs supplied by VDDIO2	-40	
$I_{INJ(PIN)}^{(3)}$	Injected current on FT, FTf and B pins	-5/+0 <sup>(4)</sup>	
	Injected current on TC and RST pin	± 5	
	Injected current on TTa pins <sup>(5)</sup>	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins) <sup>(6)</sup>	± 25	

1. All main power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
3. A positive injection is induced by  $V_{IN} > V_{DDIOx}$  while a negative injection is induced by  $V_{IN} < V_{SS}$ .  $I_{INJ(PIN)}$  must never be exceeded. Refer to [Table 21: Voltage characteristics](#) for the maximum allowed input voltage values.
4. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
5. On these I/Os, a positive injection is induced by  $V_{IN} > V_{DDA}$ . Negative injection disturbs the analog performance of the device. See note <sup>(2)</sup> below [Table 60: ADC accuracy](#).
6. When several inputs are submitted to a current injection, the maximum  $\Sigma I_{INJ(PIN)}$  is the absolute sum of the positive and negative injected currents (instantaneous values).

**Table 23. Thermal characteristics**

Symbol	Ratings	Value	Unit
$T_{STG}$	Storage temperature range	-65 to +150	°C
$T_J$	Maximum junction temperature	150	°C

## 6.3 Operating conditions

### 6.3.1 General operating conditions

Table 24. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$f_{HCLK}$	Internal AHB clock frequency		0	48	MHz
$f_{PCLK}$	Internal APB clock frequency		0	48	
$V_{DD}$	Standard operating voltage		2	3.6	V
$V_{DDIO2}$	I/O supply voltage	Must not be supplied if $V_{DD}$ is not present	1.65	3.6	V
$V_{DDA}$	Analog operating voltage (ADC and DAC not used)	Must have a potential equal to or higher than $V_{DD}$	2	3.6	V
	Analog operating voltage (ADC and DAC used)		2.4	3.6	
$V_{BAT}$	Backup operating voltage		1.65	3.6	V
$V_{IN}$	I/O input voltage	TC and RST I/O	-0.3	$V_{DDIOx}+0.3$	V
		TTa I/O	-0.3	$V_{DDA}+0.3$	
		FT and FTf I/O	-0.3	5.5 <sup>(1)</sup>	
		BOOT0	0	9.0	
$P_D$	Power dissipation at $T_A = 85\text{ °C}$ for suffix 6 or $T_A = 105\text{ °C}$ for suffix 7 <sup>(2)</sup>	UFBGA100	-	364	mW
		LQFP100	-	476	
		LQFP64	-	455	
		LQFP48	-	370	
		UFQFPN48	-	625	
		WLCSP49	-	408	
$T_A$	Ambient temperature for the suffix 6 version	Maximum power dissipation	-40	85	°C
		Low power dissipation <sup>(3)</sup>	-40	105	
	Ambient temperature for the suffix 7 version	Maximum power dissipation	-40	105	°C
		Low power dissipation <sup>(3)</sup>	-40	125	
$T_J$	Junction temperature range	Suffix 6 version	-40	105	°C
		Suffix 7 version	-40	125	

1. To sustain a voltage higher than  $V_{DDIOx}+0.3\text{ V}$ , the internal pull-up/pull-down resistors must be disabled.
2. If  $T_A$  is lower, higher  $P_D$  values are allowed as long as  $T_J$  does not exceed  $T_{Jmax}$  (see [Section 7.2: Thermal characteristics](#)).
3. In low power dissipation state,  $T_A$  can be extended to this range as long as  $T_J$  does not exceed  $T_{Jmax}$  (see [Section 7.2: Thermal characteristics](#)).

### 6.3.2 Operating conditions at power-up / power-down

The parameters given in [Table 25](#) are derived from tests performed under the ambient temperature condition summarized in [Table 24](#).

**Table 25. Operating conditions at power-up / power-down**

Symbol	Parameter	Conditions	Min	Max	Unit
t <sub>VDD</sub>	V <sub>DD</sub> rise time rate		0	∞	μs/V
	V <sub>DD</sub> fall time rate		20	∞	
t <sub>VDDA</sub>	V <sub>VDDA</sub> rise time rate		0	∞	
	V <sub>VDDA</sub> fall time rate		20	∞	

### 6.3.3 Embedded reset and power control block characteristics

The parameters given in [Table 26](#) are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 24: General operating conditions](#).

**Table 26. Embedded reset and power control block characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>POR/PDR</sub> <sup>(1)</sup>	Power on/power down reset threshold	Falling edge <sup>(2)</sup>	1.80	1.88	1.96 <sup>(3)</sup>	V
		Rising edge	1.84 <sup>(3)</sup>	1.92	2.00	V
V <sub>PDRhyst</sub>	PDR hysteresis		-	40	-	mV
t <sub>RSTTEMPO</sub> <sup>(4)</sup>	Reset temporization		1.50	2.50	4.50	ms

1. The PDR detector monitors V<sub>DD</sub> and also V<sub>VDDA</sub> (if kept enabled in the option bytes). The POR detector monitors only V<sub>DD</sub>.
2. The product behavior is guaranteed by design down to the minimum V<sub>POR/PDR</sub> value.
3. Data based on characterization results, not tested in production.
4. Guaranteed by design, not tested in production.

**Table 27. Programmable voltage detector characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>PVD0</sub>	PVD threshold 0	Rising edge	2.1	2.18	2.26	V
		Falling edge	2	2.08	2.16	V
V <sub>PVD1</sub>	PVD threshold 1	Rising edge	2.19	2.28	2.37	V
		Falling edge	2.09	2.18	2.27	V
V <sub>PVD2</sub>	PVD threshold 2	Rising edge	2.28	2.38	2.48	V
		Falling edge	2.18	2.28	2.38	V
V <sub>PVD3</sub>	PVD threshold 3	Rising edge	2.38	2.48	2.58	V
		Falling edge	2.28	2.38	2.48	V

Table 27. Programmable voltage detector characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>PVD4</sub>	PVD threshold 4	Rising edge	2.47	2.58	2.69	V
		Falling edge	2.37	2.48	2.59	V
V <sub>PVD5</sub>	PVD threshold 5	Rising edge	2.57	2.68	2.79	V
		Falling edge	2.47	2.58	2.69	V
V <sub>PVD6</sub>	PVD threshold 6	Rising edge	2.66	2.78	2.9	V
		Falling edge	2.56	2.68	2.8	V
V <sub>PVD7</sub>	PVD threshold 7	Rising edge	2.76	2.88	3	V
		Falling edge	2.66	2.78	2.9	V
V <sub>PVDhyst</sub> <sup>(1)</sup>	PVD hysteresis		-	100	-	mV
I <sub>DD(PVD)</sub>	PVD current consumption		-	0.15	0.26 <sup>(1)</sup>	μA

1. Guaranteed by design, not tested in production.

### 6.3.4 Embedded reference voltage

The parameters given in [Table 28](#) are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 24: General operating conditions](#).

Table 28. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>REFINT</sub>	Internal reference voltage	-40 °C < T <sub>A</sub> < +105 °C	1.16	1.2	1.25	V
		-40 °C < T <sub>A</sub> < +85 °C	1.16	1.2	1.24 <sup>(1)</sup>	V
t <sub>S_vrefint</sub>	ADC sampling time when reading the internal reference voltage		4 <sup>(2)</sup>	-	-	μs
ΔV <sub>REFINT</sub>	Internal reference voltage spread over the temperature range	V <sub>DDA</sub> = 3 V	-	-	10 <sup>(2)</sup>	mV
T <sub>Coeff</sub>	Temperature coefficient		-	-	100 <sup>(2)</sup>	ppm/°C

1. Data based on characterization results, not tested in production.

2. Guaranteed by design, not tested in production.

### 6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 13: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

#### Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the  $f_{HCLK}$  frequency:
  - 0 wait state and Prefetch OFF from 0 to 24 MHz
  - 1 wait state and Prefetch ON above 24 MHz
- When the peripherals are enabled  $f_{PCLK} = f_{HCLK}$

The parameters given in *Table 29* to *Table 34* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 24: General operating conditions*.

**Table 29. Typical and maximum current consumption from  $V_{DD}$  supply at  $V_{DD} = 3.6 V$**

Symbol	Parameter	Conditions	$f_{HCLK}$	All peripherals enabled			All peripherals disabled			Unit		
				Typ	Max @ $T_A^{(1)}$		Typ	Max @ $T_A^{(1)}$				
					25 °C	85 °C		105 °C	25 °C		85 °C	105 °C
$I_{DD}$	Supply current in Run mode, code executing from Flash	HSI48	48 MHz	24.3	26.9	27.2	27.9	13.1	14.8	14.9	15.5	mA
		HSE bypass, PLL on	48 MHz	24.1	26.8	27.0	27.7	13.0	14.6	14.8	15.4	
			32 MHz	16.0	18.3	18.6	19.2	8.76	9.56	9.73	10.6	
			24 MHz	12.3	13.7	14.3	14.7	7.36	7.94	8.37	8.81	
		HSE bypass, PLL off	8 MHz	4.52	5.25	5.28	5.61	2.89	3.17	3.26	3.34	
			1 MHz	1.25	1.39	1.58	1.87	0.93	1.06	1.15	1.34	
		HSI clock, PLL on	48 MHz	24.1	27.1	27.6	27.8	12.9	14.7	14.9	15.5	
			32 MHz	16.1	18.2	18.9	19.3	8.82	9.69	9.83	10.7	
			24 MHz	12.4	14.0	14.4	14.8	7.31	7.92	8.34	8.75	
		HSI clock, PLL off	8 MHz	4.52	5.25	5.35	5.61	2.87	3.16	3.25	3.33	

Table 29. Typical and maximum current consumption from V<sub>DD</sub> supply at V<sub>DD</sub> = 3.6 V (continued)

Symbol	Parameter	Conditions	f <sub>HCLK</sub>	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T <sub>A</sub> <sup>(1)</sup>			Typ	Max @ T <sub>A</sub> <sup>(1)</sup>			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I <sub>DD</sub>	Supply current in Run mode, code executing from RAM	HSI48	48 MHz	23.1	25.4	25.8	26.6	12.8	13.5	13.7	13.9	mA
		HSE bypass, PLL on	48 MHz	23.0	25.3 <sup>(2)</sup>	25.7	26.5 <sup>(2)</sup>	12.6	13.3 <sup>(2)</sup>	13.5	13.8 <sup>(2)</sup>	
			32 MHz	15.4	17.3	17.8	18.3	7.96	8.92	9.17	9.73	
			24 MHz	11.4	12.9	13.5	13.7	6.48	8.04	8.23	8.41	
		HSE bypass, PLL off	8 MHz	4.21	4.6	4.89	5.25	2.07	2.3	2.35	2.94	
			1 MHz	0.78	0.9	0.92	1.15	0.36	0.48	0.59	0.82	
		HSI clock, PLL on	48 MHz	23.1	24.5	25.0	25.2	12.6	13.7	13.9	14.0	
			32 MHz	15.4	17.4	17.7	18.2	8.05	8.85	9.16	9.94	
			24 MHz	11.5	13.0	13.6	13.9	6.49	8.06	8.21	8.47	
		HSI clock, PLL off	8 MHz	4.34	4.75	5.03	5.41	2.11	2.36	2.38	2.98	
	Supply current in Sleep mode, code executing from Flash or RAM	HSI48	48 MHz	15.1	16.6	16.8	17.5	3.08	3.43	3.56	3.61	
		HSE bypass, PLL on	48 MHz	15.0	16.5 <sup>(2)</sup>	16.7	17.3 <sup>(2)</sup>	2.93	3.28 <sup>(2)</sup>	3.41	3.46 <sup>(2)</sup>	
			32 MHz	9.9	11.4	11.6	11.9	2.0	2.24	2.32	2.49	
			24 MHz	7.43	8.17	8.71	8.82	1.63	1.82	1.88	1.9	
		HSE bypass, PLL off	8 MHz	2.83	3.09	3.26	3.66	0.76	0.88	0.91	0.93	
			1 MHz	0.42	0.54	0.55	0.67	0.28	0.39	0.41	0.43	
		HSI clock, PLL on	48 MHz	15.0	17.2	17.3	17.9	3.04	3.37	3.41	3.46	
			32 MHz	9.93	11.3	11.6	11.7	2.11	2.35	2.44	2.65	
			24 MHz	7.53	8.45	8.87	8.95	1.64	1.83	1.9	1.93	
		HSI clock, PLL off	8 MHz	2.95	3.24	3.41	3.8	0.8	0.92	0.94	0.97	

1. Data based on characterization results, not tested in production unless otherwise specified.
2. Data based on characterization results and tested in production (using one common test limit for sum of I<sub>DD</sub> and I<sub>DDA</sub>).

**Table 30. Typical and maximum current consumption from the V<sub>DDA</sub> supply**

Symbol	Parameter	Conditions (1)	f <sub>HCLK</sub>	V <sub>DDA</sub> = 2.4 V				V <sub>DDA</sub> = 3.6 V				Unit
				Typ	Max @ T <sub>A</sub> (2)			Typ	Max @ T <sub>A</sub> (2)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I <sub>DDA</sub>	Supply current in Run or Sleep mode, code executing from Flash or RAM	HSI48	48 MHz	311	326	334	343	322	337	345	354	μA
		HSE bypass, PLL on	48 MHz	152	170 <sup>(3)</sup>	178	182 <sup>(3)</sup>	165	184 <sup>(3)</sup>	196	200 <sup>(3)</sup>	
			32 MHz	105	121	126	128	113	129	136	138	
			24 MHz	81.9	95.9	99.5	101	88.7	102	107	108	
		HSE bypass, PLL off	8 MHz	2.7	3.8	4.3	4.6	3.6	4.7	5.2	5.5	
			1 MHz	2.7	3.8	4.3	4.6	3.6	4.7	5.2	5.5	
		HSI clock, PLL on	48 MHz	223	244	255	260	245	265	279	284	
			32 MHz	176	195	203	206	193	212	221	224	
			24 MHz	154	171	178	181	168	185	192	195	
		HSI clock, PLL off	8 MHz	74.2	83.4	86.4	87.3	83.4	92.5	95.3	96.6	

1. Current consumption from the V<sub>DDA</sub> supply is independent of whether the digital peripherals are enabled or disabled, being in Run or Sleep mode or executing from Flash or RAM. Furthermore, when the PLL is off, I<sub>DDA</sub> is independent from the frequency.
2. Data based on characterization results, not tested in production unless otherwise specified.
3. Data based on characterization results and tested in production (using one common test limit for sum of I<sub>DD</sub> and I<sub>DDA</sub>).



Table 31. Typical and maximum consumption in Stop and Standby modes

Sym- bol	Para- meter	Conditions	Typ @V <sub>DD</sub> (V <sub>DD</sub> = V <sub>DDA</sub> )						Max <sup>(1)</sup>			Unit	
			2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T <sub>A</sub> = 25 °C	T <sub>A</sub> = 85 °C	T <sub>A</sub> = 105 °C		
I <sub>DD</sub>	Supply current in Stop mode	Regulator in run mode, all oscillators OFF	15.4	15.5	15.6	15.7	15.8	15.9	23 <sup>(2)</sup>	49	68 <sup>(2)</sup>	μA	
		Regulator in low-power mode, all oscillators OFF	3.2	3.3	3.4	3.5	3.6	3.7	8 <sup>(2)</sup>	33	51 <sup>(2)</sup>		
	Supply current in Standby mode	LSI ON and IWDG ON	0.8	1.0	1.1	1.2	1.3	1.4	-	-	-		
		LSI OFF and IWDG OFF	0.6	0.7	0.9	0.9	1.0	1.1	2.1 <sup>(2)</sup>	2.6	3.1 <sup>(2)</sup>		
I <sub>DDA</sub>	Supply current in Stop mode	V <sub>DDA</sub> monitoring ON	Regulator in run mode, all oscillators OFF	2.1	2.2	2.3	2.5	2.6	2.8	3.5 <sup>(2)</sup>	3.6		4.6 <sup>(2)</sup>
			Regulator in low-power mode, all oscillators OFF	2.1	2.2	2.3	2.5	2.6	2.8	3.5 <sup>(2)</sup>	3.6		4.6 <sup>(2)</sup>
		Supply current in Standby mode	LSI ON and IWDG ON	2.5	2.7	2.8	3.0	3.2	3.5	-	-		-
			LSI OFF and IWDG OFF	1.9	2.1	2.2	2.3	2.5	2.6	3.5 <sup>(2)</sup>	3.6		4.6 <sup>(2)</sup>
	Supply current in Stop mode	V <sub>DDA</sub> monitoring OFF	Regulator in run mode, all oscillators OFF	1.3	1.3	1.4	1.4	1.5	1.5	-	-	-	
			Regulator in low-power mode, all oscillators OFF	1.3	1.3	1.4	1.4	1.5	1.5	-	-	-	
			LSI ON and IWDG ON	1.7	1.8	1.9	2.0	2.1	2.2	-	-	-	
		Supply current in Standby mode	V <sub>DDA</sub> monitoring OFF	LSI OFF and IWDG OFF	1.2	1.2	1.2	1.3	1.3	1.4	-	-	-

1. Data based on characterization results, not tested in production unless otherwise specified.
2. Data based on characterization results and tested in production (using one common test limit for sum of I<sub>DD</sub> and I<sub>DDA</sub>).

**Table 32. Typical and maximum current consumption from the V<sub>BAT</sub> supply**

Symbol	Parameter	Conditions	Typ @ V <sub>BAT</sub>						Max <sup>(1)</sup>			Unit
			= 1.65 V	= 1.8 V	= 2.4 V	= 2.7 V	= 3.3 V	= 3.6 V	T <sub>A</sub> = 25 °C	T <sub>A</sub> = 85 °C	T <sub>A</sub> = 105 °C	
I <sub>DD-VBAT</sub>	RTC domain supply current	LSE & RTC ON; “Xtal mode”: lower driving capability; LSEDRV[1:0] = '00'	0.5	0.6	0.7	0.8	1.1	1.2	TBD	TBD	TBD	µA
		LSE & RTC ON; “Xtal mode” higher driving capability; LSEDRV[1:0] = '11'	0.8	0.9	1.1	1.2	1.4	1.6	TBD	TBD	TBD	

1. Data based on characterization results, not tested in production.

**Typical current consumption**

The MCU is placed under the following conditions:

- V<sub>DD</sub>=V<sub>DDA</sub>=3.3 V
- All I/O pins are in analog input configuration
- The Flash access time is adjusted to f<sub>HCLK</sub> frequency:
  - 0 wait state and Prefetch OFF from 0 to 24 MHz
  - 1 wait state and Prefetch ON above 24 MHz
- When the peripherals are enabled, f<sub>PCLK</sub> = f<sub>HCLK</sub>
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8 and 16 is used for the frequencies 4 MHz, 2 MHz, 1 MHz and 500 kHz respectively



**Table 33. Typical current consumption in Run mode, code with data processing running from Flash**

Symbol	Parameter	Conditions	f <sub>HCLK</sub>	Typ		Unit
				Peripherals enabled	Peripherals disabled	
I <sub>DD</sub>	Supply current in Run mode from V <sub>DD</sub> supply	Running from HSE crystal clock 8 MHz, code executing from Flash	48 MHz	23.5	13.5	mA
			36 MHz	18.3	10.5	
			32 MHz	16.0	9.6	
			24 MHz	12.3	7.6	
			16 MHz	8.6	5.3	
			8 MHz	4.8	3.1	
			4 MHz	3.1	2.1	
			2 MHz	2.1	1.6	
			1 MHz	1.6	1.3	
			500 KHz	1.3	1.2	
I <sub>DDA</sub>	Supply current in Run mode from V <sub>DDA</sub> supply	Running from HSE crystal clock 8 MHz, code executing from Flash	48 MHz	163.3	163.3	μA
			36 MHz	124.3	124.3	
			32 MHz	111.9	111.9	
			24 MHz	87.1	87.1	
			16 MHz	62.5	62.5	
			8 MHz	2.5	2.5	
			4 MHz	2.5	2.5	
			2 MHz	2.5	2.5	
			1 MHz	2.5	2.5	
500 KHz	2.5	2.5				

**Table 34. Typical current consumption in Sleep mode, code running from Flash**

Symbol	Parameter	Conditions	f <sub>HCLK</sub>	Typ		Unit
				Peripherals enabled	Peripherals disabled	
I <sub>DD</sub>	Supply current in Sleep mode from V <sub>DD</sub> supply	Running from HSE crystal clock 8 MHz, code executing from Flash	48 MHz	14.6	3.5	mA
			36 MHz	11.1	2.9	
			32 MHz	10.0	2.7	
			24 MHz	7.8	2.2	
			16 MHz	5.5	1.7	
			8 MHz	3.1	1.2	
			4 MHz	2.2	1.1	
			2 MHz	1.6	1.0	
			1 MHz	1.4	1.0	
			500 KHz	1.2	1.0	
I <sub>DDA</sub>	Supply current in Sleep mode from V <sub>DDA</sub> supply	Running from HSE crystal clock 8 MHz, code executing from Flash	48 MHz	163.3	163.3	μA
			36 MHz	124.3	124.3	
			32 MHz	111.9	111.9	
			24 MHz	87.1	87.1	
			16 MHz	62.5	62.5	
			8 MHz	2.5	2.5	
			4 MHz	2.5	2.5	
			2 MHz	2.5	2.5	
			1 MHz	2.5	2.5	
500 KHz	2.5	2.5				

### I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

#### I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in [Table 54: I/O static characteristics](#).

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

**Caution:** Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

#### I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see [Table 36: Peripheral current consumption](#)), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDIOx} \times f_{SW} \times C$$

where

$I_{SW}$  is the current sunk by a switching I/O to charge/discharge the capacitive load

$V_{DDIOx}$  is the I/O supply voltage

$f_{SW}$  is the I/O switching frequency

$C$  is the total capacitance seen by the I/O pin:  $C = C_{INT} + C_{EXT} + C_S$

$C_S$  is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 35. Switching output I/O current consumption

Symbol	Parameter	Conditions <sup>(1)</sup>	I/O toggling frequency (f <sub>SW</sub> )	Typ	Unit
I <sub>sw</sub>	I/O current consumption	V <sub>DDIOx</sub> = 3.3 V C = C <sub>INT</sub>	4 MHz	0.07	mA
			8 MHz	0.15	
			16 MHz	0.31	
			24 MHz	0.53	
			48 MHz	0.92	
		V <sub>DDIOx</sub> = 3.3 V C <sub>EXT</sub> = 0 pF C = C <sub>INT</sub> + C <sub>EXT</sub> + C <sub>S</sub>	4 MHz	0.18	
			8 MHz	0.37	
			16 MHz	0.76	
			24 MHz	1.39	
			48 MHz	2.188	
		V <sub>DDIOx</sub> = 3.3 V C <sub>EXT</sub> = 10 pF C = C <sub>INT</sub> + C <sub>EXT</sub> + C <sub>S</sub>	4 MHz	0.32	
			8 MHz	0.64	
			16 MHz	1.25	
			24 MHz	2.23	
			48 MHz	4.442	
		V <sub>DDIOx</sub> = 3.3 V C <sub>EXT</sub> = 22 pF C = C <sub>INT</sub> + C <sub>EXT</sub> + C <sub>S</sub>	4 MHz	0.49	
			8 MHz	0.94	
			16 MHz	2.38	
			24 MHz	3.99	
			V <sub>DDIOx</sub> = 3.3 V C <sub>EXT</sub> = 33 pF C = C <sub>INT</sub> + C <sub>EXT</sub> + C <sub>S</sub>	4 MHz	
		8 MHz		1.25	
		16 MHz		3.24	
		24 MHz		5.02	
		V <sub>DDIOx</sub> = 3.3 V C <sub>EXT</sub> = 47 pF C = C <sub>INT</sub> + C <sub>EXT</sub> + C <sub>S</sub> C = C <sub>int</sub>		4 MHz	
			8 MHz	1.7	
			16 MHz	3.67	
		V <sub>DDIOx</sub> = 2.4 V C <sub>EXT</sub> = 47 pF C = C <sub>INT</sub> + C <sub>EXT</sub> + C <sub>S</sub> C = C <sub>int</sub>	4 MHz	0.66	
			8 MHz	1.43	
16 MHz	2.45				
24 MHz	4.97				

1. C<sub>S</sub> = 7 pF (estimated value).

**On-chip peripheral current consumption**

The current consumption of the on-chip peripherals is given in [Table 36](#). The MCU is placed under the following conditions:

- All I/O pins are in Analog mode
- All peripherals are disabled unless otherwise mentioned
- The given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- Ambient operating temperature and supply voltage conditions summarized in [Table 21: Voltage characteristics](#)
- The power consumption of the digital part of the on-chip peripherals is given in [Table 35](#). The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

**Table 36. Peripheral current consumption**

Peripheral		Typical consumption at 25 °C	Unit
AHB	BusMatrix <sup>(1)</sup>	2.2	µA/MHz
	CRC	1.6	
	DMA	5.7	
	Flash interface	13.0	
	GPIOA	8.2	
	GPIOB	8.5	
	GPIOC	2.3	
	GIOD	1.9	
	GPIOE	2.2	
	GPIOF	1.2	
	SRAM	0.9	
	TSC	5.0	
	ALL AHB Peripherals	52.6	

**Table 36. Peripheral current consumption (continued)**

Peripheral		Typical consumption at 25 °C	Unit
APB	APB-Bridge <sup>(2)</sup>	2.8	µA/MHz
	ADC <sup>(3)</sup>	4.1	
	CEC	1.5	
	CRS	0.8	
	DAC <sup>(3)</sup>	4.7	
	DEBUG (MCU debug feature)	0.1	
	I2C1	3.9	
	I2C2	4.0	
	PWR	1.3	
	SPI1	8.7	
	SPI2	8.5	
	SYSCFG & COMP	1.7	
	TIM1	14.9	
	TIM2	15.5	
	TIM3	11.4	
	TIM6	2.5	
	TIM7	2.3	
	TIM14	5.3	
	TIM15	9.1	
	TIM16	6.6	
	TIM17	6.8	
	USART1	17.0	
	USART2	16.7	
USART3	5.4		
USART4	5.4		
WWDG	1.4		
ALL APB Peripherals	182		

1. The BusMatrix is automatically active when at least one master is ON (CPU, DMA).
2. The APB Bridge is automatically active when at least one peripheral is ON on the Bus.
3. The power consumption of the analog part (I<sub>DDA</sub>) of peripherals such as ADC, DAC, Comparators, is not included. Refer to the tables of characteristics in the subsequent sections.

### 6.3.6 Wakeup time from low-power mode

The wakeup times given in [Table 37](#) are the latency between the event and the execution of the first user instruction. The device goes in low-power mode after the WFE (Wait For Event) instruction, in the case of a WFI (Wait For Interruption) instruction, 16 CPU cycles



must be added to the following timings due to the interrupt latency in the Cortex M0 architecture.

The SYSCLK clock source setting is kept unchanged after wakeup from Sleep mode. After wakeup from Stop or Standby mode, SYSCLK takes the default setting: HSI 8 MHz.

The wakeup source from Sleep and Stop mode is an EXTI Line configured in event mode. The wakeup source from Standby mode is the WKUP1 pin (PA0).

All timings are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 24: General operating conditions* except when explicitly mentioned

**Table 37. Low-power mode wakeup timings**

Symbol	Parameter	Conditions	Typ @VDD = VDDA					Max	Unit
			= 2.0 V	= 2.4 V	= 2.7 V	= 3 V	= 3.3 V		
t <sub>WUSTOP</sub>	Wakeup from Stop mode	Regulator in run mode	3.2	3.1	2.9	2.9	2.8	5	μs
		Regulator in low power mode	7.0	5.8	5.2	4.9	4.6	9	
t <sub>WUSTANDBY</sub>	Wakeup from Standby mode		60.4	55.6	53.5	52	51	-	
t <sub>WUSLEEP</sub>	Wakeup from Sleep mode		4 SYSCLK cycles					-	

### 6.3.7 External clock source characteristics

#### High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

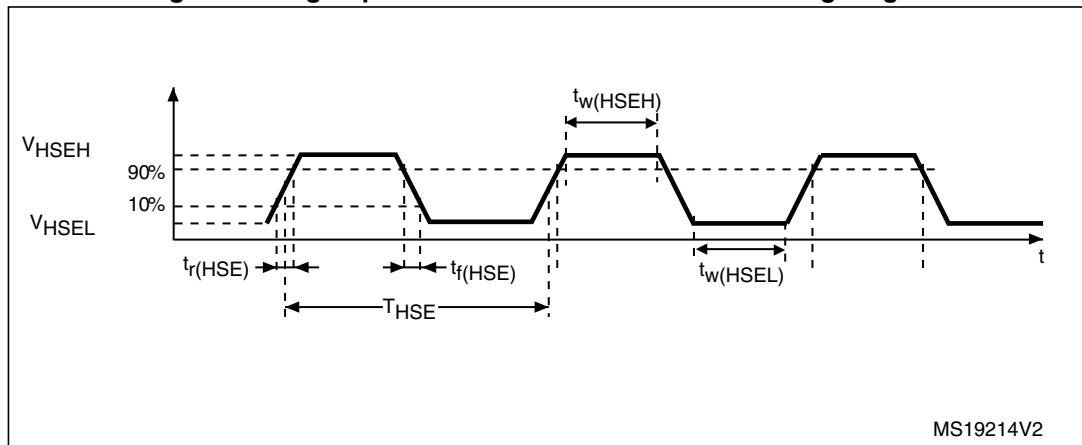
The external clock signal has to respect the I/O characteristics in [Section 6.3.14](#). However, the recommended clock input waveform is shown in [Figure 14: High-speed external clock source AC timing diagram](#).

**Table 38. High-speed external user clock characteristics**

Symbol	Parameter <sup>(1)</sup>	Conditions	Min	Typ	Max	Unit
$f_{HSE\_ext}$	User external clock source frequency		1	8	32	MHz
$V_{HSEH}$	OSC_IN input pin high level voltage		$0.7 V_{DDIOx}$	-	$V_{DDIOx}$	V
$V_{HSEL}$	OSC_IN input pin low level voltage		$V_{SS}$	-	$0.3 V_{DDIOx}$	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time		15	-	-	ns
$t_r(HSE)$ $t_f(HSE)$	OSC_IN rise or fall time		-	-	20	

1. Guaranteed by design, not tested in production.

**Figure 14. High-speed external clock source AC timing diagram**



MS19214V2

**Low-speed external user clock generated from an external source**

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

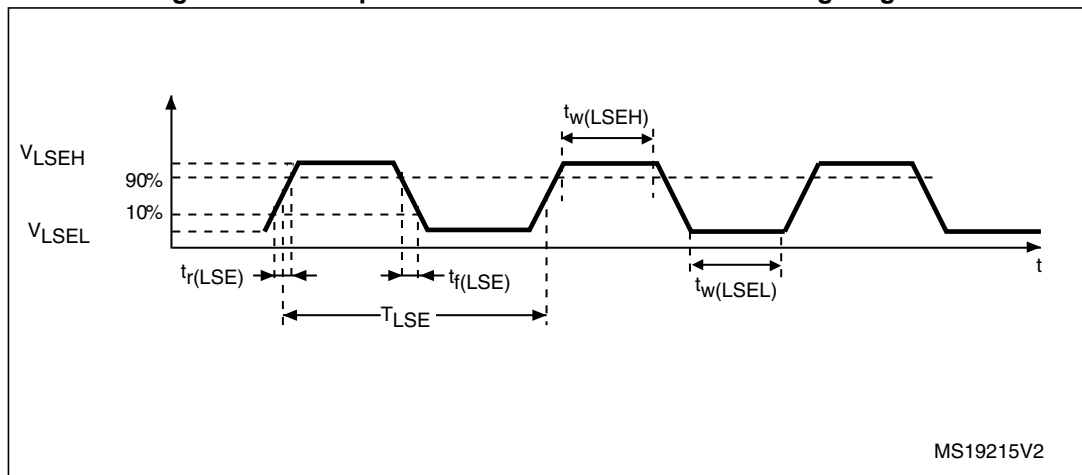
The external clock signal has to respect the I/O characteristics in [Section 6.3.14](#). However, the recommended clock input waveform is shown in [Figure 15](#).

**Table 39. Low-speed external user clock characteristics**

Symbol	Parameter <sup>(1)</sup>	Conditions	Min	Typ	Max	Unit
$f_{LSE\_ext}$	User external clock source frequency		-	32.768	1000	kHz
$V_{LSEH}$	OSC32_IN input pin high level voltage		$0.7 V_{DDIOx}$	-	$V_{DDIOx}$	V
$V_{LSEL}$	OSC32_IN input pin low level voltage		$V_{SS}$	-	$0.3 V_{DDIOx}$	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time		-	-	50	

1. Guaranteed by design, not tested in production.

**Figure 15. Low-speed external clock source AC timing diagram**



**High-speed external clock generated from a crystal/ceramic resonator**

The high-speed external (HSE) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in [Table 40](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 40. HSE oscillator characteristics**

Symbol	Parameter	Conditions <sup>(1)</sup>	Min <sup>(2)</sup>	Typ	Max <sup>(2)</sup>	Unit
f <sub>OSC_IN</sub>	Oscillator frequency		4	8	32	MHz
R <sub>F</sub>	Feedback resistor		-	200	-	kΩ
I <sub>DD</sub>	HSE current consumption	During startup <sup>(3)</sup>	-		8.5	mA
		V <sub>DD</sub> = 3.3 V, R <sub>m</sub> = 30 Ω, CL = 10 pF@8 MHz	-	0.4	-	
		V <sub>DD</sub> = 3.3 V, R <sub>m</sub> = 45 Ω, CL = 10 pF@8 MHz	-	0.5	-	
		V <sub>DD</sub> = 3.3 V, R <sub>m</sub> = 30 Ω, CL = 5 pF@32 MHz	-	0.8	-	
		V <sub>DD</sub> = 3.3 V, R <sub>m</sub> = 30 Ω, CL = 10 pF@32 MHz	-	1	-	
		V <sub>DD</sub> = 3.3 V, R <sub>m</sub> = 30 Ω, CL = 20 pF@32 MHz	-	1.5	-	
g <sub>m</sub>	Oscillator transconductance	Startup	10	-	-	mA/V
t <sub>SU(HSE)</sub> <sup>(4)</sup>	Startup time	V <sub>DD</sub> is stabilized	-	2	-	ms

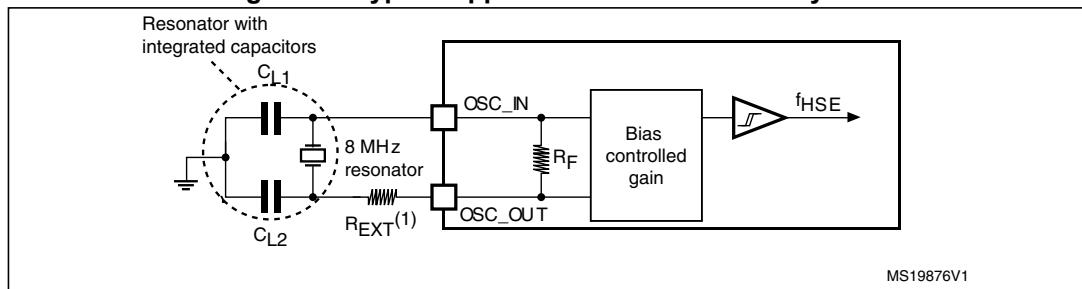
1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by design, not tested in production.
3. This consumption level occurs during the first 2/3 of the t<sub>SU(HSE)</sub> startup time
4. t<sub>SU(HSE)</sub> is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C<sub>L1</sub> and C<sub>L2</sub>, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see [Figure 16](#)). C<sub>L1</sub> and C<sub>L2</sub> are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C<sub>L1</sub> and C<sub>L2</sub>. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C<sub>L1</sub> and C<sub>L2</sub>.

*Note:* For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website [www.st.com](http://www.st.com).



Figure 16. Typical application with an 8 MHz crystal



1.  $R_{EXT}$  value depends on the crystal characteristics.

**Low-speed external clock generated from a crystal resonator**

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 41*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

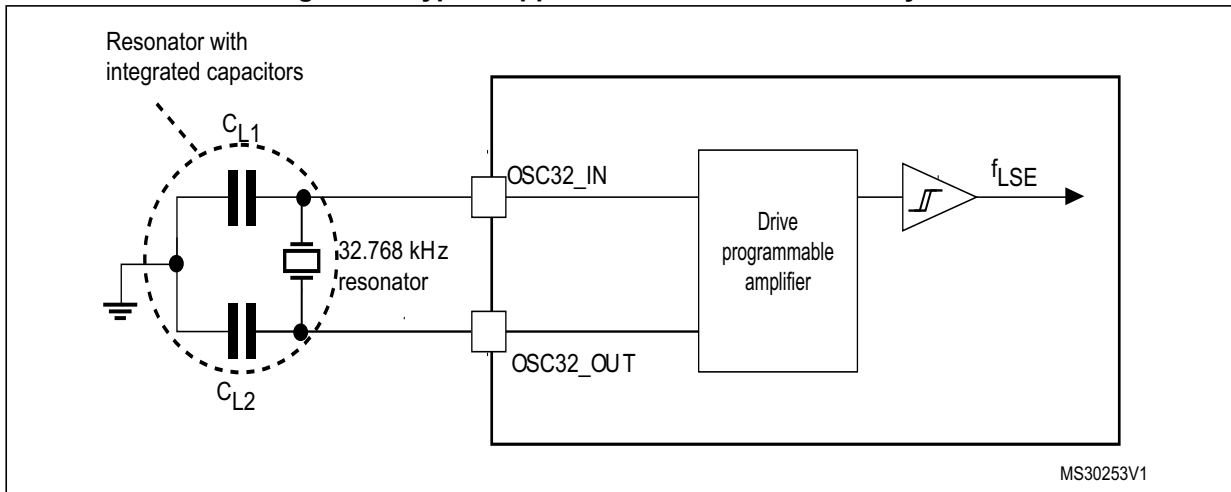
**Table 41. LSE oscillator characteristics (f<sub>LSE</sub> = 32.768 kHz)**

Symbol	Parameter	Conditions <sup>(1)</sup>	Min <sup>(2)</sup>	Typ	Max <sup>(2)</sup>	Unit
I <sub>DD</sub>	LSE current consumption	LSEDRV[1:0]=00 lower driving capability	-	0.5	0.9	μA
		LSEDRV[1:0]= 01 medium low driving capability	-	-	1	
		LSEDRV[1:0] = 10 medium high driving capability	-	-	1.3	
		LSEDRV[1:0]=11 higher driving capability	-	-	1.6	
g <sub>m</sub>	Oscillator transconductance	LSEDRV[1:0]=00 lower driving capability	5	-	-	μA/V
		LSEDRV[1:0]= 01 medium low driving capability	8	-	-	
		LSEDRV[1:0] = 10 medium high driving capability	15	-	-	
		LSEDRV[1:0]=11 higher driving capability	25	-	-	
t <sub>SU(LSE)</sub> <sup>(3)</sup>	Startup time	V <sub>DD</sub> is stabilized	-	2	-	s

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 "Oscillator design guide for ST microcontrollers".
2. Guaranteed by design, not tested in production.
3. t<sub>SU(LSE)</sub> is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

**Note:** For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website [www.st.com](http://www.st.com).

Figure 17. Typical application with a 32.768 kHz crystal



*Note:* An external resistor is not required between OSC32\_IN and OSC32\_OUT and it is forbidden to add one.

### 6.3.8 Internal clock source characteristics

The parameters given in *Table 42* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 24: General operating conditions*. The provided curves are characterization results, not tested in production.

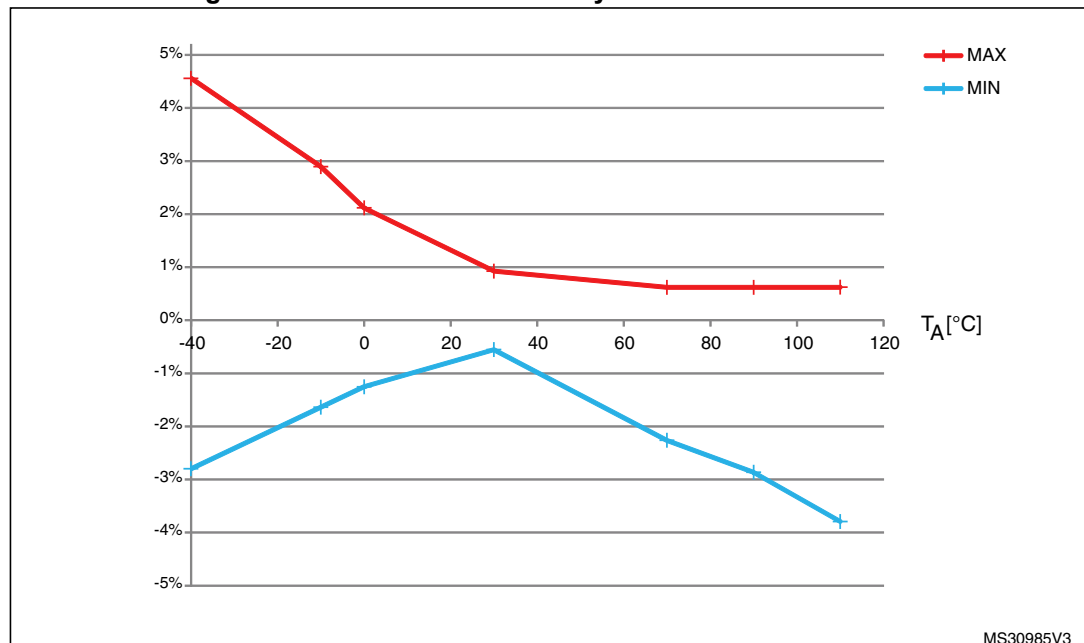
#### High-speed internal (HSI) RC oscillator

**Table 42. HSI oscillator characteristics<sup>(1)</sup>**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{\text{HSI}}$	Frequency		-	8	-	MHz
TRIM	HSI user trimming step		-	-	1 <sup>(2)</sup>	%
DuCy <sub>(HSI)</sub>	Duty cycle		45 <sup>(2)</sup>	-	55 <sup>(2)</sup>	%
ACC <sub>HSI</sub>	Accuracy of the HSI oscillator (factory calibrated)	T <sub>A</sub> = -40 to 105 °C	-3.8 <sup>(3)</sup>	-	4.6 <sup>(3)</sup>	%
		T <sub>A</sub> = -10 to 85 °C	-2.9 <sup>(3)</sup>	-	2.9 <sup>(3)</sup>	%
		T <sub>A</sub> = 0 to 70 °C	-1.3 <sup>(3)</sup>	-	2.2 <sup>(3)</sup>	%
		T <sub>A</sub> = 25 °C	-1	-	1	%
t <sub>su(HSI)</sub>	HSI oscillator startup time		1 <sup>(2)</sup>	-	2 <sup>(2)</sup>	µs
I <sub>DDA(HSI)</sub>	HSI oscillator power consumption		-	80	100 <sup>(2)</sup>	µA

1. V<sub>DDA</sub> = 3.3 V, T<sub>A</sub> = -40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.

**Figure 18. HSI oscillator accuracy characterization results**





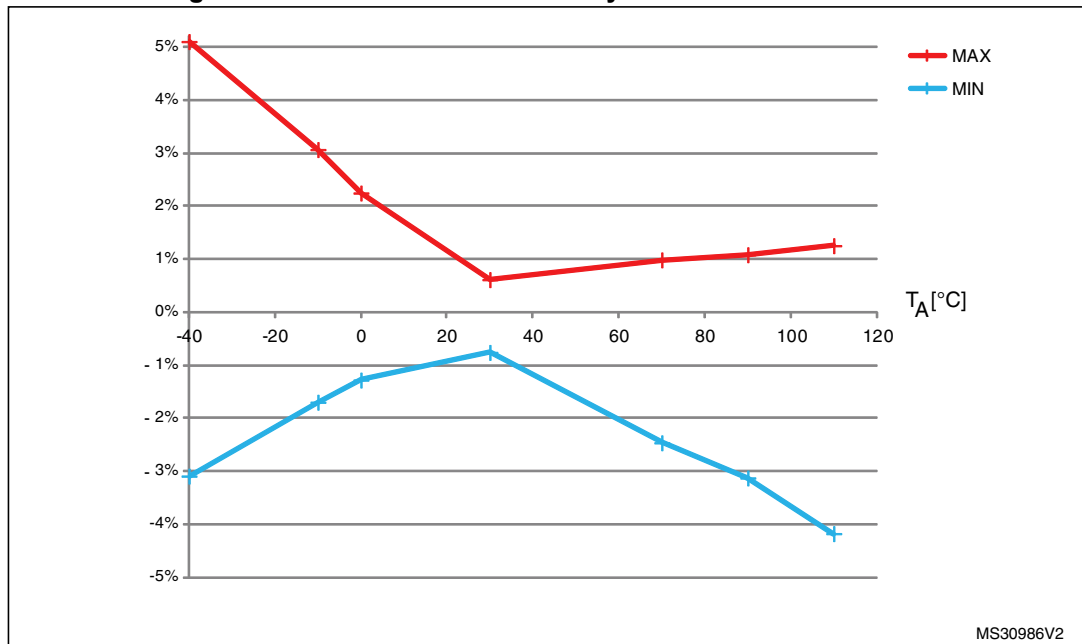
**High-speed internal 14 MHz (HSI14) RC oscillator (dedicated to ADC)**

**Table 43. HSI14 oscillator characteristics<sup>(1)</sup>**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{\text{HSI14}}$	Frequency		-	14	-	MHz
TRIM	HSI14 user-trimming step		-	-	1 <sup>(2)</sup>	%
$\text{DuCy}_{\text{(HSI14)}}$	Duty cycle		45 <sup>(2)</sup>	-	55 <sup>(2)</sup>	%
$\text{ACC}_{\text{HSI14}}$	Accuracy of the HSI14 oscillator (factory calibrated)	$T_A = -40 \text{ to } 105 \text{ }^\circ\text{C}$	-4.2 <sup>(3)</sup>	-	5.1 <sup>(3)</sup>	%
		$T_A = -10 \text{ to } 85 \text{ }^\circ\text{C}$	-3.2 <sup>(3)</sup>	-	3.1 <sup>(3)</sup>	%
		$T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}$	-1.3 <sup>(3)</sup>	-	2.2 <sup>(3)</sup>	%
		$T_A = 25 \text{ }^\circ\text{C}$	-1	-	1	%
$t_{\text{su(HSI14)}}$	HSI14 oscillator startup time		1 <sup>(2)</sup>	-	2 <sup>(2)</sup>	$\mu\text{s}$
$I_{\text{DDA(HSI14)}}$	HSI14 oscillator power consumption		-	100	150 <sup>(2)</sup>	$\mu\text{A}$

1.  $V_{\text{DDA}} = 3.3 \text{ V}$ ,  $T_A = -40 \text{ to } 105 \text{ }^\circ\text{C}$  unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.

**Figure 19. HSI14 oscillator accuracy characterization results**



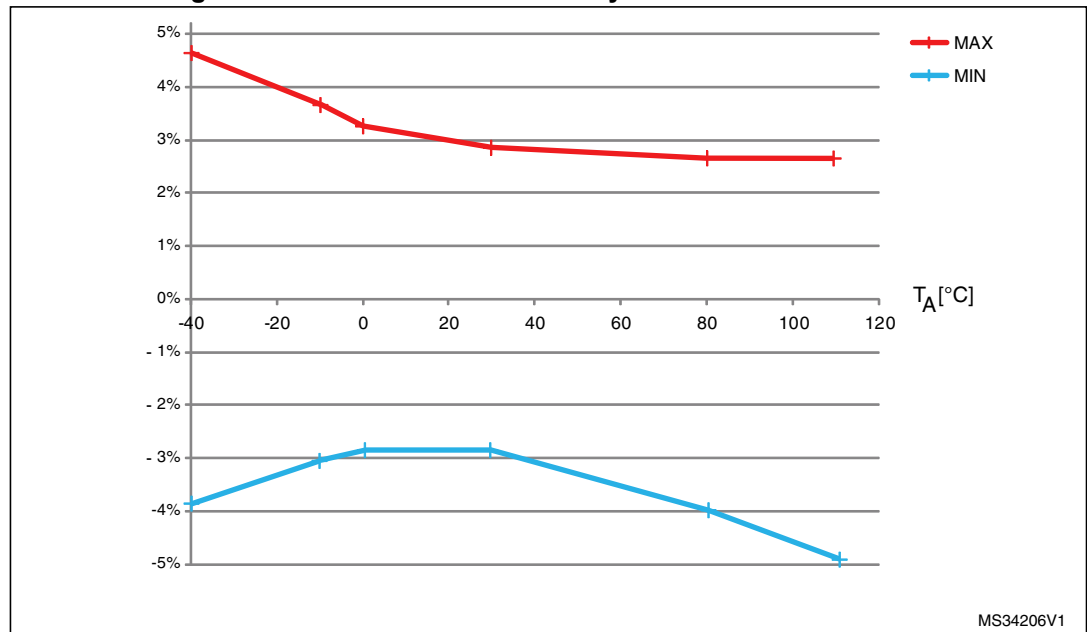
High-speed internal 48 MHz (HSI48) RC oscillator

Table 44. HSI48 oscillator characteristics<sup>(1)</sup>

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{\text{HSI48}}$	Frequency		-	48	-	MHz
TRIM	HSI48 user-trimming step		0.09 <sup>(2)</sup>	0.14	0.2 <sup>(2)</sup>	%
DuCy <sub>(HSI48)</sub>	Duty cycle		45 <sup>(2)</sup>	-	55 <sup>(2)</sup>	%
$\text{ACC}_{\text{HSI48}}$	Accuracy of the HSI48 oscillator (factory calibrated)	$T_A = -40$ to $105$ °C	-4.9 <sup>(3)</sup>	-	4.7 <sup>(3)</sup>	%
		$T_A = -10$ to $85$ °C	-4.1 <sup>(3)</sup>	-	3.7 <sup>(3)</sup>	%
		$T_A = 0$ to $70$ °C	-3.8 <sup>(3)</sup>	-	3.4 <sup>(3)</sup>	%
		$T_A = 25$ °C	-2.8	-	2.9	%
$t_{\text{su(HSI48)}}$	HSI48 oscillator startup time		-	-	6 <sup>(2)</sup>	µs
$I_{\text{DDA(HSI48)}}$	HSI48 oscillator power consumption		-	312	350 <sup>(2)</sup>	µA

- $V_{\text{DDA}} = 3.3$  V,  $T_A = -40$  to  $105$  °C unless otherwise specified.
- Guaranteed by design, not tested in production.
- Data based on characterization results, not tested in production.

Figure 20. HSI48 oscillator accuracy characterization results



### Low-speed internal (LSI) RC oscillator

**Table 45. LSI oscillator characteristics<sup>(1)</sup>**

Symbol	Parameter	Min	Typ	Max	Unit
$f_{LSI}$	Frequency	30	40	50	kHz
$t_{su(LSI)}^{(2)}$	LSI oscillator startup time	-	-	85	$\mu$ s
$I_{DDA(LSI)}^{(2)}$	LSI oscillator power consumption	-	0.75	1.2	$\mu$ A

- $V_{DDA} = 3.3$  V,  $T_A = -40$  to  $105$  °C unless otherwise specified.
- Guaranteed by design, not tested in production.

### 6.3.9 PLL characteristics

The parameters given in [Table 46](#) are derived from tests performed under ambient temperature and supply voltage conditions summarized in [Table 24: General operating conditions](#).

**Table 46. PLL characteristics**

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
$f_{PLL\_IN}$	PLL input clock <sup>(1)</sup>	1 <sup>(2)</sup>	8.0	24 <sup>(2)</sup>	MHz
	PLL input clock duty cycle	40 <sup>(2)</sup>	-	60 <sup>(2)</sup>	%
$f_{PLL\_OUT}$	PLL multiplier output clock	16 <sup>(2)</sup>	-	48	MHz
$t_{LOCK}$	PLL lock time	-	-	200 <sup>(2)</sup>	$\mu$ s
$Jitter_{PLL}$	Cycle-to-cycle jitter	-	-	300 <sup>(2)</sup>	ps

- Take care to use the appropriate multiplier factors to obtain PLL input clock values compatible with the range defined by  $f_{PLL\_OUT}$ .
- Guaranteed by design, not tested in production.

### 6.3.10 Memory characteristics

#### Flash memory

The characteristics are given at  $T_A = -40$  to  $105$  °C unless otherwise specified.

**Table 47. Flash memory characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max <sup>(1)</sup>	Unit
$t_{\text{prog}}$	16-bit programming time	$T_A = -40$ to $+105$ °C	40	53.5	60	$\mu\text{s}$
$t_{\text{ERASE}}$	Page (2 KB) erase time	$T_A = -40$ to $+105$ °C	20	-	40	ms
$t_{\text{ME}}$	Mass erase time	$T_A = -40$ to $+105$ °C	20	-	40	ms
$I_{\text{DD}}$	Supply current	Write mode	-	-	10	mA
		Erase mode	-	-	12	mA
$V_{\text{prog}}$	Programming voltage		2	-	3.6	V

1. Guaranteed by design, not tested in production.

**Table 48. Flash memory endurance and data retention**

Symbol	Parameter	Conditions	Min <sup>(1)</sup>	Unit
$N_{\text{END}}$	Endurance	$T_A = -40$ to $+105$ °C	10	kcycles
$t_{\text{RET}}$	Data retention	1 kcycle <sup>(2)</sup> at $T_A = 85$ °C	30	Years
		1 kcycle <sup>(2)</sup> at $T_A = 105$ °C	10	
		10 kcycles <sup>(2)</sup> at $T_A = 55$ °C	20	

1. Data based on characterization results, not tested in production.

2. Cycling performed over the whole temperature range.

### 6.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

#### Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB:** A Burst of Fast Transient voltage (positive and negative) is applied to  $V_{\text{DD}}$  and  $V_{\text{SS}}$  through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in [Table 49](#). They are based on the EMS levels and classes defined in application note AN1709.

**Table 49. EMS characteristics**

Symbol	Parameter	Conditions	Level/Class
V <sub>FESD</sub>	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V <sub>DD</sub> = 3.3 V, LQFP100, T <sub>A</sub> = +25 °C, f <sub>HCLK</sub> = 48 MHz, conforming to IEC 61000-4-2	2B
V <sub>EFTB</sub>	Fast transient voltage burst limits to be applied through 100 pF on V <sub>DD</sub> and V <sub>SS</sub> pins to induce a functional disturbance	V <sub>DD</sub> = 3.3 V, LQFP100, T <sub>A</sub> = +25 °C, f <sub>HCLK</sub> = 48 MHz, conforming to IEC 61000-4-4	4B

**Designing hardened software to avoid noise problems**

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

**Software recommendations**

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

**Prequalification trials**

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

**Electromagnetic Interference (EMI)**

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

**Table 50. EMI characteristics**

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f <sub>HSE</sub> /f <sub>HCLK</sub> ]	Unit
				8/48 MHz	
S <sub>EMI</sub>	Peak level	V <sub>DD</sub> = 3.6 V, T <sub>A</sub> = 25 °C, LQFP100 package compliant with IEC 61967-2	0.1 to 30 MHz	-3	dBμV
			30 to 130 MHz	23	
			130 MHz to 1GHz	14	
			EMI Level	4	-

### 6.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

#### Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

**Table 51. ESD absolute maximum ratings**

Symbol	Ratings	Conditions	Class	Maximum value <sup>(1)</sup>	Unit
V <sub>ESD(HBM)</sub>	Electrostatic discharge voltage (human body model)	T <sub>A</sub> = +25 °C, conforming to JESD22-A114	2	2000	V
V <sub>ESD(CDM)</sub>	Electrostatic discharge voltage (charge device model)	T <sub>A</sub> = +25 °C, conforming to ANSI/ESD STM5.3.1	II	500	

1. Data based on characterization results, not tested in production.

#### Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

**Table 52. Electrical sensitivities**

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T <sub>A</sub> = +105 °C conforming to JESD78A	II level A

### 6.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V<sub>SS</sub> or above V<sub>DDIOx</sub> (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

### Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the  $-5 \mu\text{A}/+0 \mu\text{A}$  range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in [Table 53](#).

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

**Table 53. I/O current injection susceptibility**

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I <sub>INJ</sub>	Injected current on BOOT0 and PF1 pins	-0	NA	mA
	Injected current on PC0 pin	-0	+5	
	Injected current on PA11 and PA12 pins with induced leakage current on adjacent pins less than -1 mA	-5	NA	
	Injected current on all other FT and FTf pins	-5	NA	
	Injected current on all other TTa, TC and RST pins	-5	+5	

### 6.3.14 I/O port characteristics

#### General input/output characteristics

Unless otherwise specified, the parameters given in [Table 54](#) are derived from tests performed under the conditions summarized in [Table 24: General operating conditions](#). All I/Os are designed as CMOS- and TTL-compliant (except BOOT0).

**Table 54. I/O static characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>IL</sub>	Low level input voltage	TC and TTa I/O	-	-	$0.3 V_{DDIOx} + 0.07^{(1)}$	V
		FT and FTf I/O	-	-	$0.475 V_{DDIOx} - 0.2^{(1)}$	
		BOOT0	-	-	$0.3 V_{DDIOx} - 0.3^{(1)}$	
		All I/Os except BOOT0 pin	-	-	$0.3 V_{DDIOx}$	

Table 54. I/O static characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IH}$	High level input voltage	TC and TTa I/O	$0.445 V_{DDIOx} + 0.398^{(1)}$	-	-	V
		FT and FTf I/O	$0.5 V_{DDIOx} + 0.2^{(1)}$	-	-	
		BOOT0	$0.2 V_{DDIOx} + 0.95^{(1)}$	-	-	
		All I/Os except BOOT0 pin	$0.7 V_{DDIOx}$	-	-	
$V_{hys}$	Schmitt trigger hysteresis	TC and TTa I/O	-	$200^{(1)}$	-	mV
		FT and FTf I/O	-	$100^{(1)}$	-	
		BOOT0	-	$300^{(1)}$	-	
$I_{Ikg}$	Input leakage current <sup>(2)</sup>	TC, FT and FTf I/O TTa in digital mode $V_{SS} \leq V_{IN} \leq V_{DDIOx}$	-	-	$\pm 0.1$	$\mu A$
		TTa in digital mode $V_{DDIOx} \leq V_{IN} \leq V_{DDA}$	-	-	1	
		TTa in analog mode $V_{SS} \leq V_{IN} \leq V_{DDA}$	-	-	$\pm 0.2$	
		FT and FTf I/O <sup>(3)</sup> $V_{DDIOx} \leq V_{IN} \leq 5 V$	-	-	10	
$R_{PU}$	Weak pull-up equivalent resistor <sup>(4)</sup>	$V_{IN} = V_{SS}$	25	40	55	k $\Omega$
$R_{PD}$	Weak pull-down equivalent resistor <sup>(4)</sup>	$V_{IN} = V_{DDIOx}$	25	40	55	k $\Omega$
$C_{IO}$	I/O pin capacitance		-	5	-	pF

1. Data based on design simulation only. Not tested in production.

2. The leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to [Table 53: I/O current injection susceptibility](#).

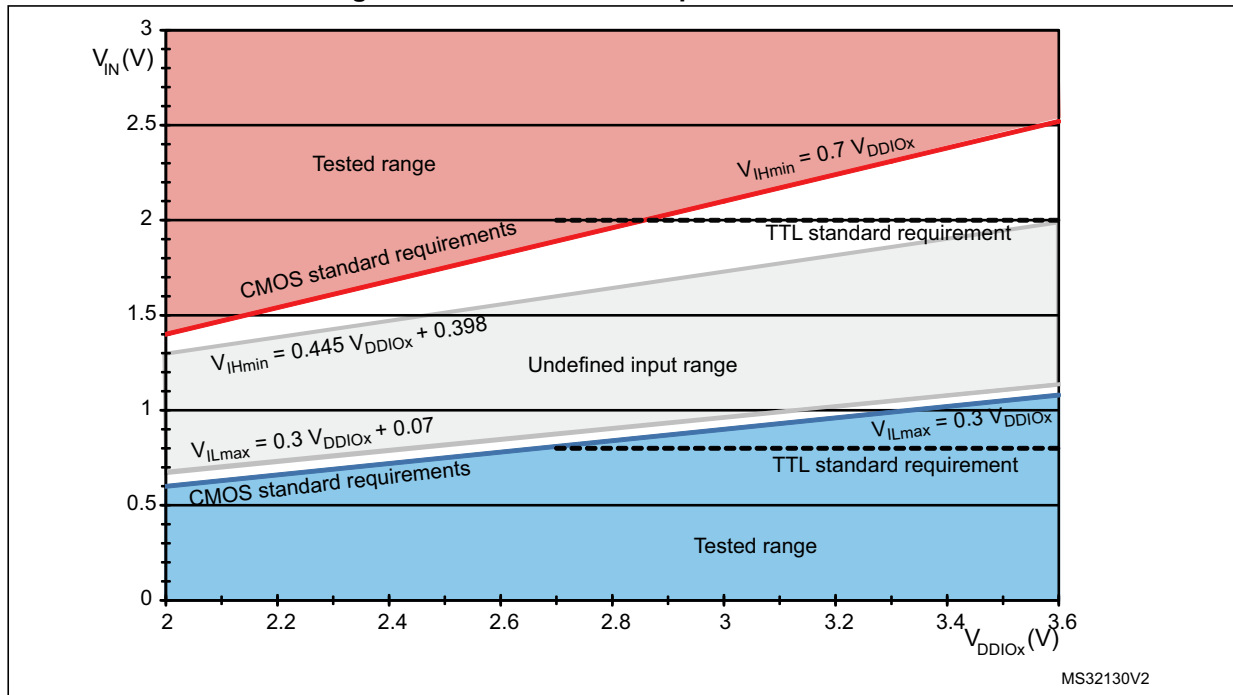
3. To sustain a voltage higher than  $V_{DDIOx} + 0.3 V$ , the internal pull-up/pull-down resistors must be disabled.

4. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

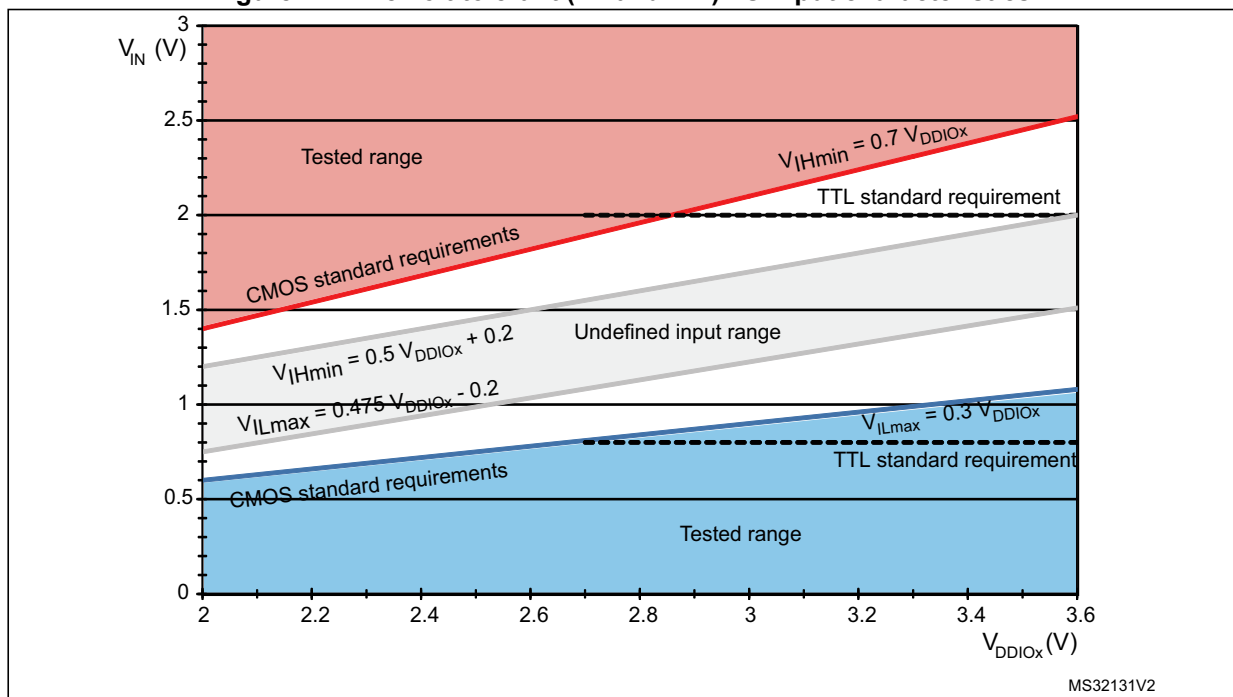


All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 20* for standard I/Os, and in *Figure 21* for 5 V tolerant I/Os.

**Figure 21. TC and TTa I/O input characteristics**



**Figure 22. Five volt tolerant (FT and FTf) I/O input characteristics**



### Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed  $V_{OL}/V_{OH}$ ).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in [Section 6.2](#):

- The sum of the currents sourced by all the I/Os on  $V_{DDIOx}$ , plus the maximum consumption of the MCU sourced on  $V_{DD}$ , cannot exceed the absolute maximum rating  $\Sigma I_{VDD}$  (see [Table 21: Voltage characteristics](#)).
- The sum of the currents sunk by all the I/Os on  $V_{SS}$ , plus the maximum consumption of the MCU sunk on  $V_{SS}$ , cannot exceed the absolute maximum rating  $\Sigma I_{VSS}$  (see [Table 21: Voltage characteristics](#)).

### Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 24: General operating conditions](#). All I/Os are CMOS- and TTL-compliant (FT, TTa or TC unless otherwise specified).

**Table 55. Output voltage characteristics<sup>(1)</sup>**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{OL}$	Output low level voltage for an I/O pin	CMOS port <sup>(2)</sup> $ I_{IO}  = 8 \text{ mA}$ $V_{DDIOx} \geq 2.7 \text{ V}$	-	0.4	V
$V_{OH}$	Output high level voltage for an I/O pin		$V_{DDIOx}-0.4$	-	
$V_{OL}$	Output low level voltage for an I/O pin	TTL port <sup>(2)</sup> $ I_{IO}  = 8 \text{ mA}$ $V_{DDIOx} \geq 2.7 \text{ V}$	-	0.4	V
$V_{OH}$	Output high level voltage for an I/O pin		2.4	-	
$V_{OL}^{(3)}$	Output low level voltage for an I/O pin	$ I_{IO}  = 20 \text{ mA}$ $V_{DDIOx} \geq 2.7 \text{ V}$	-	1.3	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$V_{DDIOx}-1.3$	-	
$V_{OL}^{(3)}$	Output low level voltage for an I/O pin	$ I_{IO}  = 6 \text{ mA}$ $V_{DDIOx} \geq 2 \text{ V}$	-	0.4	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$V_{DDIOx}-0.4$	-	
$V_{OL}^{(3)}$	Output low level voltage for an I/O pin	$ I_{IO}  = 4 \text{ mA}$	-	0.4	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$V_{DDIOx}-0.4$	-	V
$V_{OLFM+}^{(4)}$	Output low level voltage for an FTf I/O pin in FM+ mode	$ I_{IO}  = 20 \text{ mA}$ $V_{DDIOx} \geq 2.7 \text{ V}$	-	0.4	V
		$ I_{IO}  = 10 \text{ mA}$	-	0.4	V

1. The  $I_{IO}$  current sourced or sunk by the device must always respect the absolute maximum rating specified in [Table 21: Voltage characteristics](#), and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings  $\Sigma I_{IO}$ .
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Data based on characterization results. Not tested in production.
4. Data based on design simulation only. Not tested in production.

**Input/output AC characteristics**

The definition and values of input/output AC characteristics are given in *Figure 23* and *Table 56*, respectively.

Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 24: General operating conditions*.

**Table 56. I/O AC characteristics<sup>(1)(2)</sup>**

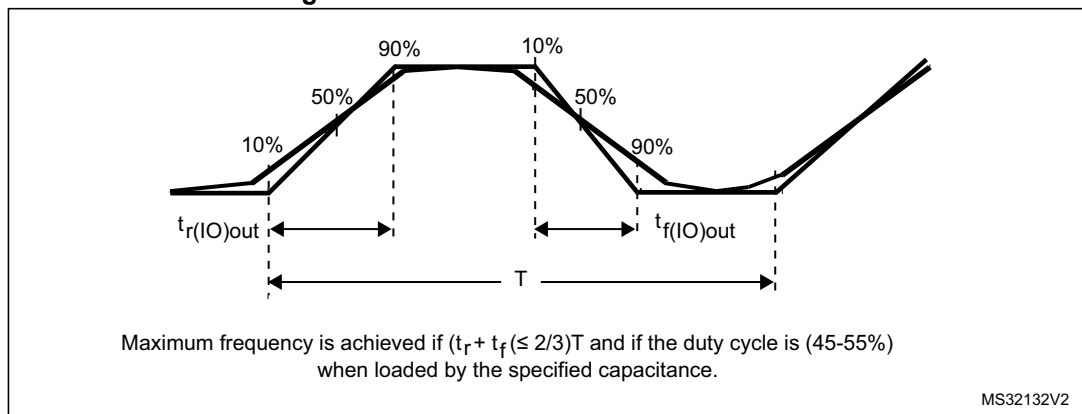
OSPEEDRy [1:0] value <sup>(1)</sup>	Symbol	Parameter	Conditions	Min	Max	Unit
x0	f <sub>max(I/O)out</sub>	Maximum frequency <sup>(3)</sup>	C <sub>L</sub> = 50 pF, V <sub>DDIOx</sub> ≥ 2 V	-	2	MHz
	t <sub>f(I/O)out</sub>	Output fall time		-	125	ns
	t <sub>r(I/O)out</sub>	Output rise time		-	125	
	f <sub>max(I/O)out</sub>	Maximum frequency <sup>(3)</sup>	C <sub>L</sub> = 50 pF, V <sub>DDIOx</sub> < 2 V	-	1	MHz
	t <sub>f(I/O)out</sub>	Output fall time		-	125	ns
	t <sub>r(I/O)out</sub>	Output rise time		-	125	
01	f <sub>max(I/O)out</sub>	Maximum frequency <sup>(3)</sup>	C <sub>L</sub> = 50 pF, V <sub>DDIOx</sub> ≥ 2 V	-	10	MHz
	t <sub>f(I/O)out</sub>	Output fall time		-	25	ns
	t <sub>r(I/O)out</sub>	Output rise time		-	25	
	f <sub>max(I/O)out</sub>	Maximum frequency <sup>(3)</sup>	C <sub>L</sub> = 50 pF, V <sub>DDIOx</sub> < 2 V	-	4	MHz
	t <sub>f(I/O)out</sub>	Output fall time		-	62.5	ns
	t <sub>r(I/O)out</sub>	Output rise time		-	62.5	
11	f <sub>max(I/O)out</sub>	Maximum frequency <sup>(3)</sup>	C <sub>L</sub> = 30 pF, V <sub>DDIOx</sub> ≥ 2.7 V	-	50	MHz
			C <sub>L</sub> = 50 pF, V <sub>DDIOx</sub> ≥ 2.7 V	-	30	
			C <sub>L</sub> = 50 pF, 2 V ≤ V <sub>DDIOx</sub> < 2.7 V	-	20	
			C <sub>L</sub> = 50 pF, V <sub>DDIOx</sub> < 2 V	-	10	
	t <sub>f(I/O)out</sub>	Output fall time	C <sub>L</sub> = 30 pF, V <sub>DDIOx</sub> ≥ 2.7 V	-	5	ns
			C <sub>L</sub> = 50 pF, V <sub>DDIOx</sub> ≥ 2.7 V	-	8	
			C <sub>L</sub> = 50 pF, 2 V ≤ V <sub>DDIOx</sub> < 2.7 V	-	12	
			C <sub>L</sub> = 50 pF, V <sub>DDIOx</sub> < 2 V	-	25	
	t <sub>r(I/O)out</sub>	Output rise time	C <sub>L</sub> = 30 pF, V <sub>DDIOx</sub> ≥ 2.7 V	-	5	
			C <sub>L</sub> = 50 pF, V <sub>DDIOx</sub> ≥ 2.7 V	-	8	
			C <sub>L</sub> = 50 pF, 2 V ≤ V <sub>DDIOx</sub> < 2.7 V	-	12	
			C <sub>L</sub> = 50 pF, V <sub>DDIOx</sub> < 2 V	-	25	

Table 56. I/O AC characteristics<sup>(1)(2)</sup> (continued)

OSPEEDRx [1:0] value <sup>(1)</sup>	Symbol	Parameter	Conditions	Min	Max	Unit
FM+ configuration <sup>(4)</sup>	$f_{\max(I/O)out}$	Maximum frequency <sup>(3)</sup>	$C_L = 50 \text{ pF}, V_{DDIOx} \geq 2 \text{ V}$	-	2	MHz
	$t_{f(I/O)out}$	Output fall time		-	12	ns
	$t_{r(I/O)out}$	Output rise time		-	34	
	$f_{\max(I/O)out}$	Maximum frequency <sup>(3)</sup>	$C_L = 50 \text{ pF}, V_{DDIOx} < 2 \text{ V}$	-	0.5	MHz
	$t_{f(I/O)out}$	Output fall time		-	16	ns
	$t_{r(I/O)out}$	Output rise time		-	44	
	$t_{EXTIpw}$	Pulse width of external signals detected by the EXTI controller		10	-	ns

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the STM32F0xxx RM0091 reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design, not tested in production.
3. The maximum frequency is defined in [Figure 23](#).
4. When FM+ configuration is set, the I/O speed control is bypassed. Refer to the STM32F0xxx reference manual RM0091 for a detailed description of FM+ I/O configuration.

Figure 23. I/O AC characteristics definition



### 6.3.15 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor,  $R_{PU}$ .

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 24: General operating conditions](#).

Table 57. NRST pin characteristics

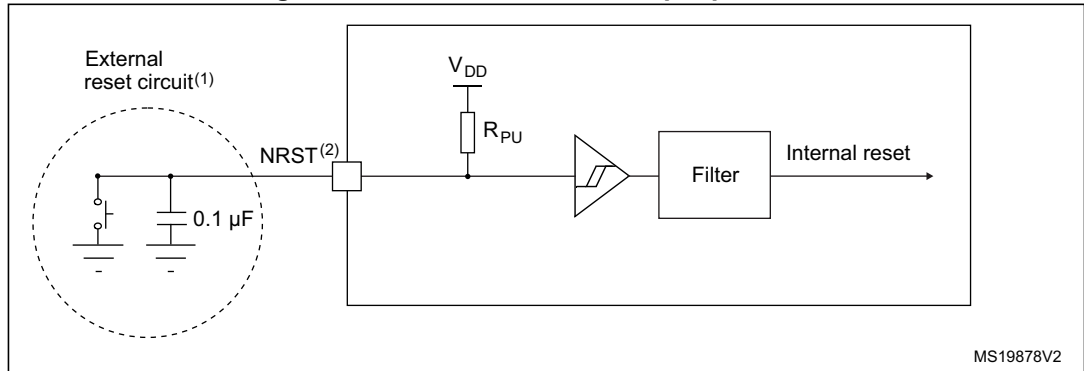
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage		-	-	$0.3 V_{DD} + 0.07^{(1)}$	V
$V_{IH(NRST)}$	NRST input high level voltage		$0.445 V_{DD} + 0.398^{(1)}$	-	-	

Table 57. NRST pin characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis		-	200	-	mV
$R_{PU}$	Weak pull-up equivalent resistor <sup>(2)</sup>	$V_{IN} = V_{SS}$	25	40	55	k $\Omega$
$V_{F(NRST)}$	NRST input filtered pulse		-	-	100 <sup>(1)</sup>	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	$2.7 < V_{DD} < 3.6$	300 <sup>(1)</sup>	-	-	ns
		$2.0 < V_{DD} < 3.6$	500 <sup>(1)</sup>	-	-	

1. Data based on design simulation only. Not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

Figure 24. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the  $V_{IL(NRST)}$  max level specified in [Table 57: NRST pin characteristics](#). Otherwise the reset will not be taken into account by the device.

### 6.3.16 12-bit ADC characteristics

Unless otherwise specified, the parameters given in [Table 58](#) are preliminary values derived from tests performed under ambient temperature,  $f_{PCLK}$  frequency and  $V_{DDA}$  supply voltage conditions summarized in [Table 24: General operating conditions](#).

Note: It is recommended to perform a calibration after each power-up.

Table 58. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DDA}$	Analog supply voltage for ADC ON		2.4	-	3.6	V
$I_{DDA(ADC)}$	Current consumption of the ADC <sup>(1)</sup>	$V_{DD} = V_{DDA} = 3.3\text{ V}$	-	0.9	-	mA
$f_{ADC}$	ADC clock frequency		0.6	-	14	MHz
$f_S^{(2)}$	Sampling rate		0.05	-	1	MHz

Table 58. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f <sub>TRIG</sub> <sup>(2)</sup>	External trigger frequency	f <sub>ADC</sub> = 14 MHz	-	-	823	kHz
			-	-	17	1/f <sub>ADC</sub>
V <sub>AIN</sub>	Conversion voltage range		0	-	V <sub>DDA</sub>	V
R <sub>AIN</sub> <sup>(2)</sup>	External input impedance	See <i>Equation 1</i> and <i>Table 59</i> for details	-	-	50	kΩ
R <sub>ADC</sub> <sup>(2)</sup>	Sampling switch resistance		-	-	1	kΩ
C <sub>ADC</sub> <sup>(2)</sup>	Internal sample and hold capacitor		-	-	8	pF
t <sub>CAL</sub> <sup>(2)</sup>	Calibration time	f <sub>ADC</sub> = 14 MHz	5.9			μs
			83			1/f <sub>ADC</sub>
W <sub>LATENCY</sub> <sup>(2)</sup>	ADC_DR register write latency	ADC clock = HSI14	1.5 ADC cycles + 2 f <sub>PCLK</sub> cycles	-	1.5 ADC cycles + 3 f <sub>PCLK</sub> cycles	
		ADC clock = PCLK/2	-	4.5	-	f <sub>PCLK</sub> cycle
		ADC clock = PCLK/4	-	8.5	-	f <sub>PCLK</sub> cycle
t <sub>itr</sub> <sup>(2)</sup>	Trigger conversion latency	f <sub>ADC</sub> = f <sub>PCLK</sub> /2 = 14 MHz	0.196			μs
		f <sub>ADC</sub> = f <sub>PCLK</sub> /2	5.5			1/f <sub>PCLK</sub>
		f <sub>ADC</sub> = f <sub>PCLK</sub> /4 = 12 MHz	0.219			μs
		f <sub>ADC</sub> = f <sub>PCLK</sub> /4	10.5			1/f <sub>PCLK</sub>
		f <sub>ADC</sub> = f <sub>HSI14</sub> = 14 MHz	0.188	-	0.259	μs
Jitter <sub>ADC</sub>	ADC jitter on trigger conversion	f <sub>ADC</sub> = f <sub>HSI14</sub>	-	1	-	1/f <sub>HSI14</sub>
t <sub>S</sub> <sup>(2)</sup>	Sampling time	f <sub>ADC</sub> = 14 MHz	0.107	-	17.1	μs
			1.5	-	239.5	1/f <sub>ADC</sub>
t <sub>STAB</sub> <sup>(2)</sup>	Power-up time		0	0	1	μs
t <sub>CONV</sub> <sup>(2)</sup>	Total conversion time (including sampling time)	f <sub>ADC</sub> = 14 MHz	1	-	18	μs
			14 to 252 (t <sub>S</sub> for sampling +12.5 for successive approximation)			1/f <sub>ADC</sub>

1. During conversion of the sampled value (12.5 x ADC clock period), an additional consumption of 100 μA on I<sub>DDA</sub> and 60 μA on I<sub>DD</sub> should be taken into account.
2. Guaranteed by design, not tested in production.

**Equation 1: R<sub>AIN</sub> max formula**

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

**Table 59. R<sub>AIN</sub> max for f<sub>ADC</sub> = 14 MHz**

T <sub>s</sub> (cycles)	t <sub>s</sub> (μs)	R <sub>AIN</sub> max (kΩ) <sup>(1)</sup>
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	NA
239.5	17.1	NA

1. Guaranteed by design, not tested in production.

**Table 60. ADC accuracy<sup>(1)(2)(3)</sup>**

Symbol	Parameter	Test conditions	Typ	Max <sup>(4)</sup>	Unit
ET	Total unadjusted error	f <sub>PCLK</sub> = 48 MHz, f <sub>ADC</sub> = 14 MHz, R <sub>AIN</sub> < 10 kΩ V <sub>DDA</sub> = 3 V to 3.6 V T <sub>A</sub> = 25 °C	±1.3	±2	LSB
EO	Offset error		±1	±1.5	
EG	Gain error		±0.5	±1.5	
ED	Differential linearity error		±0.7	±1	
EL	Integral linearity error		±0.8	±1.5	
ET	Total unadjusted error	f <sub>PCLK</sub> = 48 MHz, f <sub>ADC</sub> = 14 MHz, R <sub>AIN</sub> < 10 kΩ V <sub>DDA</sub> = 2.7 V to 3.6 V T <sub>A</sub> = -40 to 105 °C	±3.3	±4	LSB
EO	Offset error		±1.9	±2.8	
EG	Gain error		±2.8	±3	
ED	Differential linearity error		±0.7	±1.3	
EL	Integral linearity error		±1.2	±1.7	
ET	Total unadjusted error	f <sub>PCLK</sub> = 48 MHz, f <sub>ADC</sub> = 14 MHz, R <sub>AIN</sub> < 10 kΩ V <sub>DDA</sub> = 2.4 V to 3.6 V T <sub>A</sub> = 25 °C	±3.3	±4	LSB
EO	Offset error		±1.9	±2.8	
EG	Gain error		±2.8	±3	
ED	Differential linearity error		±0.7	±1.3	
EL	Integral linearity error		±1.2	±1.7	

- ADC DC accuracy values are measured after internal calibration.
- ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for I<sub>INJ(PIN)</sub> and ΣI<sub>INJ(PIN)</sub> in *Section 6.3.14* does not affect the ADC accuracy.
- Better performance may be achieved in restricted V<sub>DDA</sub>, frequency and temperature ranges.
- Data based on characterization results, not tested in production.

Figure 25. ADC accuracy characteristics

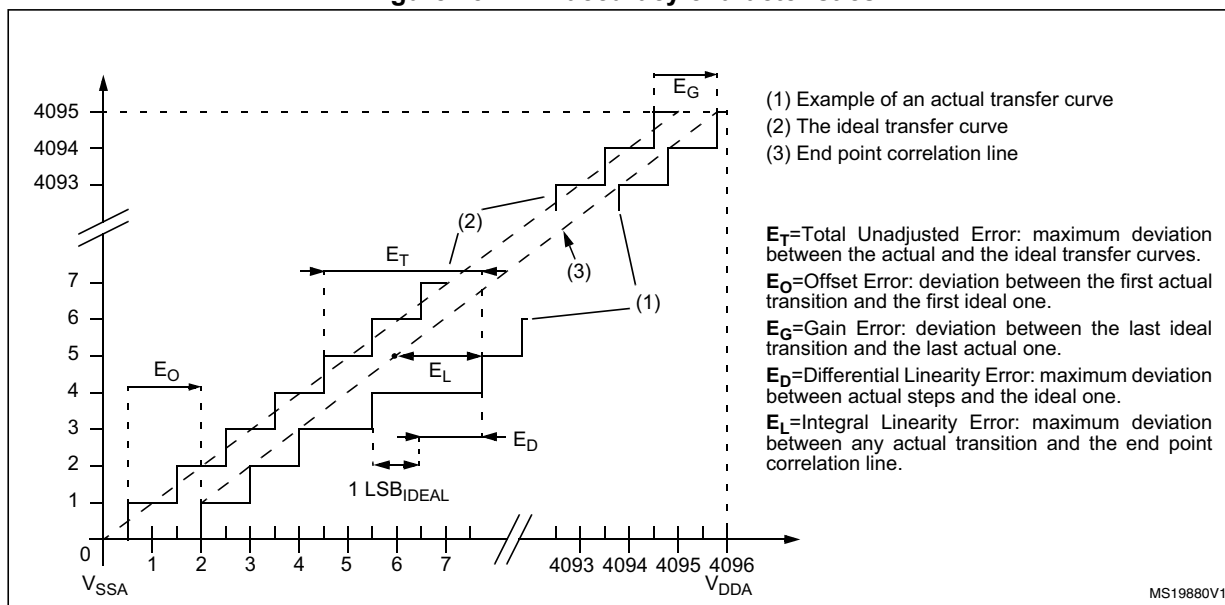
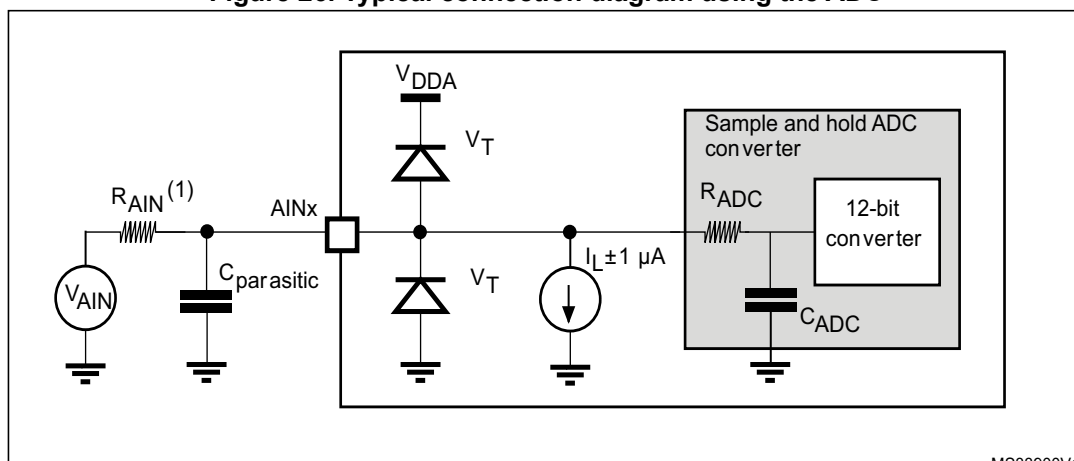


Figure 26. Typical connection diagram using the ADC



1. Refer to [Table 58: ADC characteristics](#) for the values of  $R_{AIN}$ ,  $R_{ADC}$  and  $C_{ADC}$ .
2.  $C_{parasitic}$  represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high  $C_{parasitic}$  value will downgrade conversion accuracy. To remedy this,  $f_{ADC}$  should be reduced.

**General PCB design guidelines**

Power supply decoupling should be performed as shown in [Figure 12: Power supply scheme](#). The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.



## 6.3.17 DAC electrical specifications

Table 61. DAC characteristics

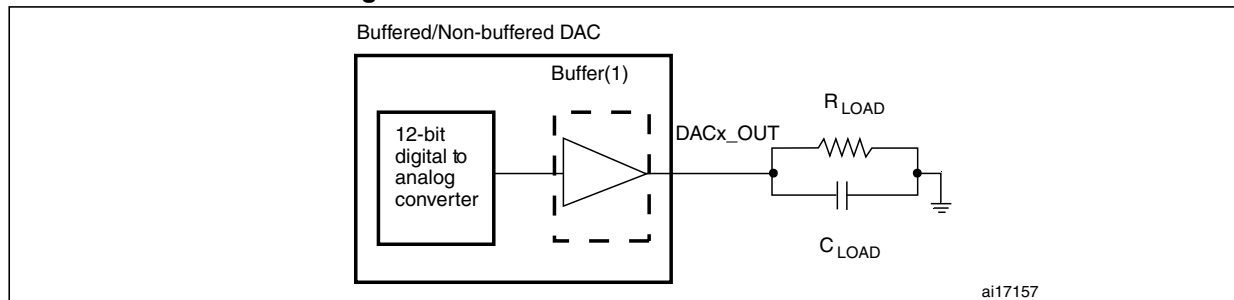
Symbol	Parameter	Min	Typ	Max	Unit	Comments
$V_{DDA}$	Analog supply voltage for DAC ON	2.4	-	3.6	V	
$R_{LOAD}^{(1)}$	Resistive load with buffer ON	5	-	-	k $\Omega$	Load is referred to ground
$R_O^{(1)}$	Impedance output with buffer OFF	-	-	15	k $\Omega$	When the buffer is OFF, the Minimum resistive load between DAC_OUT and $V_{SS}$ to have a 1% accuracy is 1.5 M $\Omega$
$C_{LOAD}^{(1)}$	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min <sup>(1)</sup>	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at $V_{DDA} = 3.6$ V and (0x155) and (0xEAB) at $V_{DDA} = 2.4$ V
DAC_OUT max <sup>(1)</sup>	Higher DAC_OUT voltage with buffer ON	-	-	$V_{DDA} - 0.2$	V	
DAC_OUT min <sup>(1)</sup>	Lower DAC_OUT voltage with buffer OFF	-	0.5	-	mV	It gives the maximum output excursion of the DAC.
DAC_OUT max <sup>(1)</sup>	Higher DAC_OUT voltage with buffer OFF	-	-	$V_{DDA} - 1\text{LSB}$	V	
$I_{DDA}$	DAC DC current consumption in quiescent mode <sup>(2)</sup>	-	-	380	$\mu$ A	With no load, middle code (0x800) on the input
		-	-	480	$\mu$ A	With no load, worst code (0xF1C) on the input
DNL <sup>(3)</sup>	Differential non linearity Difference between two consecutive code-1LSB)	-	-	$\pm 0.5$	LSB	Given for the DAC in 10-bit configuration
		-	-	$\pm 2$	LSB	Given for the DAC in 12-bit configuration
INL <sup>(3)</sup>	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	-	$\pm 1$	LSB	Given for the DAC in 10-bit configuration
		-	-	$\pm 4$	LSB	Given for the DAC in 12-bit configuration
Offset <sup>(3)</sup>	Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{DDA}/2$ )	-	-	$\pm 10$	mV	
		-	-	$\pm 3$	LSB	Given for the DAC in 10-bit at $V_{DDA} = 3.6$ V
		-	-	$\pm 12$	LSB	Given for the DAC in 12-bit at $V_{DDA} = 3.6$ V
Gain error <sup>(3)</sup>	Gain error	-	-	$\pm 0.5$	%	Given for the DAC in 12-bit configuration

Table 61. DAC characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit	Comments
$t_{SETTLING}^{(3)}$	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value $\pm 1LSB$ )	-	3	4	$\mu s$	$C_{LOAD} \leq 50\text{ pF}$ , $R_{LOAD} \geq 5\text{ k}\Omega$
Update rate <sup>(3)</sup>	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	1	MS/s	$C_{LOAD} \leq 50\text{ pF}$ , $R_{LOAD} \geq 5\text{ k}\Omega$
$t_{WAKEUP}^{(3)}$	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	6.5	10	$\mu s$	$C_{LOAD} \leq 50\text{ pF}$ , $R_{LOAD} \geq 5\text{ k}\Omega$ input code between lowest and highest possible ones.
PSRR+ <sup>(1)</sup>	Power supply rejection ratio (to $V_{DDA}$ ) (static DC measurement)	-	-67	-40	dB	No $R_{LOAD}$ , $C_{LOAD} = 50\text{ pF}$

1. Guaranteed by design, not tested in production.
2. The DAC is in “quiescent mode” when it keeps the value steady on the output so no dynamic consumption is involved.
3. Data based on characterization results, not tested in production.

Figure 27. 12-bit buffered / non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC\_CR register.

## 6.3.18 Comparator characteristics

Table 62. Comparator characteristics

Symbol	Parameter	Conditions	Min <sup>(1)</sup>	Typ	Max <sup>(1)</sup>	Unit
V <sub>DDA</sub>	Analog supply voltage		2	-	3.6	V
V <sub>IN</sub>	Comparator input voltage range		0	-	V <sub>DDA</sub>	
V <sub>SC</sub>	V <sub>REFINT</sub> scaler offset voltage		-	±5	±10	mV
t <sub>S_SC</sub>	V <sub>REFINT</sub> scaler startup time from power down		-	-	0.2	ms
t <sub>START</sub>	Comparator startup time	Startup time to reach propagation delay specification	-	-	60	µs
t <sub>D</sub>	Propagation delay for 200 mV step with 100 mV overdrive	Ultra-low power mode	-	2	4.5	µs
		Low power mode	-	0.7	1.5	
		Medium power mode	-	0.3	0.6	
		High speed mode	V <sub>DDA</sub> ≥ 2.7 V	-	50	100
	V <sub>DDA</sub> < 2.7 V		-	100	240	
	Propagation delay for full range step with 100 mV overdrive	Ultra-low power mode	-	2	7	µs
		Low power mode	-	0.7	2.1	
		Medium power mode	-	0.3	1.2	
High speed mode		V <sub>DDA</sub> ≥ 2.7 V	-	90	180	ns
	V <sub>DDA</sub> < 2.7 V	-	110	300		
V <sub>offset</sub>	Comparator offset error		-	±4	±10	mV
dV <sub>offset</sub> /dT	Offset error temperature coefficient		-	18	-	µV/°C
I <sub>DD(COMP)</sub>	COMP current consumption	Ultra-low power mode	-	1.2	1.5	µA
		Low power mode	-	3	5	
		Medium power mode	-	10	15	
		High speed mode	-	75	100	

**Table 62. Comparator characteristics (continued)**

Symbol	Parameter	Conditions	Min <sup>(1)</sup>	Typ	Max <sup>(1)</sup>	Unit	
V <sub>hys</sub>	Comparator hysteresis	No hysteresis (COMPxHYST[1:0]=00)	-	0	-	mV	
		Low hysteresis (COMPxHYST[1:0]=01)	High speed mode	3	8		13
			All other power modes	5			10
		Medium hysteresis (COMPxHYST[1:0]=10)	High speed mode	7	15		26
			All other power modes	9			19
		High hysteresis (COMPxHYST[1:0]=11)	High speed mode	18	31		49
			All other power modes	19			40

1. Data based on characterization results, not tested in production.

### 6.3.19 Temperature sensor characteristics

**Table 63. TS characteristics**

Symbol	Parameter	Min	Typ	Max	Unit
T <sub>L</sub> <sup>(1)</sup>	V <sub>SENSE</sub> linearity with temperature	-	± 1	± 2	°C
Avg_Slope <sup>(1)</sup>	Average slope	4.0	4.3	4.6	mV/°C
V <sub>30</sub>	Voltage at 30 °C (± 5 °C) <sup>(2)</sup>	1.34	1.43	1.52	V
t <sub>START</sub> <sup>(1)</sup>	Startup time	4	-	10	µs
t <sub>S_temp</sub> <sup>(1)</sup>	ADC sampling time when reading the temperature	4	-	-	µs

1. Guaranteed by design, not tested in production.

2. Measured at V<sub>DDA</sub> = 3.3 V ± 10 mV. The V<sub>30</sub> ADC conversion result is stored in the TS\_CAL1 byte. Refer to [Table 3: Temperature sensor calibration values](#).

### 6.3.20 V<sub>BAT</sub> monitoring characteristics

**Table 64. V<sub>BAT</sub> monitoring characteristics**

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V <sub>BAT</sub>	-	50	-	kΩ
Q	Ratio on V <sub>BAT</sub> measurement	-	2	-	
Er <sup>(1)</sup>	Error on Q	-1	-	+1	%
t <sub>S_vbat</sub> <sup>(1)</sup>	ADC sampling time when reading the V <sub>BAT</sub>	4	-	-	µs

1. Guaranteed by design, not tested in production.

### 6.3.21 Timer characteristics

The parameters given in the following tables are guaranteed by design.

Refer to [Section 6.3.14: I/O port characteristics](#) for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

**Table 65. TIMx<sup>(1)</sup> characteristics**

Symbol	Parameter	Conditions	Min	Max	Unit
t <sub>res(TIM)</sub>	Timer resolution time		1	-	t <sub>TIMxCLK</sub>
		f <sub>TIMxCLK</sub> = 48 MHz	20.8	-	ns
f <sub>EXT</sub>	Timer external clock frequency on CH1 to CH4		0	f <sub>TIMxCLK</sub> /2	MHz
		f <sub>TIMxCLK</sub> = 48 MHz	0	24	MHz
Res <sub>TIM</sub>	Timer resolution	TIMx (except TIM2)	-	16	bit
		TIM2	-	32	
t <sub>COUNTER</sub>	16-bit counter clock period		1	65536	t <sub>TIMxCLK</sub>
		f <sub>TIMxCLK</sub> = 48 MHz	0.0208	1365	μs
t <sub>MAX_COUNT</sub>	Maximum possible count with 32-bit counter		-	65536 × 65536	t <sub>TIMxCLK</sub>
		f <sub>TIMxCLK</sub> = 48 MHz	-	89.48	s

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3, TIM6, TIM14, TIM15, TIM16 and TIM17 timers.

**Table 66. IWDG min/max timeout period at 40 kHz (LSI)<sup>(1)</sup>**

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0]= 0x000	Max timeout RL[11:0]= 0xFFF	Unit
/4	0	0.1	409.6	ms
/8	1	0.2	819.2	
/16	2	0.4	1638.4	
/32	3	0.8	3276.8	
/64	4	1.6	6553.6	
/128	5	3.2	13107.2	
/256	6 or 7	6.4	26214.4	

1. These timings are given for a 40 kHz clock but the microcontroller's internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 67. WWDG min/max timeout value at 48 MHz (PCLK)

Prescaler	WDGTB	Min timeout value	Max timeout value	Unit
1	0	0.0853	5.4613	ms
2	1	0.1706	10.9226	
4	2	0.3413	21.8453	
8	3	0.6826	43.6906	

## 6.3.22 Communication interfaces

### I<sup>2</sup>C interface characteristics

The I2C interface meets the timings requirements of the I<sup>2</sup>C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I2C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to Reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V<sub>DDIOx</sub> is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement. Refer to [Section 6.3.14: I/O port characteristics](#) for the I2C I/Os characteristics.

All I2C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

Table 68. I2C analog filter characteristics<sup>(1)</sup>

Symbol	Parameter	Min	Max	Unit
t <sub>AF</sub>	Maximum pulse width of spikes that are suppressed by the analog filter	50 <sup>(2)</sup>	260 <sup>(3)</sup>	ns

1. Guaranteed by design, not tested in production.
2. Spikes with widths below t<sub>AF(min)</sub> are filtered.
3. Spikes with widths above t<sub>AF(max)</sub> are not filtered

### SPI/I<sup>2</sup>S characteristics

Unless otherwise specified, the parameters given in [Table 69](#) for SPI or in [Table 70](#) for I<sup>2</sup>S are derived from tests performed under the ambient temperature,  $f_{PCLKX}$  frequency and supply voltage conditions summarized in [Table 24: General operating conditions](#).

Refer to [Section 6.3.14: I/O port characteristics](#) for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I<sup>2</sup>S).

**Table 69. SPI characteristics<sup>(1)</sup>**

Symbol	Parameter	Conditions	Min	Max	Unit
$f_{SCK}$ $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 15 pF	-	6	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	4Tpclk	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2Tpclk + 10	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, $f_{PCLK} = 36$ MHz, presc = 4	Tpclk/2 - 2	Tpclk/2 + 1	
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode	4	-	
		Slave mode	5	-	
$t_{h(MI)}$ $t_{h(SI)}$	Data input hold time	Master mode	4	-	
		Slave mode	5	-	
$t_{a(SO)}^{(2)}$	Data output access time	Slave mode, $f_{PCLK} = 20$ MHz	0	3Tpclk	
$t_{dis(SO)}^{(3)}$	Data output disable time	Slave mode	0	18	
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge)	-	22.5	
$t_{v(MO)}$	Data output valid time	Master mode (after enable edge)	-	6	
$t_{h(SO)}$ $t_{h(MO)}$	Data output hold time	Slave mode (after enable edge)	11.5	-	
		Master mode (after enable edge)	2	-	
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	25	75	

1. Data based on characterization results, not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

Figure 28. SPI timing diagram - slave mode and CPHA = 0

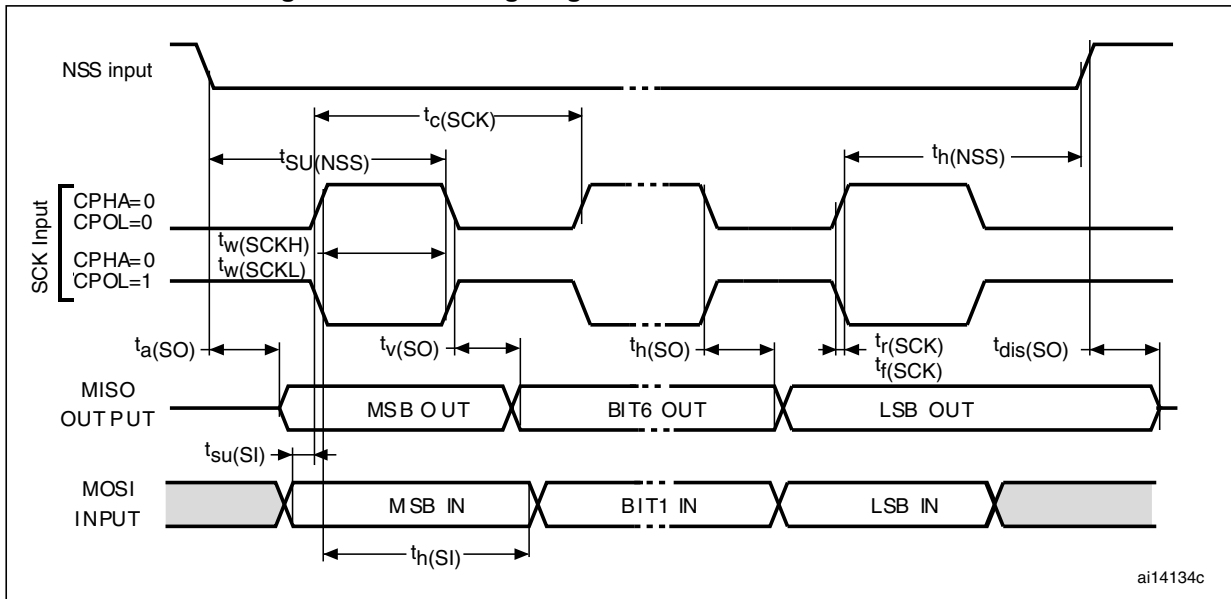
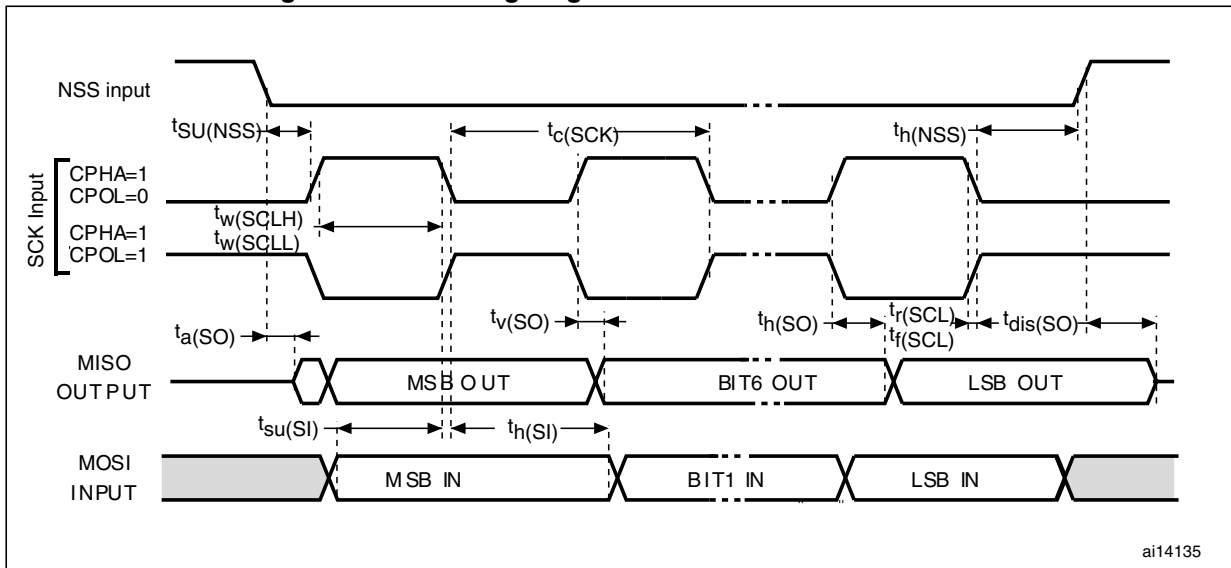


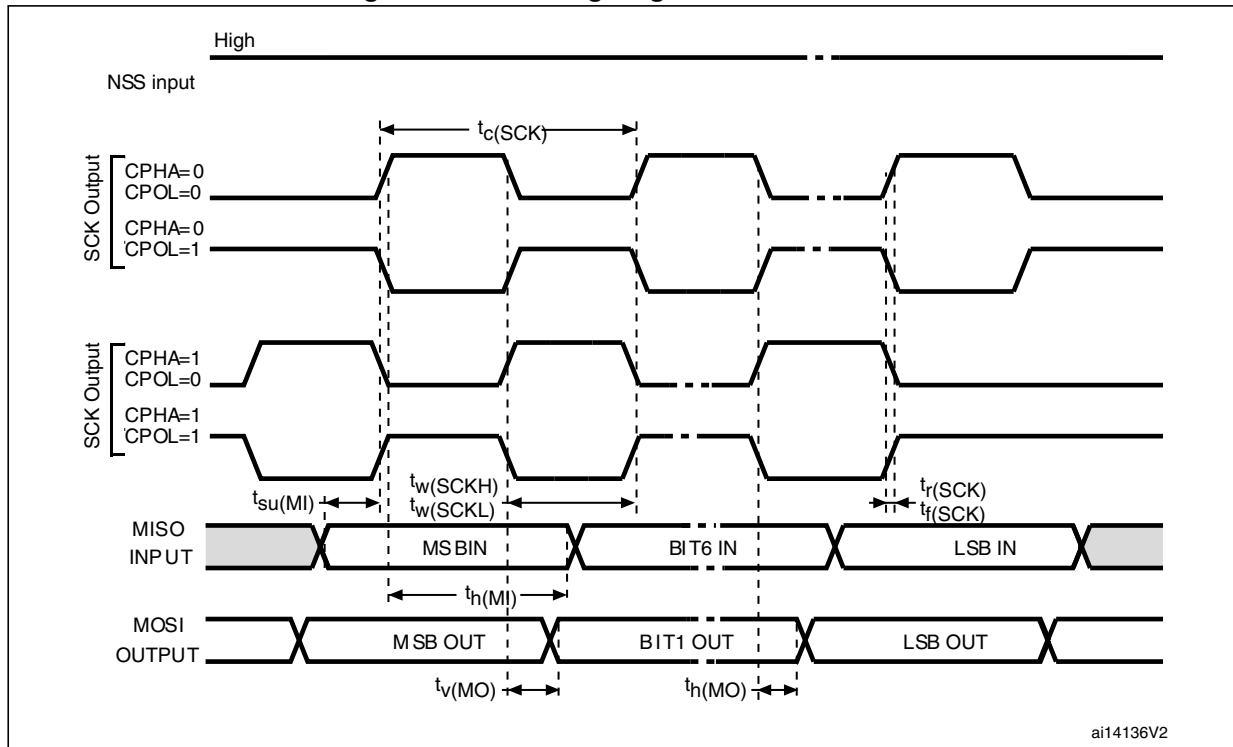
Figure 29. SPI timing diagram - slave mode and CPHA = 1



1. Measurement points are done at CMOS levels: 0.3  $V_{DD}$  and 0.7  $V_{DD}$ .



Figure 30. SPI timing diagram - master mode



1. Measurement points are done at CMOS levels: 0.3 V<sub>DD</sub> and 0.7 V<sub>DD</sub>.

Table 70. I<sup>2</sup>S characteristics<sup>(1)</sup>

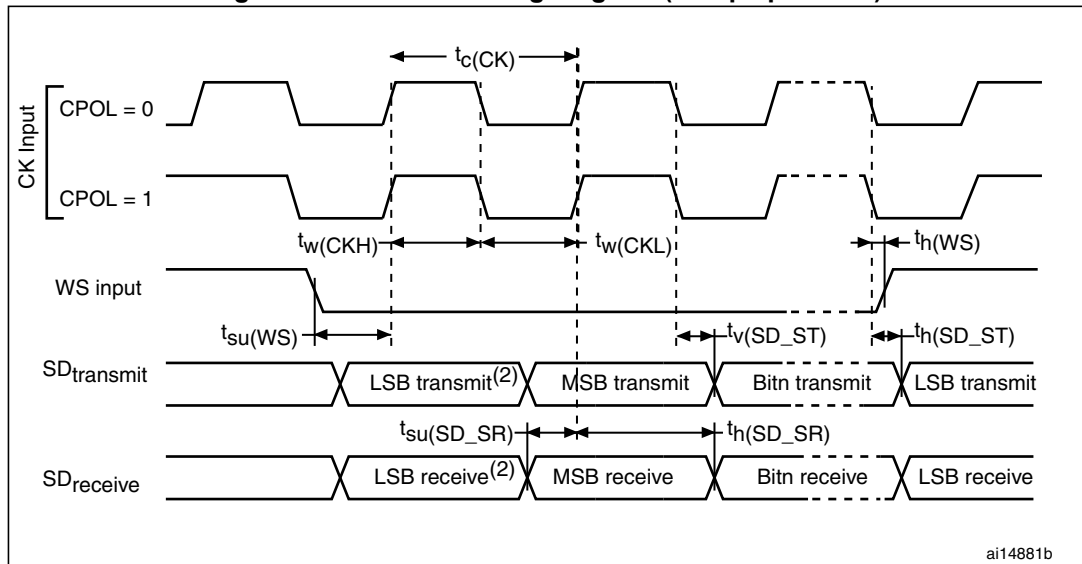
Symbol	Parameter	Conditions	Min	Max	Unit
$f_{CK}$ $1/t_c(CK)$	I <sup>2</sup> S clock frequency	Master mode (data: 16 bits, Audio frequency = 48 kHz)	1.597	1.601	MHz
		Slave mode	0	6.5	
$t_r(CK)$	I <sup>2</sup> S clock rise time	Capacitive load C <sub>L</sub> = 15 pF	-	10	ns
$t_f(CK)$	I <sup>2</sup> S clock fall time		-	12	
$t_w(CKH)$	I2S clock high time	Master $f_{PCLK} = 16$ MHz, audio frequency = 48 kHz	306	-	
$t_w(CKL)$	I2S clock low time		312	-	
$t_v(WS)$	WS valid time	Master mode	2	-	
$t_h(WS)$	WS hold time	Master mode	2	-	
$t_{su}(WS)$	WS setup time	Slave mode	7	-	
$t_h(WS)$	WS hold time	Slave mode	0	-	
DuCy(SCK)	I2S slave input clock duty cycle	Slave mode	25	75	

Table 70. I<sup>2</sup>S characteristics<sup>(1)</sup> (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	6	-	ns
$t_{su(SD\_SR)}$	Data input setup time	Slave receiver	2	-	
$t_h(SD\_MR)^{(2)}$	Data input hold time	Master receiver	4	-	
$t_h(SD\_SR)^{(2)}$		Slave receiver	0.5	-	
$t_v(SD\_ST)^{(2)}$	Data output valid time	Slave transmitter (after enable edge)	-	20	
$t_h(SD\_ST)$	Data output hold time	Slave transmitter (after enable edge)	13	-	
$t_v(SD\_MT)^{(2)}$	Data output valid time	Master transmitter (after enable edge)	-	4	
$t_h(SD\_MT)$	Data output hold time	Master transmitter (after enable edge)	0	-	

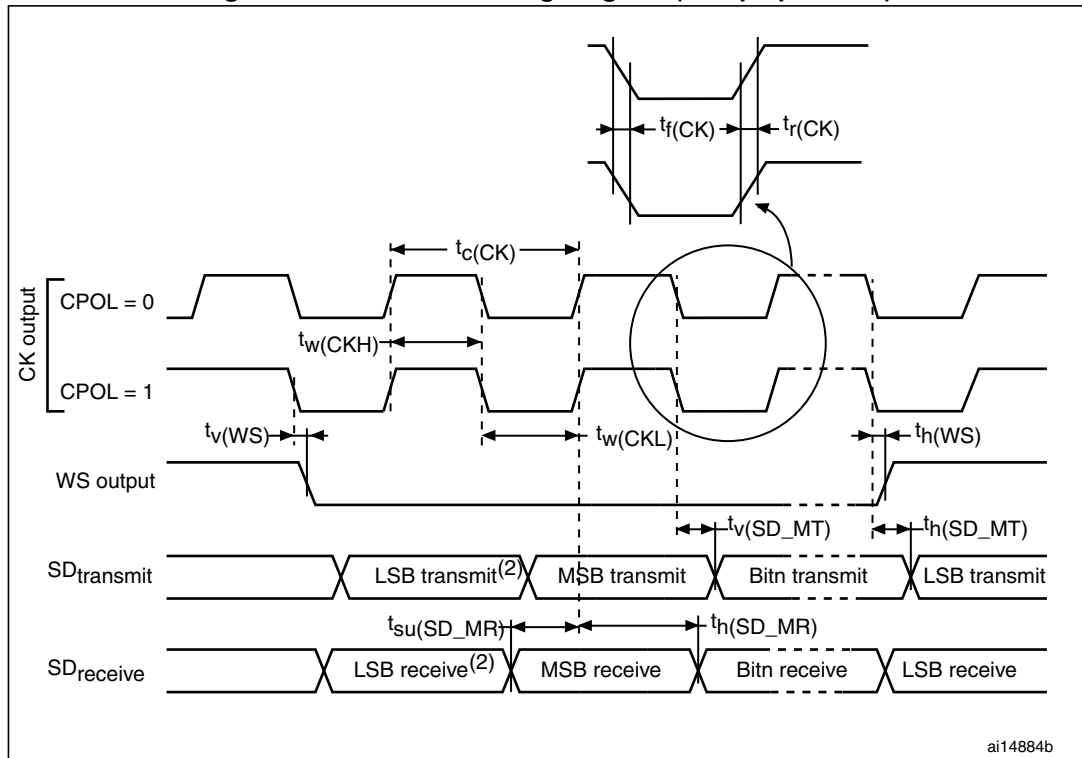
1. Data based on design simulation and/or characterization results, not tested in production.
2. Depends on  $f_{PCLK}$ . For example, if  $f_{PCLK} = 8 \text{ MHz}$ , then  $T_{PCLK} = 1/f_{PCLK} = 125 \text{ ns}$ .

Figure 31. I2S slave timing diagram (Philips protocol)



1. Measurement points are done at CMOS levels:  $0.3 \times V_{DDIOx}$  and  $0.7 \times V_{DDIOx}$ .
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 32. I2S master timing diagram (Philips protocol)



ai14884b

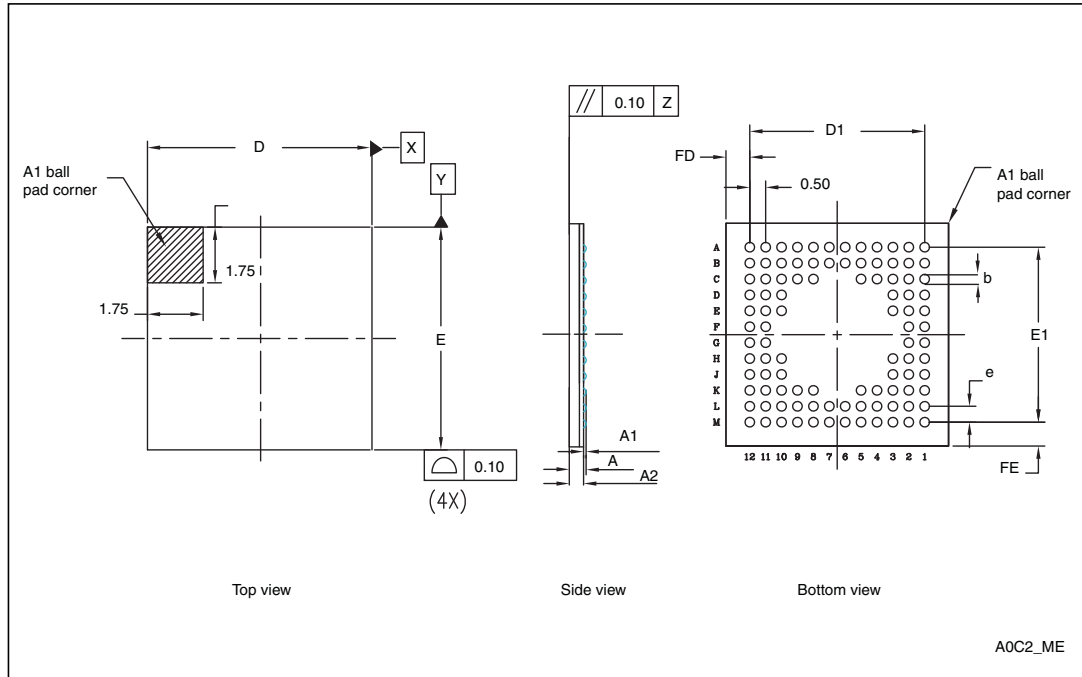
1. Data based on characterization results, not tested in production.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

## 7 Package characteristics

### 7.1 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Figure 33. UFBGA100 – ultra fine pitch ball grid array, 7 x 7 mm, 0.50 mm pitch, package outline



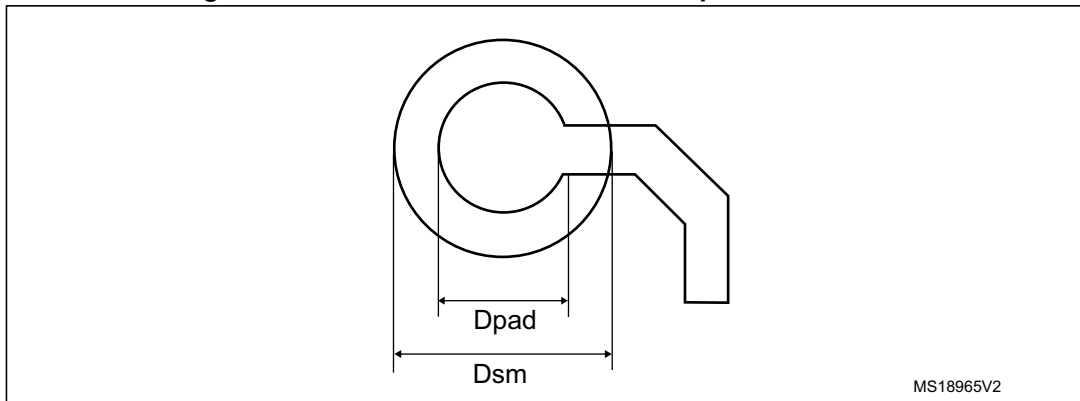
1. Drawing is not to scale.

Table 71. UFBGA100 – ultra fine pitch ball grid array, 7 x 7 mm, 0.50 mm pitch, package mechanical data

Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.060	0.080	0.100	0.0024	0.0031	0.0039
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
D	-	7.000	-	-	0.2756	-
D1	-	5.500	-	-	0.2165	-
E	-	7.000	-	-	0.2756	-
E1	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
FD	-	0.750	-	-	0.0295	-
FE	-	0.750	-	-	0.0295	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 34. UFBGA100 recommended footprint



MS18965V2

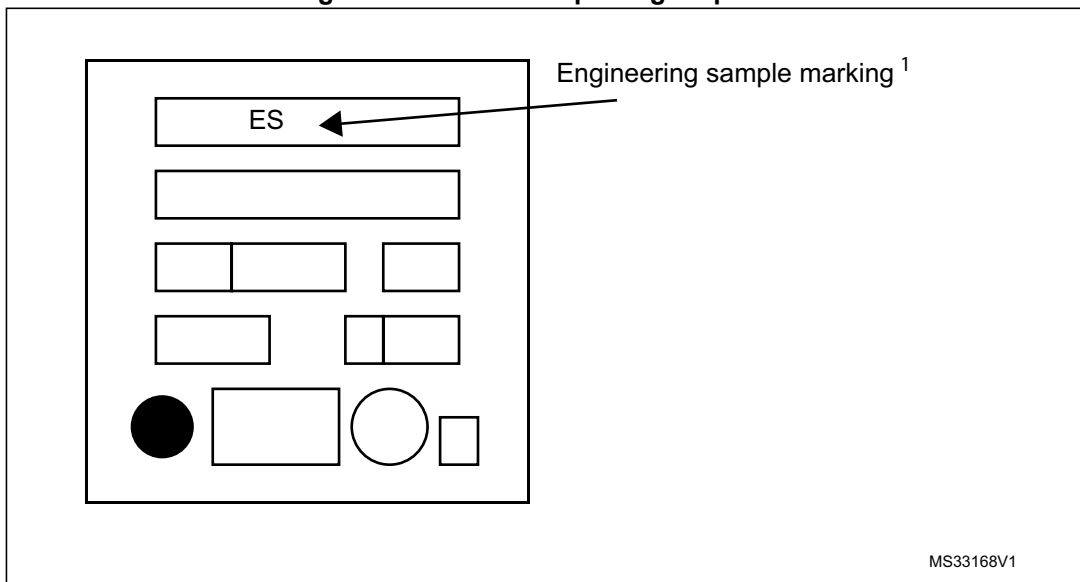
Table 72. UFBGA100 recommended PCB design rules

Dimension	Recommended values
Pitch	0.50 mm
Dpad	0.27 mm
Dsm	0.35 mm typ (depending on the soldermask registration tolerance)
Solder paste	0.27 mm aperture diameter

**Marking of engineering samples for UFBGA100**

The following figure shows the engineering sample marking for the UFBGA100 package. Only the information field containing the engineering sample marking is shown.

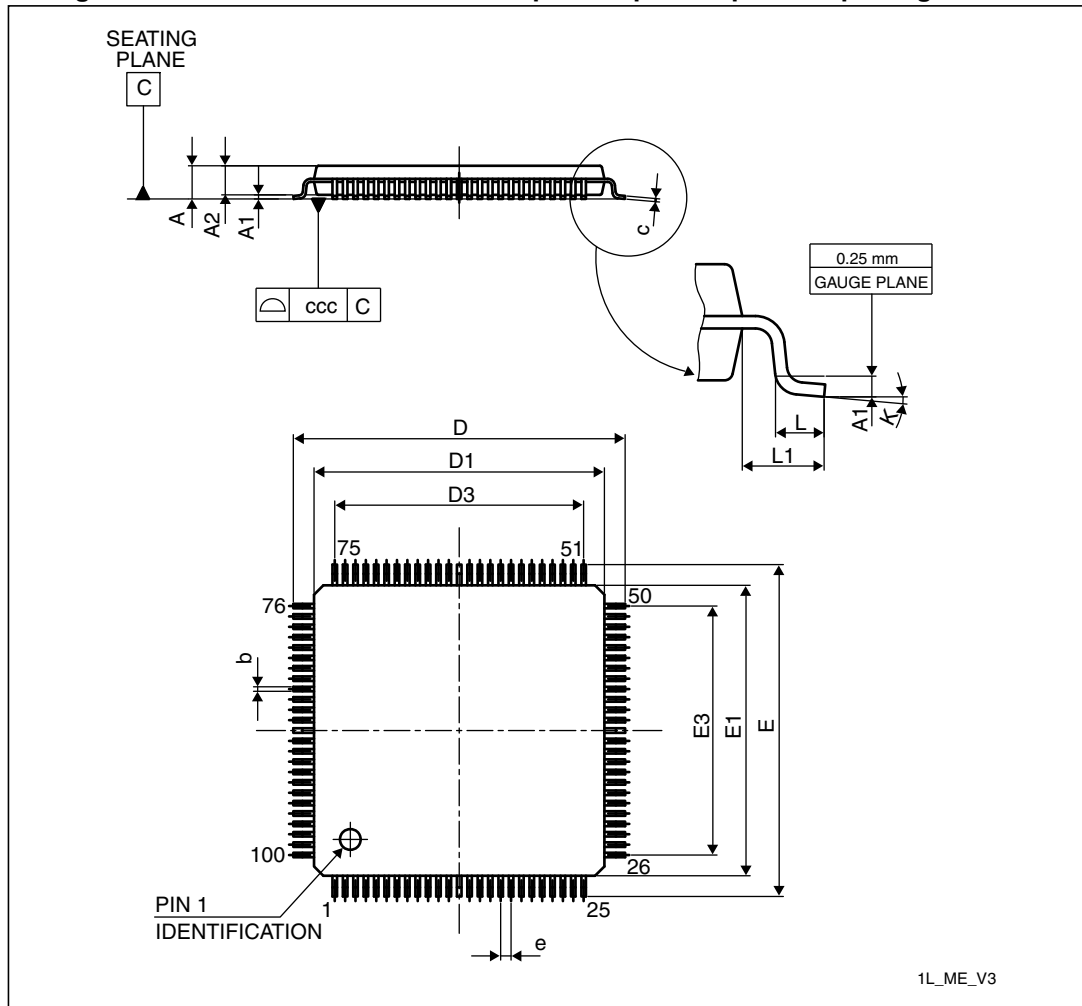
Figure 35. UFBGA100 package top view



MS33168V1

1. Samples marked "E" are to be considered as "Engineering Samples": i.e. they are intended to be sent to customer for electrical compatibility evaluation and may be used to start customer qualification where specifically authorized by ST in writing. In no event ST will be liable for any customer usage in production. Only if ST has authorized in writing the customer qualification Engineering Samples can be used for reliability qualification trials.

Figure 36. LQFP100 – 14 x 14 mm 100 pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 73. LQFP100 – 14 x 14 mm low-profile quad flat package mechanical data

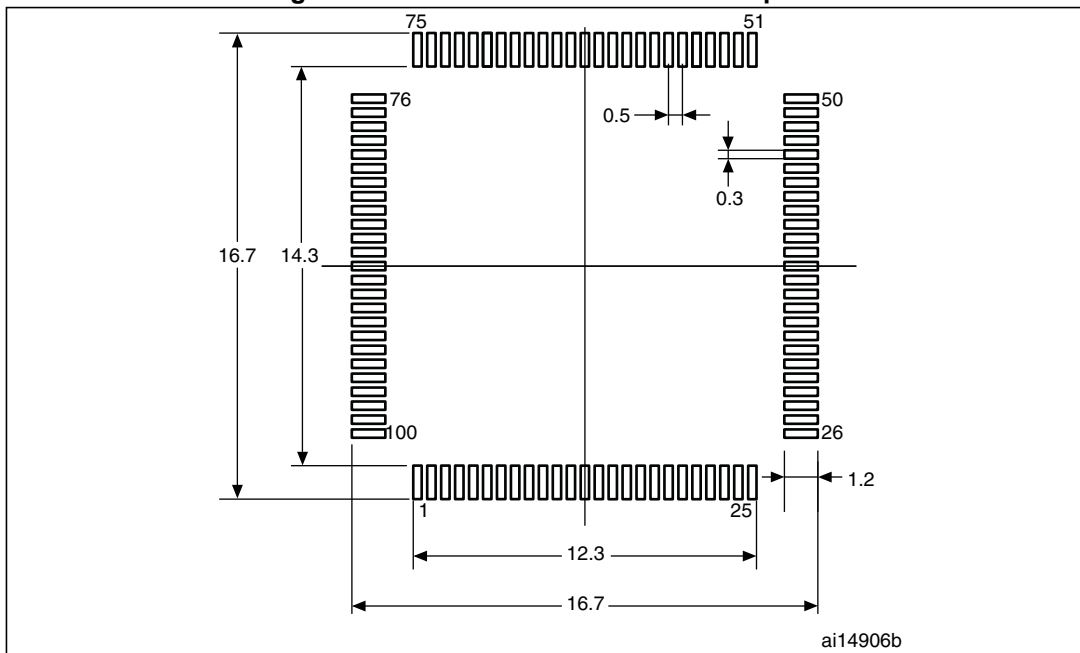
Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378

Table 73. LQFP100 – 14 x 14 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031
K	0°	3.5°	7°	0°	3.5°	7°

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 37. LQFP100 recommended footprint



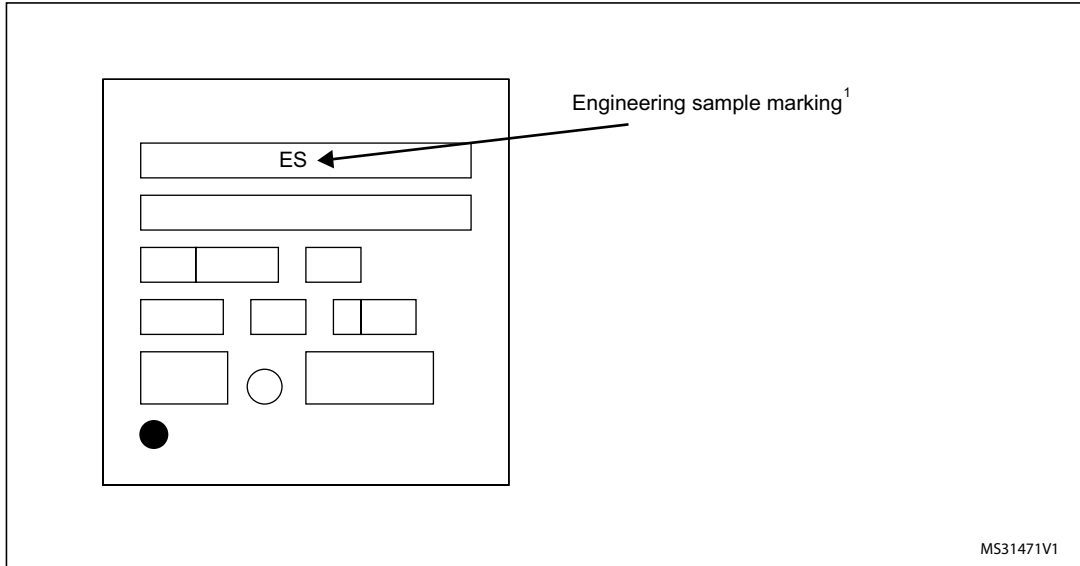
1. Dimensions are in millimeters.



### Marking of engineering samples for LQFP100

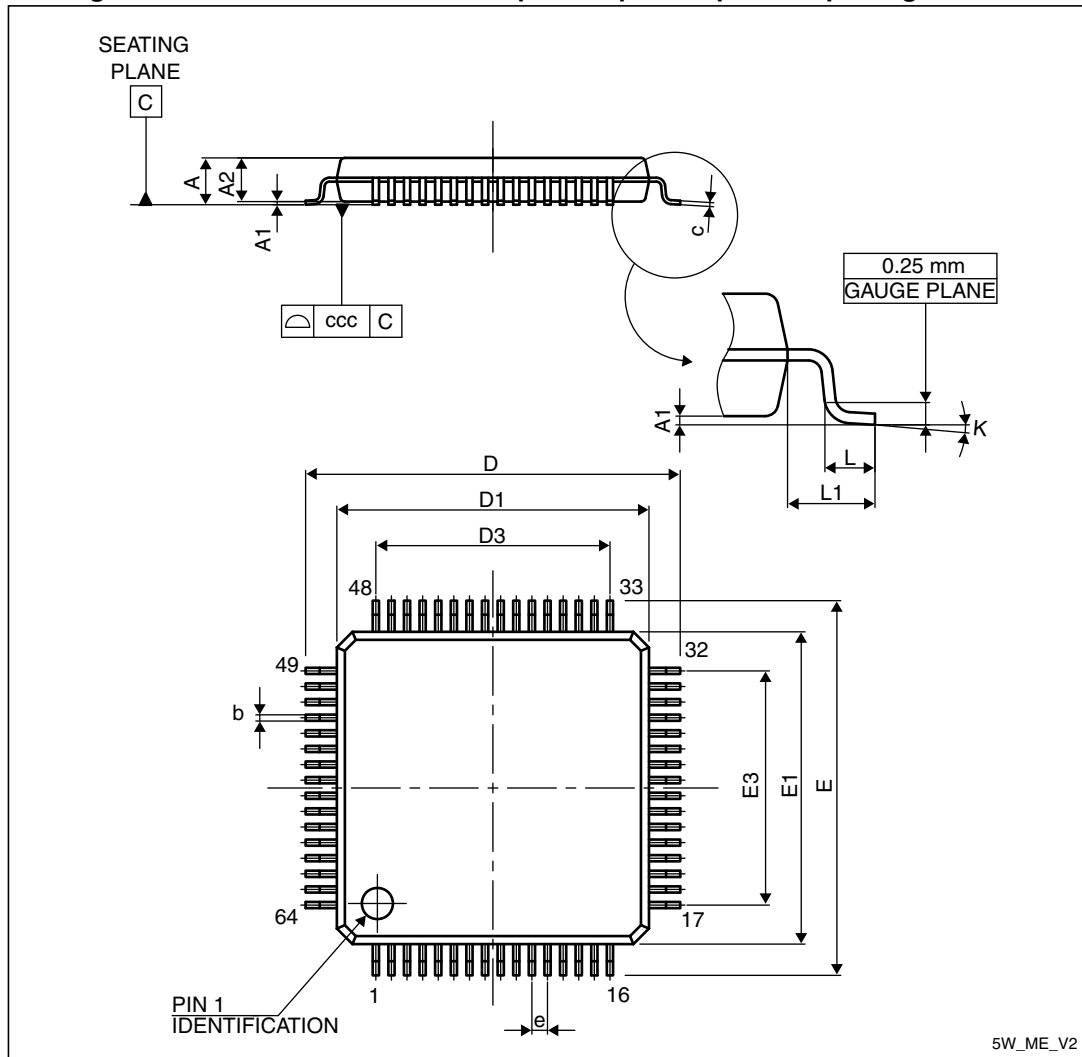
The following figure shows the engineering sample marking for the LQFP100 package. Only the information field containing the engineering sample marking is shown.

Figure 38. LQFP100 package top view



1. Samples marked "ES" are to be considered as "Engineering Samples": i.e. they are intended to be sent to customer for electrical compatibility evaluation and may be used to start customer qualification where specifically authorized by ST in writing. In no event ST will be liable for any customer usage in production. Only if ST has authorized in writing the customer qualification Engineering Samples can be used for reliability qualification trials.

Figure 39. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 74. LQFP64 – 10 x 10 mm low-profile quad flat package mechanical data

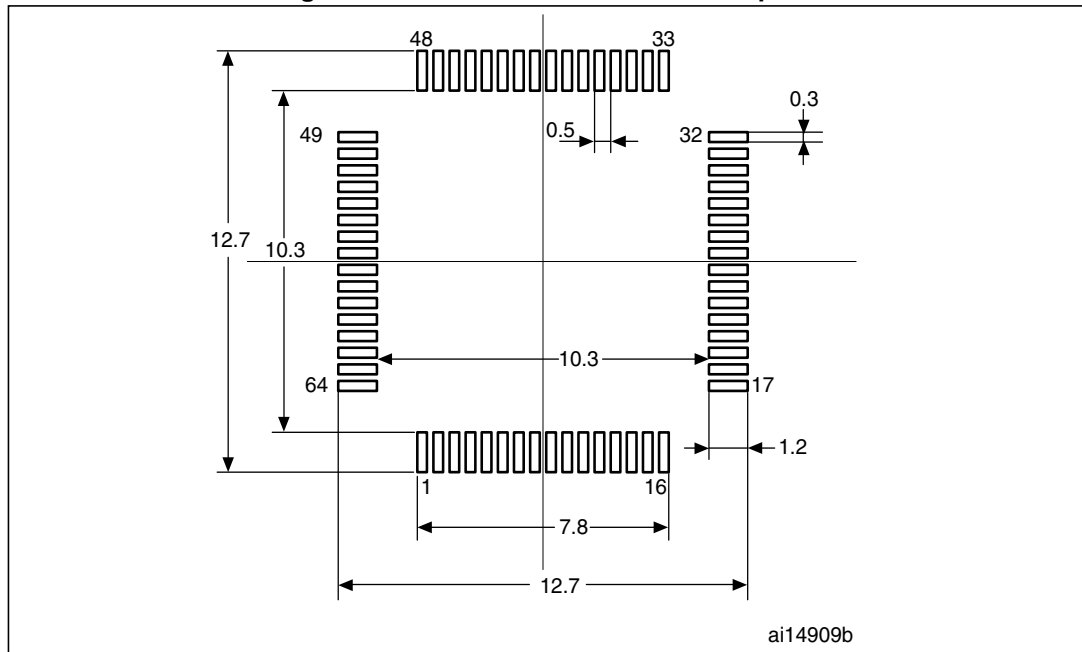
Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090		0.200	0.0035	-	0.0079
D	11.800	12.000	12.200	0.4646	0.4724	0.4803
D1	9.800	10.000	10.200	0.3858	0.3937	0.4016
D3	-	7.500	-	-	0.2953	-

Table 74. LQFP64 – 10 x 10 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
E	11.800	12.000	12.200	0.4646	0.4724	0.4803
E1	9.800	10.000	10.200	0.3858	0.3937	0.4016
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031
K	0°	3.5°	7°	0°	3.5°	7°

1. Values in inches are converted from mm and rounded to 4 decimal digits.

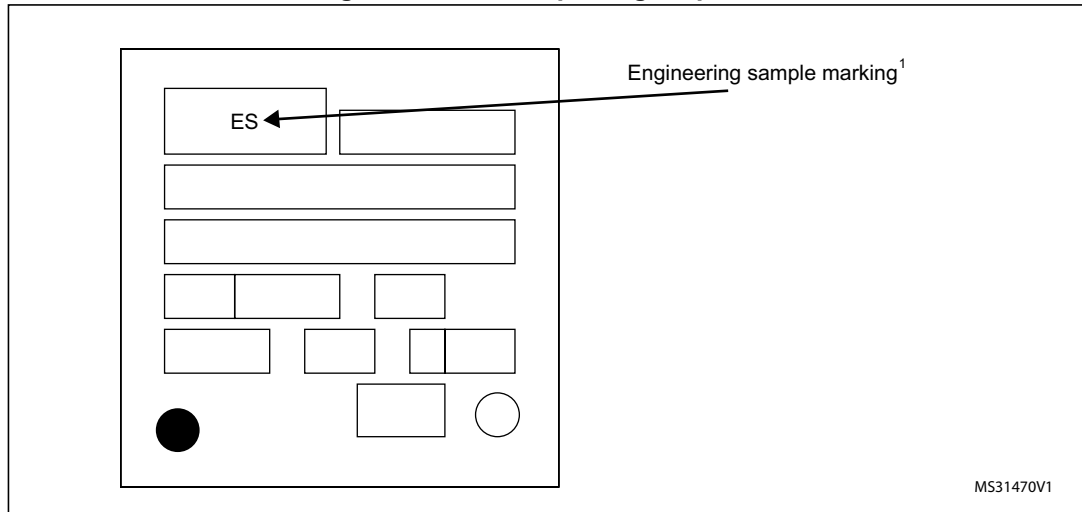
Figure 40. LQFP64 recommended footprint



1. Dimensions are in millimeters.

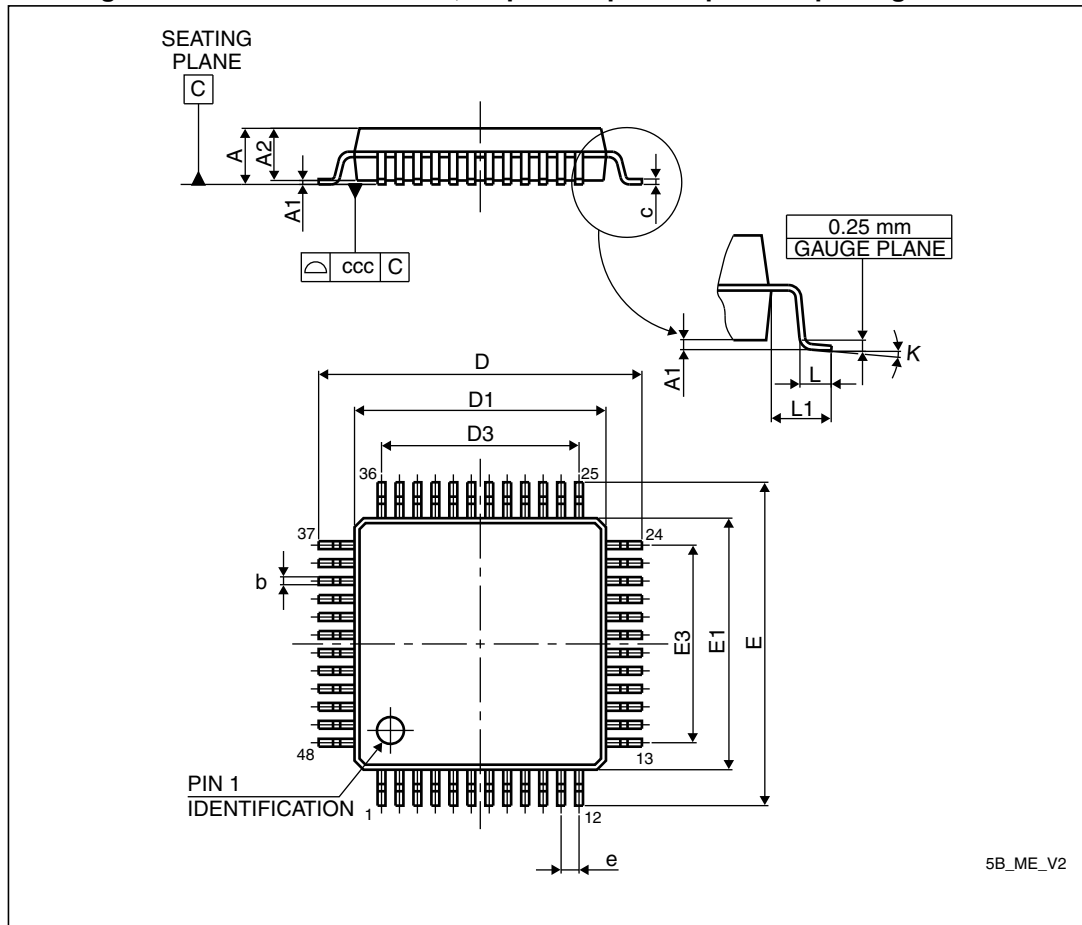
**Marking of engineering samples for LQFP64**

The following figure shows the engineering sample marking for the LQFP64 package. Only the information field containing the engineering sample marking is shown.

**Figure 41. LQFP64 package top view**

1. Samples marked "ES" are to be considered as "Engineering Samples": i.e. they are intended to be sent to customer for electrical compatibility evaluation and may be used to start customer qualification where specifically authorized by ST in writing. In no event ST will be liable for any customer usage in production. Only if ST has authorized in writing the customer qualification Engineering Samples can be used for reliability qualification trials.

Figure 42. LQFP48 – 7 x 7 mm, 48 pin low-profile quad flat package outline



5B\_ME\_V2

1. Drawing is not to scale.

Table 75. LQFP48 – 7 x 7 mm low-profile quad flat package mechanical data

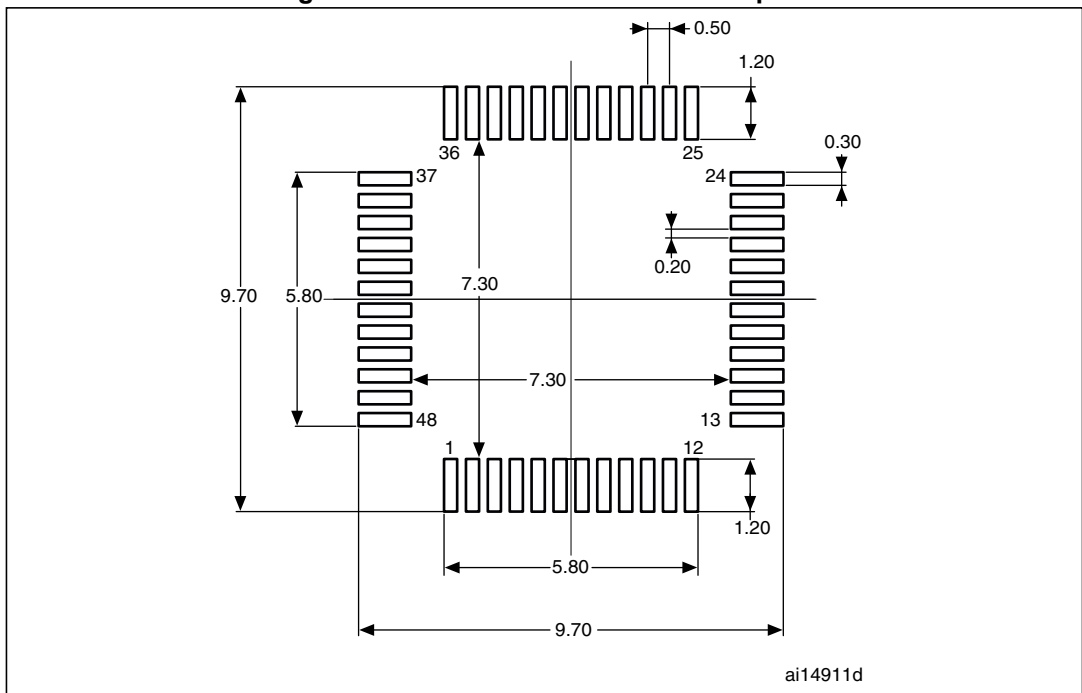
Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-

Table 75. LQFP48 – 7 x 7 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031
K	0°	3.5°	7°	0°	3.5°	7°

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 43. LQFP48 recommended footprint

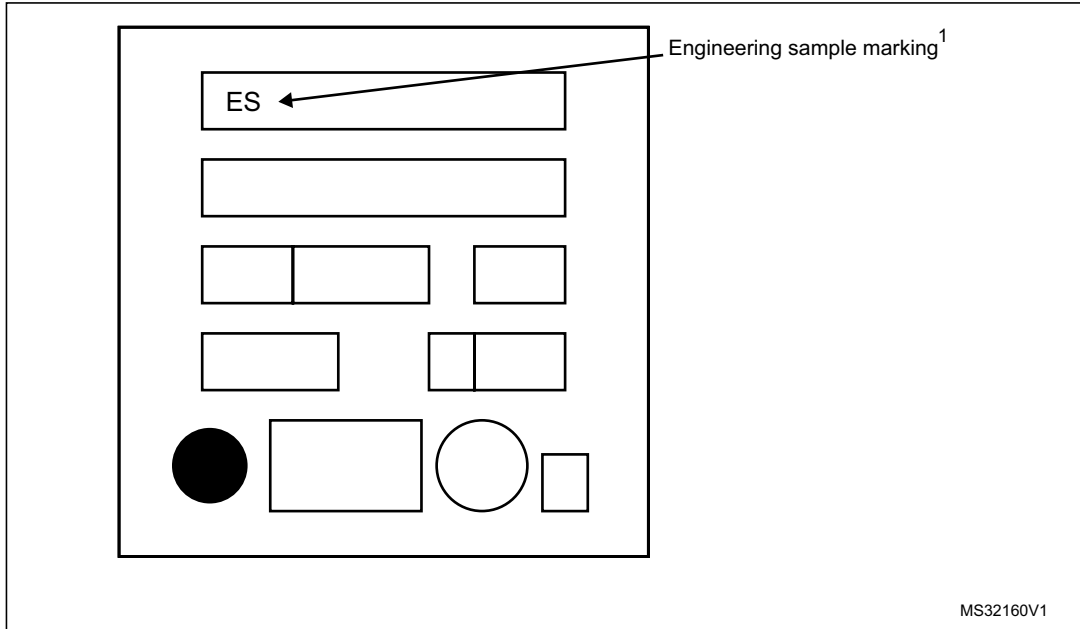


1. Dimensions are in millimeters.

**Marking of engineering samples for LQFP48**

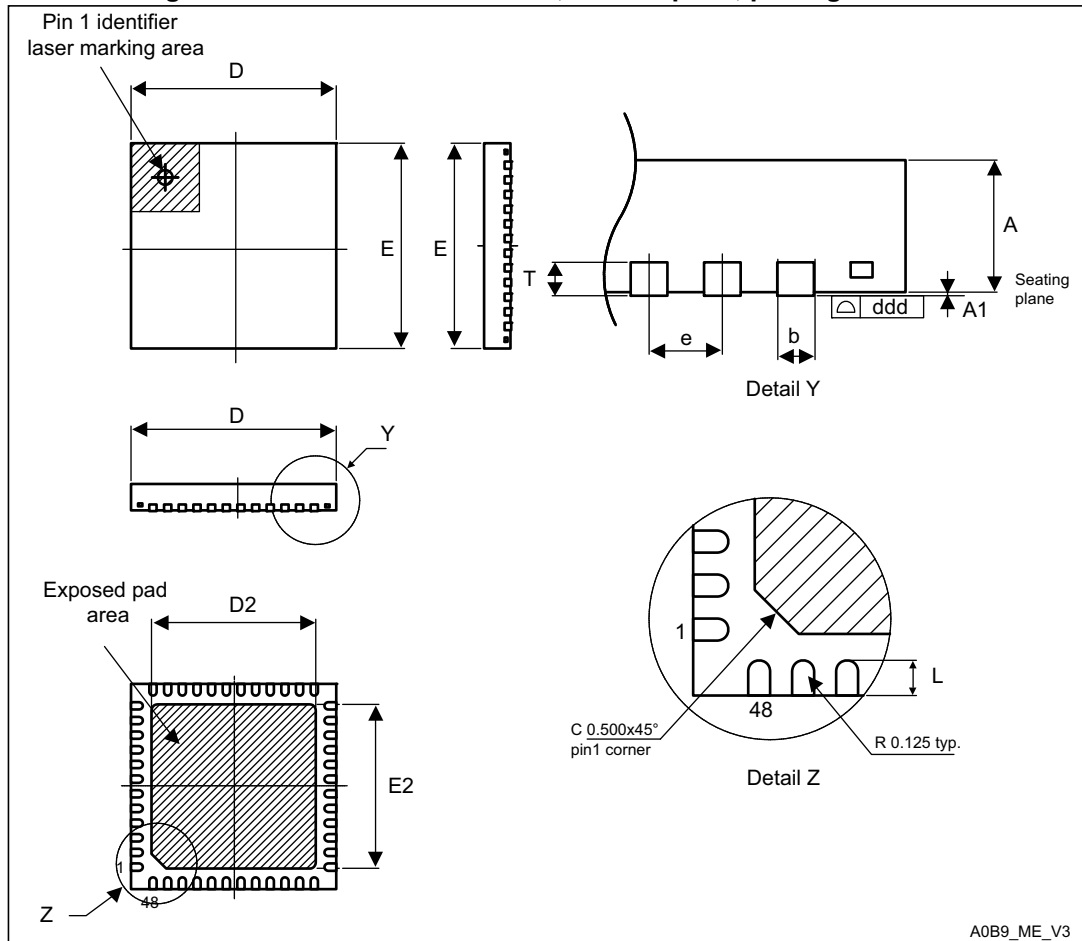
The following figure shows the engineering sample marking for the LQFP48 package. Only the information field containing the engineering sample marking is shown.

**Figure 44. LQFP48 package top view**



1. Samples marked "ES" are to be considered as "Engineering Samples": i.e. they are intended to be sent to customer for electrical compatibility evaluation and may be used to start customer qualification where specifically authorized by ST in writing. In no event ST will be liable for any customer usage in production. Only if ST has authorized in writing the customer qualification Engineering Samples can be used for reliability qualification trials.

Figure 45. UFQFPN48 – 7 x 7 mm, 0.5 mm pitch, package outline



A0B9\_ME\_V3

1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

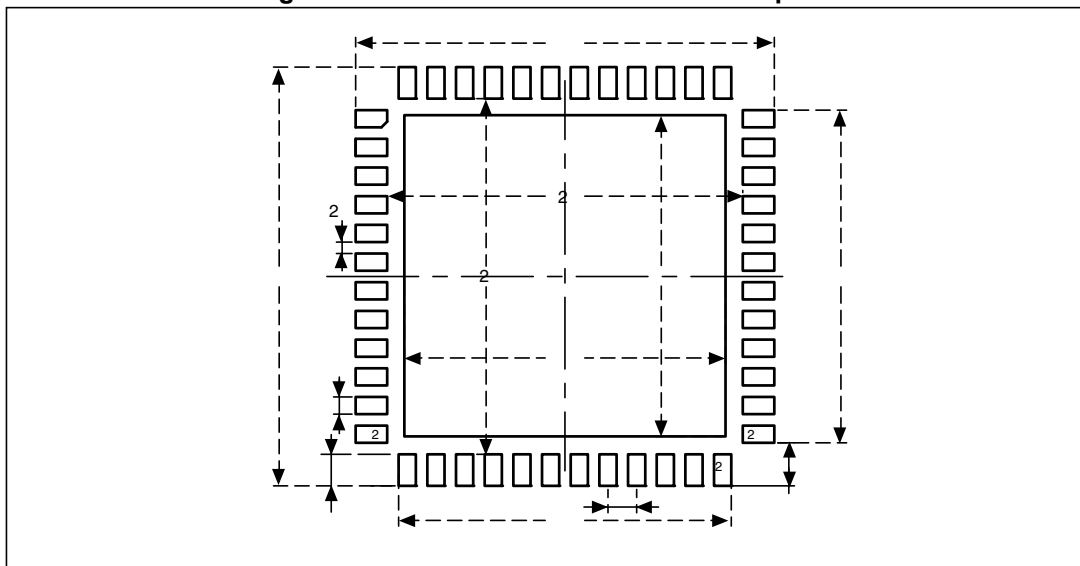


Table 76. UFQFPN48 – 7 x 7 mm, 0.5 mm pitch, package mechanical data

Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.

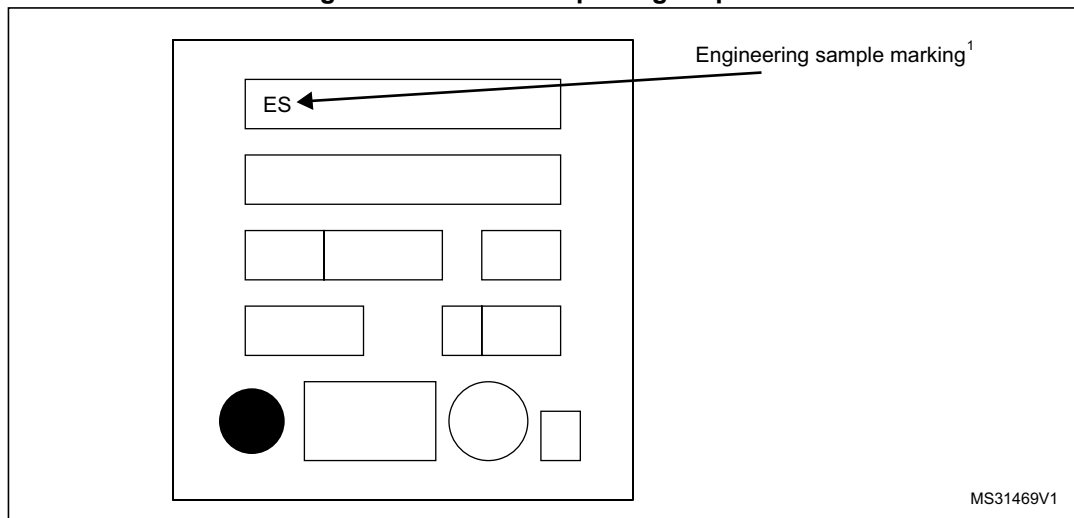
Figure 46. UFQFPN48 recommended footprint



1. Dimensions are in millimeters.

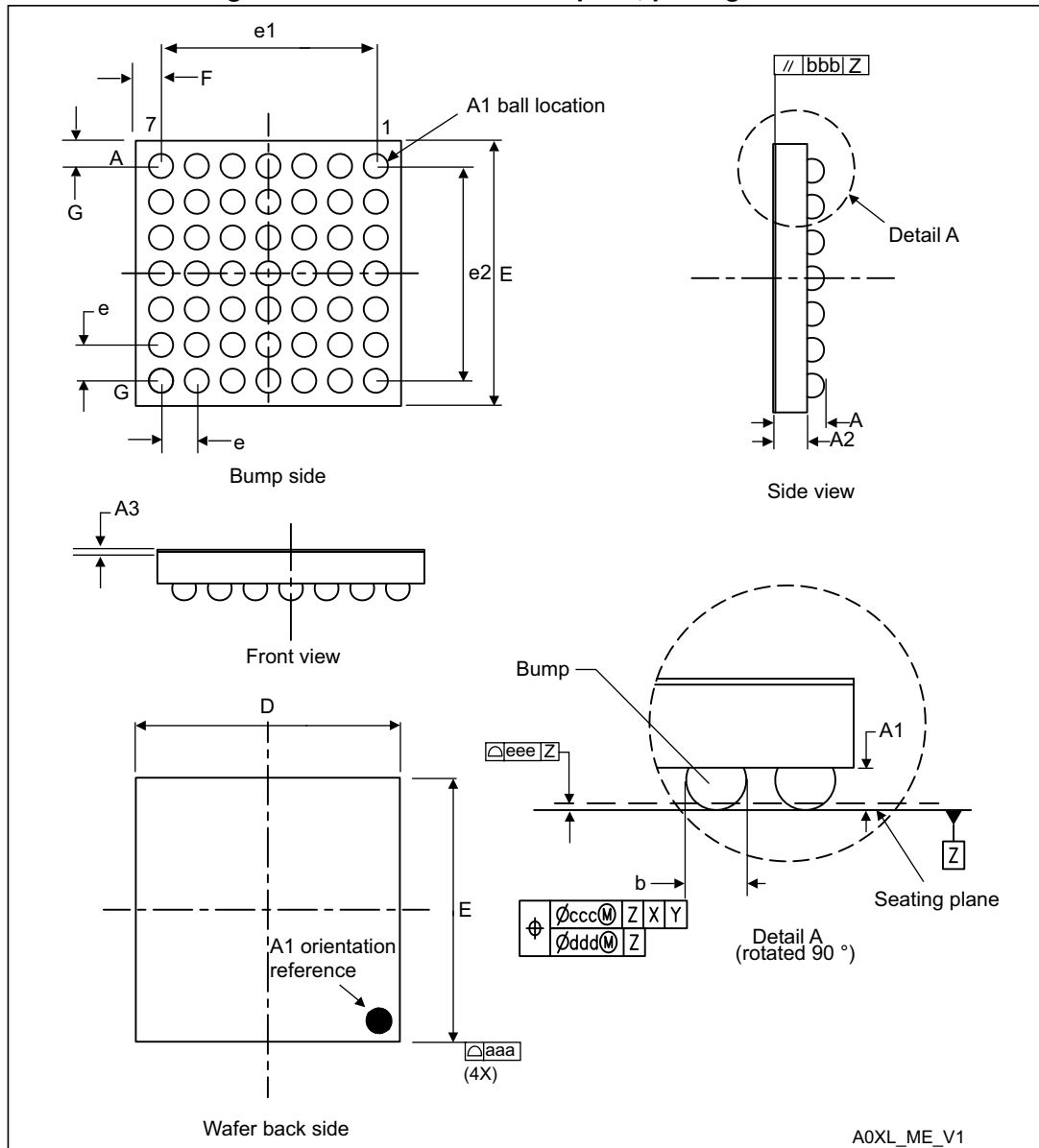
**Marking of engineering samples for UFQFPN48**

The following figure shows the engineering sample marking for the UFQFPN48 package. Only the information field containing the engineering sample marking is shown.

**Figure 47. UFQFPN48 package top view**

1. Samples marked "ES" are to be considered as "Engineering Samples": i.e. they are intended to be sent to customer for electrical compatibility evaluation and may be used to start customer qualification where specifically authorized by ST in writing. In no event ST will be liable for any customer usage in production. Only if ST has authorized in writing the customer qualification Engineering Samples can be used for reliability qualification trials.

Figure 48. WLCSP49 – 0.4 mm pitch, package outline



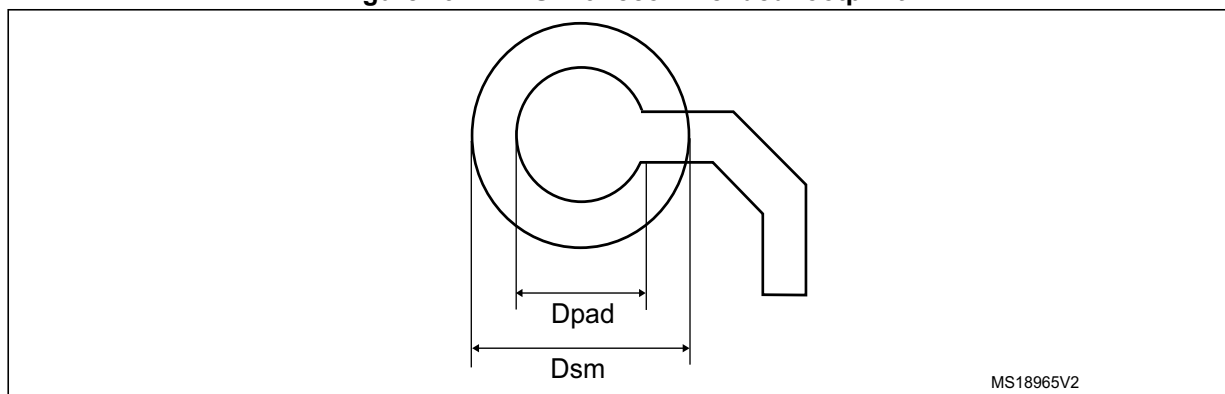
1. Drawing is not to scale.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z

Table 77. WLCSP49 – 0.4 mm pitch package mechanical data

Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.175	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3	-	0.025	-	-	0.0010	-
b	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	3.242	3.277	3.312	0.1276	0.1290	0.1304
E	3.074	3.109	3.144	0.1210	0.1224	0.1238
e	-	0.400	-	-	0.0157	-
e1	-	2.400	-	-	0.0945	-
e2	-	2.400	-	-	0.0945	-
F	-	0.438	-	-	0.0173	-
G	-	0.354	-	-	0.0140	-
N	49					
aaa	-	0.100	-	-	0.0039	-
bbb	-	0.100	-	-	0.0039	-
ccc	-	0.100	-	-	0.0039	-
ddd	-	0.050	-	-	0.0020	-
eee	-	0.050	-	-	0.0020	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 49. WLCSP49 recommended footprint



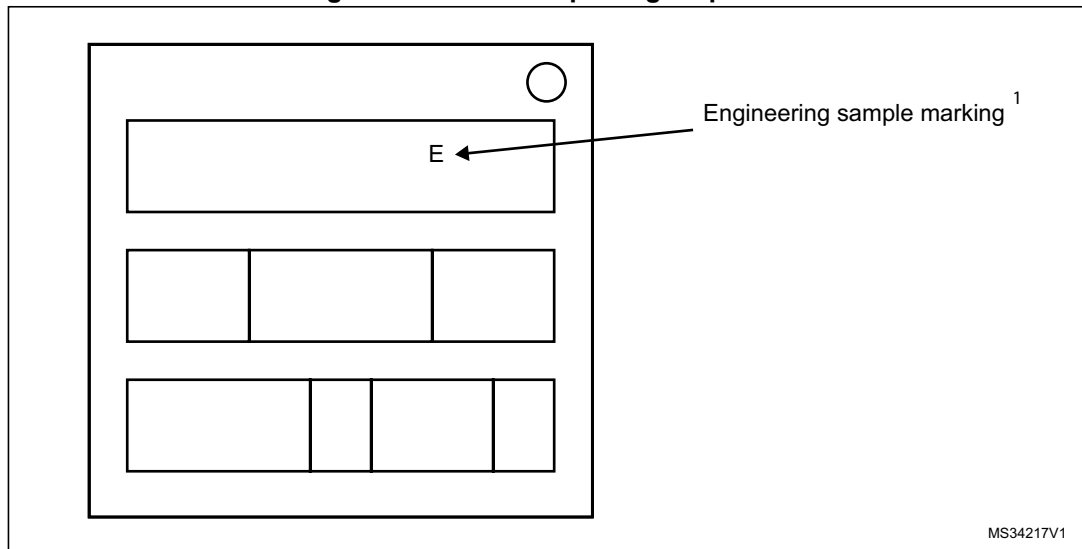
**Table 78. WLCSP49 recommended PCB design rules (0.4 mm pitch BGA)**

Dimension	Recommended values
Pitch	0.4 mm
Dpad	260 µm max. (circular) 220 µm recommended
Dsm	300 µm min. (for 260 µm diameter pad)
PCB pad design	Non-solder mask defined via underbump allowed

**Marking of engineering samples for WLCSP49**

The following figure shows the engineering sample marking for the WLCSP49 package. Only the information field containing the engineering sample marking is shown.

**Figure 50. WLCSP49 package top view**



1. Samples marked "E" are to be considered as "Engineering Samples": i.e. they are intended to be sent to customer for electrical compatibility evaluation and may be used to start customer qualification where specifically authorized by ST in writing. In no event ST will be liable for any customer usage in production. Only if ST has authorized in writing the customer qualification Engineering Samples can be used for reliability qualification trials.

## 7.2 Thermal characteristics

The maximum chip junction temperature ( $T_{Jmax}$ ) must never exceed the values given in [Table 24: General operating conditions](#).

The maximum chip-junction temperature,  $T_J$  max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- $T_A$  max is the maximum temperature in °C,
- $\Theta_{JA}$  is the package junction-to- thermal resistance, in °C/W,
- $P_D$  max is the sum of  $P_{INT}$  max and  $P_{I/O}$  max ( $P_D$  max =  $P_{INT}$  max +  $P_{I/O}$ max),
- $P_{INT}$  max is the product of  $I_{DD}$  and  $V_{DD}$ , expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$  max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual  $V_{OL} / I_{OL}$  and  $V_{OH} / I_{OH}$  of the I/Os at low and high level in the application.

**Table 79. Package thermal characteristics**

Symbol	Parameter	Value	Unit
$\Theta_{JA}$	Thermal resistance junction- UFBGA100 - 7 × 7 mm	55	°C/W
	Thermal resistance junction- LQFP100 - 14 × 14 mm	42	
	Thermal resistance junction- LQFP64 - 10 × 10 mm / 0.5 mm pitch	44	
	Thermal resistance junction- LQFP48 - 7 × 7 mm	54	
	Thermal resistance junction- UFQFPN48 - 7 × 7 mm	32	
	Thermal resistance junction- WLCSP49 - 0.4 mm pitch	49	

### 7.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from [www.jedec.org](http://www.jedec.org)

### 7.2.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in [Section 8: Part numbering](#).

Each temperature range suffix corresponds to a specific guaranteed temperature at maximum dissipation and to a specific maximum junction temperature.

As applications do not commonly use the STM32F071xx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range is best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

### Example 1: High-performance application

Assuming the following application conditions:

Maximum temperature  $T_{Amax} = 82\text{ °C}$  (measured according to JESD51-2),  $I_{DDmax} = 50\text{ mA}$ ,  $V_{DD} = 3.5\text{ V}$ , maximum 20 I/Os used at the same time in output at low level with  $I_{OL} = 8\text{ mA}$ ,  $V_{OL} = 0.4\text{ V}$  and maximum 8 I/Os used at the same time in output at low level with  $I_{OL} = 20\text{ mA}$ ,  $V_{OL} = 1.3\text{ V}$

$$P_{INTmax} = 50\text{ mA} \times 3.5\text{ V} = 175\text{ mW}$$

$$P_{IOmax} = 20 \times 8\text{ mA} \times 0.4\text{ V} + 8 \times 20\text{ mA} \times 1.3\text{ V} = 272\text{ mW}$$

This gives:  $P_{INTmax} = 175\text{ mW}$  and  $P_{IOmax} = 272\text{ mW}$ :

$$P_{Dmax} = 175 + 272 = 447\text{ mW}$$

Using the values obtained in [Table 79](#)  $T_{Jmax}$  is calculated as follows:

– For LQFP64,  $45\text{ °C/W}$

$$T_{Jmax} = 82\text{ °C} + (45\text{ °C/W} \times 447\text{ mW}) = 82\text{ °C} + 20.115\text{ °C} = 102.115\text{ °C}$$

This is within the range of the suffix 6 version parts ( $-40 < T_J < 105\text{ °C}$ ).

In this case, parts must be ordered at least with the temperature range suffix 6 (see [Section 8: Part numbering](#)).

*Note:* With this given  $P_{Dmax}$  we can find the  $T_{Amax}$  allowed for a given device temperature range (order code suffix 6 or 7).

$$\text{Suffix 6: } T_{Amax} = T_{Jmax} - (45\text{ °C/W} \times 447\text{ mW}) = 105 - 20.115 = 84.885\text{ °C}$$

$$\text{Suffix 7: } T_{Amax} = T_{Jmax} - (45\text{ °C/W} \times 447\text{ mW}) = 125 - 20.115 = 104.885\text{ °C}$$

### Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high temperatures with a low dissipation, as long as junction temperature  $T_J$  remains within the specified range.

Assuming the following application conditions:

Maximum temperature  $T_{Amax} = 100\text{ °C}$  (measured according to JESD51-2),  $I_{DDmax} = 20\text{ mA}$ ,  $V_{DD} = 3.5\text{ V}$ , maximum 20 I/Os used at the same time in output at low level with  $I_{OL} = 8\text{ mA}$ ,  $V_{OL} = 0.4\text{ V}$

$$P_{INTmax} = 20\text{ mA} \times 3.5\text{ V} = 70\text{ mW}$$

$$P_{IOmax} = 20 \times 8\text{ mA} \times 0.4\text{ V} = 64\text{ mW}$$

This gives:  $P_{INTmax} = 70\text{ mW}$  and  $P_{IOmax} = 64\text{ mW}$ :

$$P_{Dmax} = 70 + 64 = 134\text{ mW}$$

Thus:  $P_{Dmax} = 134\text{ mW}$

Using the values obtained in [Table 79](#)  $T_{Jmax}$  is calculated as follows:

– For LQFP64,  $45\text{ °C/W}$

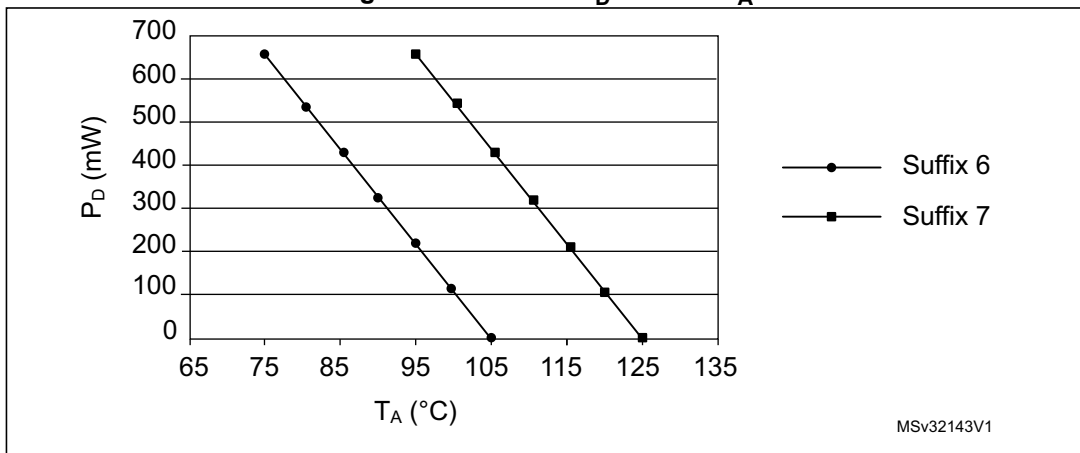
$$T_{Jmax} = 100\text{ °C} + (45\text{ °C/W} \times 134\text{ mW}) = 100\text{ °C} + 6.03\text{ °C} = 106.03\text{ °C}$$

This is above the range of the suffix 6 version parts ( $-40 < T_J < 105\text{ }^\circ\text{C}$ ).

In this case, parts must be ordered at least with the temperature range suffix 7 (see [Section 8: Part numbering](#)) unless we reduce the power dissipation in order to be able to use suffix 6 parts.

Refer to [Figure 51](#) to select the required temperature range (suffix 6 or 7) according to your temperature or power requirements.

Figure 51. LQFP64  $P_D$  max vs.  $T_A$





## 8 Part numbering

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

**Table 80. Ordering information scheme**

Example:	STM32	F	071	R	B	T	6	x
<b>Device family</b> STM32 = ARM-based 32-bit microcontroller								
<b>Product type</b> F = General-purpose								
<b>Sub-family</b> 071 = STM32F071xx								
<b>Pin count</b> C = 48/49 pins R = 64 pins V = 100 pins								
<b>Code size</b> 8 = 64 Kbytes of Flash memory B = 128 Kbytes of Flash memory								
<b>Package</b> H = UFBGA T = LQFP U = UFQFPN Y = WLCSP								
<b>Temperature range</b> 6 = -40 to 85 °C 7 = -40 to 105 °C								
<b>Options</b> xxx = programmed parts TR = tape and reel								

## 9 Revision history

**Table 81. Document revision history**

Date	Revision	Changes
13-Jan-2014	1	Initial draft
21-Feb-2014	2	<p>Added part number STM32F071V8.</p> <p>Changed status of document from “Preliminary data” to “Production data”.</p> <p>Updated “Reset and power management” data in <i>Features</i>.</p> <p>Updated <math>t_{S\_vrefint}</math> in <i>Table 28: Embedded internal reference voltage</i>.</p> <p>Updated <math>V_{HSEH}</math> and <math>V_{HSEL}</math> in <i>Table 38: High-speed external user clock characteristics</i>.</p> <p>Updated <math>V_{LSEH}</math> and <math>V_{LSEL}</math> in <i>Table 39: Low-speed external user clock characteristics</i>.</p> <p>Updated <math>t_{S\_temp}</math> in <i>Table 63: TS characteristics</i>.</p> <p>Updated <math>t_{S\_vbat}</math> in <i>Table 64: VBAT monitoring characteristics</i>.</p> <p>Updated <i>I2C interface characteristics</i> section.</p> <p>Updated <i>Figure 35: UFBGA100 package top view</i> and <i>Figure 50: WLCSP49 package top view</i>.</p> <p>Modified value of <math>t_{s\_sc}</math> and removed row <math>V_{BG}</math> in <i>Table 62: Comparator characteristics</i>.</p>

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