19-4459; Rev 0; 2/09

EVALUATION KIT AVAILABLE

Overvoltage Protection with USB Charger Detection, LDO, and ESD Protection on D+/D-

MAX14529E/MAX14530E

General Description

The MAX14529E/MAX14530E are overvoltage-protection devices with USB charger detection, a low-dropout (LDO) regulator, and ESD protection. These devices feature a low 35mΩ (typ) R_{ON} internal FET switch and protect low-voltage systems against voltage faults up to 28V. When the input voltage exceeds the overvoltage threshold, the internal FET switch is turned off to prevent damage to the protected components.

The charger detection detects a short between the USB D+ and D- data lines. If the data lines are shorted together and a dedicated charger is attached, the phone draws more than 500mA to charge the battery.

The overvoltage thresholds (OVLO) are preset to 5.75V (MAX14529E) or 6.8V (MAX14530E).

The LDO output (LOUT) is powered from OUT and supplies 3.3V to the USB transceiver. The LDO features a 100mA (min) current capability and low output noise.

The MAX14529E/MAX14530E feature ±15kV HBM ESD protection with low (3pF) capacitance suitable for Hi-Speed USB 2.0.

Both devices are offered in a small 12-bump, 1.5mm x 2mm WLP package and operate over the -40°C to +85°C extended temperature range.

Applications

Cell Phones

MP3 Players

PDAs and Palmtop Devices

Features

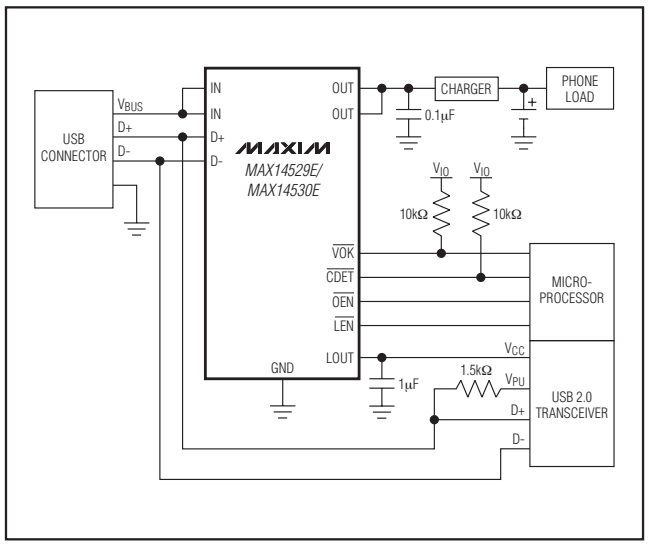
- **Input Voltage Protection Up to 28V**
- **High-Current USB Charger Detection**
- **3.3V, 100mA LDO**
- **Preset Overvoltage Protection Trip Level**
  - **5.75V (MAX14529E)**
  - **6.8V (MAX14530E)**
- **Integrated Low R_{ON} 35mΩ (typ) FET Switch**
- **Low-Capacitance USB High-Speed Data Line ESD Protection (3pF)**
  - **±15kV Human Body Model (HBM)**
  - **±15kV IEC 61000-4-2 Air Gap**
  - **±8kV IEC 61000-4-2 Contact**
- **Thermal-Shutdown Protection**
- **12-Bump, 1.5mm x 2mm WLP Package**
- **-40°C to +85°C Operating Temperature Range**

Ordering Information/ Selector Guide

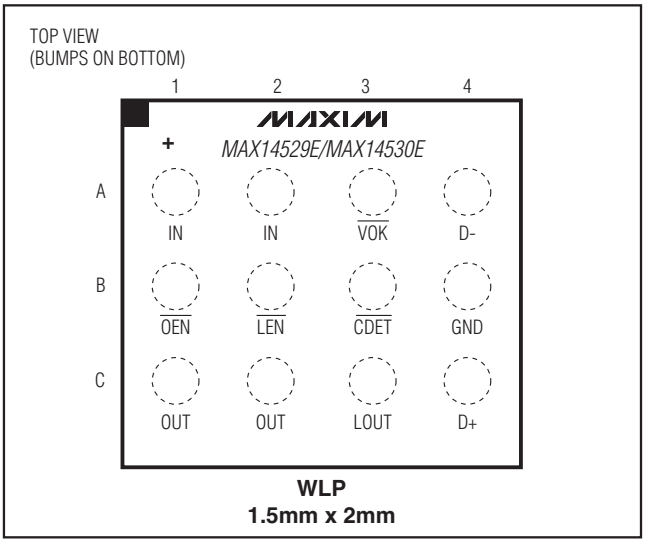
PART	PIN-PACKAGE	TOP MARK	OVLO (V)
MAX14529EEWC+T	12 WLP	AAP	5.75
MAX14530EEWC+T	12 WLP	AAQ	6.8

Note: *Both devices are specified over the -40°C to +85°C operating temperature range.*
+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Typical Operating Circuit



Pin Configuration



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Overvoltage Protection with USB Charger Detection, LDO, and ESD Protection on D+/D-

ABSOLUTE MAXIMUM RATINGS

IN to GND .....-0.3V to +30V
OUT to GND .....-0.3V to min (+12V, IN + 0.3V)
$\overline{OEN}$, $\overline{LEN}$, $\overline{VOK}$, $\overline{CDET}$ to GND .....-0.3V to +6V
LOUT to GND .....-0.3V to +6V
Continuous Current IN to OUT per Ball.....1.74A
Continuous Power Dissipation (T_A = +70°C)
12-Bump WLP (derate 8.5mW/°C above +70°C).....678mW
Junction-to-Ambient Thermal Resistance (θ_{JA})
(Note 1) .....118°C/W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....-40°C to +150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, go to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 2.2V to 28V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{IN} = +5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OVERVOLTAGE PROTECTION							
Input-Voltage Range	V_{IN}			2.2		28	V
Overvoltage Trip Level	V_{OVLO}	V_{IN} rising	MAX14529E	5.6	5.75	5.9	V
			MAX14530E	6.6	6.8	6.94	
		V_{IN} falling	MAX14529E	5.4			
			MAX14530E	6.5			
IN Overvoltage Lockout Hysteresis					1		%
Supply Current	I_{IN}	$V_{\overline{OEN}}$ = 0, $V_{\overline{LEN}}$ = 5V, 2.2V < V_{IN} < V_{OVLO}			95	190	µA
		$V_{\overline{OEN}}$ = $V_{\overline{LEN}}$ = 0, 2.2V < V_{IN} < V_{OVLO}			145	300	
		$V_{\overline{OEN}}$ = $V_{\overline{LEN}}$ = 5V, 2.2V < V_{IN} < V_{OVLO}			50	120	
Internal FET R_{ON}	R_{ON}	I_{LOAD} = 100mA, V_{IN} = 4.5V to 5.5V			35	60	mΩ
Maximum Capacitor on OUT	C_{OUTMAX}					1000	µF
LOW-DROPOUT REGULATOR							
LDO Output Voltage	V_{LOUT}	V_{IN} = 5V		3.219	3.3	3.383	V
LOUT Line Regulation		V_{IN} = 4.2V to 6V			1.65	3.3	mV/V
LOUT Load Regulation		I_{OUT} = 0.1mA to 100mA			0.33	0.66	mV/mA
Current Limit				100		400	mA
Dropout Voltage		I_{OUT} = 50mA (Note 3)			300	500	mV
LOUT Noise		f = 10kHz to 100kHz, I_{OUT} = 1mA			355		$µV_{RMS}$
$\overline{CDET}$ FILTER							
Cutoff Frequency	f_{FILT}				0.6		kHz
D- Rising DC Threshold	$V_{THFILT,R}$			2.375	2.5	2.625	V
D- Falling DC Threshold	$V_{THFILT,F}$				2.35		V
DIGITAL SIGNALS							
Open-Drain Output Low Voltage	V_{OL}	I_{SINK} = 1mA				0.4	V
Open-Drain Leakage Current		$V_{\overline{OEN}}$ = $V_{\overline{LEN}}$ = 5V, $\overline{VOK}$ and $\overline{CDET}$ high impedance				1	µA
Input High Voltage	V_{IH}			1.4			V

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 2.2V to 28V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{IN} = 5V, T_A = +25°C.) (Note 2)

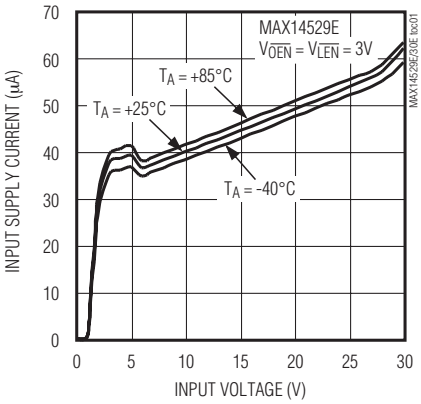
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}				0.4	V
Input Leakage Current		$V_{\overline{OEN}}$ = $V_{\overline{LEN}}$ = 5V	-1		+1	µA
TIMING CHARACTERISTICS (Figure 1)						
Debounce Time	t_{INDBC}	2.2V < V_{IN} < V_{OVLO} to V_{OUT} = 10% of V_{IN}		20		ms
Switch Turn-On Time	t_{ON}	2.2V < V_{IN} < V_{OVLO}, R_L = 100Ω, V_{OUT} = 10% to 80% of V_{IN}, C_L = 1mF		2		ms
Switch Turn-Off Time	t_{OFF}	V_{IN} > V_{OVLO} to V_{OUT} = 80% of V_{OVLO}, R_L = 10Ω		1.5	3.5	µs
THERMAL PROTECTION						
Thermal Shutdown		Low to high		150		°C
Thermal Hysteresis				20		°C
ESD PROTECTION						
D+ and D-		Human Body Model		±15		kV
		IEC 61000-4-2 Air Gap		±15		kV
		IEC 61000-4-2 Contact		±8		kV

Note 2: Devices are production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design.
Note 3: Dropout voltage is defined as V_{OUT} - V_{LOUT} when V_{LOUT} is at $V_{LOUT(min)}$.

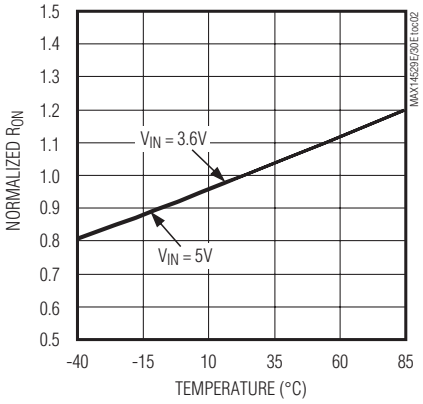
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

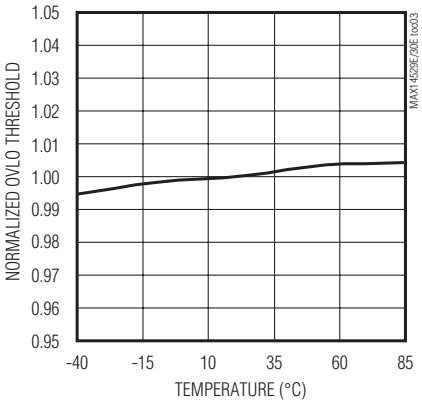
INPUT SUPPLY CURRENT vs. INPUT VOLTAGE



NORMALIZED R_{ON} vs. TEMPERATURE



NORMALIZED OVLO THRESHOLD vs. TEMPERATURE

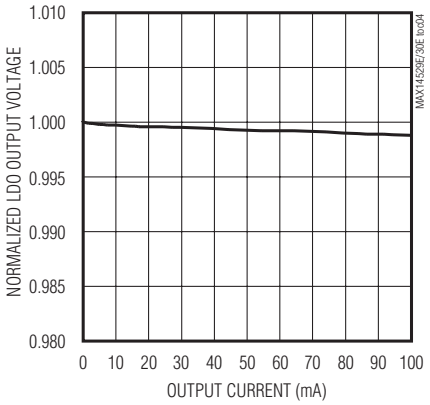


Overvoltage Protection with USB Charger Detection, LDO, and ESD Protection on D+/D-

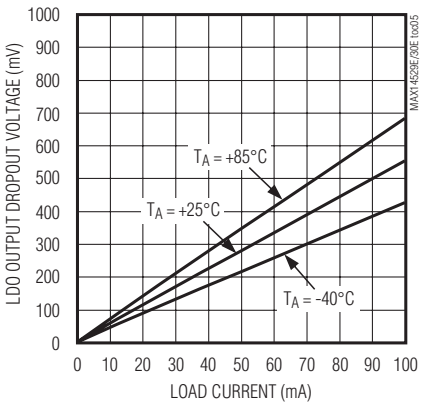
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

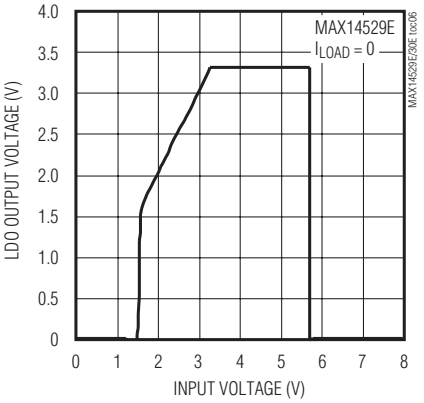
NORMALIZED LDO OUTPUT VOLTAGE vs. OUTPUT CURRENT



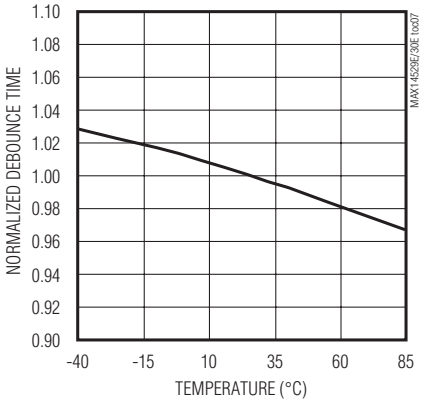
LDO OUTPUT DROPOUT VOLTAGE vs. LOAD CURRENT



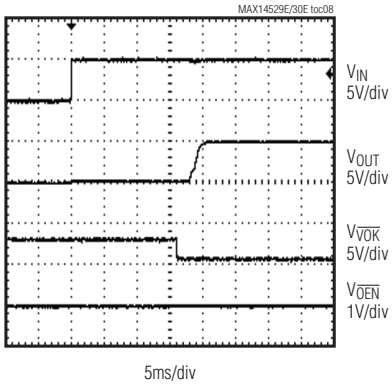
LDO OUTPUT VOLTAGE vs. INPUT VOLTAGE



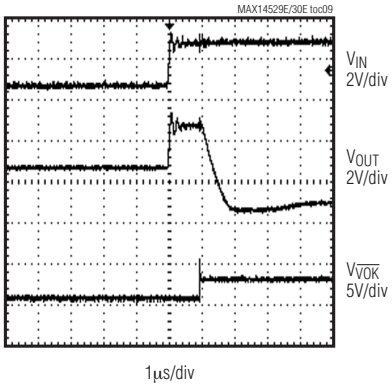
NORMALIZED DEBOUNCE TIME vs. TEMPERATURE



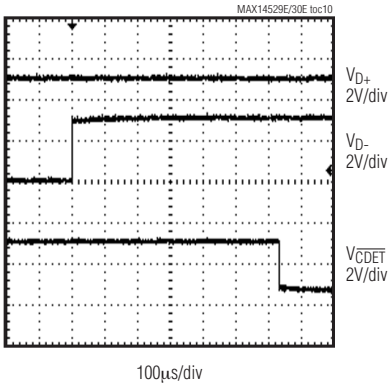
POWER-UP RESPONSE



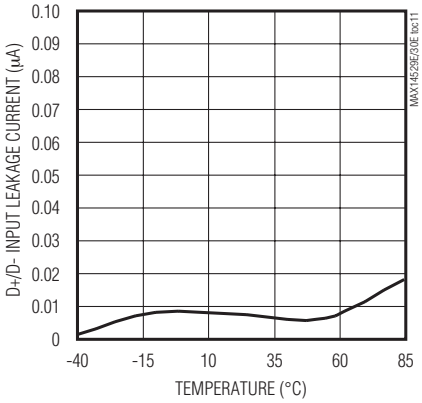
OVERVOLTAGE FAULT RESPONSE



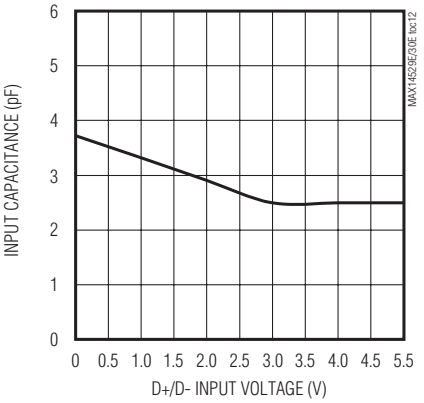
$\overline{CDET}$ RESPONSE



D+/D- INPUT LEAKAGE CURRENT vs. TEMPERATURE



INPUT CAPACITANCE vs. D+/D- INPUT VOLTAGE



Pin Description

PIN	NAME	FUNCTION
A1, A2	IN	Overvoltage-Protection Input. Bypass IN with a 1µF ceramic capacitor as close as possible to the device to obtain ±15kV HBM ESD protection. No capacitor required to obtain ±2kV HBM ESD protection.
A3	$\overline{VOK}$	Voltage Input Good Open-Drain Output. $\overline{VOK}$ is low impedance when $\overline{OEN}$ is driven low after the debounce time is expired (2.2V < V_{IN} < V_{OVLO}).
A4	D-	USB Data Line with ESD Protection
B1	$\overline{OEN}$	Overvoltage Protection Active-Low Enable Input. Drive $\overline{OEN}$ high to disconnect OUT from IN.
B2	$\overline{LEN}$	Low-Dropout Active-Low Enable Input.
B3	$\overline{CDET}$	Charger Detection Open-Drain Output. $\overline{CDET}$ is low if D+ and D- are shorted.
B4	GND	Ground
C1, C2	OUT	Overvoltage Switch Output. Bypass OUT with a 0.1µF ceramic capacitor as close as possible to the device.
C3	LOUT	Low-Dropout Power Output. Bypass LOUT with a 1µF ceramic capacitor as close as possible to the device.
C4	D+	USB Data Line with ESD Protection

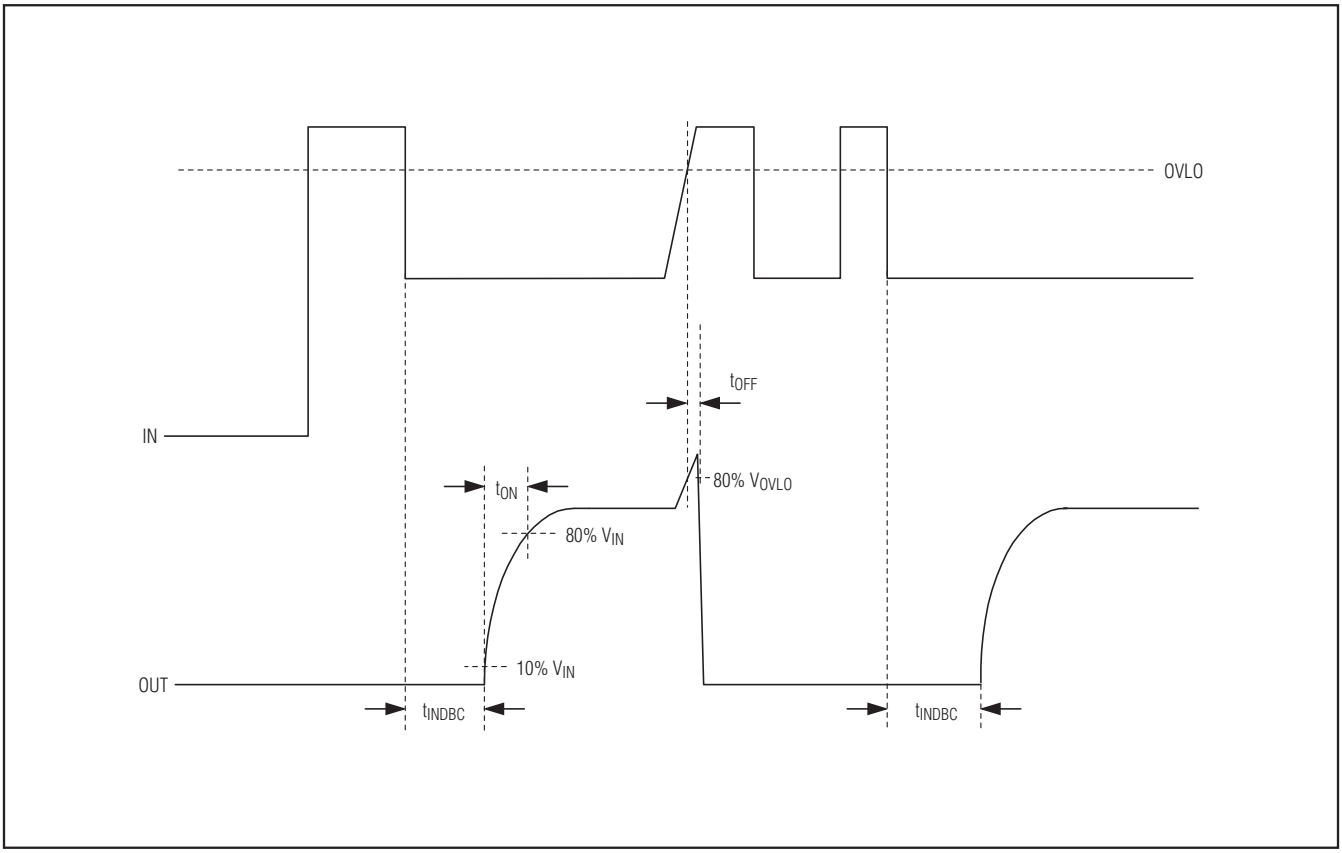


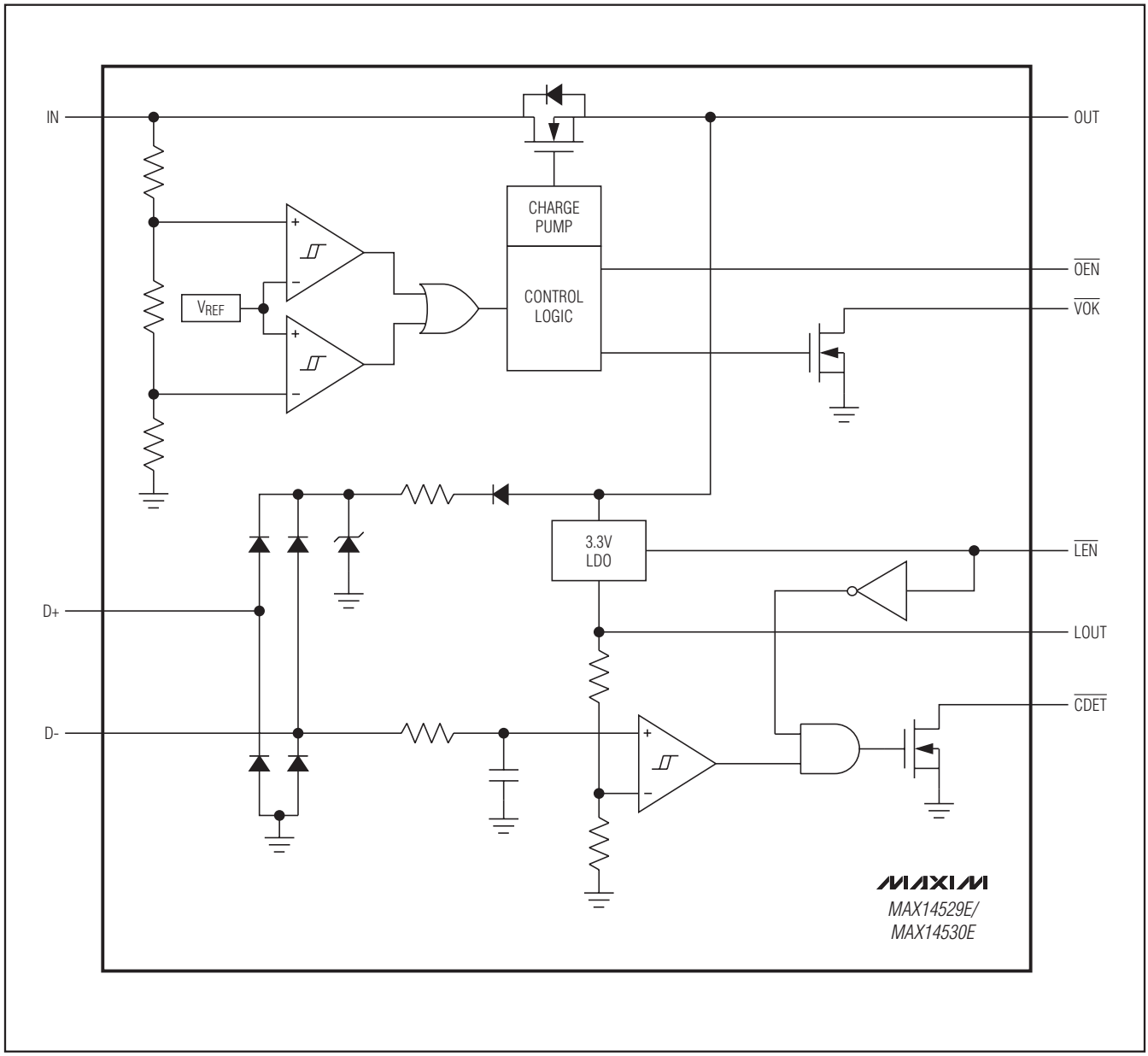
Figure 1. MAX14529E/MAX14530E Timing Diagram

Overvoltage Protection with USB Charger Detection, LDO, and ESD Protection on D+/D-

Detailed Description

The MAX14529E/MAX14530E are overvoltage-protection devices with USB charger detection, a low-dropout (LDO) regulator, and ESD protection. These devices feature a low R_{ON} internal FET switch and protect low-voltage systems against voltage faults up to 28V. When the input voltage exceeds the overvoltage threshold, the internal FET switch is turned off to prevent damage to the protected components. The 20ms debounce time prevents false turn-on of the internal FET switch during startup.

Functional Diagram



Device Operation

The MAX14529E/MAX14530E have an internal oscillator and charge pump that control the turn-on of the internal FET switch. The internal oscillator controls the timers that enable the turn-on of the charge pump and controls the state of the open-drain $\overline{VOK}$ output. If $V_{IN} > V_{OVLO}$, the internal oscillator remains off, thus disabling the charge pump. If $2.2V < V_{IN} < V_{OVLO}$, the internal charge pump is enabled. The charge-pump turns on the internal FET switch and asserts $\overline{VOK}$. At any time, if V_{IN} drops below 2.2V or rises above V_{OVLO}, $\overline{VOK}$ goes high and the charge pump is disabled, disconnecting OUT from IN.

Overvoltage Lockout (OVLO)

The MAX14529E has a 5.75V (typ) overvoltage threshold (OVLO), while the MAX14530E has a 6.8V (typ) OVLO.

Low Dropout

The low-dropout regulator (LOUT) is powered from input voltage and supplies 3.3V (typ) to the USB transceiver. If a lithium-ion (Li+) battery is used to power the USB transceiver, a boost converter is needed. The LDO features a minimum 100mA current capability and low output noise. Drive $\overline{LEN}$ high to disable the LDO.

Charger Detection

The charger detection detects if there is a short between the USB D+ and D- data lines. If the data lines are shorted together and a dedicated charger is attached, the phone draws more than 500mA to charge the battery; $\overline{CDET}$ asserts low. If the data lines are not biased properly, then an unidentified device is present and the phone draws no more than 500mA or does not charge at all, depending on its USB compliance level.

Thermal-Shutdown Protection

The MAX14529E/MAX14530E feature thermal-shutdown circuitry. The internal switch turns off when the junction temperature exceeds +150°C (typ) and immediately goes into a fault mode. The device exits thermal shutdown after the junction temperature cools by 20°C (typ).

Applications Information

IN Bypass Capacitor

Bypass IN to GND with a 1µF ceramic capacitor as close as possible to the device for ±15kV HBM ESD protection on IN. No capacitor required to obtain ±2kV HBM protection. If the power source has significant inductance due to long lead length, take care to prevent overshoots due to the LC tank circuit and provide protection.

ESD Test Conditions

ESD performance depends on a number of conditions. The MAX14529E/MAX14530E are specified for ±15kV HBM typical ESD protection on the D+, D-, and IN pins when IN is bypassed to ground with a 1µF ceramic capacitor.

Human Body Model

Figure 2 shows the Human Body Model, and Figure 3 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest that is then discharged into the device through a 1.5kΩ resistor.

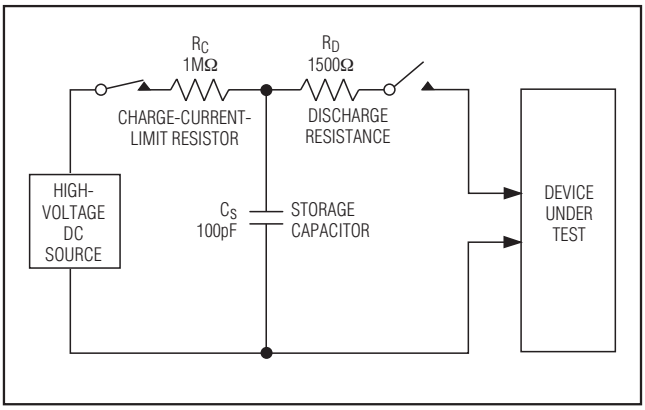


Figure 2. Human Body ESD Test Model

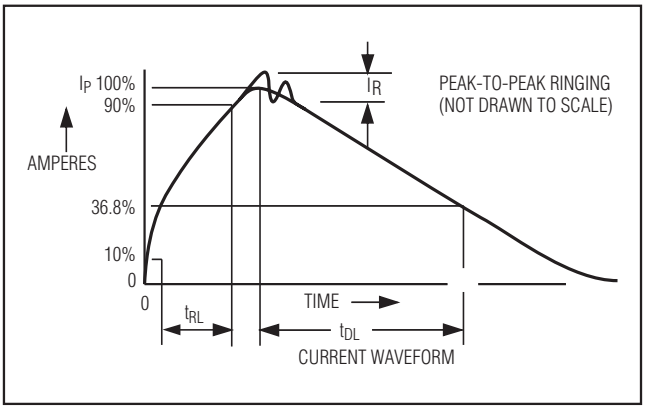


Figure 3. Human Body Current Waveform

Overvoltage Protection with USB Charger Detection, LDO, and ESD Protection on D+/D-

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. It does not specifically refer to integrated circuits. The MAX14529E/MAX14530E are specified for ±15kV Air-Gap Discharge and ±8kV Contact Discharge IEC 61000-4-2 on the D+ and D- pins.

The main difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2. Because series resistance is lower in the IEC 61000-4-2 ESD test model (Figure 4), the ESD-withstand voltage measured to this standard is generally lower than that measured using the Human Body Model. Figure 5 shows the current waveform for the ±8kV IEC 61000-4-2 Level 4 ESD Contact Discharge test. The Air-Gap Discharge test involves approaching the device with a charged probe. The Contact Discharge method connects the probe to the device before the probe is energized.

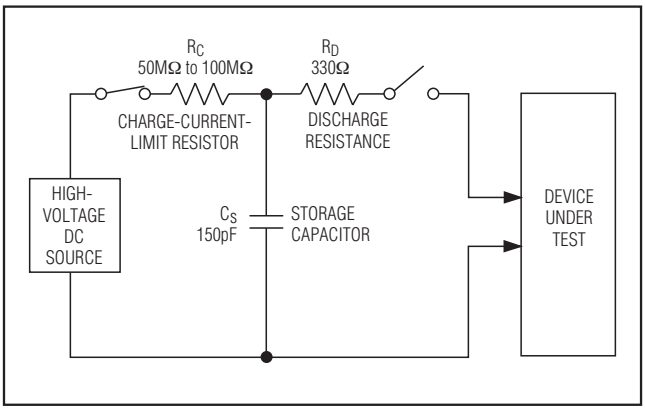


Figure 4. IEC 61000-4-2 ESD Test Model

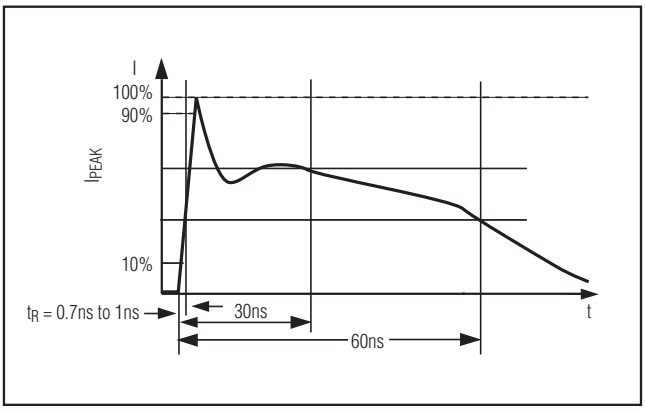


Figure 5. IEC 61000-4-2 ESD Generator Current Waveform

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
12 WLP	W121B2+1	21-0009

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