GGB LC75805PE

смов IC 1/1 to 1/4 Duty General-Purpose LCD Display Driver with LED Driver

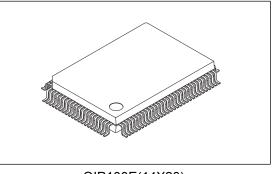


LC75805PE is the 1/1 to 1/4 duty general-purpose LCD display driver with the LED driver to use for the instrument panel display by control with the controller. In addition, LC75805PE is able to drive up to 48 LED and LCD of up to 140 segments directly, and has a built-in 7ch PWM function for brightness adjustment of LED. Furthermore, because of built-in the oscillator circuit, it is possible to reduce external resister and capacitor for oscillation.

Features

- Switch of Static Drive, 1/2 Duty Drive, 1/3 Duty Drive and 1/4 Duty Drive can be controlled by serial data.
 - Static Drive (1/1 Duty Drive) : Capable of driving up to 38 segments.
 - 1/2 Duty Drive
- Capable of driving up to 74 segments.Capable of driving up to 108 segments.
- 1/3 Duty Drive
- 1/4 Duty Drive : Capable of driving up to 140 segments.
- Frame frequency of common and segment output waveform can be controlled by serial data.
- Turning on/off LED can be controlled by serial data. (Capable of driving up to 48 LED)
- Built-in 7ch PWM function for brightness adjustment of LED. (Resolution of 128 steps)
- Frame frequency of LED driver output waveform can be controlled by serial data.
- Serial data input supports CCB format communication with the system controller. (Support 5V operation)
- Backup function and forced turning off all segments by power-saving mode can be controlled by serial data.
- Switch of the internal oscillator operating mode and the external clock operating mode can be controlled by serial data.
- High generality, since display data is displayed directly without the intervention of a decoder circuit.
- The $\overline{\text{INH}}$ pin allows the display to be forced to the off state.
- Built-in Oscillator circuit (Built-in resister and capacitor for oscillation)

• CCB is ON Semiconductor[®] 's original format. All addresses are managed by ON Semiconductor[®] for this format.



QIP100E(14X20)

• CCB is a registered trademark of Semiconductor Components Industries, LLC.

ORDERING INFORMATION

See detailed ordering and shipping information on page 34 of this data sheet.



Specifications

Absolute Maximum Ratings at $Ta = 25^{\circ}C$, $V_{SS} = 0V$

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------------|---------------------|-------------------------|------------------------------|------|
| Maximum supply voltage | V _{DD} max | V _{DD} | -0.3 to +6.5 | V |
| Input voltage | V _{IN} 1 | CE, CL, DI, INH, OSCI | -0.3 to +6.5 | V |
| Output voltage | V _{OUT} 1 | S1 to S38, COM1 to COM4 | -0.3 to V _{DD} +0.3 | |
| | V _{OUT} 2 | LD1 to LD48 | -0.3 to +35 | V |
| Output current | IOUT1 | S1 to S38 | 300 | μA |
| | I _{OUT} 2 | COM1 to COM4 | 3 | |
| | IOUT3 | LD1 to LD48 | 30 | mA |
| Allowable power dissipation | Pd max | Ta=95°C | 400 | mW |
| Operating temperature | Topr | | -40 to +95 | °C |
| Storage temperature | Tstg | | -55 to +150 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Allowable Operating Ranges at Ta = -40 to $+95^{\circ}C$, $V_{SS} = 0V$

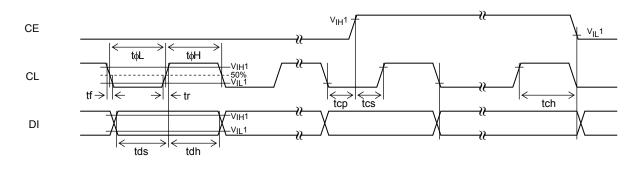
| Deremeter | Ourseh al | Conditions | | Ratings | | | Unit |
|------------------------------------|-------------------|-------------------------------------|-----------|--------------------|-----|--------------------|------|
| Parameter | Symbol | | | min | typ | max | Unit |
| Supply voltage | V _{DD} | V _{DD} | | 4.5 | | 5.5 | V |
| Input high-level voltage | V _{IH} 1 | CE, CL, DI, INH | | 0.8V _{DD} | | 5.5 | V |
| | V _{IH} 2 | OSCI | | 0.8V _{DD} | | 5.5 | v |
| Input low-level voltage | V _{IL} 1 | CE, CL, DI, INH | | 0 | | 0.2V _{DD} | V |
| | V _{IL} 2 | OSCI | | 0 | | 0.2V _{DD} | v |
| Output pull-up voltage | VOUP | LD1 to LD48, V_{DD} = 4.5 to 5.5V | | 0 | | 30 | V |
| External clock operating frequency | ^f CK | OSCI, External clock operating mode | [Fig 3] | 100 | 300 | 600 | kHz |
| External clock duty | DCK | OSCI, External clock operating mode | [Fig 3] | 30 | 50 | 70 | % |
| Data setup time | tds | CL, DI [Fig 1] | , [Fig 2] | 160 | | | ns |
| Data hold time | tdh | CL, DI [Fig 1] | , [Fig 2] | 160 | | | ns |
| CE wait time | tcp | CE, CL [Fig 1] | , [Fig 2] | 160 | | | ns |
| CE setup time | tcs | CE, CL [Fig 1] | , [Fig 2] | 160 | | | ns |
| CE hold time | tch | CE, CL [Fig 1] | , [Fig 2] | 160 | | | ns |
| High-level clock pulse width | tφH | CL [Fig 1] | , [Fig 2] | 160 | | | ns |
| Low-level clock pulse width | tøL | CL [Fig 1] | , [Fig 2] | 160 | | | ns |
| Rise time | tr | CE, CL, DI [Fig 1] | , [Fig 2] | | 160 | | ns |
| Fall time | tf | CE, CL, DI [Fig 1] | , [Fig 2] | | 160 | | ns |
| INH switching time | tc | INH, CE [Fig 4], [Fig 5], [Fig 6] | , [Fig 7] | 10 | | | μs |

| Deremeter | Cumbal | Dia | Conditions | | Ratings | | Unit |
|-----------------------------|--------------------|--------------------|--|----------------------------|--------------------|----------------------------|------|
| Parameter | Symbol | Pin | Conditions | min | typ | max | Unit |
| Hysteresis | v_{H} | CE, CL, DI, INH | | | 0.1V _{DD} | | V |
| Input high-level current | I _{IH} 1 | CE, CL, DI, INH | V _I = 5.5V | | | 5.0 | |
| | I _{IH} 2 | OSCI | V _I = 5.5V | | | 5.0 | μA |
| Input low-level current | I _{IL} 1 | CE, CL, DI, INH | V _I = 0V | -5.0 | | | |
| | I _{IL} 2 | OSCI | V _I = 0V | -5.0 | | | μA |
| Output OFF leak current | IOFFH | LD1 to LD48 | V _O = 30V | | | 5.0 | μA |
| Output high-level voltage | V _{OH} 1 | S1 to S38 | I _O = -20μA | V _{DD} -0.9 | | | |
| | V _{OH} 2 | COM1 to COM4 | I _O = -100μA | V _{DD} -0.9 | | | V |
| Output low-level voltage | V _{OL} 1 | S1 to S38 | I _O = 20μA | | | 0.9 | |
| | V _{OL} 2 | COM1 to COM4 | I _O = 100μA | | | 0.9 | V |
| | V _{OL} 3 | LD1 to LD48 | I _O = 20mA | | 0.25 | 0.5 | 1 |
| Output middle-level voltage | V _{MID} 1 | S1 to S36 | 1/3 bias I _O = $\pm 20\mu$ A | 2/3V _{DD} -0.9 | | 2/3V _{DD} +0.9 | |
| · | V _{MID} 2 | S1 to S36 | 1/3 bias I _O = ±20µA | 1/3V _{DD} -0.9 | | 1/3V _{DD} +0.9 | V |
| | V _{MID} 3 | COM1 to COM4 | 1/3 bias I _O = ±100μA | 2/3V _{DD} -0.9 | | 2/3V _{DD} +0.9 | |
| | V _{MID} 4 | COM1 to COM4 | 1/3 bias I _O = ±100μA | 1/3V _{DD} -0.9 | | 1/3V _{DD} +0.9 | |
| | V _{MID} 5 | COM1, COM2 | 1/2 bias I _O = ±100μA | 1/2V _{DD} -0.9 | | 1/2V _{DD} +0.9 | |
| Oscillator frequency | fosc | Oscillator circuit | Internal oscillator operating mode | 240 | 300 | 360 | kHz |
| Current drain | I _{DD} 1 | V _{DD} | Power save mode | | | 15 | |
| | I _{DD} 2 | V _{DD} | V _{DD} = 5.5V Output open, Internal oscillator operating mode | | 750 | 1500 | |
| | I _{DD} 3 | V _{DD} | $V_{DD} = 5.5V$ Output open, External clock operating mode $f_{CK} = 300kHz$ $V_{IH}2 = 0.9V_{DD}$ $V_{IL}2 = 0.1V_{DD}$ | | 750 | 1500 | μA |

Electrical Characteristics for the Allowable Operating Ranges

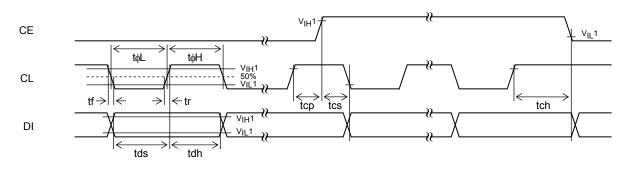
* Electrical Characteristics might be changed for the improvement without notice.

1. When CL is stopped at the low level.



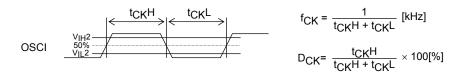


2. When CL is stopped at the high level.



[Fig 2]

3. OSCI pin clock timing in external clock operating mode.



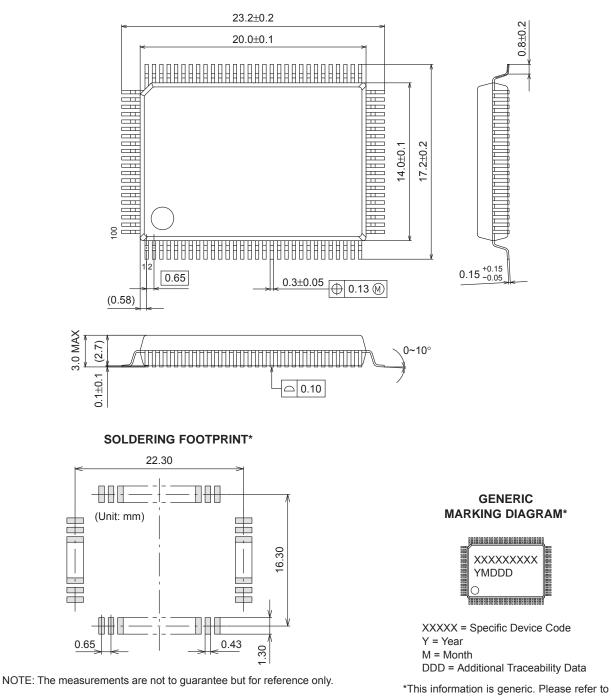
[Fig 3]

Package Dimensions

unit : mm

PQFP100 14x20 / QIP100E

CASE 122BV ISSUE A



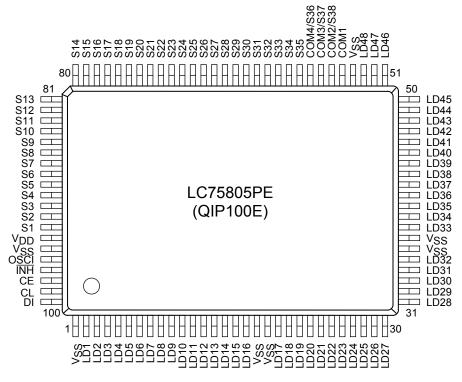
*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

No.A2119-5/34

device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■",

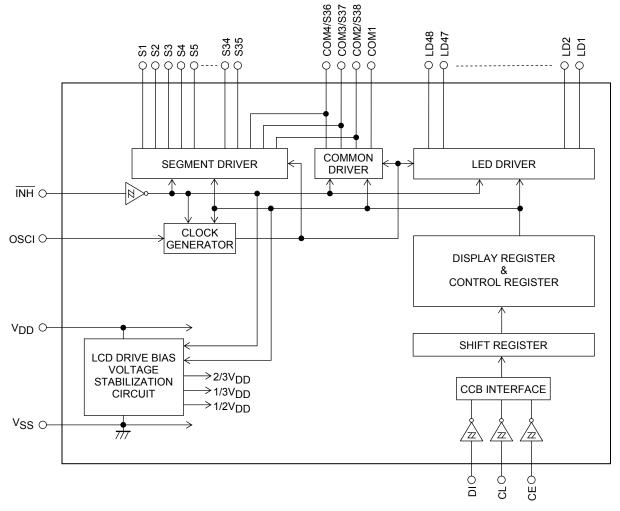
may or may not be present.

Pin Assignment



Top view





Pin Functions

| Symbol | Pin No. | Function | Active | I/O | Handling when unused |
|---|---------------------------------------|--|--------|-----|----------------------------|
| LD1 to LD16 LD17 to LD32 LD33 to LD48 | 2 to 17 20 to 35 38 to 53 | These are LED driver output pins that display the display data for LED transferred by serial data input, and high- voltage open-drain output pins. (Pull-up voltage is 30[V] maximum.) In addition, brightness adjustment of LED is possible by PWM function, too. | - | 0 | OPEN |
| COM1 COM2/S38 COM3/S37 COM4/S36 | 55 56 57 58 | These are common driver output pins, and Frame frequency is fo [Hz]. COM2/S38, COM3/S37 and COM4/S36 are possible to be used as the segment output by control data. | - | 0 | OPEN |
| S35 to S1 | 59 to 93 | These are segment output pins that display the display data for LCD transferred by serial data input. | - | 0 | OPEN |
| OSCI | 96 | This is input pin for the external clock. Input the clock whose frequency (f_{CK}) is between 100 and 600[kHz] at external clock operating mode. Furthermore, connect to GND at internal oscillator operating mode. | - | I | GND |
| CE | 98 | These are input pins for serial data transfer, and connect to the controller. | н | I | |
| CL | 99 | CE: Chip enable | | I | GND |
| DI | 100 | CL: Synchronized clock DI: Transfer data | - | Т | |
| ĪNH | 97 | Display off control input pin • INH = Low-level (V _{SS})Display forced off LD1 to LD48 = Z (High-impedance) COM1 = L (V _{SS}) COM2/S38 to COM4/S36 = L (V _{SS}) S1 to S35 = L (V _{SS}) Internal oscillator operation is stopped. External clock input is forbidden. • INH = High-level (V _{DD})Display on Internal oscillator operation is possible. (At Internal oscillator operating mode) External clock operating mode) However, serial data can be transferred during turn off. | L | I | GND |
| V _{DD} | 94 | This is power supply pin. Supply the voltage between 4.5V and 5.5V. | - | - | - |
| V _{SS} | 1 18 19 36 37 54 95 | These are power supply pins. Connect to GND. | - | - | - |

Serial Data Transfer Format

1/4 Duty Drive

(1) When CL is stopped at the low level

| CE_ | | | | | | | | | | Ļ |
|---------|--|------------------------------------|-----------------------------------|-----------------------|-------------------|---------------|-----------------------------|---|---------------|------------------|
| CL_ | | ΠΠΓ | | | | | | | | ЛЦ |
| ы] | (1 | 1 XD2X XD133 | XD134XD135XD136XD137X | D138XD139XD140X | οχοχοχ | οχοχοχ | ο χ ο χος χεοχεί | C1XFC2XFC3XDT0XDT1 | (scХвиХо) | |
| | ← CCB address → ← 8 bits | | data for LCD — 40 bits | > . | < | | - Control data - 17 bits | | | DD→ bits |
| ح | | | | | | | | | | Ļ |
| ح | | Γ.ΓΓ | | | | | | | | ЛŲ |
| रे २ | (1 X 1 X 1 X 0 X 0 X 0 X 0 X 1 X L1 B0 B1 B2 B3 A0 A1 A2 A3 | A XL1BX | | | .47CXL48AXL48BXL4 | 8CXPF0XPF1XP | | | (0)(0)(1) | |
| I | CCB address → ← 8 bits | | | trol data — 8 bits | | | >I< | Fixed data — 9 bits | | DD → bits |
| ے | | | | | | | | | | |
| ` ج | mm | | | ЛЛЛ | | ЛЛЛ | | | | |
| रे र | <u>(1 </u> | 1 XLT2XXLT47 XLT48 | <u>(o X o X o X</u> | w10Xw11Xw12X | w13Xw14Xw15Xv | /16XW20XW21XW | 122XW23XW24XW25XW | 26XW30XW31XW32XW33 | (w34Xw35Xw36) | |
| | B0 B1 B2 B3 A0 A1 A2 A3 CCB address > < 8 bits | Display data for LED 48 bits | <fixed data<br="">12 bits</fixed> | < | | | | Control data 49 bits | | |
| | | | | | | | | | | |
| | | | | | | | | | | |
| | 1 | · (W40XW41XW42XW43 | (w44Xw45Xw46Xw50X | w51XW52XW53XV | v54Xw55Xw56Xv | 60Xw61Xw62Xw | 63XW64XW65XW66XW | 70XW71XW72XW73XW74) | (W75XW76X 1 X | 1 🛛 0 🗡 |
| | | | | | | | | | | $DD \rightarrow$ |

(Note 1) The input of serial data is taken in at the rising edge of CL, and latched at the falling edge of CE. In addition, this IC has the function that counts the number of CL clock to receive the correct serial data. That is to say, because it isn't latched at the falling edge of CE when the number of the count of CL in each serial data is wrong, receiving wrong serial data can be prevented.

(Note 2) DD • • • Direction Data

| • CCB address | "87H" |
|--|---|
| • D1 to D140 | Display data for LCD |
| • OC | Control data for switch of internal oscillator operating mode and external clock operating mode |
| • FC0 to FC3 | Control data for setting of the frame frequency of common and segment output waveform |
| • DT0, DT1 | Control data for setting of drive scheme (setting of 1/1 to 1/4 Duty Drive scheme) of LCD |
| • SC | Control data for turning on/off segments |
| • BU | Control data for switch of Normal mode and Power-saving mode |
| • L1A, L1B, L1C to L48A, L48B, L48C | Control data for Ch settings of PWM circuits that adjust brightness of LED |
| • PF0 to PF3 | Control data for setting of the frame frequency of LED driver output waveform |
| • LT1 to LT48 | Display data for LED |
| • W10 to W16, W20 to W26, | PWM data of PWM circuits of LED driver output |
| W30 to W36, W40 to W46, | |
| W50 to W56, W60 to W66 | |
| W70 to W76 | |

| (2) When CL is stopped at | the high level | | |
|---|--|--|---|
| | | | |
| | | | |
| DI $X 1 X 1 X 1 X 0 X 0 X 0 X 0 X 1 X D$ B0 B1 B2 B3 A0 A1 A2 A3 < CCB address $>$ $<8 bits$ | 1 <u>XD2X X0133</u> X0134X0135X0136X0137X0138X0139X0140X 0 ———————————————————————————————————— | X 0 X 0 X 0 X 0 X 0 X 0 X 0 X 0 X 0 X 0 | $\left \left $ |
| | | | |
| $\begin{vmatrix} 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 $ | AXL1BX XL45AXL45BXL45CXL46AXL46BXL46CXL47AXL47AXL47A Control data 148 bits | СХL484XL48BXL48CXPF0XPF1XPF2XPF3X 0 X 0 X 0 X > | $\begin{array}{c c} \hline \langle 0 & X & 0 & X & 0 & X & 0 & X & 0 & X & 0 & X & 0 & X & 1 & X & 0 & X & 1 & X \\ \hline \\ \hline \\ Fixed data &> & & & & & & & \\ 9 & bits & 3 & bits & 3 & bits & & & & & \\ \end{array}$ |
| | | | |
| $\begin{array}{c c} & 1 \\ & 1$ | Display data Fixed data | 3Xw14Xw15Xw16Xw20Xw21Xw22Xw23Xw24Xw25Xw26 | (w30Xw31Xw32Xw33Xw34Xw35Xw36) - Control data 49 bits |
| | <u>{w40Xw41Xw42Xw43Xw44Xw45Xw46Xw50Xw51Xw52Xw53Xw5</u> | 4 <u>X</u> W55 <u>X</u> W56 <u>X</u> W60 <u>XW61XW62</u> XW63 <u>XW64</u> XW65 <u>XW66</u> XW70 <u>X</u> | W71XW72XW73XW74XW75XW76X 1 X 1 X 0 X → |

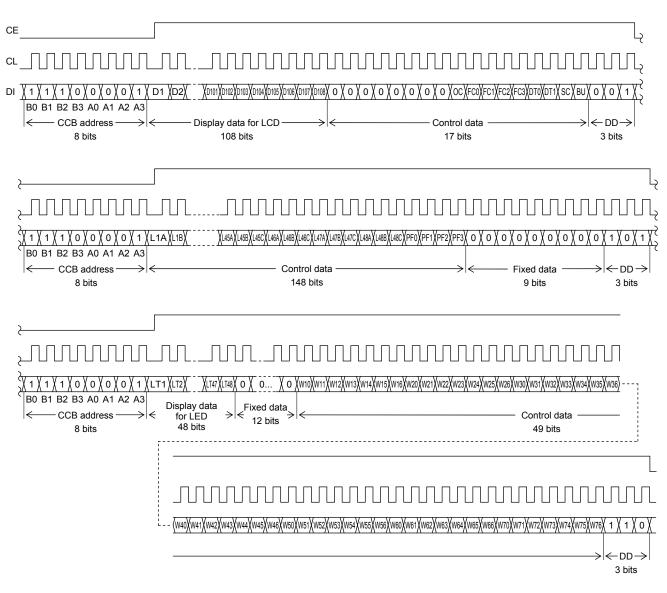
(Note 1) The input of serial data is taken in at the rising edge of CL, and latched at the falling edge of CE. In addition, this IC has the function that counts the number of CL clock to receive the correct serial data. That is to say, because it isn't latched at the falling edge of CE when the number of the count of CL in each serial data is wrong, receiving wrong serial data can be prevented.

(Note 2) DD ••• Direction Data

| • CCB address | "87H" |
|---------------------------|---|
| • D1 to D140 | Display data for LCD |
| • OC | Control data for switch of internal oscillator operating mode and external clock operating mode |
| • FC0 to FC3 | Control data for setting of the frame frequency of common and segment output waveform |
| • DT0, DT1 | Control data for setting of drive scheme (setting of 1/1 to 1/4 Duty Drive scheme) of LCD |
| • SC | Control data for turning on/off segments |
| • BU | Control data for switch of Normal mode and Power-saving mode |
| • L1A, L1B, L1C to L48A, | Control data for Ch settings of PWM circuits that adjust brightness of LED |
| L48B, L48C | |
| • PF0 to PF3 | Control data for setting of the frame frequency of LED driver output waveform |
| • LT1 to LT48 | |
| • W10 to W16, W20 to W26, | PWM data of PWM circuits of LED driver output |
| W30 to W36, W40 to W46, | |
| W50 to W56, W60 to W66 | |
| W70 to W76 | |
| | |

1/3 Duty Drive

(1) When CL is stopped at the low level



(Note 1) The input of serial data is taken in at the rising edge of CL, and latched at the falling edge of CE. In addition, this IC has the function that counts the number of CL clock to receive the correct serial data. That is to say, because it isn't latched at the falling edge of CE when the number of the count of CL in each serial data is wrong, receiving wrong serial data can be prevented.

(Note 2) DD • • • Direction Data

| • CCB address | "87H" |
|---------------------------|---|
| • D1 to D108 | Display data for LCD |
| • OC | Control data for switch of internal oscillator operating mode and external clock operating mode |
| • FC0 to FC3 | Control data for setting of the frame frequency of common and segment output waveform |
| • DT0, DT1 | Control data for setting of drive scheme (setting of 1/1 to 1/4 Duty Drive scheme) of LCD |
| • SC | Control data for turning on/off segments |
| • BU | Control data for switch of Normal mode and Power-saving mode |
| | Control data for Ch settings of PWM circuits that adjust brightness of LED |
| L48B, L48C | |
| | Control data for setting of the frame frequency of LED driver output waveform |
| • LT1 to LT48 | Display data for LED |
| • W10 to W16, W20 to W26, | PWM data of PWM circuits of LED driver output |
| W30 to W36, W40 to W46, | |
| W50 to W56, W60 to W66 | |
| W70 to W76 | |

| (2) When CL is stopped a | t the high level | | |
|--|---|--|--|
| CE | | | |
| | | | |
| DI $X 1 X 1 X 1 X 0 X 0 X 0 X 0 X 1 BO B1 B2 B3 A0 A1 A2 A3CCB address 8 bits$ | | 0 X 0 X 0 X 0 X 0 X 0 X 0 X 0 X 0 X 0 X | $\frac{2}{2} \frac{1}{2} \frac{1}$ |
| | | | |
| $\begin{cases} 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 $ | <u>⟨L1A)⟨L1B)⟨ 454)⟨L458)⟨L450)⟨L464)⟨L468)⟨L460)⟨L47A)⟨L478)</u> < Control data 148 bits | | $\begin{array}{c c} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 0 \\ \hline 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 &$ |
| | | | |
| $\begin{cases} \begin{array}{c} & & \\ & & \\ & & \\ \\ & & \\ \\ & \\ \end{array} \\ \begin{array}{c} \\ & \\ \\ & \\ \end{array} \\ \begin{array}{c} \\ & \\ \\ \\ & \\ \end{array} \\ \begin{array}{c} \\ & \\ \\ \\ \\ \end{array} \\ \begin{array}{c} \\ & \\ \end{array} \\ \begin{array}{c} \\ \\ & \\ \end{array} \\ \begin{array}{c} \\ & \\ \end{array} \\ \begin{array}{c} \\ & \\ \end{array} \\ \begin{array}{c} \\ \\ & \\ \end{array} \\ \begin{array}{c} \\ \\ & \\ \end{array} \\ \begin{array}{c} \\ \\ \end{array} \\ \end{array} \\ \begin{array}{c} \\ \end{array} \\ \end{array} \\ \begin{array}{c} \\ \end{array} \\ \end{array} \\ \begin{array}{c} \\ \\ \end{array} \\ \end{array} \\ \begin{array}{c} \\ \end{array} \\ \end{array} \\ \end{array} \\ \end{array} \\ \begin{array}{c} \\ \end{array} \\ $ | (LT1)/LT2) | w13Xw14Xw15Xw16Xw20Xw21Xw22Xw23Xw24Xw25Xw26X | ^{₩30} ₩31Ҳ₩32Ҳ₩33Ҳ₩34Ҳ₩35Ҳ₩36) - Control data ———— 49 bits |
| | | | VITIXW72XW73XW74XW75XW76X 1 X 1 X 0 X |
| | | עריעייאלעייאלעייאלעייאלעייאלעייאלעייאלעי | |

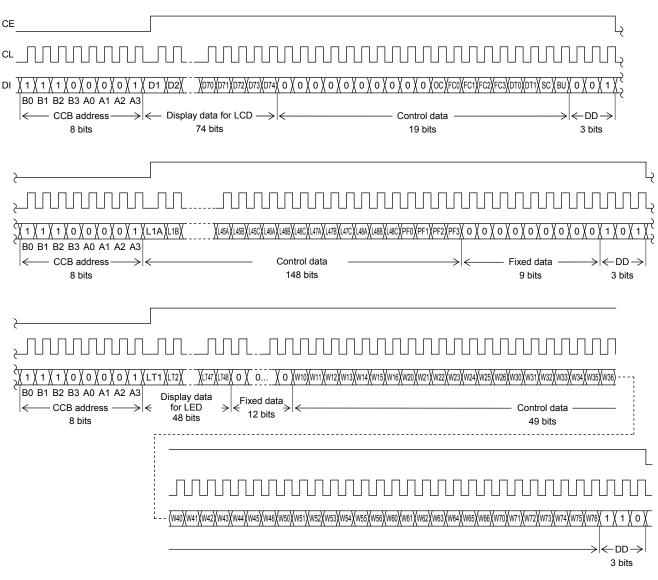
(Note 1) The input of serial data is taken in at the rising edge of CL, and latched at the falling edge of CE. In addition, this IC has the function that counts the number of CL clock to receive the correct serial data. That is to say, because it isn't latched at the falling edge of CE when the number of the count of CL in each serial data is wrong, receiving wrong serial data can be prevented.

(Note 2) $DD \bullet \bullet \bullet$ Direction Data

| • CCB address | "87H" |
|---------------------------|---|
| • D1 to D108 | Display data for LCD |
| • OC | Control data for switch of internal oscillator operating mode and external clock operating mode |
| • FC0 to FC3 | Control data for setting of the frame frequency of common and segment output waveform |
| • DT0, DT1 | Control data for setting of drive scheme (setting of 1/1 to 1/4 Duty Drive scheme) of LCD |
| | Control data for turning on/off segments |
| • BU | Control data for switch of Normal mode and Power-saving mode |
| • L1A, L1B, L1C to L48A, | Control data for Ch settings of PWM circuits that adjust brightness of LED |
| L48B, L48C | |
| • PF0 to PF3 | Control data for setting of the frame frequency of LED driver output waveform |
| • LT1 to LT48 | Display data for LED |
| • W10 to W16, W20 to W26, | PWM data of PWM circuits of LED driver output |
| W30 to W36, W40 to W46, | |
| W50 to W56, W60 to W66 | |
| W70 to W76 | |
| | |

1/2 Duty Drive

(1) When CL is stopped at the low level



(Note 1) The input of serial data is taken in at the rising edge of CL, and latched at the falling edge of CE. In addition, this IC has the function that counts the number of CL clock to receive the correct serial data. That is to say, because it isn't latched at the falling edge of CE when the number of the count of CL in each serial data is wrong, receiving wrong serial data can be prevented.

(Note 2) DD ••• Direction Data

| • CCB address • D1 to D74 • OC | |
|--|---|
| | Control data for setting of the frame frequency of common and segment output waveform |
| • DT0, DT1 | Control data for setting of drive scheme (setting of 1/1 to 1/4 Duty Drive scheme) of LCD |
| | Control data for turning on/off segments |
| • BU | Control data for switch of Normal mode and Power-saving mode |
| • L1A, L1B, L1C to L48A, L48B, L48C | Control data for Ch settings of PWM circuits that adjust brightness of LED |
| • PF0 to PF3 | Control data for setting of the frame frequency of LED driver output waveform |
| • LT1 to LT48 | Display data for LED |
| • W10 to W16, W20 to W26, | PWM data of PWM circuits of LED driver output |
| W30 to W36, W40 to W46, | |
| W50 to W56, W60 to W66 | |
| W70 to W76 | |
| | |

| (2) When CL is stopped | l at the high level | | | | |
|---|--|---|---|---------------------------------------|--|
| CE | | | | | |
| | | | | | |
| DI $X 1 X 1 X 1 X 0 X 0 X 0 X 0 X 1$ B0 B1 B2 B3 A0 A1 A2 A3 CCB address | $-\eta - \alpha - \alpha - \alpha - \alpha - \alpha - \alpha - \alpha$ |)74X o X o X o X o X o X o X o X > | 0 X 0 X 0 X 0 X 0 XOCXFC0XFC1XFC2X Control data 19 bits | FC3XDT0XDT1XSCXBUX 0 X 0 | \rightarrow |
| | 「 ¬ | | | MMM | |
| $\begin{array}{c} & \begin{array}{c} & \end{array} \\ & \begin{array}{c} & \end{array} \\ & \begin{array}{c} \\ \\ \end{array} \\ & \end{array} \\ & \begin{array}{c} \\ \\ \end{array} \\ \end{array} \\ & \begin{array}{c} \\ \end{array} \\ \end{array} \\ & \begin{array}{c} \\ \\ \end{array} \\ \end{array} \\ & \begin{array}{c} \\ \\ \end{array} \\ \end{array} \\ & \begin{array}{c} \\ \\ \end{array} \\ & \begin{array}{c} \\ \\ \end{array} \\ & \begin{array}{c} \\ \end{array} \\ & \begin{array}{c} \\ \end{array} \\ & \begin{array}{c} \\ \\ \\ \end{array} \\ & \begin{array}{c} \\ \\ \end{array} \\ & \begin{array}{c} \\ \end{array} \\ & \end{array} \\ \\ \end{array} \\ \end{array} \\ \end{array} \\ \\ \end{array} \\ \end{array} \\ \end{array} \\$ | $-\Lambda$ Λ Λ $-\Lambda$ Λ Λ Λ Λ | 464XL466XL46cXL47AXL47BXL47CXL48AXL — Control data ——— 148 bits | 488XL48CXPF0XPF1XPF2XPF3X O X O X | | $\begin{array}{c c} & 1 \\ \hline \\ & 1 \\ \hline \\ & -DD \\ \hline \\ & 3 \\ \end{array}$ |
| $\begin{array}{c} \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\$ | $\begin{array}{c c} & & \\ \hline \\ \hline$ | | Γ ν15χ₩16 <u>χ</u> ₩20χ₩21χ₩22χ₩23χ₩24χ₩25χ | ـــــــــــــــــــــــــــــــــــــ | 5 <u><u></u> (1) (5<u>)</u> (1) (1) (1) (1) (1) (1) (1) (1) (1) (1)</u> |
| | <u>{W40XW41XW42XW43XW44XW45X</u> v | Г /46XW50XW51XW52XW53XW54XW55XV | Г v56Xw60Xw61Xw62Xw63Xw64Xw65Xw66X | | $\begin{array}{c} \hline \\ \hline $ |

(Note 1) The input of serial data is taken in at the rising edge of CL, and latched at the falling edge of CE. In addition, this IC has the function that counts the number of CL clock to receive the correct serial data. That is to say, because it isn't latched at the falling edge of CE when the number of the count of CL in each serial data is wrong, receiving wrong serial data can be prevented.

(Note 2) DD $\bullet \bullet \bullet$ Direction Data

| • CCB address | "87H" |
|---------------------------|---|
| • D1 to D74 | Display data for LCD |
| • OC | Control data for switch of internal oscillator operating mode and external clock operating mode |
| • FC0 to FC3 | Control data for setting of the frame frequency of common and segment output waveform |
| • DT0, DT1 | Control data for setting of drive scheme (setting of 1/1 to 1/4 Duty Drive scheme) of LCD |
| • SC | Control data for turning on/off segments |
| • BU | Control data for switch of Normal mode and Power-saving mode |
| • L1A, L1B, L1C to L48A, | Control data for Ch settings of PWM circuits that adjust brightness of LED |
| L48B, L48C | |
| • PF0 to PF3 | Control data for setting of the frame frequency of LED driver output waveform |
| • LT1 to LT48 | Display data for LED |
| • W10 to W16, W20 to W26, | PWM data of PWM circuits of LED driver output |
| W30 to W36, W40 to W46, | |
| W50 to W56, W60 to W66 | |
| W70 to W76 | |
| | |

| Static Drive (1/1 Duty Driv (1) When CL is stopped a | | | |
|--|---|--|---|
| CE | | | L, |
| ∝ | | uuuuuu | nnnnn, |
| DI $X 1 X 1 X 1 X 0 X 0 X 0 X 0 X 1 X 0$ BO B1 B2 B3 A0 A1 A2 A3 \leftarrow CCB address \rightarrow $<$ 8 bits | Display data | 0 X 0 X 0 X 0 X 0 X 0 X 0 X 0 X 0 X 0 X | $\frac{C3(DT0(DT1)(SC)(BU)(0)(0)(1)(2)}{<} < DD \rightarrow 3$ bits |
| | | | Ļ |
| | | mmm | |
| $\begin{array}{c} \begin{array}{c} \begin{array}{c} \begin{array}{c} \begin{array}{c} \begin{array}{c} \end{array}\\ \end{array}\\ \end{array}\\ \begin{array}{c} \begin{array}{c} \end{array}\\ \end{array}\\ \end{array}\\ \end{array}\\ \end{array}\\ \end{array}\\ \begin{array}{c} \end{array}\\ \end{array}\\ \end{array}\\ \end{array}\\ \begin{array}{c} \begin{array}{c} \end{array}\\ \end{array}\\ \end{array}\\ \end{array}\\ \begin{array}{c} \end{array}\\ \end{array}\\ \end{array}\\ \begin{array}{c} \end{array}\\ \end{array}\\ \end{array}\\ \begin{array}{c} \end{array}\\ \end{array}\\ \begin{array}{c} \end{array}\\ \end{array}\\ \begin{array}{c} \end{array}\\ \end{array}\\ \begin{array}{c} \begin{array}{c} \end{array}\\ \end{array}\\ \end{array}\\ \begin{array}{c} \end{array}\\ \end{array}\\ \end{array}\\ \end{array}\\ \begin{array}{c} \end{array}\\ \end{array}\\ \end{array}\\ \end{array}\\ \end{array}\\ \end{array}\\ \begin{array}{c} \end{array}\\ \end{array}\\ \end{array}\\ \end{array}\\ \end{array}\\ \end{array}\\ \end{array}\\ \end{array}\\ \end{array}\\ \end{array}$ \\ \begin{array}{c} \end{array}\\ | | 78XL47CXL48AXL488XL48CXPF0XPF1XPF2XPF3X 0 X 0 X 0 > | $ \begin{array}{c c} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $ |
| $\begin{array}{c} \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\$ | Display data for LED 48 bits | | |
| | (w40Xw41Xw42Xw43Xw44Xw45Xw46Xw50Xw51Xw52Xw5 | зХм54Хм55Хм56Хм60Хм61Хм62Хм63Хм64Хм66Хм66Хм | 70 <u>(</u> ₩71 <u>/</u> ₩72 <u>/</u> ₩73 <u>/</u> ₩74 <u>/</u> ₩75 <u>/</u> ₩76 <u>/</u> 1 <u>/</u> 1 <u>/</u> 0 <u>/</u> → |

(Note 1) The input of serial data is taken in at the rising edge of CL, and latched at the falling edge of CE. In addition, this IC has the function that counts the number of CL clock to receive the correct serial data. That is to say, because it isn't latched at the falling edge of CE when the number of the count of CL in each serial data is wrong, receiving wrong serial data can be prevented.

(Note 2) DD • • • Direction Data

| CCB address | |
|---|--|
| • FC0 to FC3 Control data for setting of the frame frequency of common and segment output waveform | |
| DT0, DT1 Control data for setting of drive scheme (setting of 1/1 to 1/4 Duty Drive scheme) of LCD SC Control data for turning on/off segments | |
| • BU Control data for switch of Normal mode and Power-saving mode | |
| • L1A, L1B, L1C to L48A, Control data for Ch settings of PWM circuits that adjust brightness of LED L48B, L48C | |
| • PF0 to PF3 Control data for setting of the frame frequency of LED driver output waveform | |
| LT1 to LT48 Display data for LED | |
| • W10 to W16, W20 to W26, PWM data of PWM circuits of LED driver output | |
| W30 to W36, W40 to W46, | |
| W50 to W56, W60 to W66 | |
| W70 to W76 | |
| | |

| (2) When CL is stopped | at the high level | | | | |
|---|---|--|--|---|---|
| CE | | | | | |
| | | | | | ΛĻ |
| DI $\overline{\langle 1 \rangle \langle 1 \rangle \langle 1 \rangle \langle 0 \rangle \langle 0 \rangle \langle 0 \rangle \langle 0 \rangle \langle 1}$ B0 B1 B2 B3 A0 A1 A2 A3 CCB address 8 bits | Display data ↓ Control Contr | (o X o X o X o X o X o X o X o X o X o | X 0 X 0 X 0 X 0 X 0 XOCXFC0XFC1XFC Control data | | $0 \times 1 \times 2$ DD \rightarrow bits |
| ا ۲۰۰۰٬۰۰۰٬۰۰۰٬۰۰۰٬ | ······ | | | | |
| X 1 X 1 X 1 X 0 X 0 X 0 X 0 X 1 B0 B1 B2 B3 A0 A1 A2 A3 ← CCB address 8 bits | <u> </u> | (1458)(1456)(1464)(1468)(1466)(1474)(1478)(1470)(148 | X1488X148CXPF0XPF1XPF2XPF3X 0 X 0 > | X 0 X 0 X 0 X 0 X 0 X 0 X 0 X ── Fixed data ──── 9 bits | $ \begin{array}{c c} \hline 0 & 1 & 0 & 1 \\ \hline 0 & 1 & 0 & 1 \\ \hline \\ \hline \\ \hline \\ \hline \\ \hline \\ \\ \\ \hline \\ \\ \\ \\ \hline \\$ |
| | Display uala | <pre> [</pre> | <u>\</u> \ <u>\</u> \ <u>\</u> W15\Xw16\Xw20\Xw21\Xw22\Xw23\Xw24\Xw2 | ∑W26∑W30∑W31∑W32∑W33∑W34∑ —— Control data — 49 bits | мз <u>бХизб</u>) |
| | | (w44Xw45Xw46Xw50Xw51Xw52Xw53Xw54Xw5 | L Xw56Xw60Xw61Xw62Xw63Xw64Xw65Xw66 | <u>}</u> | $\frac{1}{3 \text{ bits}}$ |

(Note 1) The input of serial data is taken in at the rising edge of CL, and latched at the falling edge of CE. In addition, this IC has the function that counts the number of CL clock to receive the correct serial data. That is to say, because it isn't latched at the falling edge of CE when the number of the count of CL in each serial data is wrong, receiving wrong serial data can be prevented.

(Note 2) DD • • • Direction Data

| • CCB address | "87H" |
|---------------------------|---|
| • D1 to D38 | Display data for LCD |
| • OC | Control data for switch of internal oscillator operating mode and external clock operating mode |
| • FC0 to FC3 | Control data for setting of the frame frequency of common and segment output waveform |
| • DT0, DT1 | Control data for setting of drive scheme (setting of 1/1 to 1/4 Duty Drive scheme) of LCD |
| • SC | Control data for turning on/off segments |
| • BU | Control data for switch of Normal mode and Power-saving mode |
| • L1A, L1B, L1C to L48A, | Control data for Ch settings of PWM circuits that adjust brightness of LED |
| L48B, L48C | |
| • PF0 to PF3 | Control data for setting of the frame frequency of LED driver output waveform |
| • LT1 to LT48 | |
| • W10 to W16, W20 to W26, | PWM data of PWM circuits of LED driver output |
| W30 to W36, W40 to W46, | |
| W50 to W56, W60 to W66 | |
| W70 to W76 | |
| | |

Control data Functions

(1) OC ... Control data for switch of internal oscillator operating mode and external clock operating mode This control data bit selects either the internal oscillator operating mode or external clock operating mode.

| OC | Fundamental clock operating mode | Input pin (OSCI) state |
|----|------------------------------------|--|
| 0 | Internal oscillator operating mode | Connect to GND |
| 1 | External clock operating mode | Input the clock (f _{CK} = 100 to 600 [kHz]) from the outside |

(2) FC0 to FC3 ... Control data for setting of the frame frequency of common and segment output waveform. These control data bits set the frame frequency of common and segment output waveform.

| | | | | Frame frequency of common and segment output waveform fo [Hz] | | |
|-----|-----|-----|-----|---|---|--|
| FC0 | FC1 | FC2 | FC3 | Internal oscillator operating mode (Control data OC ="0", fosc = 300 [kHz] typ) | External clock operating mode (Control data OC ="1", f _{CK} = 300 [kHz] typ) | |
| 0 | 0 | 0 | 0 | fosc/4992 | f _{CK} /4992 | |
| 1 | 0 | 0 | 0 | fosc/4608 | f _{CK} /4608 | |
| 0 | 1 | 0 | 0 | fosc/4224 | f _{CK} /4224 | |
| 1 | 1 | 0 | 0 | fosc/3840 | f _{CK} /3840 | |
| 0 | 0 | 1 | 0 | fosc/3456 | f _{CK} /3456 | |
| 1 | 0 | 1 | 0 | fosc/3072 | f _{CK} /3072 | |
| 0 | 1 | 1 | 0 | fosc/2688 | f _{CK} /2688 | |
| 1 | 1 | 1 | 0 | fosc/2496 | f _{CK} /2496 | |
| 0 | 0 | 0 | 1 | fosc/2448 | f _{CK} /2448 | |
| 1 | 0 | 0 | 1 | fosc/2304 | f _{CK} /2304 | |
| 0 | 1 | 0 | 1 | fosc/2112 | f _{CK} /2112 | |
| 1 | 1 | 0 | 1 | fosc/1920 | f _{CK} /1920 | |
| 0 | 0 | 1 | 1 | fosc/1728 | f _{CK} /1728 | |
| 1 | 0 | 1 | 1 | fosc/1536 | f _{CK} /1536 | |
| 0 | 1 | 1 | 1 | fosc/1344 | f _{CK} /1344 | |
| 1 | 1 | 1 | 1 | fosc/1152 | f _{CK} /1152 | |

(3) DT0, DT1 ... Control data for setting of drive scheme (setting of 1/1 to 1/4 Duty Drive scheme) of LCD These control bits select 1/4-Duty 1/3-Bias Drive, 1/3-Duty 1/3-Bias Drive, 1/2-Duty 1/2-Bias Drive, or Static Drive (1/1-Duty Drive) of LCD.

| | | Each pin state | | | |
|-----|-----|-------------------------------|----------|----------|----------|
| DT0 | DT1 | DT1 Drive scheme for LCD | COM2/S38 | COM3/S37 | COM4/S36 |
| 0 | 0 | 1/4-Duty 1/3-Bias Drive | COM2 | COM3 | COM4 |
| 1 | 0 | 1/3-Duty 1/3-Bias Drive | COM2 | COM3 | S36 |
| 0 | 1 | 1/2-Duty 1/2-Bias Drive | COM2 | S37 | S36 |
| 1 | 1 | Static Drive (1/1-Duty Drive) | S38 | S37 | S36 |

Note) COM2 to COM4: Common output / S38 to S36: Segment output

(4) SC ... Control data for turning on/off segments

This control data bit controls the on/off state of the segments.

| SC | Display state |
|----|---------------|
| 0 | On |
| 1 | Off |

Note that when the segments are turned off by setting SC to 1, the segments are turning off by outputting segment off waveforms from the segment output pins.

(5) BU ... Control data for switch of Normal mode and Power-saving mode

This control data bit selects either Normal mode or Power-saving mode.

| BU | Mode |
|----|---|
| 0 | Normal mode |
| 1 | Power-saving mode (The oscillation of internal oscillator circuit is stopped when internal oscillator operating mode (OC = [0]), and the receiving of external clock isn't admitted when external clock operating mode (OC = [1]). In addition, common and segment output pins are V _{SS} level, and LED driver output pins are High impedance. |

(6) L1A, L1B, L1C to L48A, L48B, L48C ... Control data for Ch settings of PWM circuits that adjust brightness of LED These control data bits set the Ch of PWM circuit for LED driver output pins, LD1 to LD48.

| LnA | LnB | LnC | Ch of PWM circuit for LED driver output LDn |
|-----|-----|-----|---|
| 0 | 0 | 0 | PWM circuit is not selected. (The setting of turning on/off of the duty 100% by Display data LTn for LED is possible.) |
| 1 | 0 | 0 | PWM circuit (Ch1) is selected. |
| 0 | 1 | 0 | PWM circuit (Ch2) is selected. |
| 1 | 1 | 0 | PWM circuit (Ch3) is selected. |
| 0 | 0 | 1 | PWM circuit (Ch4) is selected. |
| 1 | 0 | 1 | PWM circuit (Ch5) is selected. |
| 0 | 1 | 1 | PWM circuit (Ch6) is selected. |
| 1 | 1 | 1 | PWM circuit (Ch7) is selected. |

Note) LnA, LnB, LnC (n = 1 to 48) data are control data that set the Ch of PWM circuit for LED driver output pins LDn (n = 1 to 48).

For example, if (L1A, L1B, L1C) = (1, 0, 0), (L11A, L11B, L11C) = (1, 1, 0) and (L21A, L21B, L21C) = (0, 1, 1) is set, LED driver output pin LD1 select PWM circuit (Ch1) and LED driver output pin LD11 select PWM circuit (Ch3) and LED driver output pin LD21 select PWM circuit (Ch6).

(7) PF0 to PF3 ... Control data for setting of the frame frequency of LED driver output waveform These control data bits set the frame frequency of LED driver output waveform of LED output pin setting PWM circuit (Ch1 to Ch7).

| | | | | Frame frequency of LED driver output waveform fp [Hz] | | | | | |
|-----|---------------|---|-----|---|---|--|--|--|--|
| PF0 | PF0 PF1 PF2 F | | PF3 | Internal oscillator operating mode (Control data OC ="0", fosc = 300 [kHz] typ) | External clock operating mode (Control data OC ="1", f _{CK} = 300 [kHz] typ) | | | | |
| 0 | 0 | 0 | 0 | fosc/1664 | f _{CK} /1664 | | | | |
| 1 | 0 | 0 | 0 | fosc/1536 | f _{CK} /1536 | | | | |
| 0 | 1 | 0 | 0 | fosc/1408 | f _{CK} /1408 | | | | |
| 1 | 1 | 0 | 0 | fosc/1280 | f _{CK} /1280 | | | | |
| 0 | 0 | 1 | 0 | fosc/1152 | f _{CK} /1152 | | | | |
| 1 | 0 | 1 | 0 | fosc/1024 | f _{CK} /1024 | | | | |
| 0 | 1 | 1 | 0 | fosc/896 | f _{CK} /896 | | | | |
| 1 | 1 | 1 | 0 | fosc/768 | f _{CK} /768 | | | | |
| 0 | 0 | 0 | 1 | fosc/640 | f _{CK} /640 | | | | |
| 1 | 0 | 0 | 1 | fosc/512 | f _{CK} /512 | | | | |

Note) If (PF0, PF1, PF2, PF3) = (X, 1, 0, 1), (X, X, 1, 1) are set, the frame frequency (fosc/1408, fCK/1408) of setting (PF0, PF1, PF2, PF3) = (0, 1, 0, 0) is selected.

(8) W10 to W16, W20 to W26, W30 to W36, W40 to W46, W50 to W56, W60 to W66, W70 to W76

... PWM data of PWM circuit for LED driver output These control data bits set LED lighting time per 1 frame of LED driver output waveform of LED driver

| | | | | | - | - | $C_{1,7}$ | 0 01 | | | outpt | | cronn | 101 1 | | |
|-------|---------|---------|--------------|---------|----------|-------|----------------------------------|------|-----|-----|-------|-----|-------|-------|-----|----------------------------------|
| outpu | t pin s | setting | <u>g</u> PWN | VI CITC | <u> </u> | h1 to | | I | | | | | | | | |
| Wn0 | Wn1 | Wn2 | Wn3 | Wn4 | Wn5 | Wn6 | LED lighting time per 1 frame | | Wn0 | Wn1 | Wn2 | Wn3 | Wn4 | Wn5 | Wn6 | LED lighting time per 1 frame |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | (1/128) × Tp | | 0 | 0 | 0 | 0 | 0 | 0 | 1 | (65/128) × Tp |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | (1/128) × Tp (2/128) × Tp | | 1 | 0 | 0 | 0 | 0 | 0 | 1 | (66/128) × Tp |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | (3/128) × Tp | | 0 | 1 | 0 | 0 | 0 | 0 | 1 | (67/128) × Tp |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | (4/128) × Tp | | 1 | 1 | 0 | 0 | 0 | 0 | 1 | (68/128) × Tp |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | (5/128) × Tp | | 0 | 0 | 1 | 0 | 0 | 0 | 1 | (69/128) × Tp |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | (6/128) × Tp | | 1 | 0 | 1 | 0 | 0 | 0 | 1 | (70/128) × Tp |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | (7/128) × Tp | | 0 | 1 | 1 | 0 | 0 | 0 | 1 | (71/128) × Tp |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | (8/128) × Tp | | 1 | 1 | 1 | 0 | 0 | 0 | 1 | (72/128) × Tp |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | (9/128) × Tp (10/128) × Tp | | 0 | 0 | 0 | 1 | 0 | 0 | 1 | (73/128) × Tp (74/128) × Tp |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | (10/128) × Tp (11/128) × Tp | | 0 | 1 | 0 | 1 | 0 | 0 | 1 | (75/128) × Tp |
| 1 | 1 | 0 0 | 1 | 0 | 0 | 0 | (12/128) × Tp | | 1 | 1 | 0 | 1 | 0 | 0 | 1 | (76/128) × Tp |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | (13/128) × Tp | | 0 | 0 | 1 | 1 | 0 | 0 | 1 | (77/128) × Tp |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | (14/128) × Tp | | 1 | 0 | 1 | 1 | 0 | 0 | 1 | (78/128) × Tp |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | (15/128) × Tp | | 0 | 1 | 1 | 1 | 0 | 0 | 1 | (79/128) × Tp |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | (16/128) × Tp | | 1 | 1 | 1 | 1 | 0 | 0 | 1 | (80/128) × Tp |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | (17/128) × Tp | | 0 | 0 | 0 | 0 | 1 | 0 | 1 | (81/128) × Tp |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | (18/128) × Tp | | 1 | 0 | 0 | 0 | 1 | 0 | 1 | (82/128) × Tp |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | (19/128) × Tp (20/128) × Tp | | 0 | 1 | 0 | 0 | 1 | 0 | 1 | (83/128) × Tp (84/128) × Tp |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | (20/128) × Tp (21/128) × Tp | | 0 | 0 | 1 | 0 | 1 | 0 | 1 | (84/128) × Tp (85/128) × Tp |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | (22/128) × Tp | | 1 | 0 | 1 | 0 | 1 | 0 | 1 | (86/128) × Tp |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | (23/128) × Tp | | 0 | 1 | 1 | 0 | 1 | 0 | 1 | (87/128) × Tp |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | (24/128) × Tp | | 1 | 1 | 1 | 0 | 1 | 0 | 1 | (88/128) × Tp |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | (25/128) × Tp | | 0 | 0 | 0 | 1 | 1 | 0 | 1 | (89/128) × Tp |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | (26/128) × Tp | | 1 | 0 | 0 | 1 | 1 | 0 | 1 | (90/128) × Tp |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | (27/128) × Tp | | 0 | 1 | 0 | 1 | 1 | 0 | 1 | (91/128) × Tp |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | (28/128) × Tp (29/128) × Tp | | 1 | 1 | 0 | 1 | 1 | 0 | 1 | (92/128) × Tp |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | (29/128) × Tp (30/128) × Tp | | 1 | 0 | 1 | 1 | 1 | 0 | 1 | (93/128) × Tp (94/128) × Tp |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | (31/128) × Tp | | 0 | 1 | 1 | 1 | 1 | 0 | 1 | (95/128) × Tp |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | (32/128) × Tp | | 1 | 1 | 1 | 1 | 1 | 0 | 1 | (96/128) × Tp |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | (33/128) × Tp | | 0 | 0 | 0 | 0 | 0 | 1 | 1 | (97/128) × Tp |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | (34/128) × Tp | | 1 | 0 | 0 | 0 | 0 | 1 | 1 | (98/128) × Tp |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | (35/128) × Tp | | 0 | 1 | 0 | 0 | 0 | 1 | 1 | (99/128) × Tp |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | (36/128) × Tp | | 1 | 1 | 0 | 0 | 0 | 1 | 1 | (100/128) × Tp |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | (37/128) × Tp | | 0 | 0 | 1 | 0 | 0 | 1 | 1 | (101/128) × Tp |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | (38/128) × Tp (39/128) × Tp | | 1 | 0 | 1 | 0 | 0 | 1 | 1 | (102/128) × Tp (103/128) × Tp |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | (40/128) × Tp | | 1 | 1 | 1 | 0 | 0 | 1 | 1 | (103/128) × Tp (104/128) × Tp |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | (41/128) × Tp | | 0 | 0 | 0 | 1 | 0 | 1 | 1 | (105/128) × Tp |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | (42/128) × Tp | | 1 | 0 | 0 | 1 | 0 | 1 | 1 | (106/128) × Tp |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | (43/128) × Tp | | 0 | 1 | 0 | 1 | 0 | 1 | 1 | (107/128) × Tp |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | (44/128) × Tp | | 1 | 1 | 0 | 1 | 0 | 1 | 1 | (108/128) × Tp |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | (45/128) × Tp | | 0 | 0 | 1 | 1 | 0 | 1 | 1 | (109/128) × Tp |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | (46/128) × Tp | | 1 | 0 | 1 | 1 | 0 | 1 | 1 | (110/128) × Tp |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | (47/128) × Tp | | 0 | 1 | 1 | 1 | 0 | 1 | 1 | (111/128) × Tp (112/128) × Tp |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | (48/128) × Tp (49/128) × Tp | | 0 | 0 | 0 | 0 | 1 | 1 | 1 | (112/128) × Tp (113/128) × Tp |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | (50/128) × Tp | | 1 | 0 | 0 | 0 | 1 | 1 | 1 | (113/128) × Tp (114/128) × Tp |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | (51/128) × Tp | | 0 | 1 | 0 | 0 | 1 | 1 | 1 | (115/128) × Tp |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | (52/128) × Tp | | 1 | 1 | 0 | 0 | 1 | 1 | 1 | (116/128) × Tp |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | (53/128) × Tp | | 0 | 0 | 1 | 0 | 1 | 1 | 1 | (117/128) × Tp |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | (54/128) × Tp | | 1 | 0 | 1 | 0 | 1 | 1 | 1 | (118/128) × Tp |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | (55/128) × Tp | | 0 | 1 | 1 | 0 | 1 | 1 | 1 | (119/128) × Tp |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | (56/128) × Tp | | 1 | 1 | 1 | 0 | 1 | 1 | 1 | (120/128) × Tp |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | (57/128) × Tp | | 0 | 0 | 0 | 1 | 1 | 1 | 1 | (121/128) × Tp |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | (58/128) × Tp (59/128) × Tp | | 1 | 0 | 0 | 1 | 1 | 1 | 1 | (122/128) × Tp (123/128) × Tp |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | (60/128) × Tp | | 1 | 1 | 0 | 1 | 1 | 1 | 1 | (123/128) × Tp (124/128) × Tp |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | (61/128) × Tp | | 0 | 0 | 1 | 1 | 1 | 1 | 1 | (124/128) × Tp (125/128) × Tp |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | (62/128) × Tp | | 1 | 0 | 1 | 1 | 1 | 1 | 1 | (126/128) × Tp |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | (63/128) × Tp | | 0 | 1 | 1 | 1 | 1 | 1 | 1 | (127/128) × Tp |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | (64/128) × Tp | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | (128/128) × Tp |
| | | | | | | | A circuit (Ch1) / | | | | | - | | | | |

Note) W10 to W16 : PWM data of PWM circuit (Ch1) / W20 to W26 : PWM data of PWM circuit (Ch2) W30 to W36 : PWM data of PWM circuit (Ch3) / W40 to W46 : PWM data of PWM circuit (Ch4) W50 to W56 : PWM data of PWM circuit (Ch5) / W60 to W66 : PWM data of PWM circuit (Ch6) W70 to W76 : PWM data of PWM circuit (Ch7)

 $Tp = \frac{1}{fp}$

Descriptions of Display data for LCD

(1) Correspondence of output pins to display data for LCD at 1/4 Duty Drive

| Contespondent | e or outpu | it philo to t | ispiaj aai | a for LCD |
|---------------|------------|---------------|------------|-----------|
| Output Pin | COM1 | COM2 | COM3 | COM4 |
| S1 | D1 | D2 | D3 | D4 |
| S2 | D5 | D6 | D7 | D8 |
| S3 | D9 | D10 | D11 | D12 |
| S4 | D13 | D14 | D15 | D16 |
| S5 | D17 | D18 | D19 | D20 |
| S6 | D21 | D22 | D23 | D24 |
| S7 | D25 | D26 | D27 | D28 |
| S8 | D29 | D30 | D31 | D32 |
| S9 | D33 | D34 | D35 | D36 |
| S10 | D37 | D38 | D39 | D40 |
| S11 | D41 | D42 | D43 | D44 |
| S12 | D45 | D46 | D47 | D48 |
| S13 | D49 | D50 | D51 | D52 |
| S14 | D53 | D54 | D55 | D56 |
| S15 | D57 | D58 | D59 | D60 |
| S16 | D61 | D62 | D63 | D64 |
| S17 | D65 | D66 | D67 | D68 |
| S18 | D69 | D70 | D71 | D72 |
| | | | | |

| 1/4 Duty Dilve | | | | |
|----------------|------|------|------|------|
| Output Pin | COM1 | COM2 | COM3 | COM4 |
| S19 | D73 | D74 | D75 | D76 |
| S20 | D77 | D78 | D79 | D80 |
| S21 | D81 | D82 | D83 | D84 |
| S22 | D85 | D86 | D87 | D88 |
| S23 | D89 | D90 | D91 | D92 |
| S24 | D93 | D94 | D95 | D96 |
| S25 | D97 | D98 | D99 | D100 |
| S26 | D101 | D102 | D103 | D104 |
| S27 | D105 | D106 | D107 | D108 |
| S28 | D109 | D110 | D111 | D112 |
| S29 | D113 | D114 | D115 | D116 |
| S30 | D117 | D118 | D119 | D120 |
| S31 | D121 | D122 | D123 | D124 |
| S32 | D125 | D126 | D127 | D128 |
| S33 | D129 | D130 | D131 | D132 |
| S34 | D133 | D134 | D135 | D136 |
| S35 | D137 | D138 | D139 | D140 |

For example, the table below lists the output states for the S21 output pin.

| Display data | | | Output nin (S21) state | | | | |
|--------------|-----|-----|------------------------|--|--|--|--|
| D81 | D82 | D83 | D84 | Output pin (S21) state | | | |
| 0 | 0 | 0 | 0 | The LCD segments corresponding to COM1, COM2, COM3 and COM4 are off. | | | |
| 0 | 0 | 0 | 1 | The LCD segment corresponding to COM4 is on. | | | |
| 0 | 0 | 1 | 0 | The LCD segment corresponding to COM3 is on. | | | |
| 0 | 0 | 1 | 1 | The LCD segments corresponding to COM3 and COM4 are on. | | | |
| 0 | 1 | 0 | 0 | The LCD segment corresponding to COM2 is on. | | | |
| 0 | 1 | 0 | 1 | The LCD segments corresponding to COM2 and COM4 are on. | | | |
| 0 | 1 | 1 | 0 | The LCD segments corresponding to COM2 and COM3 are on. | | | |
| 0 | 1 | 1 | 1 | The LCD segments corresponding to COM2, COM3 and COM4 are on. | | | |
| 1 | 0 | 0 | 0 | The LCD segment corresponding to COM1 is on. | | | |
| 1 | 0 | 0 | 1 | The LCD segments corresponding to COM1 and COM4 are on. | | | |
| 1 | 0 | 1 | 0 | The LCD segments corresponding to COM1 and COM3 are on. | | | |
| 1 | 0 | 1 | 1 | The LCD segments corresponding to COM1, COM3 and COM4 are on. | | | |
| 1 | 1 | 0 | 0 | The LCD segments corresponding to COM1 and COM2 are on. | | | |
| 1 | 1 | 0 | 1 | The LCD segments corresponding to COM1, COM2 and COM4 are on. | | | |
| 1 | 1 | 1 | 0 | The LCD segments corresponding to COM1, COM2 and COM3 are on. | | | |
| 1 | 1 | 1 | 1 | The LCD segments corresponding to COM1, COM2, COM3 and COM4 are on. | | | |

(2) Correspondence of output pins to display data for LCD at 1/3 Duty Drive

| Output Pin | COM1 | COM2 | COM3 |
|------------|------|------|------|
| S1 | D1 | D2 | D3 |
| S2 | D4 | D5 | D6 |
| S3 | D7 | D8 | D9 |
| S4 | D10 | D11 | D12 |
| S5 | D13 | D14 | D15 |
| S6 | D16 | D17 | D18 |
| S7 | D19 | D20 | D21 |
| S8 | D22 | D23 | D24 |
| S9 | D25 | D26 | D27 |
| S10 | D28 | D29 | D30 |
| S11 | D31 | D32 | D33 |
| S12 | D34 | D35 | D36 |
| S13 | D37 | D38 | D39 |
| S14 | D40 | D41 | D42 |
| S15 | D43 | D44 | D45 |
| S16 | D46 | D47 | D48 |
| S17 | D49 | D50 | D51 |
| S18 | D52 | D53 | D54 |
| S19 | D55 | D56 | D57 |

| IOI LCD at 1/ | I LCD at 1/3 Duty Drive | | | | | | |
|---------------|-------------------------|----|------|------|--|--|--|
| Output Pi | n CC | M1 | COM2 | COM3 | | | |
| S20 | D | 58 | D59 | D60 | | | |
| S21 | D | 61 | D62 | D63 | | | |
| S22 | D | 64 | D65 | D66 | | | |
| S23 | D | 67 | D68 | D69 | | | |
| S24 | D | 70 | D71 | D72 | | | |
| S25 | D | 73 | D74 | D75 | | | |
| S26 | D | 76 | D77 | D78 | | | |
| S27 | D | 79 | D80 | D81 | | | |
| S28 | D | 82 | D83 | D84 | | | |
| S29 | D | 85 | D86 | D87 | | | |
| S30 | D | 88 | D89 | D90 | | | |
| S31 | D | 91 | D92 | D93 | | | |
| S32 | D | 94 | D95 | D96 | | | |
| S33 | D | 97 | D98 | D99 | | | |
| S34 | D1 | 00 | D101 | D102 | | | |
| S35 | D1 | 03 | D104 | D105 | | | |
| S36/COM | 4 D1 | 06 | D107 | D108 | | | |
| | | | | | | | |

Note) S36/COM4 pin is selected segment output.

For example, the table below lists the output states for the S21 output pin.

| [| Display dat | а | | | | |
|-----|-------------|-----|--|--|--|--|
| D61 | D62 | D63 | Output pin (S21) state | | | |
| 0 | 0 | 0 | The LCD segments corresponding to COM1, COM2 and COM3 are off. | | | |
| 0 | 0 | 1 | The LCD segment corresponding to COM3 is on. | | | |
| 0 | 1 | 0 | The LCD segment corresponding to COM2 is on. | | | |
| 0 | 1 | 1 | The LCD segments corresponding to COM2 and COM3 are on. | | | |
| 1 | 0 | 0 | The LCD segment corresponding to COM1 is on. | | | |
| 1 | 0 | 1 | The LCD segments corresponding to COM1 and COM3 are on. | | | |
| 1 | 1 | 0 | The LCD segments corresponding to COM1 and COM2 are on. | | | |
| 1 | 1 | 1 | The LCD segments corresponding to COM1, COM2 and COM3 are on. | | | |

| (3) | Correspondenc | e of outpu | it pins to c | lisp | lay data for LC | D at 1/2 L | Duty Drive |
|-----|---------------|------------|--------------|------|-----------------|------------|------------|
| | Output Pin | COM1 | COM2 | | Output Pin | COM1 | COM2 |
| | S1 | D1 | D2 | | S20 | D39 | D40 |
| | S2 | D3 | D4 | | S21 | D41 | D42 |
| | S3 | D5 | D6 | | S22 | D43 | D44 |
| | S4 | D7 | D8 | | S23 | D45 | D46 |
| | S5 | D9 | D10 | | S24 | D47 | D48 |
| | S6 | D11 | D12 | | S25 | D49 | D50 |
| | S7 | D13 | D14 | | S26 | D51 | D52 |
| | S8 | D15 | D16 | | S27 | D53 | D54 |
| | S9 | D17 | D18 | | S28 | D55 | D56 |
| | S10 | D19 | D20 | | S29 | D57 | D58 |
| | S11 | D21 | D22 | | S30 | D59 | D60 |
| | S12 | D23 | D24 | | S31 | D61 | D62 |
| | S13 | D25 | D26 | | S32 | D63 | D64 |
| | S14 | D27 | D28 | | S33 | D65 | D66 |
| | S15 | D29 | D30 | | S34 | D67 | D68 |
| | S16 | D31 | D32 | | S35 | D69 | D70 |
| | S17 | D33 | D34 | | S36/COM4 | D71 | D72 |
| | S18 | D35 | D36 | | S37/COM3 | D73 | D74 |
| | S19 | D37 | D38 | | | | |
| | | | | | | | |

(3) Correspondence of output pins to display data for LCD at 1/2 Duty Drive

Note) S36/COM4 and S37/COM3 pins are selected segment output.

For example, the table below lists the output states for the S21 output pin.

| Displa | iy data | Output pin (S21) state | | | |
|--------|---------|--|--|--|--|
| D41 | D42 | | | | |
| 0 | 0 | The LCD segments corresponding to COM1 and COM2 are off. | | | |
| 0 | 1 | The LCD segment corresponding to COM2 is on. | | | |
| 1 | 0 | The LCD segment corresponding to COM1 is on. | | | |
| 1 | 1 | The LCD segment corresponding to COM1 and COM2 are on. | | | |

(4) Correspondence of output pins to display data for LCD at Static Drive (1/1 Duty Drive)

| conceptine | | n pi | no to anopiaj a | |
|------------|------|------|-----------------|------|
| Output Pin | COM1 | | Output Pin | COM1 |
| S1 | D1 | | S21 | D21 |
| S2 | D2 | | S22 | D22 |
| S3 | D3 | | S23 | D23 |
| S4 | D4 | | S24 | D24 |
| S5 | D5 | | S25 | D25 |
| S6 | D6 | | S26 | D26 |
| S7 | D7 | | S27 | D27 |
| S8 | D8 | | S28 | D28 |
| S9 | D9 | | S29 | D29 |
| S10 | D10 | | S30 | D30 |
| S11 | D11 | | S31 | D31 |
| S12 | D12 | | S32 | D32 |
| S13 | D13 | | S33 | D33 |
| S14 | D14 | | S34 | D34 |
| S15 | D15 | | S35 | D35 |
| S16 | D16 | | S36/COM4 | D36 |
| S17 | D17 | | S37/COM3 | D37 |
| S18 | D18 | | S38/COM2 | D38 |
| S19 | D19 | | | |
| S20 | D20 | | | |

Note) S36/COM4, S37/COM3 and S38/COM2 pins are selected segment output.

| East amountaile | the toble haloses | L'ata the a continuet atatas | fourthe CO1 continued in the |
|-----------------|-------------------|------------------------------|------------------------------|
| For example | The range below | insis the olimbilit states | s for the SZT olliptit pin |
| i or example, | | moto the output bluter | s for the S21 output pin. |

| Display data | | | | | | |
|--------------|---------------------------------|--|--|--|--|--|
| D21 | Output pin (S21) state | | | | | |
| 0 | The LCD segment to COM1 is off. | | | | | |
| 1 | The LCD segment to COM1 is on. | | | | | |

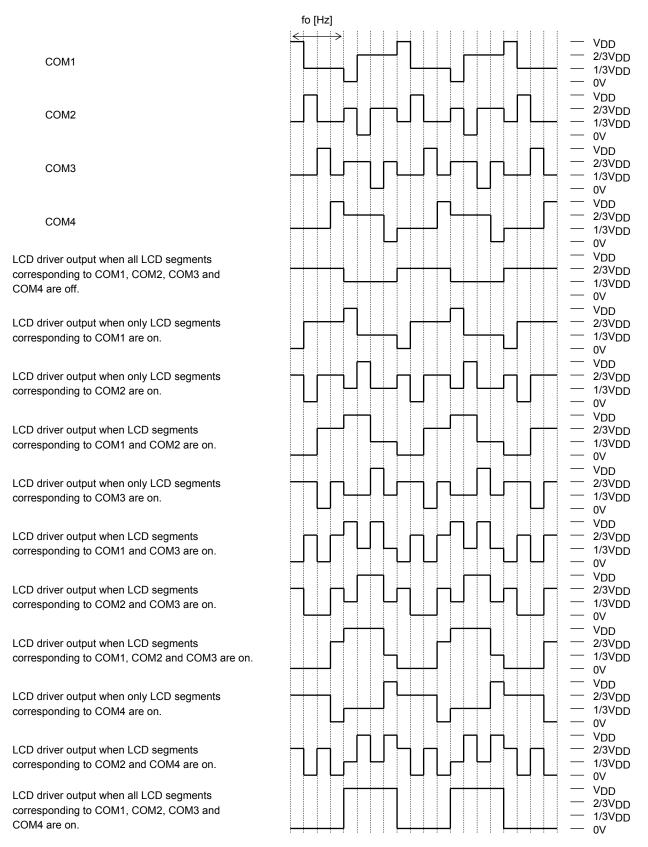
| Correspondence | e of output pins to | o di | splay data for | LED |
|----------------|---------------------|------|----------------|--------------|
| Output Pin | Display data | | Output Pin | Display data |
| LD1 | LT1 | | LD25 | LT25 |
| LD2 | LT2 | | LD26 | LT26 |
| LD3 | LT3 | | LD27 | LT27 |
| LD4 | LT4 | | LD28 | LT28 |
| LD5 | LT5 | | LD29 | LT29 |
| LD6 | LT6 | | LD30 | LT30 |
| LD7 | LT7 | | LD31 | LT31 |
| LD8 | LT8 | | LD32 | LT32 |
| LD9 | LT9 | | LD33 | LT33 |
| LD10 | LT10 | | LD34 | LT34 |
| LD11 | LT11 | | LD35 | LT35 |
| LD12 | LT12 | | LD36 | LT36 |
| LD13 | LT13 | | LD37 | LT37 |
| LD14 | LT14 | | LD38 | LT38 |
| LD15 | LT15 | | LD39 | LT39 |
| LD16 | LT16 | | LD40 | LT40 |
| LD17 | LT17 | | LD41 | LT41 |
| LD18 | LT18 | | LD42 | LT42 |
| LD19 | LT19 | | LD43 | LT43 |
| LD20 | LT20 | | LD44 | LT44 |
| LD21 | LT21 | | LD45 | LT45 |
| LD22 | LT22 | | LD46 | LT46 |
| LD23 | LT23 | | LD47 | LT47 |
| LD24 | LT24 | | LD48 | LT48 |

Correspondence of output pins to display data for LED

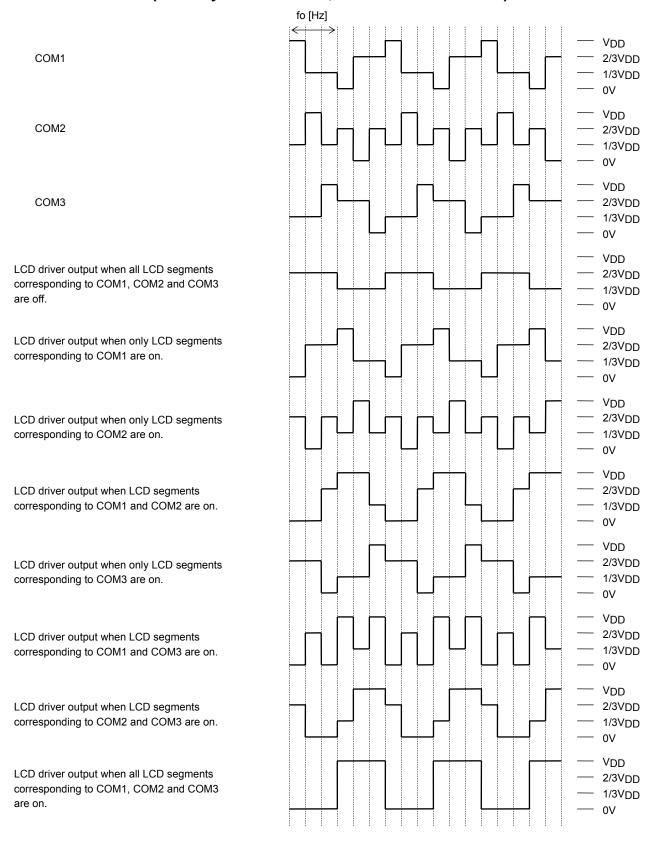
For example, the table below lists the output states for the LD21 output pin.

| Display data | Output pin (LD21) state |
|-----------------|--|
| LT21 | |
| 0 | LED is off. (High impedance output) |
| 1 | LED is on. Note) If (L21A, L21B, L21C) = (0, 0, 0) is set, the LED by 100% duty is on. If (L21A, L21B, L21C) = (1, 0, 0) is set, the LED depending on the contents of PWM data, W10 to W16, of PWM circuit (Ch1) is on. If (L21A, L21B, L21C) = (0, 1, 0) is set, the LED depending on the contents of PWM data, W20 to W26, of PWM circuit (Ch2) is on. If (L21A, L21B, L21C) = (1, 1, 0) is set, the LED depending on the contents of PWM data, W30 to W36, of PWM circuit (Ch3) is on. If (L21A, L21B, L21C) = (0, 0, 1) is set, the LED depending on the contents of PWM data, W40 to W46, of PWM circuit (Ch4) is on. If (L21A, L21B, L21C) = (0, 0, 1) is set, the LED depending on the contents of PWM data, W40 to W46, of PWM circuit (Ch4) is on. If (L21A, L21B, L21C) = (1, 0, 1) is set, the LED depending on the contents of PWM data, W50 to W56, of PWM circuit (Ch5) is on. If (L21A, L21B, L21C) = (0, 1, 1) is set, the LED depending on the contents of PWM data, W60 to W66, of PWM circuit (Ch6) is on. If (L21A, L21B, L21C) = (0, 1, 1) is set, the LED depending on the contents of PWM data, W60 to W66, of PWM circuit (Ch6) is on. If (L21A, L21B, L21C) = (1, 1, 1) is set, the LED depending on the contents of PWM data, W70 to W76, of PWM circuit (Ch7) is on. |

LCD drive waveform (1/4-Duty 1/3-Bias drive, Frame inversion drive)



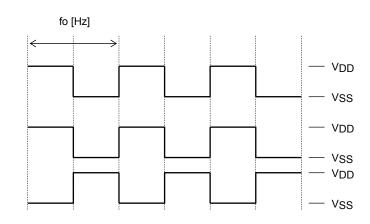
LCD drive waveform (1/3-Duty 1/3-Bias drive, Frame inversion drive)



LCD drive waveform (1/2-Duty 1/2-Bias drive, Frame inversion drive)

fo [Hz] VDD COM1 1/2VDD VSS VDD COM2 1/2VDD Vss - Vdd LCD driver output when all LCD segments corresponding to COM1 and COM2 are off. - Vss - Vdd LCD driver output when only LCD segments corresponding to COM1 are on. - Vss - VDD LCD driver output when only LCD segments corresponding to COM2 are on. - Vss - Vdd LCD driver output when all LCD segments corresponding to COM1 and COM2 are on. - Vss

LCD drive waveform (Static Drive)



COM1

LCD driver output when LCD segments are off.

LCD driver output when LCD segments are on.

| | | | | Frame frequency of common and s | egment output waveform fo [Hz] |
|-----|-----|-----|-----|---|--|
| FC0 | FC1 | FC2 | FC3 | Internal oscillator operating mode (Control data OC = "0", | External clock operating mode (Control data OC = "1", |
| 0 | 0 | 0 | 0 | fosc = 300 [kHz] typ) | $f_{CK} = 300 [\text{kHz}] \text{typ}$ |
| 0 | 0 | 0 | 0 | fosc/4992 | f _{CK} /4992 |
| 1 | 0 | 0 | 0 | fosc/4608 | f _{CK} /4608 |
| 0 | 1 | 0 | 0 | fosc/4224 | f _{CK} /4224 |
| 1 | 1 | 0 | 0 | fosc/3840 | f _{CK} /3840 |
| 0 | 0 | 1 | 0 | fosc/3456 | f _{CK} /3456 |
| 1 | 0 | 1 | 0 | fosc/3072 | f _{CK} /3072 |
| 0 | 1 | 1 | 0 | fosc/2688 | f _{CK} /2688 |
| 1 | 1 | 1 | 0 | fosc/2496 | f _{CK} /2496 |
| 0 | 0 | 0 | 1 | fosc/2448 | f _{CK} /2448 |
| 1 | 0 | 0 | 1 | fosc/2304 | f _{CK} /2304 |
| 0 | 1 | 0 | 1 | fosc/2112 | f _{CK} /2112 |
| 1 | 1 | 0 | 1 | fosc/1920 | f _{CK} /1920 |
| 0 | 0 | 1 | 1 | fosc/1728 | f _{CK} /1728 |
| 1 | 0 | 1 | 1 | fosc/1536 | f _{CK} /1536 |
| 0 | 1 | 1 | 1 | fosc/1344 | f _{CK} /1344 |
| 1 | 1 | 1 | 1 | fosc/1152 | f _{CK} /1152 |

LED drive waveform

| LD1 to LD6 (PWM Ch1) | < Lighting | | \rightarrow | ← | (4.4.4 | | | \rightarrow | — V _{OUP} — V _{SS} |
|--------------------------------|--|-----------------------------------|---------------|----------|---------|--------------|------------------|---------------|---|
| LD7 to LD12 (PWM Ch2) | | 3) × 1p g period > 28) × Tp | > | | ← | 2/128) : | | \rightarrow | — V _{OUP} — V _{SS} |
| LD13 to LD18 (PWM Ch3) | | ting perio /128) × Tr | _ | | (; ~ | | 28) × T | | |
| LD19 to LD24 (PWM Ch4) | | (16/128) | k i | < Lighti | ng per | iod > | 6/128) | _ ← | —————————————————————————————————————— |
| LD25 to LD30 (PWM Ch5) | | (32/128) | \rightarrow | < Lighti | ng per | iod > | , ← 2/128) | \rightarrow | —————————————————————————————————————— |
| LD31 to LD36 (PWM Ch6) | | (48/128) | \rightarrow | < Lighti | ng per | Ľ | < <u> </u> | × Tp | —————————————————————————————————————— |
| LD37 to LD42 (PWM Ch7) | Ĺ | ighting peri (64/128) | ~ | | | _< (6/ | 4/128) | → × Tp | —————————————————————————————————————— |
| LD43 to LD45 | < Continuous I | ights out > | > | | | | | | — V _{OUP} — V _{SS} |
| LD46 to LD48 | < Continuous | lighting > | | | | | | | — V _{OUP} — V _{SS} |
| | <tp< td=""><td></td><td></td><td></td><td></td><td>Тр</td><td></td><td>\rightarrow</td><td>Tp=$\frac{1}{\text{fp}}$</td></tp<> | | | | | Тр | | \rightarrow | Tp= $\frac{1}{\text{fp}}$ |
| | | | | | | | | | |
| | to L6B L1C to L6C | W10 | W11 | W12 | W13 | W14 0 | W15 | W16 | PWM (Ch) PWM Ch1, (112/128) x Tp |
| | 0 | 1 ' | ' | | ' | U | ' | ' | 1 WW OIT, (112/120) X IP |
| LT7 to LT12 L7A to L12A L7B to | D L12B L7C to L120 | C W20 | W21 | W22 | W23 | W24 | W25 | W26 | PWM (Ch) |
| 1 0 | 1 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | PWM Ch2, (96/128) x Tp |

| LT13 to LT18 | L13A to L18A | L13B to L18B | L13C to L18C | W30 | W31 | W32 | W33 | W34 | W35 | W36 | PWM (Ch) |
|--------------|----------------|----------------|----------------|-----|-----|-----|-----|-----|-----|-----|------------------------|
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | PWM Ch3, (80/128) x Tp |
| | | | | | | | | | | | |
| T19 to T24 | 1 19A to 1 24A | I 19B to I 24B | 1 19C to 1 24C | W40 | W41 | W42 | W43 | W44 | W45 | W46 | PWM (Ch) |

| LT19 to | LT24 | L19A to L24A | L19B to L24B | L19C to L24C | W40 | W41 | W42 | W43 | W44 | W45 | W46 | PWM (Ch) |
|---------|------|--------------|--------------|--------------|-----|-----|-----|-----|-----|-----|-----|------------------------|
| 1 | | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | PWM Ch4, (16/128) x Tp |

| 1 1 0 1 1 1 1 1 0 0 PWM Ch5, (32/128) x Tp | | LT25 to LT30 | L25A to L30A | L25B to L30B | L25C to L30C | W50 | W51 | W52 | W53 | W54 | W55 | W56 | PWM (Ch) |
|--|---|--------------|--------------|--------------|--------------|-----|-----|-----|-----|-----|-----|-----|------------------------|
| | ſ | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | PWM Ch5, (32/128) x Tp |

| [| LT31 to LT36 | L31A to L36A | L31B to L36B | L31C to L36C | W60 | W61 | W62 | W63 | W64 | W65 | W66 | PWM (Ch) |
|---|--------------|--------------|--------------|--------------|-----|-----|-----|-----|-----|-----|-----|------------------------|
| | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | PWM Ch6, (48/128) x Tp |

| LT37 to LT42 | L37A to L42A | L37B to L42B | L37C to L42C | W70 | W71 | W72 | W73 | W74 | W75 | W76 | PWM (Ch) |
|--------------|--------------|--------------|--------------|-----|-----|-----|-----|-----|-----|-----|------------------------|
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | PWM Ch7, (64/128) x Tp |

| LT43 to LT45 | L43A to L45A | L43B to L45B | L43C to L45C | PWM (Ch) |
|--------------|--------------|--------------|--------------|----------------------------|
| 0 | 0 | 0 | 0 | No select PWM, Turning off |

| LT46 to LT48 | L46A to L48A | L46B to L48B | L46C to L48C | PWM (Ch) |
|--------------|--------------|--------------|--------------|---------------------------|
| 1 | 0 | 0 | 0 | No select PWM, Turning on |

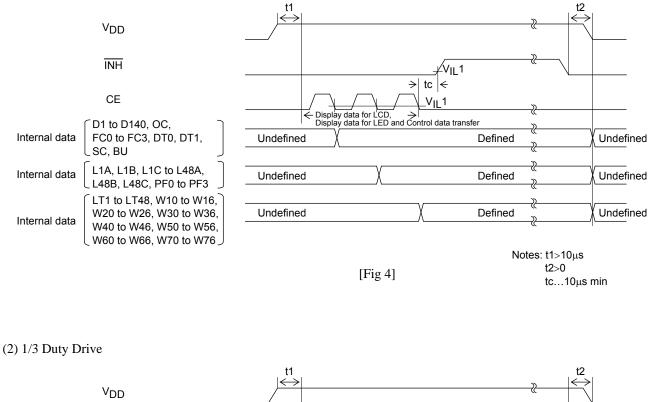
| PF0 | PF1 | PF2 | PF3 | Frame frequency of LED driver output waveform fp [Hz] | |
|-----|-----|-----|-----|---|---|
| | | | | Internal oscillator operating mode (Control data OC ="0", fosc = 300 [kHz] typ) | External clock operating mode (Control data OC ="1", f _{CK} = 300 [kHz] typ) |
| 0 | 0 | 0 | 0 | fosc/1664 | f _{CK} /1664 |
| 1 | 0 | 0 | 0 | fosc/1536 | f _{CK} /1536 |
| 0 | 1 | 0 | 0 | fosc/1408 | f _{CK} /1408 |
| 1 | 1 | 0 | 0 | fosc/1280 | f _{CK} /1280 |
| 0 | 0 | 1 | 0 | fosc/1152 | f _{CK} /1152 |
| 1 | 0 | 1 | 0 | fosc/1024 | f _{CK} /1024 |
| 0 | 1 | 1 | 0 | fosc/896 | f _{CK} /896 |
| 1 | 1 | 1 | 0 | fosc/768 | f _{CK} /768 |
| 0 | 0 | 0 | 1 | fosc/640 | f _{CK} /640 |
| 1 | 0 | 0 | 1 | fosc/512 | f _{CK} /512 |

Note) If (PF0, PF1, PF2, PF3) = (X, 1, 0, 1) or (X, X, 1, 1) are set, frame frequency (fosc/1408, f_{CK}/1408) of setting (PF0, PF1, PF2, PF3) = (0, 1, 0, 0) is selected.

Display Control and the INH Pin

Since the LSI internal data (1/4 Duty Drive: LCD display data D1 to D140 + LED display data LT1 to LT48 + control data, 1/3 Duty Drive: LCD display data D1 to D108 + LED display data LT1 to LT48 + control data, 1/2 Duty Drive: LCD display data D1 to D74 + LED display data LT1 to LT48 + control data, Static Drive: LCD display data D1 to D38 + LED display data LT1 to LT48 + control data) is undefined when power is first applied, applications should set the INH pin low at the same time as power is applied to turn off the display of LCD and LED (LD1 to LD48 • • • High impedance, COM1 and COM2/S38 to COM4/S36 and S35 to S1 • • • VSS level). The serial data is transferred from the controller during this period, and then input $\overline{INH} = "H"$ after the serial data is transferred. This procedure prevents meaningless display at power on. (See [Fig 4], [Fig 5], [Fig 6], [Fig 7])

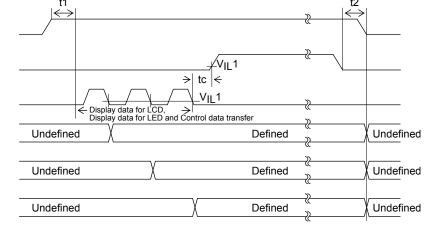
(1) 1/4 Duty Drive



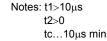


CE

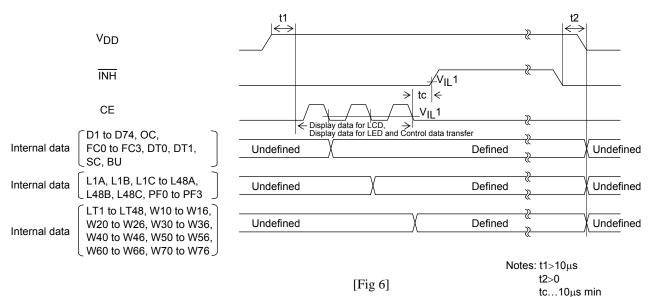
| Internal data | D1 to D108, OC, FC0 to FC3, DT0, DT1, SC, BU | |
|---------------|---|-------------|
| Internal data | L1A, L1B, L1C to L48A, L48B, L48C, PF0 to PF3 | |
| Internal data | LT1 to LT48, W10 to W16 W20 to W26, W30 to W36 W40 to W46, W50 to W56 W60 to W66, W70 to W76 | , , , |



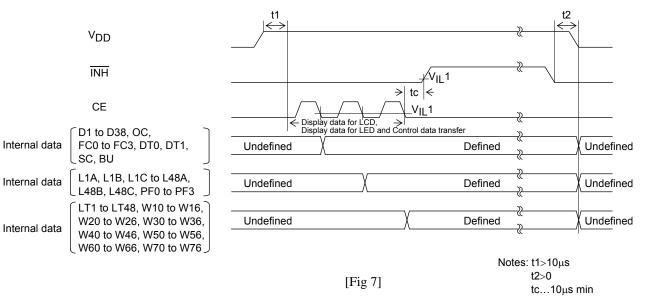
[Fig 5]



(3) 1/2 Duty Drive



(4) Static Drive (1/1 Duty Drive)

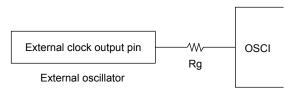


OSCI pin Peripheral Circuit

Internal oscillator operating mode (Control data OC ="0")
 Connect OSCI pin to GND if internal oscillator operating mode is selected.

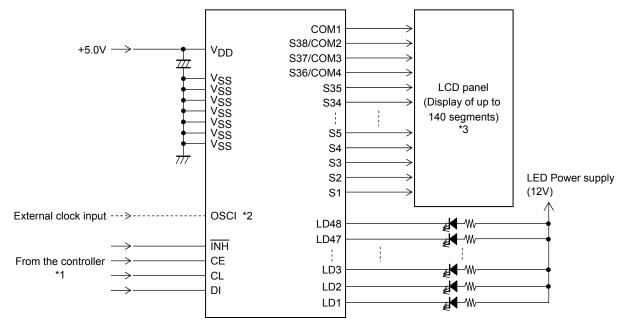


(2) External clock operating mode (Control data OC ="1") Input the external clock (f_{CK} = 100 to 600 [kHz]) to OSCI pin if external clock operating mode is selected.



Application Circuit Example 1

1/4-Duty, 1/3-Bias

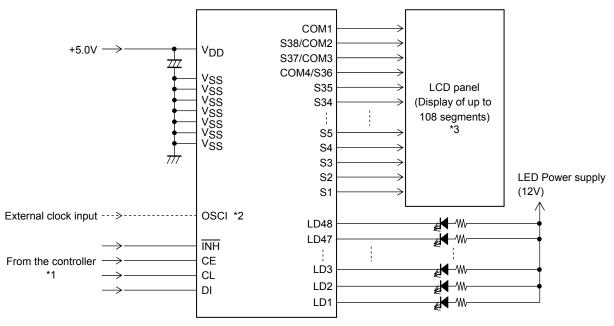


*1 Pins (CE, CL, DI, INH) connected to the controller are supported 5V.

- *2 External clock input pin OSCI is supported 5V. Connect to GND at internal oscillator operating mode, and input the external clock (f_{CK} = 100 to 600 [kHz]) to OSCI pin at external clock operating mode. (See "OSCI pin peripheral circuit")
- *3 Load capacity of the LCD panel is recommended 9000 [pF] or less.

Application Circuit Example 2

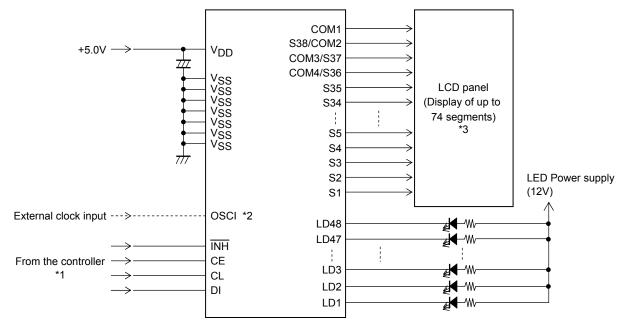
1/3-Duty, 1/3-Bias



- *1 Pins (CE, CL, DI, INH) connected to the controller are supported 5V.
- *2 External clock input pin OSCI is supported 5V. Connect to GND at internal oscillator operating mode, and input the external clock (f_{CK} = 100 to 600 [kHz]) to OSCI pin at external clock operating mode. (See "OSCI pin peripheral circuit")
- *3 Load capacity of the LCD panel is recommended 9000 [pF] or less.

Application Circuit Example 3

1/2-Duty, 1/2-Bias

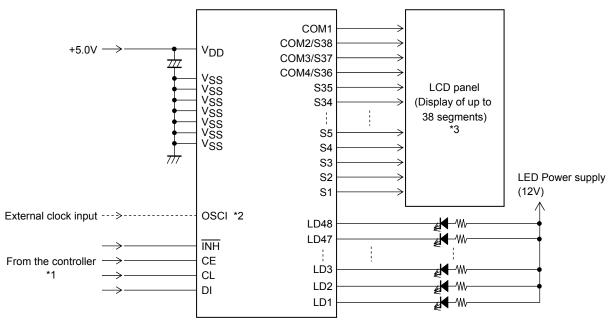


*1 Pins (CE, CL, DI, INH) connected to the controller are supported 5V.

- *2 External clock input pin OSCI is supported 5V. Connect to GND at internal oscillator operating mode, and input the external clock (f_{CK} = 100 to 600 [kHz]) to OSCI pin at external clock operating mode. (See "OSCI pin peripheral circuit")
- *3 Load capacity of the LCD panel is recommended 9000 [pF] or less.

Application Circuit Example 4

Static (1/1-Duty)



- *1 Pins (CE, CL, DI, INH) connected to the controller are supported 5V.
- *2 External clock input pin OSCI is supported 5V. Connect to GND at internal oscillator operating mode, and input the external clock (f_{CK} = 100 to 600 [kHz]) to OSCI pin at external clock operating mode. (See "OSCI pin peripheral circuit")
- *3 Load capacity of the LCD panel is recommended 9000 [pF] or less.

ORDERING INFORMATION

| Device | Package | Shipping (Qty / Packing) |
|---------------|--|--------------------------|
| LC75805PEH-3H | QIP100E(14X20) (Pb-Free / Halogen Free) | 250 / Tray Foam |
| LC75805PES-3H | QIP100E(14X20) (Pb-Free / Halogen Free) | 250 / Tray Foam |

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