



FAN54015

USB-Compliant Single-Cell Li-Ion Switching Charger with USB-OTG Boost Regulator

Features

- Fully Integrated, High-Efficiency Charger for Single-Cell Li-Ion and Li-Polymer Battery Packs
- Faster Charging than Linear
- Charge Voltage Accuracy: $\pm 0.5\%$ at 25°C
 $\pm 1\%$ from 0 to 125°C
- $\pm 5\%$ Input Current Regulation Accuracy
- $\pm 5\%$ Charge Current Regulation Accuracy
- 20 V Absolute Maximum Input Voltage
- 6 V Maximum Input Operating Voltage
- 1.45 A Maximum Charge Rate
- Programmable through High-Speed I²C Interface (3.4 Mb/s) with Fast Mode Plus Compatibility
 - Input Current
 - Fast-Charge / Termination Current
 - Charger Voltage
 - Termination Enable
- 3 MHz Synchronous Buck PWM Controller with Wide Duty Cycle Range
- Small Footprint 1 μH External Inductor
- Safety Timer with Reset Control
- 1.8 V Regulated Output from VBUS for Auxiliary Circuits
- Dynamic Input Voltage Control
- Low Reverse Leakage to Prevent Battery Drain to VBUS
- 5 V, 500 mA Boost Mode for USB OTG for 3.0 V to 4.5 V Battery Input
- Available in a 1.96 x 1.87 mm, 20-bump, 0.4 mm Pitch WLCSP Package

Applications

- Cell Phones, Smart Phones, PDAs
- Tablet, Portable Media Players
- Gaming Device, Digital Cameras

Description

The FAN54015 combines a highly integrated switch-mode charger, to minimize single-cell Lithium-ion (Li-ion) charging time from a USB power source, and a boost regulator to power a USB peripheral from the battery.

The charging parameters and operating modes are programmable through an I²C Interface that operates up to 3.4 Mbps. The charger and boost regulator circuits switch at 3 MHz to minimize the size of external passive components.

The FAN54015 provides battery charging in three phases: conditioning, constant current and constant voltage.

To ensure USB compliance and minimize charging time, the input current limit can be changed through the I²C by the host processor. Charge termination is determined by a programmable minimum current level. A safety timer with reset control provides a safety backup for the I²C host. Charge status is reported to the host through the I²C port.

The integrated circuit (IC) automatically restarts the charge cycle when the battery falls below an internal threshold. If the input source is removed, the IC enters a high-impedance mode, preventing leakage from the battery to the input. Charge current is reduced when the die temperature reaches 120°C , protecting the device and PCB from damage.

The FAN54015 can operate as a boost regulator on command from the system. The boost regulator includes a soft-start that limits inrush current from the battery and uses the same external components used for charging the battery.

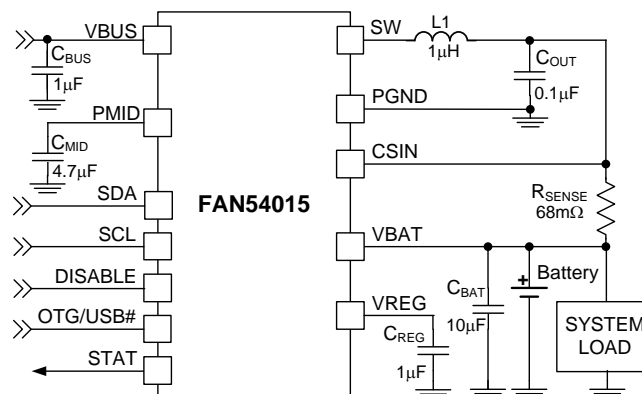


Figure 1. Typical Application

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Ordering Information

| Part Number | Temperature Range | Package | PN Bits: IC_INFO[4:2] | Packing Method |
|-----------------------------|-------------------|--|--------------------------|----------------|
| FAN54015UCX | -40 to 85°C | 20-Bump, Wafer-Level Chip-Scale Package (WLCSP), 0.4 mm Pitch, Estimated Size: 1.96 x 1.87 mm | 101 | Tape and Reel |
| FAN54015BUCX ⁽¹⁾ | | | | |

Note:

1. FAN54015BUCX includes backside lamination.

Table 1. Feature Summary

| Part Number | Slave Address | Automatic Charge | Special Charger ⁽²⁾ | Safety Limits | Battery Absent Behavior | E2 Pin | VREG (E3 Pin) |
|-------------|---------------|------------------|--------------------------------|---------------|-------------------------|---------|---------------|
| FAN54015UCX | 1101010 | Yes | Yes | Yes | ON | DISABLE | 1.8 V |

Note:

2. A “special charger” is a current-limited charger that is not a USB compliant source.

Block Diagram

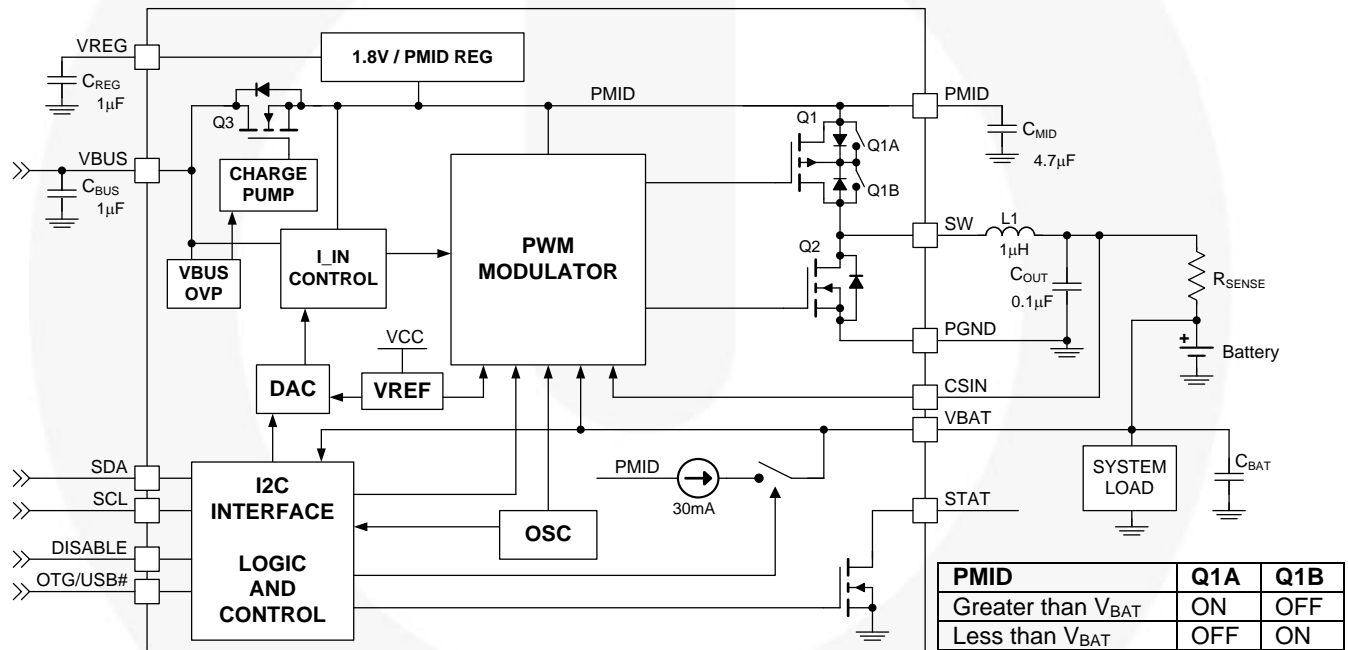


Figure 2. IC and System Block Diagram

Table 2. Recommended External Components

| Component | Description | Vendor | Parameter | Typ. | Unit |
|------------------|--|---|------------------|------|---------|
| L1 | 1 μ H \pm 20%, 1.6 A, DCR=55 m Ω , 2520 | Murata: LQM2HPN1R0 | L | 1.0 | μ H |
| | 1 μ H \pm 30%, 1.4 A, DCR=85 m Ω , 2016 | Murata: LQM2MPN1R0 | | | |
| C _{BAT} | 10 μ F, 20%, 6.3 V, X5R, 0603 | Murata: GRM188R60J106M TDK: C1608X5R0J106M | C | 10 | μ F |
| C _{MID} | 4.7 μ F, 10%, 6.3 V, X5R, 0603 | Murata: GRM188R60J475K TDK: C1608X5R0J475K | C ⁽³⁾ | 4.7 | μ F |
| C _{BUS} | 1.0 μ F, 10%, 25 V, X5R, 0603 | Murata GRM188R61E105K TDK: C1608X5R1E105M | C | 1.0 | μ F |

Note:

3. A 6.3 V rating is sufficient for C_{MID} because PMID is protected from over-voltage surges on VBUS by Q3 (Figure 2).

Pin Configuration



Figure 3. WLCSP-20 Pin Assignments

Pin Definitions

| Pin # | Name | Description |
|--------|---------|--|
| A1, A2 | VBUS | Charger Input Voltage and USB-OTG output voltage. Bypass with a 1 μ F capacitor to PGND. |
| A3 | NC | No Connect. No external connection is made between this pin and the IC's internal circuitry. |
| A4 | SCL | I²C Interface Serial Clock. This pin should not be left floating. |
| B1-B3 | PMID | Power Input Voltage. Power input to the charger regulator, bypass point for the input current sense, and high-voltage input switch. Bypass with a minimum of 4.7 μ F, 6.3 V capacitor to PGND. |
| B4 | SDA | I²C Interface Serial Data. This pin should not be left floating. |
| C1-C3 | SW | Switching Node. Connect to output inductor. |
| C4 | STAT | Status. Open-drain output indicating charge status. The IC pulls this pin LOW when charging. |
| D1-D3 | PGND | Power Ground. Power return for gate drive and power transistors. The connection from this pin to the bottom of C _{MID} should be as short as possible. |
| D4 | OTG | On-The-Go. Enables boost regulator in conjunction with OTG_EN and OTG_PL bits (see Table 16). On VBUS Power-On Reset (POR), this pin sets the input current limit for t _{15MIN} charging. |
| E1 | CSIN | Current-Sense Input. Connect to the sense resistor in series with the battery. The IC uses this node to sense current into the battery. Bypass this pin with a 0.1 μ F capacitor to PGND. |
| E2 | DISABLE | Charge Disable. If this pin is HIGH, charging is disabled. When LOW, charging is controlled by the I ² C registers. When this pin is HIGH, the 15-minute timer is reset. This pin does not affect the 32-second timer. |
| E3 | VREG | Regulator Output. Connect to a 1 μ F capacitor to PGND. This pin can supply up to 2mA of DC load current. The output voltage is PMID, which is limited to 1.8 V. |
| E4 | VBAT | Battery Voltage. Connect to the positive (+) terminal of the battery pack. Bypass with a 0.1 μ F capacitor to PGND if the battery is connected through long leads. |

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | | Min. | Max. | Unit |
|-----------------------|---|---------------------------------------|------|--------------------|------|
| V _{BUS} | VBUS Voltage | Continuous | −1.4 | 20.0 | V |
| | | Pulsed, 100 ms Maximum Non-Repetitive | −2.0 | | |
| V _{STAT} | STAT Voltage | | −0.3 | 16.0 | V |
| V _I | PMID Voltage | | | 7.0 | V |
| | SW, CSIN, VBAT, DISABLE Voltage | | −0.3 | 7.0 | |
| V _O | Voltage on Other Pins | | −0.3 | 6.5 ⁽⁴⁾ | V |
| $\frac{dV_{BUS}}{dt}$ | Maximum V _{BUS} Slope above 5.5 V when Boost or Charger are Active | | | 4 | V/μs |
| ESD | Electrostatic Discharge Protection Level | Human Body Model per JESD22-A114 | 2000 | | V |
| | | Charged Device Model per JESD22-C101 | 500 | | |
| T _J | Junction Temperature | | −40 | +150 | °C |
| T _{STG} | Storage Temperature | | −65 | +150 | °C |
| T _L | Lead Soldering Temperature, 10 Seconds | | | +260 | °C |

Note:

4. Lesser of 6.5 V or V_I + 0.3 V.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol | Parameter | | Min. | Max. | Unit |
|-----------------------|--|-----------------------|------|------|------|
| V _{BUS} | Supply Voltage | | 4 | 6 | V |
| V _{BAT(MAX)} | Maximum Battery Voltage when Boost enabled | | | 4.5 | V |
| $\frac{dV_{BUS}}{dt}$ | Negative V _{BUS} Slew Rate during V _{BUS} Short Circuit, C _{MID} ≤ 4.7 μF (see V _{BUS} Short While Charging) | T _A ≤ 60°C | | 4 | V/μs |
| | | T _A ≥ 60°C | | 2 | |
| T _A | Ambient Temperature | | −30 | +85 | °C |
| T _J | Junction Temperature (see Thermal Regulation and Protection section) | | −30 | +120 | °C |

Thermal Properties

Junction-to-ambient thermal resistance is a function of application and board layout. This data is measured with four-layer 2s2p boards in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature T_{J(max)} at a given ambient temperature T_A. For measured data, see Table 11.

| Symbol | Parameter | Typical | Unit |
|-----------------|--|---------|------|
| θ _{JA} | Junction-to-Ambient Thermal Resistance | 60 | °C/W |
| θ _{JB} | Junction-to-PCB Thermal Resistance | 20 | °C/W |

Electrical Specifications

Unless otherwise specified: according to the circuit of Figure 1; recommended operating temperature range for T_J and T_A ; $V_{BUS}=5.0$ V; HZ_MODE ; $OPA_MODE=0$; (Charge Mode); SCL , SDA , $OTG=0$ or 1.8 V; and typical values are for $T_J=25^\circ\text{C}$.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|--------------------------------------|---|---|-------|------|-------|------|
| Power Supplies | | | | | | |
| I _{VBUS} | VBUS Current | V _{BUS} > V _{BUS(min)} , PWM Switching | | 10 | | mA |
| | | V _{BUS} > V _{BUS(min)} ; PWM Enabled, Not Switching (Battery OVP Condition); I _{IN} Setting=100 mA | | 2.5 | | mA |
| | | 0°C < T _J < 85°C, HZ_MODE=1 V _{BAT} < V _{LOWV} , 32S Mode | | 63 | 90 | μA |
| I _{LKG} | VBAT to VBUS Leakage Current | 0°C < T _J < 85°C, HZ_MODE=1, V _{BAT} =4.2 V, V _{BUS} =0 V | | 0.2 | 5.0 | μA |
| I _{BAT} | Battery Discharge Current in High-Impedance Mode | 0°C < T _J < 85°C, HZ_MODE=1, V _{BAT} =4.2 V | | | 20 | μA |
| | | DISABLE=1, 0°C < T _J < 85°C, V _{BAT} =4.2 V | | | 10 | |
| Charger Voltage Regulation | | | | | | |
| V _{OREG} | Charge Voltage Range | | 3.5 | | 4.4 | V |
| | Charge Voltage Accuracy | T _A =25°C | −0.5% | | +0.5% | |
| | | T _J =0 to 125°C | −1% | | +1% | |
| Charging Current Regulation | | | | | | |
| I _{OCHRG} | Output Charge Current Range | V _{LOWV} < V _{BAT} < V _{OREG} , R _{SENSE} =68 mΩ | 550 | | 1450 | mA |
| | Charge Current Accuracy Across R _{SENSE} | 20 mV ≤ V _{I_{REG}} ≤ 40 mV | 92 | 97 | 102 | % |
| | | V _{I_{REG}} > 40 mV | 94 | 97 | 100 | % |
| Weak Battery Detection | | | | | | |
| V _{LOWV} | Weak Battery Threshold Range | | 3.4 | | 3.7 | V |
| | Weak Battery Threshold Accuracy | | −5 | | +5 | % |
| | Weak Battery Deglitch Time | Rising Voltage | | 30 | | ms |
| Logic Levels: DISABLE, SDA, SCL, OTG | | | | | | |
| V _{I_H} | High-Level Input Voltage | | 1.05 | | | V |
| V _{I_L} | Low-Level Input Voltage | | | | 0.4 | V |
| I _{IN} | Input Bias Current | Input Tied to GND or V _{IN} | | 0.01 | 1.00 | μA |
| Charge Termination Detection | | | | | | |
| I _(TERM) | Termination Current Range | V _{BAT} > V _{OREG} − V _{RCH} , R _{SENSE} =68 mΩ | 50 | | 400 | mA |
| | Termination Current Accuracy | [V _{CSIN} − V _{BAT}] from 3 mV to 20 mV | −25 | | +25 | % |
| | | [V _{CSIN} − V _{BAT}] from 20 mV to 40 mV | −5 | | +5 | |
| | Termination Current Deglitch Time | 2 mV Overdrive | | 30 | | ms |
| 1.8V Linear Regulator | | | | | | |
| V _{REG} | 1.8V Regulator Output | I _{REG} from 0 to 2 mA | 1.7 | 1.8 | 1.9 | V |
| Input Power Source Detection | | | | | | |
| V _{IN(MIN)1} | VBUS Input Voltage Rising | To Initiate and Pass VBUS Validation | | 4.29 | 4.42 | V |
| V _{IN(MIN)2} | Minimum VBUS During Charge | During Charging | | 3.71 | 3.94 | V |
| t _{VBUS_VALID} | VBUS Validation Time | | | 30 | | ms |

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Electrical Specifications

Unless otherwise specified: according to the circuit of Figure 1; recommended operating temperature range for T_J and T_A ; $V_{BUS}=5.0$ V; HZ_MODE ; $OPA_MODE=0$; (Charge Mode); SCL , SDA , $OTG=0$ or 1.8 V; and typical values are for $T_J=25^\circ\text{C}$.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|--|--|--|------|-------|------|------|
| Special Charger (V _{BUS}) | | | | | | |
| V _{SP} | Special Charger Setpoint Accuracy | | −3 | | +3 | % |
| Input Current Limit | | | | | | |
| I _{INLIM} | Input Current Limit Threshold | I _{IN} Set to 100 mA | 88 | 93 | 98 | mA |
| | | I _{IN} Set to 500 mA | 450 | 475 | 500 | |
| V _{REF} Bias Generator | | | | | | |
| V _{REF} | Bias Regulator Voltage | V _{BUS} > V _{IN(MIN)} or V _{BAT} > V _{BAT(MIN)} | | | 6.5 | V |
| | Short-Circuit Current Limit | | | 20 | | mA |
| Battery Recharge Threshold | | | | | | |
| V _{RCH} | Recharge Threshold | Below V _(OREG) | 100 | 120 | 150 | mV |
| | Deglitch Time | V _{BAT} Falling Below V _{RCH} Threshold | | 130 | | ms |
| STAT Output | | | | | | |
| V _{STAT(OL)} | STAT Output Low | I _{STAT} =10 mA | | | 0.4 | V |
| I _{STAT(OH)} | STAT High Leakage Current | V _{STAT} =5 V | | | 1 | μA |
| Battery Detection | | | | | | |
| I _{DETECT} | Battery Detection Current before Charge Done (Sink Current) ⁽⁵⁾ | Begins after Termination Detected and V _{BAT} ≤ V _{OREG} −V _{RCH} | | −0.80 | | mA |
| t _{DETECT} | Battery Detection Time | | | 262 | | ms |
| Sleep Comparator | | | | | | |
| V _{SLP} | Sleep-Mode Entry Threshold, V _{BUS} − V _{BAT} | 2.3 V ≤ V _{BAT} ≤ V _{OREG} , V _{BUS} Falling | 0 | 0.04 | 0.10 | V |
| t _{SLP_EXIT} | Deglitch Time for V _{BUS} Rising Above V _{BAT} by V _{SLP} | Rising Voltage | | 30 | | ms |
| Power Switches (see Figure 2) | | | | | | |
| R _{DS(ON)} | Q3 On Resistance (V _{BUS} to PMID) | I _{IN(LIMIT)} =500 mA | | 180 | 250 | mΩ |
| | Q1 On Resistance (PMID to SW) | | | 130 | 225 | |
| | Q2 On Resistance (SW to GND) | | | 150 | 225 | |
| Charger PWM Modulator | | | | | | |
| f _{SW} | Oscillator Frequency | | 2.7 | 3.0 | 3.3 | MHz |
| D _{MAX} | Maximum Duty Cycle | | | | 100 | % |
| D _{MIN} | Minimum Duty Cycle | | | 0 | | % |
| I _{SYNC} | Synchronous to Non-Synchronous Current Cut-Off Threshold ⁽⁶⁾ | Low-Side MOSFET (Q2) Cycle-by-Cycle Current Limit | | 140 | | mA |
| Boost Mode Operation (OPA_MODE=1, HZ_MODE=0) | | | | | | |
| V _{BOOST} | Boost Output Voltage at V _{BUS} | 2.5 V < V _{BAT} < 4.5 V, I _{LOAD} from 0 to 200 mA | 4.80 | 5.07 | 5.17 | V |
| | | 3.0 V < V _{BAT} < 4.5 V, I _{LOAD} from 0 to 500 mA | 4.77 | 5.07 | 5.17 | |
| I _{BAT(BOOST)} | Boost Mode Quiescent Current | PFM Mode, V _{BAT} =3.6 V, I _{OUT} =0 | | 140 | 300 | μA |
| I _{LIMPK(BST)} | Q2 Peak Current Limit | | 1272 | 1590 | 1908 | mA |
| UVLO _{BST} | Minimum Battery Voltage for Boost Operation | While Boost Active | | 2.42 | | V |
| | | To Start Boost Regulator | | 2.58 | 2.70 | |

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Electrical Specifications

Unless otherwise specified: according to the circuit of Figure 1; recommended operating temperature range for T_J and T_A ; $V_{BUS}=5.0$ V; HZ_MODE ; $OPA_MODE=0$; (Charge Mode); SCL, SDA, OTG=0 or 1.8 V; and typical values are for $T_J=25^\circ\text{C}$.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|-------------------------|---|---------------------------------------|------|------|------|------|
| VBUS Load Resistance | | | | | | |
| R _{VBUS} | VBUS to PGND Resistance | Normal Operation | | 1500 | | kΩ |
| | | Charger Validation | | 100 | | Ω |
| Protection and Timers | | | | | | |
| VBUS _{OVP} | VBUS Over-Voltage Shutdown | V _{BUS} Rising | 6.09 | 6.29 | 6.49 | V |
| | Hysteresis | V _{BUS} Falling | | 100 | | mV |
| I _{LIMPK(CHG)} | Q1 Cycle-by-Cycle Peak Current Limit | Charge Mode | | 2.3 | | A |
| V _{SHORT} | Battery Short-Circuit Threshold | V _{BAT} Rising | 1.95 | 2.00 | 2.05 | V |
| | Hysteresis | V _{BAT} Falling | | 100 | | mV |
| I _{SHORT} | Linear Charging Current | V _{BAT} < V _{SHORT} | 20 | 30 | 40 | mA |
| T _{SHUTDWN} | Thermal Shutdown Threshold ⁽⁷⁾ | T _J Rising | | 145 | | °C |
| | Hysteresis ⁽⁷⁾ | T _J Falling | | 10 | | |
| T _{CF} | Thermal Regulation Threshold ⁽⁷⁾ | Charge Current Reduction Begins | | 120 | | °C |
| t _{INT} | Detection Interval | | | 2.1 | | s |
| t _{32S} | 32-Second Timer ⁽⁸⁾ | Charger Enabled | 20.5 | 25.2 | 28.0 | s |
| | | Charger Disabled | 18.0 | 25.2 | 34.0 | |
| t _{15MIN} | 15-Minute Timer | 15-Minute Mode | 12.0 | 13.5 | 15.0 | min |
| Δt _{LF} | Low-Frequency Timer Accuracy | Charger Inactive | −25 | | 25 | % |

Notes:

- Negative current is current flowing from the battery to VBUS (discharging the battery).
- Q2 always turns on for 60 ns, then turns off if current is below I_{SYNC} .
- Guaranteed by design; not tested in production.
- This tolerance (%) applies to all timers on the IC, including soft-start and deglitching timers.

I²C Timing Specifications

Guaranteed by design.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---------------------------------------|--|--|----------------------|------|------|------|
| f _{SCL} | SCL Clock Frequency | Standard Mode | | | 100 | kHz |
| | | Fast Mode | | | 400 | |
| | | High-Speed Mode, C _B ≤ 100 pF | | | 3400 | |
| | | High-Speed Mode, C _B ≤ 400 pF | | | 1700 | |
| t _{BUF} | Bus-Free Time between STOP and START Conditions | Standard Mode | | 4.7 | | μs |
| | | Fast Mode | | 1.3 | | |
| t _{HD;STA} | START or Repeated START Hold Time | Standard Mode | | 4 | | μs |
| | | Fast Mode | | 600 | | ns |
| | | High-Speed Mode | | 160 | | ns |
| t _{LOW} | SCL LOW Period | Standard Mode | | 4.7 | | μs |
| | | Fast Mode | | 1.3 | | μs |
| | | High-Speed Mode, C _B ≤ 100 pF | | 160 | | ns |
| | | High-Speed Mode, C _B ≤ 400 pF | | 320 | | ns |
| t _{HIGH} | SCL HIGH Period | Standard Mode | | 4 | | μs |
| | | Fast Mode | | 600 | | ns |
| | | High-Speed Mode, C _B ≤ 100 pF | | 60 | | ns |
| | | High-Speed Mode, C _B ≤ 400 pF | | 120 | | ns |
| t _{SU;STA} | Repeated START Setup Time | Standard Mode | | 4.7 | | μs |
| | | Fast Mode | | 600 | | ns |
| | | High-Speed Mode | | 160 | | ns |
| t _{SU;DAT} | Data Setup Time | Standard Mode | | 250 | | ns |
| | | Fast Mode | | 100 | | |
| | | High-Speed Mode | | 10 | | |
| t _{HD;DAT} | Data Hold Time | Standard Mode | 0 | | 3.45 | μs |
| | | Fast Mode | 0 | | 900 | ns |
| | | High-Speed Mode, C _B ≤ 100 pF | 0 | | 70 | ns |
| | | High-Speed Mode, C _B ≤ 400 pF | 0 | | 150 | ns |
| t _{RCL} | SCL Rise Time | Standard Mode | 20+0.1C _B | | 1000 | ns |
| | | Fast Mode | 20+0.1C _B | | 300 | |
| | | High-Speed Mode, C _B ≤ 100 pF | | 10 | 80 | |
| | | High-Speed Mode, C _B ≤ 400 pF | | 20 | 160 | |
| t _{FCL} | SCL Fall Time | Standard Mode | 20+0.1C _B | | 300 | ns |
| | | Fast Mode | 20+0.1C _B | | 300 | |
| | | High-Speed Mode, C _B ≤ 100 pF | | 10 | 40 | |
| | | High-Speed Mode, C _B ≤ 400 pF | | 20 | 80 | |
| t _{RDA} t _{RCL1} | SDA Rise Time Rise Time of SCL after a Repeated START Condition and after ACK Bit | Standard Mode | 20+0.1C _B | | 1000 | ns |
| | | Fast Mode | 20+0.1C _B | | 300 | |
| | | High-Speed Mode, C _B ≤ 100 pF | | 10 | 80 | |
| | | High-Speed Mode, C _B ≤ 400 pF | | 20 | 160 | |

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I²C Timing Specifications

Guaranteed by design.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|--------------|------------------------------|------------------------------------|------|-------------|------|---------|
| t_{FDA} | SDA Fall Time | Standard Mode | | $20+0.1C_B$ | 300 | ns |
| | | Fast Mode | | $20+0.1C_B$ | 300 | |
| | | High-Speed Mode, $C_B \leq 100$ pF | | 10 | 80 | |
| | | High-Speed Mode, $C_B \leq 400$ pF | | 20 | 160 | |
| $t_{SU;STO}$ | Stop Condition Setup Time | Standard Mode | | 4 | | μ s |
| | | Fast Mode | | 600 | | ns |
| | | High-Speed Mode | | 160 | | ns |
| C_B | Capacitive Load for SDA, SCL | | | | 400 | pF |

Timing Diagrams

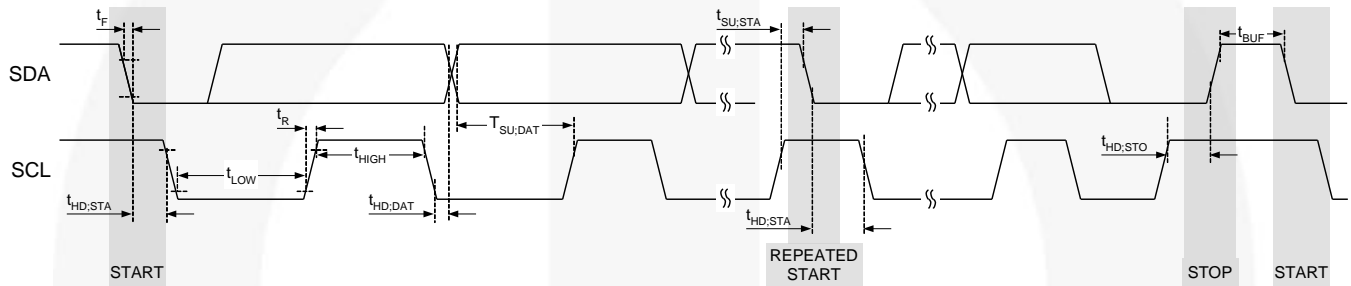
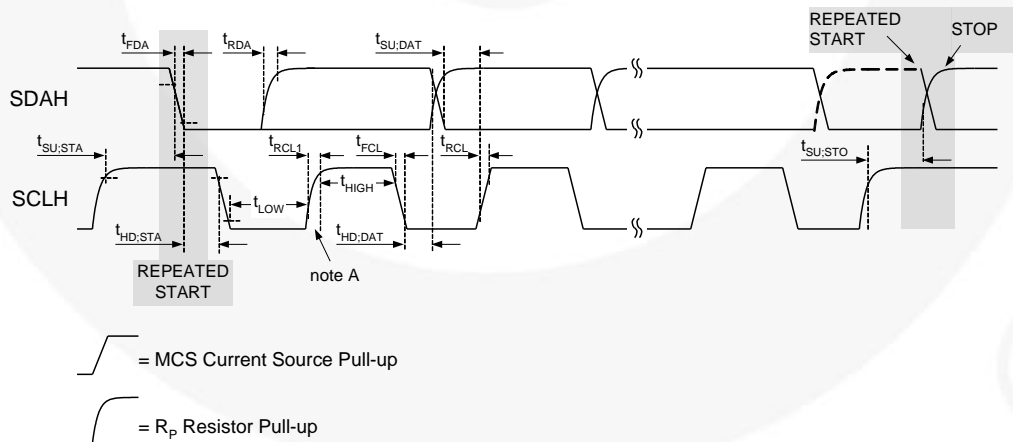


Figure 4. I²C Interface Timing for Fast and Slow Modes



Note A: First rising edge of SCLH after Repeated Start and after each ACK bit.

Figure 5. I²C Interface Timing for High-Speed Mode

Charge Mode Typical Characteristics

Unless otherwise specified, circuit of Figure 1, $V_{OREG}=4.2\text{ V}$, $V_{BUS}=5.0\text{ V}$, and $T_A=25^\circ\text{C}$.

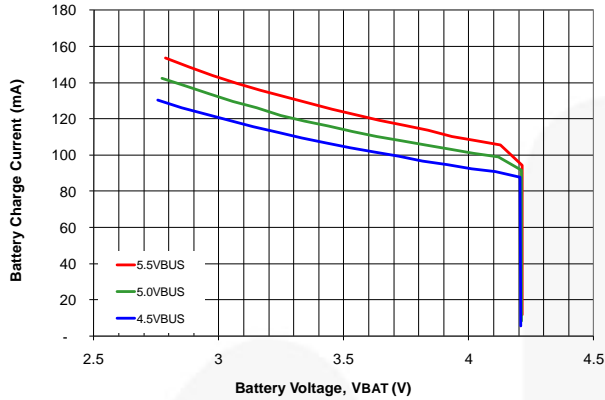


Figure 6. Battery Charge Current vs. V_{BUS} with $I_{INLIM}=100\text{ mA}$

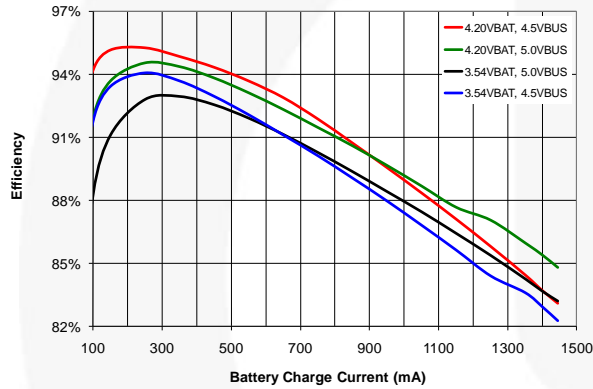


Figure 8. Charger Efficiency, No I_{INLIM} , $I_{CHARGE}=1450\text{ mA}$

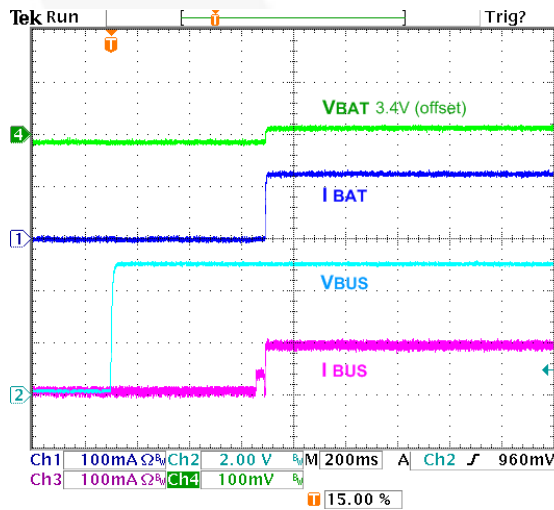


Figure 10. Auto-Charge Startup at V_{BUS} Plug-in, $I_{INLIM}=100\text{ mA}$, $OTG=1$, $V_{BAT}=3.4\text{ V}$

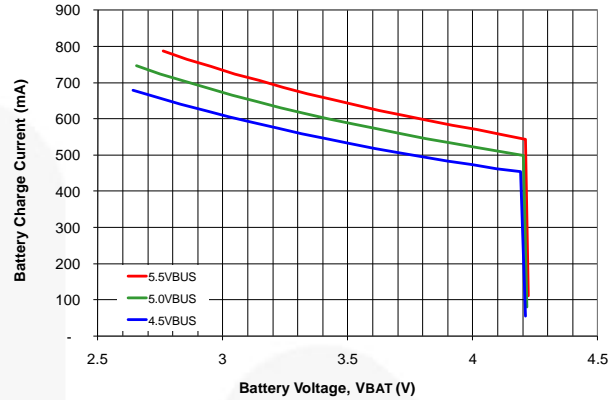


Figure 7. Battery Charge Current vs. V_{BUS} with $I_{INLIM}=500\text{ mA}$

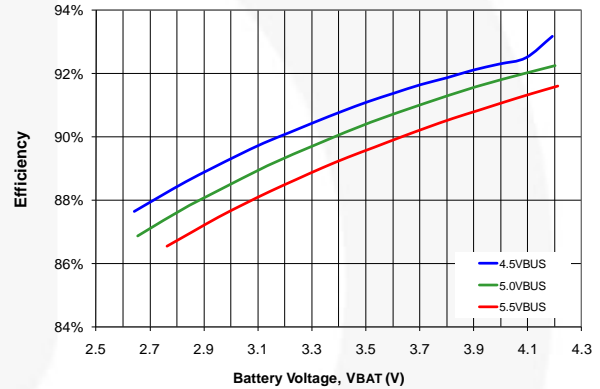


Figure 9. Charger Efficiency vs. V_{BUS} , $I_{INLIM}=500\text{ mA}$

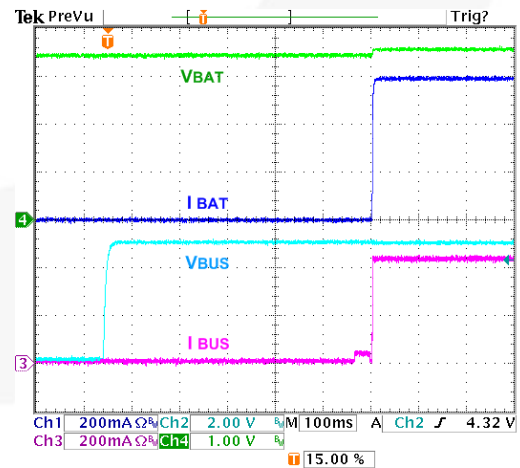


Figure 11. Auto-Charge Startup at V_{BUS} Plug-in, $I_{INLIM}=500\text{ mA}$, $OTG=1$, $V_{BAT}=3.4\text{ V}$

Charge Mode Typical Characteristics

Unless otherwise specified, circuit of Figure 1, $V_{OREG}=4.2\text{ V}$, $V_{BUS}=5.0\text{ V}$, and $T_A=25^\circ\text{C}$.

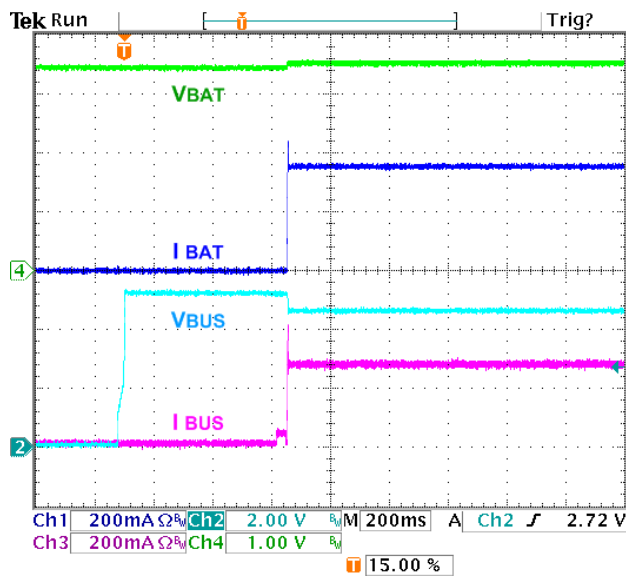


Figure 12. AutoCharge Startup with 300mA Limited Charger / Adaptor, $I_{NLIM}=500\text{ mA}$, $OTG=1$, $V_{BAT}=3.4\text{ V}$

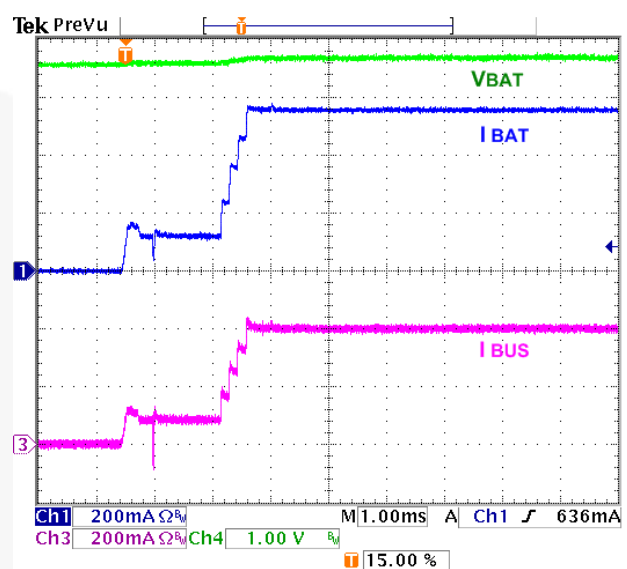


Figure 13. Charger Startup with HZ_MODE Bit Reset, $I_{NLIM}=500\text{ mA}$, $I_{OCHARGE}=1050\text{ mA}$, $OREG=4.2\text{ V}$, $V_{BAT}=3.6\text{ V}$

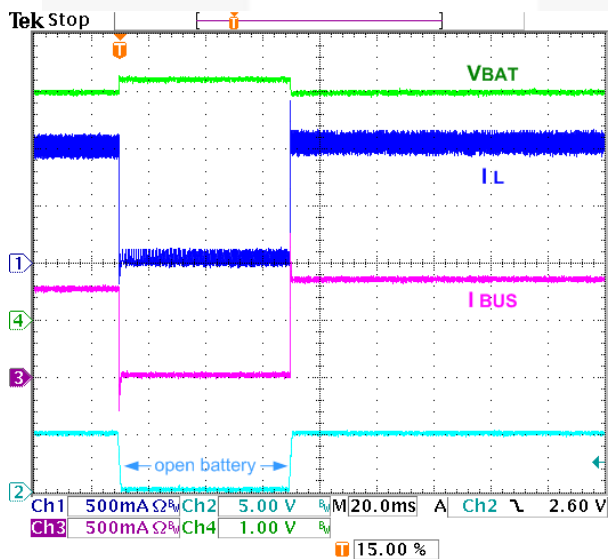


Figure 14. Battery Removal / Insertion During Charging, $V_{BAT}=3.9\text{ V}$, $I_{OCHARGE}=1050\text{ mA}$, No I_{NLIM} , $TE=0$

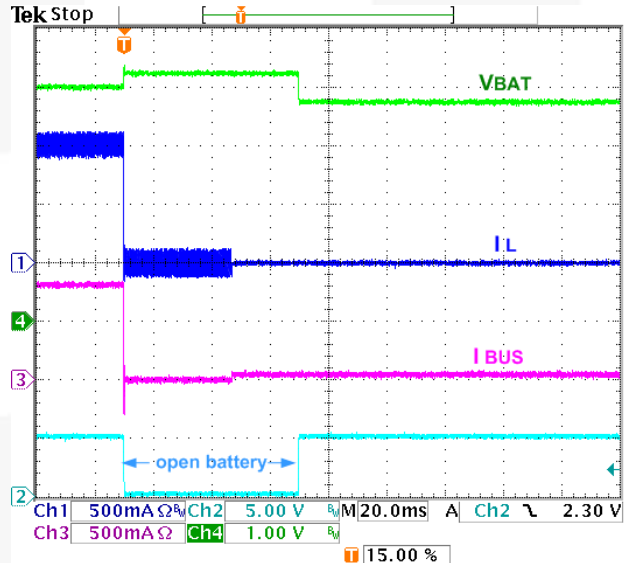


Figure 15. Battery Removal / Insertion During Charging, $V_{BAT}=3.9\text{ V}$, $I_{OCHARGE}=1050\text{ mA}$, No I_{NLIM} , $TE=1$

Charge Mode Typical Characteristics

Unless otherwise specified, circuit of Figure 1, $V_{OREG}=4.2\text{ V}$, $V_{BUS}=5.0\text{ V}$, and $T_A=25^\circ\text{C}$.

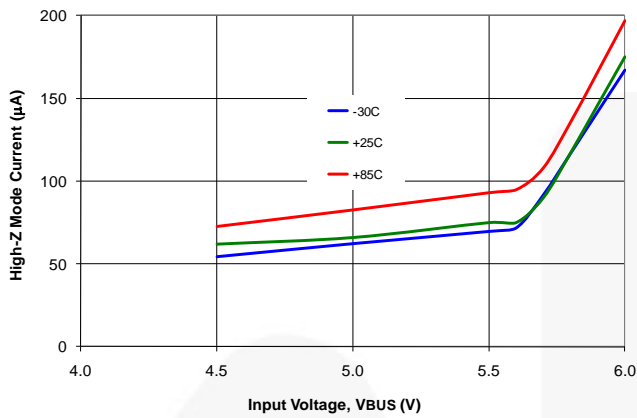


Figure 16. V_{BUS} Current in High-Impedance Mode with Battery Open

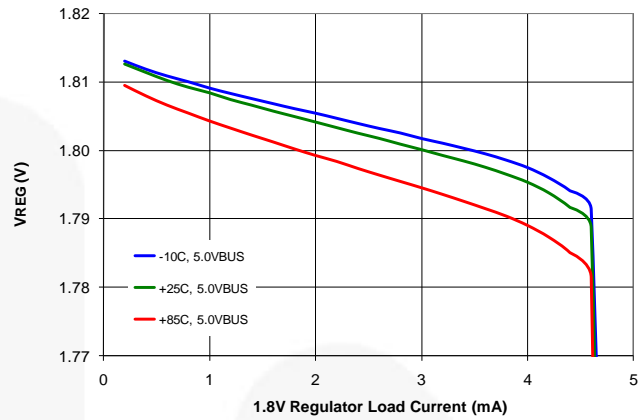


Figure 17. V_{REG} 1.8 V Output Regulation

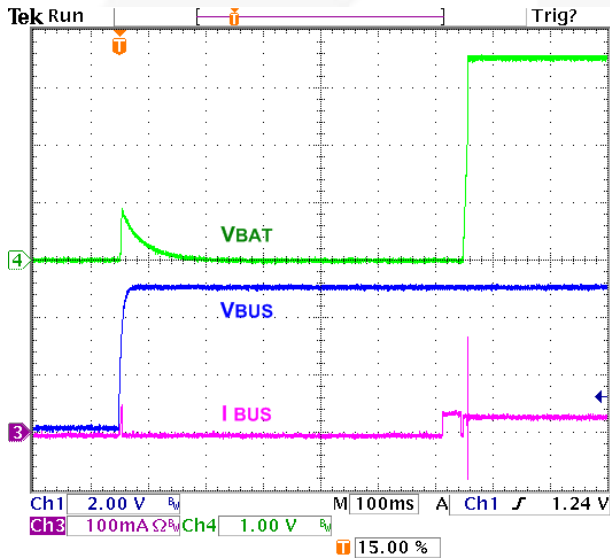


Figure 18. No Battery, V_{BUS} at Power Up

Boost Mode Typical Characteristics

Unless otherwise specified, using circuit of Figure 1, $V_{BAT}=3.6\text{ V}$, $T_A=25^\circ\text{C}$.

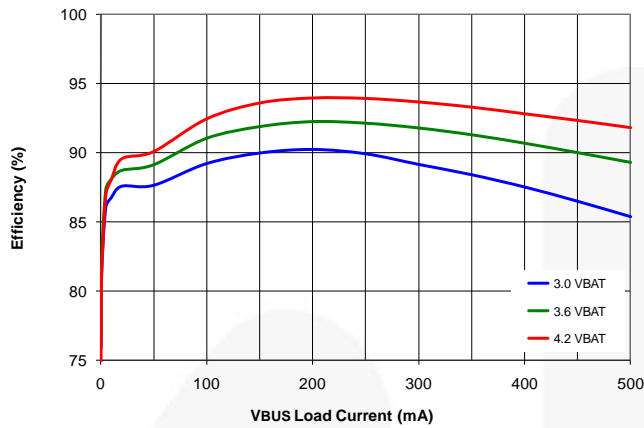


Figure 19. Efficiency vs. V_{BAT}

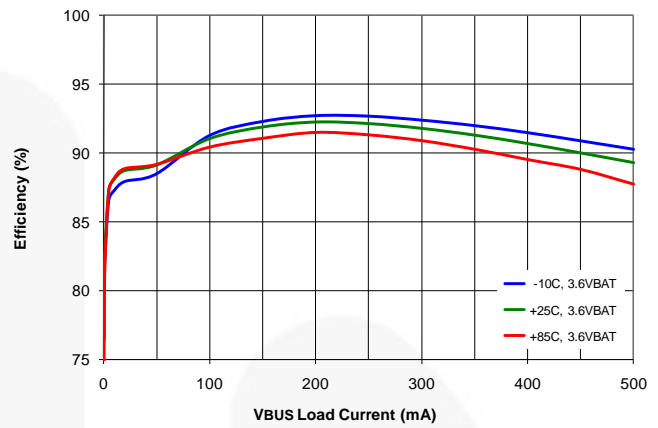


Figure 20. Efficiency Over Temperature

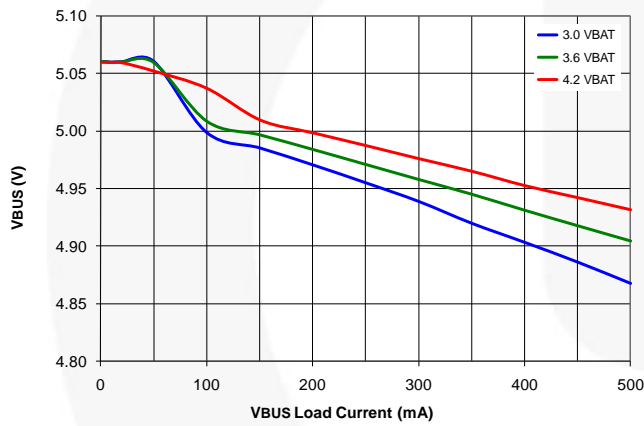


Figure 21. Output Regulation vs. V_{BAT}

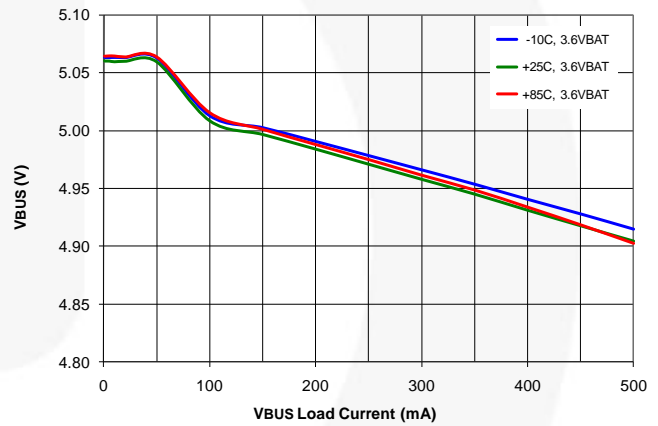


Figure 22. Output Regulation Over Temperature

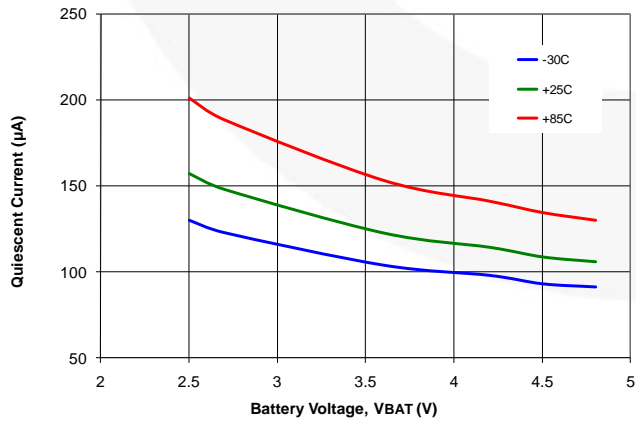


Figure 23. Quiescent Current

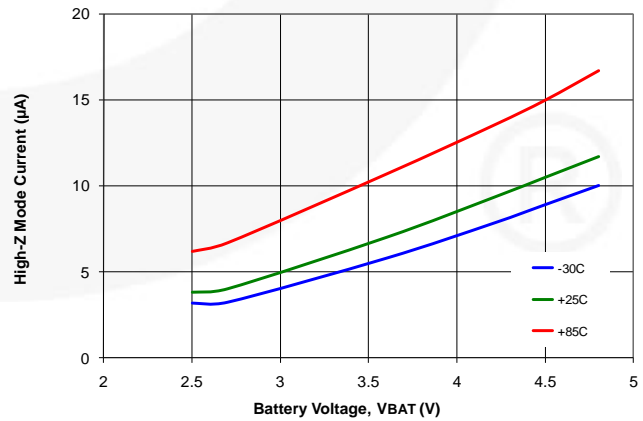


Figure 24. High-Impedance Mode Battery Current

Boost Mode Typical Characteristics

Unless otherwise specified, using circuit of Figure 1, $V_{BAT}=3.6\text{ V}$, $T_A=25^\circ\text{C}$.

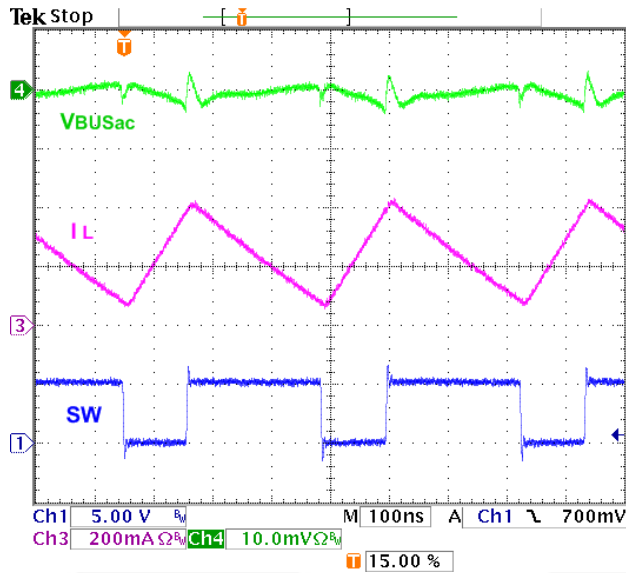


Figure 25. Boost PWM Waveform

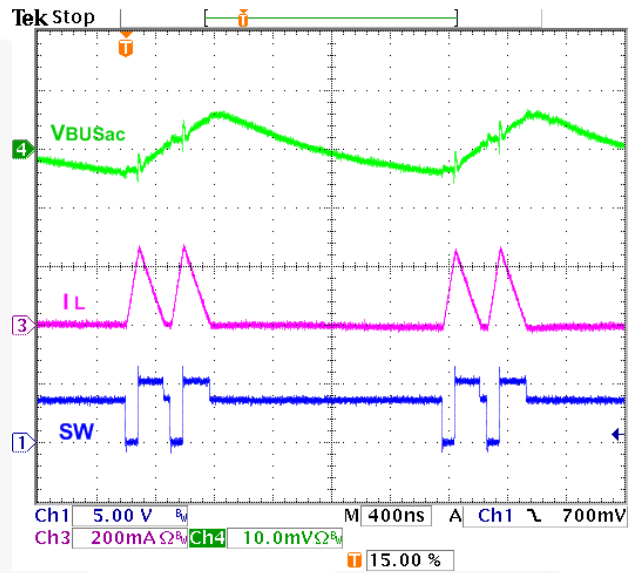


Figure 26. Boost PFM Waveform

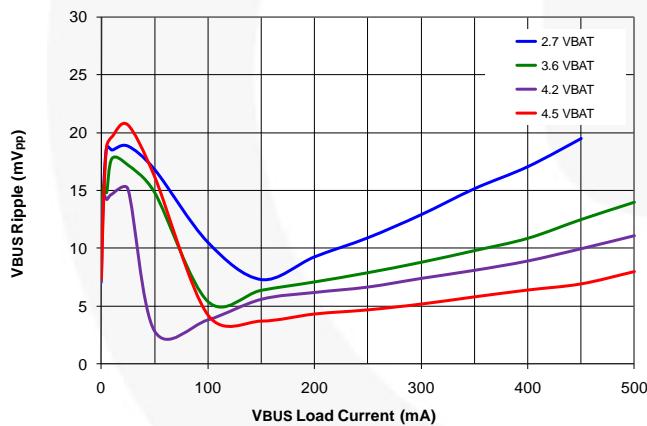


Figure 27. Output Ripple vs. V_{BAT}

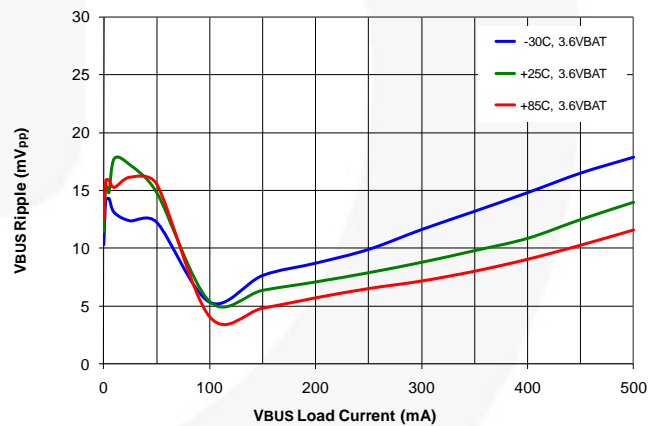


Figure 28. Output Ripple vs. Temperature

Boost Mode Typical Characteristics

Unless otherwise specified, using circuit of Figure 1, $V_{BAT}=3.6\text{ V}$, $T_A=25^\circ\text{C}$.

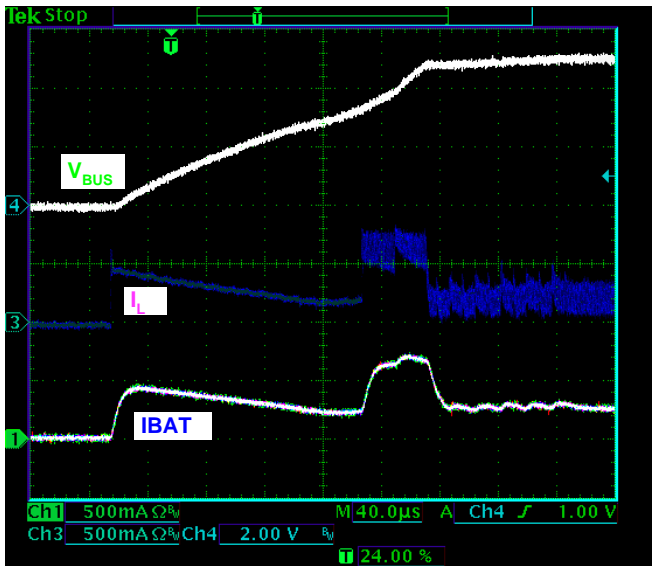


Figure 29. Startup, 3.6 V_{BAT} , $44\ \Omega$ Load, Additional $10\ \mu\text{F}$, X5R Across V_{BUS}

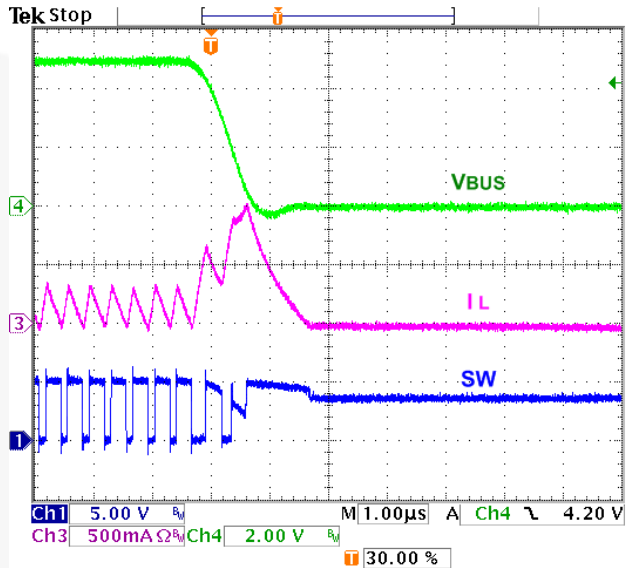


Figure 30. V_{BUS} Fault Response, 3.6 V_{BAT}

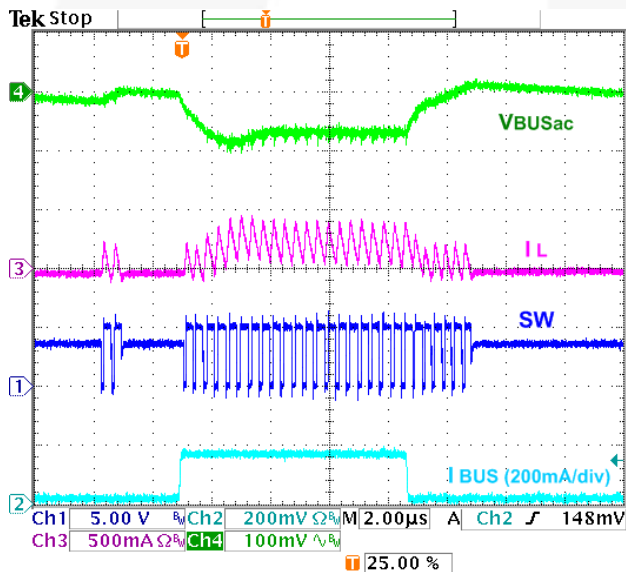


Figure 31. Load Transient, 5-155-5 mA, $t_R=t_F=100\text{ ns}$

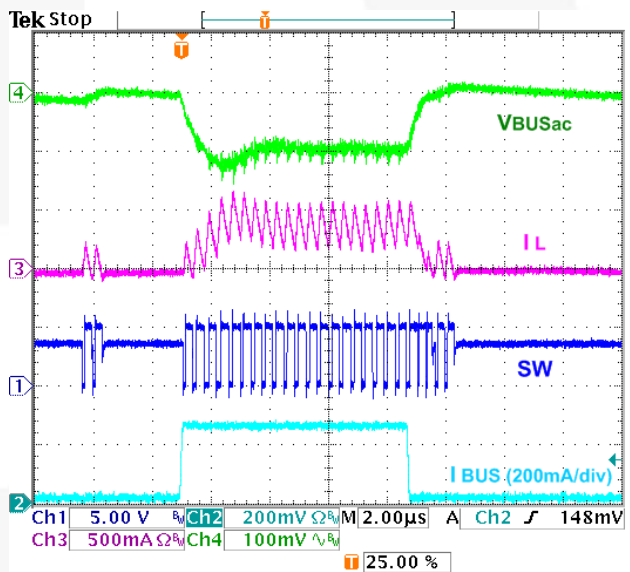


Figure 32. Load Transient, 5-255-5 mA, $t_R=t_F=100\text{ ns}$

Circuit Description / Overview

When charging batteries with a current-limited input source, such as USB, a switching charger's high efficiency over a wide range of output voltages minimizes charging time.

FAN54015 combines a highly integrated synchronous buck regulator for charging with a synchronous boost regulator, which can supply 5 V to USB On-The-Go (OTG) peripherals. The regulator employs synchronous rectification for both the charger and boost regulators to maintain high efficiency over a wide range of battery voltages and charge states.

The FAN54015 has three operating modes:

1. **Charge Mode:**
Charges a single-cell Li-ion or Li-polymer battery.
2. **Boost Mode:**
Provides 5 V power to USB-OTG with an integrated synchronous rectification boost regulator using the battery as input.
3. **High-Impedance Mode:**
Both the boost and charging circuits are OFF in this mode. Current flow from VBUS to the battery or from the battery to VBUS is blocked in this mode. This mode consumes very little current from VBUS or the battery.

Note: Default settings are denoted by **bold typeface**.

Charge Mode

In Charge Mode, FAN54015 employs four regulation loops:

1. **Input Current:** Limits the amount of current drawn from VBUS. This current is sensed internally and can be programmed through the I²C interface.
2. **Charging Current:** Limits the maximum charging current. This current is sensed using an external R_{SENSE} resistor.
3. **Charge Voltage:** The regulator is restricted from exceeding this voltage. As the internal battery voltage rises, the battery's internal impedance and R_{SENSE} work in conjunction with the charge voltage regulation to decrease the amount of current flowing to the battery. Battery charging is completed when the voltage across R_{SENSE} drops below the I_{TERM} threshold.
4. **Temperature:** If the IC's junction temperature reaches 120°C, charge current is reduced until the IC's temperature stabilizes at 120°C.
5. An additional loop limits the amount of drop on VBUS to a programmable voltage (V_{SP}) to accommodate "special chargers" that limit current to a lower current than might be available from a "normal" USB wall charger.

Battery Charging Curve

If the battery voltage is below V_{SHORT}, a linear current source pre-charges the battery until V_{BAT} reaches V_{SHORT}. The PWM charging circuit is then started and the battery is charged with a constant current if sufficient input power is available. The current slew rate is limited to prevent overshoot.

The FAN54015 is designed to work with a current-limited input source at VBUS. During the current regulation phase of charging, I_{INLIM} or the programmed charging current limits the amount of current available to charge the battery and power the system. The effect of I_{INLIM} on I_{CHARGE} can be seen in Figure 34.

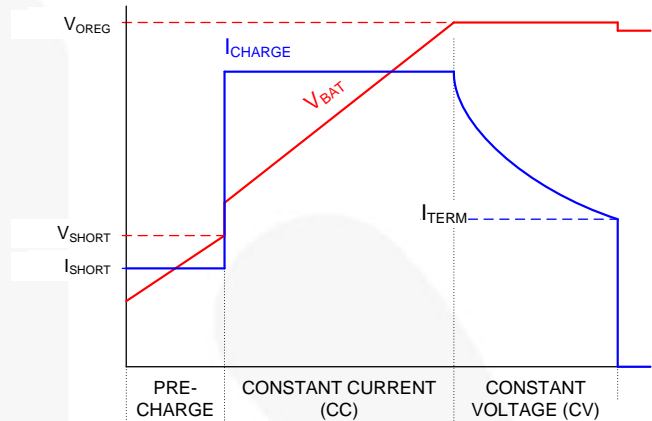


Figure 33. Charge Curve, I_{CHARGE} Not Limited by I_{INLIM}

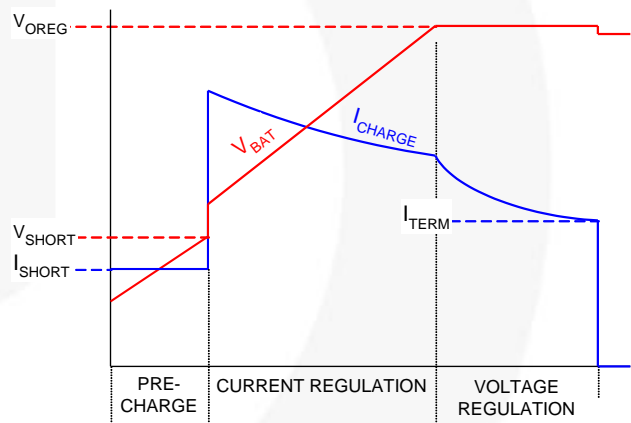


Figure 34. Charge Curve, I_{INLIM} Limits I_{CHARGE}

Assuming that V_{OREG} is programmed to the cell's fully charged "float" voltage, the current that the battery accepts with the PWM regulator limiting its output (sensed at V_{BAT}) to V_{OREG} declines, and the charger enters the voltage regulation phase of charging. When the current declines to the programmed I_{TERM} value, the charge cycle is complete. Charge current termination can be disabled by resetting the TE bit (REG1[3]).

The charger output or "float" voltage can be programmed by the OREG bits from 3.5 V to 4.44 V in 20 mV increments, as shown in Table 3.

Table 3. OREG Bits (OREG[7:2]) vs. Charger V_{OUT} (V_{OREG}) Float Voltage

| Decimal | Hex | VOREG | Decimal | Hex | VOREG |
|---------|-----|-------|---------|-----|-------|
| 0 | 00 | 3.50 | 32 | 20 | 4.14 |
| 1 | 01 | 3.52 | 33 | 21 | 4.16 |
| 2 | 02 | 3.54 | 34 | 22 | 4.18 |
| 3 | 03 | 3.56 | 35 | 23 | 4.20 |
| 4 | 04 | 3.58 | 36 | 24 | 4.22 |
| 5 | 05 | 3.60 | 37 | 25 | 4.24 |
| 6 | 06 | 3.62 | 38 | 26 | 4.26 |
| 7 | 07 | 3.64 | 39 | 27 | 4.28 |
| 8 | 08 | 3.66 | 40 | 28 | 4.30 |
| 9 | 09 | 3.68 | 41 | 29 | 4.32 |
| 10 | 0A | 3.70 | 42 | 2A | 4.34 |
| 11 | 0B | 3.72 | 43 | 2B | 4.36 |
| 12 | 0C | 3.74 | 44 | 2C | 4.38 |
| 13 | 0D | 3.76 | 45 | 2D | 4.40 |
| 14 | 0E | 3.78 | 46 | 2E | 4.42 |
| 15 | 0F | 3.80 | 47 | 2F | 4.44 |
| 16 | 10 | 3.82 | 48 | 30 | 4.44 |
| 17 | 11 | 3.84 | 49 | 31 | 4.44 |
| 18 | 12 | 3.86 | 50 | 32 | 4.44 |
| 19 | 13 | 3.88 | 51 | 33 | 4.44 |
| 20 | 14 | 3.90 | 52 | 34 | 4.44 |
| 21 | 15 | 3.92 | 53 | 35 | 4.44 |
| 22 | 16 | 3.94 | 54 | 36 | 4.44 |
| 23 | 17 | 3.96 | 55 | 37 | 4.44 |
| 24 | 18 | 3.98 | 56 | 38 | 4.44 |
| 25 | 19 | 4.00 | 57 | 39 | 4.44 |
| 26 | 1A | 4.02 | 58 | 3A | 4.44 |
| 27 | 1B | 4.04 | 59 | 3B | 4.44 |
| 28 | 1C | 4.06 | 60 | 3C | 4.44 |
| 29 | 1D | 4.08 | 61 | 3D | 4.44 |
| 30 | 1E | 4.10 | 62 | 3E | 4.44 |

The following charging parameters can be programmed by the host through I²C:

Table 4. Programmable Charging Parameters

| Parameter | Name | Register |
|--------------------------------|-------------|-----------|
| Output Voltage Regulation | V_{OREG} | REG2[7:2] |
| Battery Charging Current Limit | I_{OCHRG} | REG4[6:4] |
| Input Current Limit | I_{INLIM} | REG1[7:6] |
| Charge Termination Limit | I_{TERM} | REG4[2:0] |
| Weak Battery Voltage | V_{LOWV} | REG1[5:4] |

A new charge cycle begins when one of the following occurs:

- The battery voltage falls below $V_{OREG} - V_{RCH}$
- VBUS Power on Reset (POR) clears and the battery voltage is below the weak battery threshold (V_{LOWV}).
- \overline{CE} or HZ_MODE is reset through I²C write to CONTROL1 (R1) register.

Charge Current Limit ($I_{OCHARGE}$)**Table 5. $I_{OCHARGE}$ (REG4 [6:4]) Current as Function of $I_{OCHARGE}$ Bits and R_{SENSE} Resistor Values**

| DEC | BIN | HEX | V_{RSENSE} (mV) | $I_{OCHARGE}$ (mA) | |
|-----|-----|-----|-------------------|--------------------|----------------|
| | | | | 68 m Ω | 100 m Ω |
| 0 | 000 | 00 | 37.4 | 550 | 374 |
| 1 | 001 | 01 | 44.2 | 650 | 442 |
| 2 | 010 | 02 | 51.0 | 750 | 510 |
| 3 | 011 | 03 | 57.8 | 850 | 578 |
| 4 | 100 | 04 | 71.4 | 1050 | 714 |
| 5 | 101 | 05 | 78.2 | 1150 | 782 |
| 6 | 110 | 06 | 91.8 | 1350 | 918 |
| 7 | 111 | 07 | 98.6 | 1450 | 986 |

Termination Current Limit

Current charge termination is enabled when TE (REG1[3])=1. Typical termination current values are given in Table 6.

Table 6. I_{TERM} Current as Function of I_{TERM} Bits (REG4[2:0]) and R_{SENSE} Resistor Values

| I_{TERM} | V_{RSENSE} (mV) | I_{TERM} (mA) | |
|------------|-------------------|-----------------|----------------|
| | | 68 m Ω | 100 m Ω |
| 0 | 3.3 | 49 | 33 |
| 1 | 6.6 | 97 | 66 |
| 2 | 9.9 | 146 | 99 |
| 3 | 13.2 | 194 | 132 |
| 4 | 16.5 | 243 | 165 |
| 5 | 19.8 | 291 | 198 |
| 6 | 23.1 | 340 | 231 |
| 7 | 26.4 | 388 | 264 |

When the charge current falls below I_{TERM} , PWM charging stops and the STAT bits change to READY (00) for about 500 ms while the IC determines whether the battery and charging source are still connected. STAT then changes to CHARGE DONE (10), provided the battery and charger are still connected.

PWM Controller in Charge Mode

The IC uses a current-mode PWM controller to regulate the output voltage and battery charge currents. The synchronous rectifier (Q2) has a current limit that which off the FET when the current is negative by more than 140mA peak. This prevents current flow from the battery.

Safety Timer

Section references Figure 39.

At the beginning of charging, the IC starts a 15-minute timer (t_{15MIN}). When this times out, charging is terminated. Writing to any register through I²C stops and resets the t_{15MIN} timer, which in turn starts a 32-second timer (t_{32S}). Setting the TMR_RST bit (REG0[7]) resets the t_{32S} timer. If the t_{32S} timer times out; charging is terminated, the registers are set to their default values, and charging resumes using the default values with the t_{15MIN} timer running.

Normal charging is controlled by the host with the t_{32S} timer running to ensure that the host is alive. Charging with the t_{15MIN} timer running is used for charging that is unattended by the host. If the t_{15MIN} timer expires; the IC turns off the charger, sets the \overline{CE} bit, and indicates a timer fault (110) on the FAULT bits (REG0[2:0]). This sequence prevents overcharge if the host fails to reset the t_{32S} timer.

V_{BUS} POR / Non-Compliant Charger Rejection

When the IC detects that V_{BUS} has risen above V_{IN(MIN)1} (4.4 V), the IC applies a 100 Ω load from V_{BUS} to GND. To clear the V_{BUS} POR (Power-On-Reset) and begin charging, V_{BUS} must remain above V_{IN(MIN)1} and below V_{BUS_OVP} for t_{VBUS_VALID} (30 ms) before the IC initiates charging. The V_{BUS} validation sequence always occurs before charging is initiated or re-initiated (for example, after a V_{BUS} OVP fault or a V_{RCH} recharge initiation).

t_{VBUS_VALID} ensures that unfiltered 50 / 60 Hz chargers and other non-compliant chargers are rejected.

USB-Friendly Boot Sequence

At V_{BUS} POR, when the battery voltage is above the weak battery threshold (V_{LOWV}), the IC operates in accordance with its I²C register settings. If V_{BAT} < V_{LOWV}, the IC sets all registers to their default values and enables the charger using an input current limit controlled by the OTG pin (100mA if OTG is LOW and 500 mA if OTG is HIGH). This feature can revive a battery whose voltage is too low to ensure reliable host operation. Charging continues in the absence of host communication even after the battery has reached V_{OREG}, whose default value is 3.54 V, and the charger remains active until t_{15MIN} times out. Once the host processor begins writing to the IC, charging parameters are set by the host, which must continually reset the t_{32S} timer to continue charging using the programmed charging parameters. If t_{32S} times out, the register defaults are loaded, the FAULT bits are set to 110, STAT is pulsed HIGH, and charging continues with default charge parameters.

Input Current Limiting

To minimize charging time without overloading V_{BUS} current limitations, the IC's input current limit can be programmed by the I_{INLIM} bits (REG1[7:6]).

Table 7. Input Current Limit

| I _{INLIM} REG1[7:6] | Input Current Limit |
|------------------------------|---------------------|
| 00 | 100 mA |
| 01 | 500 mA |
| 10 | 800 mA |
| 11 | No limit |

The OTG pin establishes the input current limit when t_{15MIN} is running.

Flow Charts

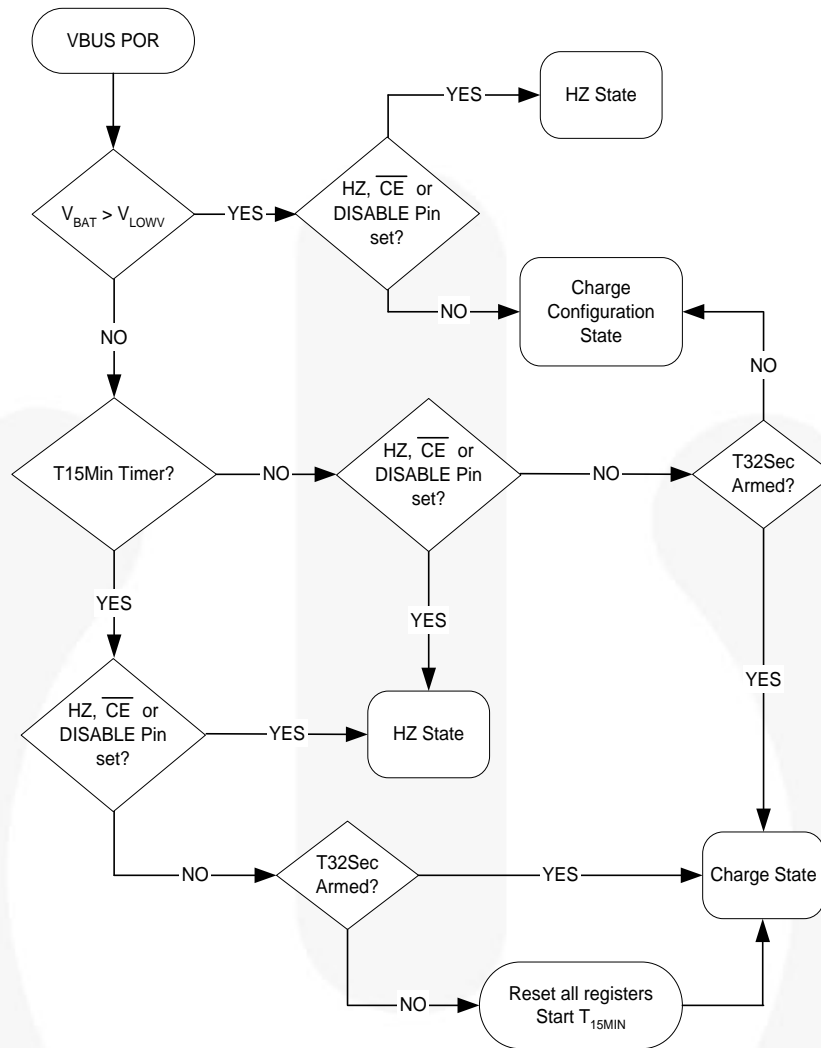


Figure 35. Charger VBUS POR

Flow Charts (Continued)

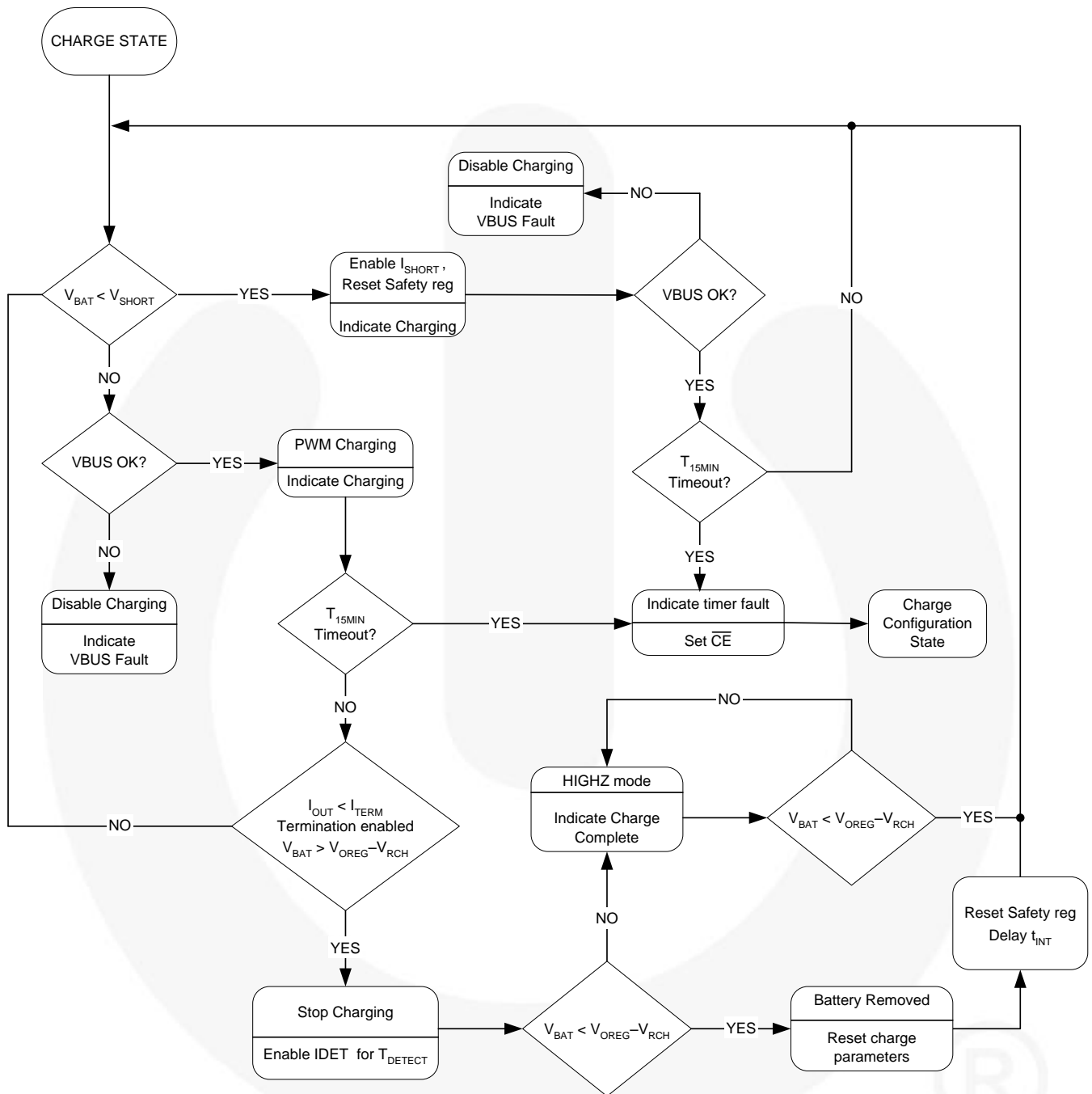


Figure 36. Charge Mode

Flow Charts (Continued)

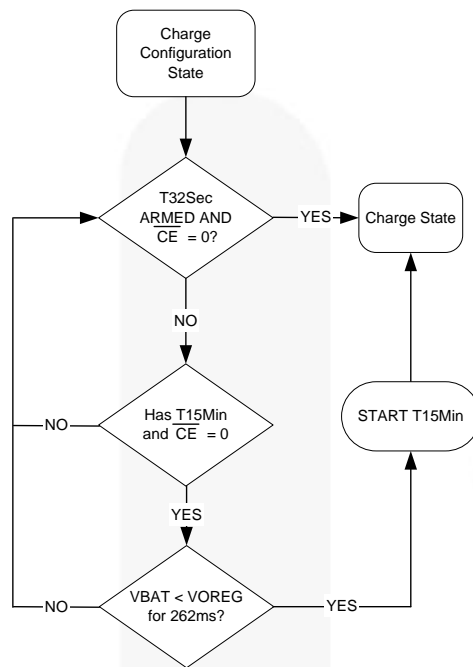


Figure 37. Charge Configuration

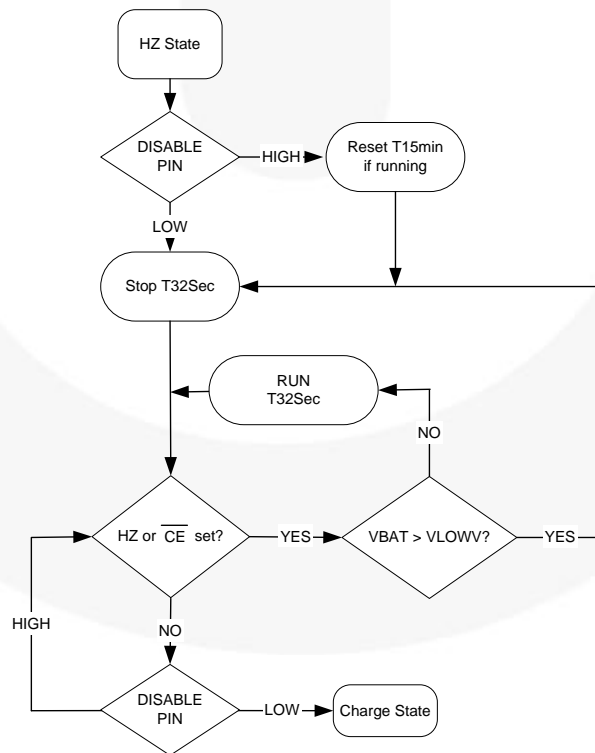


Figure 38. HZ-State

Flow Charts (Continued)

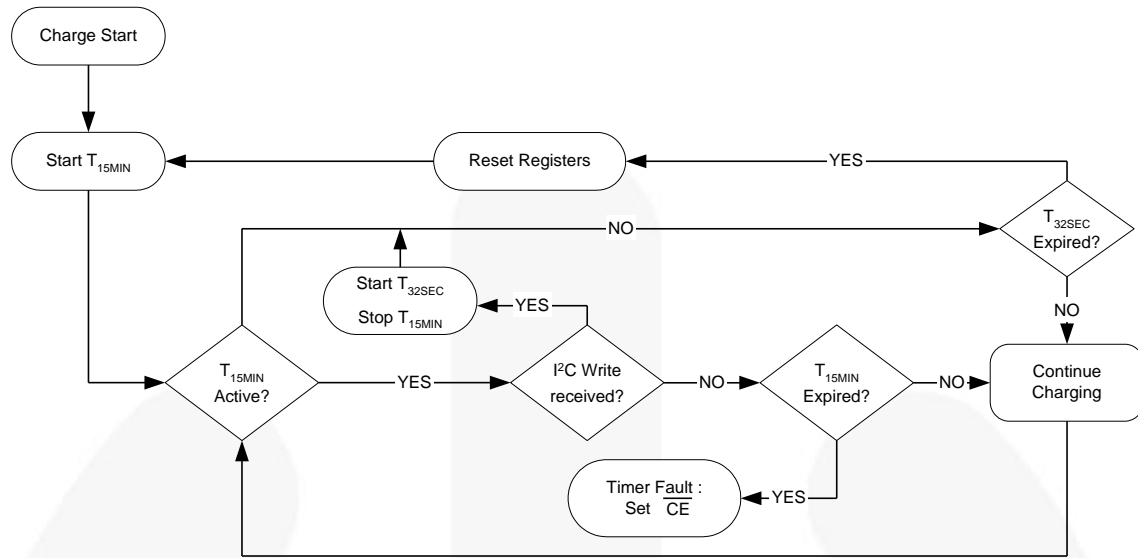


Figure 39. Timer Flow Chart

Special Charger

The FAN54015 has additional functionality to limit input current in case a current-limited “special charger” is supplying V_{BUS}. These slowly increase the charging current until either:

- I_{INLIM} or I_{CHARGE} is reached

or

- V_{BUS}=V_{SP}.

If V_{BUS} collapses to V_{SP} when the current is ramping up, the FAN54015 charge with an input current that keeps V_{BUS}=V_{SP}. When the V_{SP} control loop is limiting the charge current, the SP bit (REG5[4]) is set.

Table 8. V_{SP} as Function of SP Bits (REG5[2:0])

| SP (REG5[2:0]) | | | |
|----------------|-----|-----|-----------------|
| DEC | BIN | HEX | V _{SP} |
| 0 | 000 | 00 | 4.213 |
| 1 | 001 | 01 | 4.293 |
| 2 | 010 | 02 | 4.373 |
| 3 | 011 | 03 | 4.453 |
| 4 | 100 | 04 | 4.533 |
| 5 | 101 | 05 | 4.613 |
| 6 | 110 | 06 | 4.693 |
| 7 | 111 | 07 | 4.773 |

Safety Settings

FAN54015 contain a SAFETY register (REG6) that prevents the values in OREG (REG2[7:2]) and IOCHARGE (REG4[6:4]) from exceeding the values of the VSAFE and ISAFE values.

After V_{BAT} exceeds V_{SHORT}, the SAFETY register is loaded with its default value and may be written only before any other register is written. The entire desired Safety register value should be written twice to ensure the register bits are set. After writing to any other register, the SAFETY register is locked until V_{BAT} falls below V_{SHORT}.

The ISAFE (REG6[6:4]) and VSAFE (REG6[3:0]) registers establish values that limit the maximum values of I_{CHARGE} and V_{OREG} used by the control logic. If the host attempts to write a value higher than VSAFE or ISAFE to OREG or IOCHARGE, respectively; the VSAFE, ISAFE value appears as the OREG, IOCHARGE register value, respectively.

Table 9. I_{SAFE} (I_{CHARGE} Limit) as Function of ISAFE Bits (REG6[6:4])

| ISAFE (REG6[6:4]) | | | V _{RSENSE} (mV) | I _{SAFE} (mA) | |
|-------------------|-----|-----|--------------------------|------------------------|--------|
| DEC | BIN | HEX | | 68 mΩ | 100 mΩ |
| 0 | 000 | 00 | 37.4 | 550 | 374 |
| 1 | 001 | 01 | 44.2 | 650 | 442 |
| 2 | 010 | 02 | 51.0 | 750 | 510 |
| 3 | 011 | 03 | 57.8 | 850 | 578 |
| 4 | 100 | 04 | 71.4 | 1050 | 714 |
| 5 | 101 | 05 | 78.2 | 1150 | 782 |
| 6 | 110 | 06 | 91.8 | 1350 | 918 |
| 7 | 111 | 07 | 98.6 | 1450 | 986 |

Table 10. V_{SAFE} (V_{OREG} Limit) as Function of VSAFE Bits (REG6[3:0])

| VSAFE (REG6[3:0]) | | | Max. OREG (REG2[7:2]) | VOREG Max. |
|-------------------|------|-----|-----------------------|------------|
| DEC | BIN | HEX | | |
| 0 | 0000 | 00 | 100011 | 4.20 |
| 1 | 0001 | 01 | 100100 | 4.22 |
| 2 | 0010 | 02 | 100101 | 4.24 |
| 3 | 0011 | 03 | 100110 | 4.26 |
| 4 | 0100 | 04 | 100111 | 4.28 |
| 5 | 0101 | 05 | 101000 | 4.30 |
| 6 | 0110 | 06 | 101001 | 4.32 |
| 7 | 0111 | 07 | 101010 | 4.34 |
| 8 | 1000 | 08 | 101011 | 4.36 |
| 9 | 1001 | 09 | 101100 | 4.38 |
| 10 | 1010 | 0A | 101101 | 4.40 |
| 11 | 1011 | 0B | 101110 | 4.42 |
| 12 | 1100 | 0C | 101111 | 4.44 |
| 13 | 1101 | 0D | 110000 | 4.44 |
| 14 | 1110 | 0E | 110001 | 4.44 |
| 15 | 1111 | 0F | 110010 | 4.44 |

Thermal Regulation and Protection

When the IC's junction temperature reaches T_{CF} (about 120°C), the charger reduces its output current to 550 mA to prevent overheating. If the temperature increases beyond T_{SHUTDOWN}; charging is suspended, the FAULT bits are set to 101, and STAT is pulsed HIGH. In Suspend Mode, all timers stop and the state of the IC's logic is preserved. Charging resumes at programmed current after the die cools to about 120°C.

Additional θ_{JA} data points, measured using the FAN54015 evaluation board, are given in Table 11 (measured with $T_A=25^\circ\text{C}$). Note that as power dissipation increases, the effective θ_{JA} decreases due to the larger difference between the die temperature and ambient.

Table 11. Evaluation Board Measured θ_{JA}

| Power (W) | θ_{JA} |
|-----------|---------------|
| 0.504 | 54°C/W |
| 0.844 | 50°C/W |
| 1.506 | 46°C/W |

Charge Mode Input Supply Protection

Sleep Mode

When V_{BUS} falls below $V_{BAT} + V_{SLP}$, and V_{BUS} is above $V_{IN(MIN)}$, the IC enters Sleep Mode to prevent the battery from draining into V_{BUS} . During Sleep Mode, reverse current is disabled by body switching Q1.

Input Supply Low-Voltage Detection

The IC continuously monitors V_{BUS} during charging. If V_{BUS} falls below $V_{IN(MIN)}$, the IC:

1. Terminates charging
2. Pulses the STAT pin, sets the STAT bits to 11, and sets the FAULT bits to 011.

If V_{BUS} recovers above the $V_{IN(MIN)}$ rising threshold after time t_{INT} (about two seconds), the charging process is repeated. This function prevents the USB power bus from collapsing or oscillating when the IC is connected to a suspended USB port or a low-current-capable OTG device.

Input Over-Voltage Detection

When the V_{BUS} exceeds $V_{BUS_{OVP}}$, the IC:

1. Turns off Q3
2. Suspends charging
3. Sets the FAULT bits to 001, sets the STAT bits to 11, and pulses the STAT pin.

When V_{BUS} falls about 150 mV below $V_{BUS_{OVP}}$, the fault is cleared and charging resumes after V_{BUS} is revalidated (see *VBUS POR / Non-Compliant Charger Rejection*).

VBUS Short While Charging

If V_{BUS} is shorted with a very low impedance while the IC is charging with $I_{INLIMIT}=100\text{ mA}$, the IC may not meet datasheet specifications until power is removed. To trigger this condition, V_{BUS} must be driven from 5 V to GND with a high slew rate. Achieving this slew rate requires a $0\ \Omega$ short to the USB cable less than 10cm from the connector.

Charge Mode Battery Detection & Protection

VBAT Over-Voltage Protection

The OREG voltage regulation loop prevents V_{BAT} from overshooting the OREG voltage by more than 50 mV when the battery is removed. When the PWM charger runs with no battery, the TE bit is not set and a battery is inserted that is charged to a voltage higher than V_{OREG} ; PWM pulses stop. If no further pulses occur for 30 ms, the IC sets the FAULT bits to 100, sets the STAT bits to 11, and pulses the STAT pin.

Battery Detection During Charging

The IC can detect the presence, absence, or removal of a battery if the termination bit (TE) is set. During normal charging, once V_{BAT} is close to V_{OREG} and the termination charge current is detected, the IC terminates charging and sets the STAT bits to 10. It then turns on a discharge current, I_{DETECT} , for t_{DETECT} . If V_{BAT} is still above $V_{OREG} - V_{RCH}$, the battery is present and the IC sets the FAULT bits to 000. If V_{BAT} is below $V_{OREG} - V_{RCH}$, the battery is absent and the IC:

1. Sets the registers to their default values.
2. Sets the FAULT bits to 111.
3. Resumes charging with default values after t_{INT} .

Battery Short-Circuit Protection

If the battery voltage is below the short-circuit threshold (V_{SHORT}); a linear current source, I_{SHORT} , supplies V_{BAT} until $V_{BAT} > V_{SHORT}$.

System Operation with No Battery

The FAN54015 continues charging after V_{BUS} POR with the default parameters, regulating the V_{BAT} line to 3.54 V until the host processor issues commands or the 15-minute timer expires. In this way, the FAN54015 can start the system without a battery.

The FAN54015 soft-start function can interfere with the system supply with battery absent. The soft-start activates whenever V_{OREG} , $I_{INLIMIT}$, or $I_{OCHARGE}$ are set from a lower to higher value. During soft-start, the I_{IN} limit drops to 100 mA for about 1ms unless $I_{INLIMIT}$ is set to 11 (no limit). This could cause the system processor to fail to start. To avoid this behavior, use the following sequence.

1. Set the OTG pin HIGH. When V_{BUS} is plugged in, $I_{INLIMIT}$ is set to 500 mA until the system processor powers up and can set parameters through I^2C .
2. Program the Safety Register.
3. Set $I_{INLIMIT}$ to 11 (no limit).
4. Set OREG to the desired value (typically 4.18).
5. Reset the IO_LEVEL bit, then set IOCHARGE.
6. Set $I_{INLIMIT}$ to 500mA if a USB source is connected.

During the initial system startup, while the charger IC is being programmed, the system current is limited to 500mA for 1ms during steps 4 and 5. This is the value of the soft-start ICHARGE current used when $I_{INLIMIT}$ is set to No Limit.

If the system is powered up without a battery present, the CV bit should be set. When a battery is inserted, the CV bit is cleared.

Charger Status / Fault Status

The STAT pin indicates the operating condition of the IC and provides a fault indicator for interrupt driven systems.

Table 12. STAT Pin Function

| EN_STAT | Charge State | STAT Pin |
|---------|---------------------------|------------------------------|
| 0 | X | OPEN |
| X | Normal Conditions | OPEN |
| 1 | Charging | LOW |
| X | Fault (Charging or Boost) | 128 μ s Pulse, then OPEN |

The FAULT bits (R0[2:0]) indicate the type of fault in Charge Mode (see Table 13).

Table 13. Fault Status Bits During Charge Mode

| Fault Bit | | | Fault Description |
|-----------|----|----|-------------------|
| B2 | B1 | B0 | |
| 0 | 0 | 0 | Normal (No Fault) |
| 0 | 0 | 1 | VBUS OVP |
| 0 | 1 | 0 | Sleep Mode |
| 0 | 1 | 1 | Poor Input Source |
| 1 | 0 | 0 | Battery OVP |
| 1 | 0 | 1 | Thermal Shutdown |
| 1 | 1 | 0 | Timer Fault |
| 1 | 1 | 1 | No Battery |

Charge Mode Control Bits

Setting either HZ_MODE or \overline{CE} through I²C disables the charger and puts the IC into High-Impedance Mode and resets t_{32S} . If $V_{BAT} < V_{LOWV}$ while in High-Impedance Mode, t_{32S} begins running and, when it overflows, all registers (except SAFETY) reset, which enables t_{15MIN} charging on versions with the 15-minute timer.

When t_{15MIN} overflows, the IC sets the \overline{CE} bit and the IC enters High-Impedance Mode. If \overline{CE} was set by t_{15MIN} overflow, a new charge cycle can only be initiated through I²C or VBUS POR.

Setting the RESET bit clears all registers. If HZ_MODE or \overline{CE} bits were set when the RESET bit is set, these bits are also cleared, but the t_{32S} timer is not started, and the IC remains in High-Impedance Mode.

Table 14. DISABLE Pin and \overline{CE} Bit Functionality

| Charging | DISABLE Pin | \overline{CE} | HZ_MODE |
|----------|-------------|-----------------|---------|
| ENABLE | 0 | 0 | 0 |
| DISABLE | X | 1 | X |
| DISABLE | X | X | 1 |
| DISABLE | 1 | X | X |

Raising the DISABLE pin stops t_{32S} from advancing, but does not reset it. If the DISABLE pin is raised during t_{15MIN} charging, the t_{15MIN} timer is reset.

Operational Mode Control

OPA_MODE (REG1[0]) and the HZ_MODE (REG1[1]) bits in conjunction with the FAULT state define the operational mode of the charger.

Table 15. Operation Mode Control

| HZ_MODE | OPA_MODE | FAULT | Operation Mode |
|---------|----------|-------|------------------|
| 0 | 0 | 0 | Charge |
| 0 | X | 1 | Charge Configure |
| 0 | 1 | 0 | Boost |
| 1 | X | X | High Impedance |

The IC resets the OPA_MODE bit whenever the boost is deactivated, whether due to a fault or being disabled by setting the HZ_MODE bit.

Boost Mode

Boost Mode can be enabled if the IC is in 32-Second Mode with the OTG pin and OPA_MODE bits as indicated in Table 16. The OTG pin ACTIVE state is 1 if OTG_PL=1 and 0 when OTG_PL=0.

If boost is active using the OTG pin, Boost Mode is initiated even if the HZ_MODE=1. The HZ_MODE bit overrides the OPA_MODE bit.

Table 16. Enabling Boost

| OTG_EN | OTG Pin | HZ_MODE | OPA_MODE | BOOST |
|--------|---------------------|---------|----------|----------|
| 1 | ACTIVE | X | X | Enabled |
| X | X | 0 | 1 | Enabled |
| X | \overline{ACTIVE} | X | 0 | Disabled |
| 0 | X | 1 | X | Disabled |
| 1 | \overline{ACTIVE} | 1 | 1 | Disabled |
| 0 | ACTIVE | 0 | 0 | Disabled |

To remain in Boost Mode, the TMR_RST must be set by the host before the t_{32S} timer times out. If t_{32S} times out in Boost Mode; the IC resets all registers, pulses the STAT pin, sets the FAULT bits to 110, and resets the BOOST bit. VBUS POR or reading R0 clears the fault condition.

Boost PWM Control

The IC uses a minimum on-time and computed minimum off-time to regulate VBUS. The regulator achieves excellent transient response by employing current-mode modulation. This technique causes the regulator to exhibit a load line. During PWM Mode, the output voltage drops slightly as the input current rises. With a constant V_{BAT} , this appears as a constant output resistance.

The “droop” caused by the output resistance when a load is applied allows the regulator to respond smoothly to load transients with no undershoot from the load line. This can be seen in Figure 31 and Figure 40.

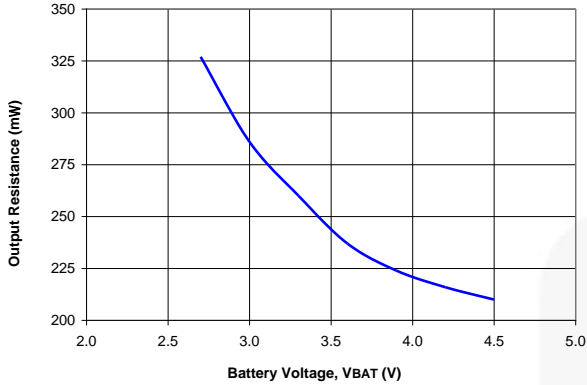


Figure 40. Output Resistance (R_{OUT})

V_{BUS} as a function of I_{LOAD} can be computed when the regulator is in PWM Mode (continuous conduction) as:

$$V_{OUT} = 5.07 - R_{OUT} \cdot I_{LOAD} \quad \text{EQ. 1}$$

At $V_{BAT}=3.3$ V, and $I_{LOAD}=200$ mA, V_{BUS} would drop to:

$$V_{OUT} = 5.07 - 0.26 \cdot 0.2 = 5.018\text{V} \quad \text{EQ. 1A}$$

At $V_{BAT}=2.7$ V, and $I_{LOAD}=200$ mA, V_{BUS} would drop to:

$$V_{OUT} = 5.07 - 0.327 \cdot 0.2 = 5.005\text{V} \quad \text{EQ. 1B}$$

PFM Mode

If $V_{BUS} > V_{REF_BOOST}$ (nominally 5.07 V) when the minimum off-time has ended, the regulator enters PFM Mode. Boost pulses are inhibited until $V_{BUS} < V_{REF_BOOST}$. The minimum on-time is increased to enable the output to pump up sufficiently with each PFM boost pulse. Therefore the regulator behaves like a constant on-time regulator, with the bottom of its output voltage ripple at 5.07 V in PFM Mode.

Table 17. Boost PWM Operating States

| Mode | Description | Invoked When |
|------|----------------------|---|
| LIN | Linear Startup | $V_{BAT} > V_{BUS}$ |
| SS | Boost Soft-Start | $V_{BUS} < V_{BST}$ |
| BST | Boost Operating Mode | $V_{BAT} > UVLO_{BST}$ and SS Completed |

Startup

When the boost regulator is shut down, current flow is prevented from V_{BAT} to V_{BUS} , as well as reverse flow from V_{BUS} to V_{BAT} .

LIN State

When EN rises, if $V_{BAT} > UVLO_{BST}$, the regulator first attempts to bring PMID within 400 mV of V_{BAT} using an internal 450 mA current source from V_{BAT} (LIN State). If PMID has not achieved $V_{BAT} - 400$ mV after 560 μs , a FAULT state is initiated.

SS State

When $PMID > V_{BAT} - 400$ mV, the boost regulator begins switching with a reduced peak current limit of about 50% of its normal current limit. The output slews up until V_{BUS} is within 5% of its setpoint; at which time, the regulation loop is closed and the current limit is set to 100%.

If the output fails to achieve 95% of its setpoint (V_{BST}) within 128 μs , the current limit is increased to 100%. If the output fails to achieve 95% of its setpoint after this second 384 μs period, a fault state is initiated.

BST State

This is the normal operating mode of the regulator. The regulator uses a minimum t_{OFF} -minimum t_{ON} modulation scheme. The minimum t_{OFF} is proportional to $\frac{V_{IN}}{V_{OUT}}$, which

keeps the regulator's switching frequency reasonably constant in CCM. $t_{ON(MIN)}$ is proportional to V_{BAT} and is a higher value if the inductor current reached 0 before $t_{OFF(MIN)}$ in the prior cycle.

To ensure the V_{BUS} does not pump significantly above the regulation point, the boost switch remains off as long as $FB > V_{REF}$.

Boost Faults

If a BOOST fault occurs:

1. The STAT pin pulses.
2. OPA_MODE bit is reset.
3. The power stage is in High-Impedance Mode.
4. The FAULT bits (REG0[2:0]) are set per Table 18.

Restart After Boost Faults

If boost was enabled with the OPA_MODE bit and $OTG_EN=0$, Boost Mode can only be enabled through subsequent I²C commands since OPA_MODE is reset on boost faults. If $OTG_EN=1$ and the OTG pin is still ACTIVE (see Table 16), the boost restarts after a 5.2 ms delay, as shown in Figure 41. If the fault condition persists, restart is attempted every 5ms until the fault clears or an I²C command disables the boost.

Table 18. Fault Bits During Boost Mode

| Fault Bit | | | Fault Description |
|-----------|----|----|--|
| B2 | B1 | B0 | |
| 0 | 0 | 0 | Normal (no fault) |
| 0 | 0 | 1 | $V_{BUS} > V_{BUS_OVP}$ |
| 0 | 1 | 0 | V_{BUS} fails to achieve the voltage required to advance to the next state during soft-start or sustained (>50 μs) current limit during the BST state. |
| 0 | 1 | 1 | $V_{BAT} < UVLO_{BST}$ |
| 1 | 0 | 0 | N/A: This code does not appear. |
| 1 | 0 | 1 | Thermal shutdown |
| 1 | 1 | 0 | Timer fault; all registers reset. |
| 1 | 1 | 1 | N/A: This code does not appear. |

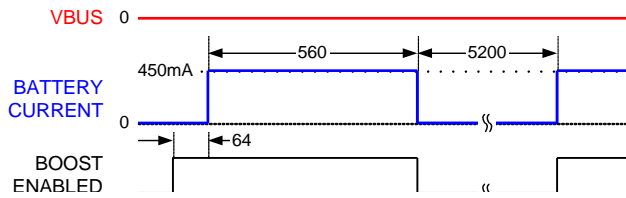


Figure 41. Boost Response Attempting to Start into V_{BUS} Short Circuit (Times in μs)

VREG Pin

The 1.8 V regulated output on this pin can be disabled through I²C by setting the DIS_VREG bit (REG5[6]). VREG

can supply up to 2 mA. This circuit, which is powered from PMID, is enabled only when PMID > V_{BAT} and does not drain current from the battery. During boost, V_{REG} is off. It is also off when the HZ_MODE bit (REG1[1])=1.

Monitor Register (Reg10H)

Additional status monitoring bits enable the host processor to have more visibility into the status of the IC. The monitor bits are real-time status indicators and are not internally debounced or otherwise time qualified.

The state of the MONITOR register bits listed in High-Impedance Mode is only valid when V_{BUS} is valid.

Table 19. MONITOR Register Bit Definitions

| BIT# | NAME | STATE | | Active When |
|--------------------------|------------|--|--|---------------------|
| | | 0 | 1 | |
| MONITOR Address 10H | | | | |
| 7 | ITERM_CMP | $V_{CSIN} - V_{BAT} < V_{ITERM}$ | $V_{CSIN} - V_{BAT} > V_{ITERM}$ | Charging with TE=1 |
| | | $V_{CSIN} - V_{BAT} < 1\text{ mV}$ | $V_{CSIN} - V_{BAT} > 1\text{mV}$ | Charging with TE=0 |
| 6 | VBAT_CMP | $V_{BAT} < V_{SHORT}$ | $V_{BAT} > V_{SHORT}$ | Charging |
| | | $V_{BAT} < V_{LOWV}$ | $V_{BAT} > V_{LOWV}$ | High-Impedance Mode |
| | | $V_{BAT} < UVLO_{BST}$ | $V_{BAT} > UVLO_{BST}$ | Boosting |
| 5 | LINCHG | Linear Charging Not Enabled | Linear Charging Enabled | Charging |
| 4 | T_120 | $T_J < 120^{\circ}\text{C}$ | $T_J > 120^{\circ}\text{C}$ | |
| 3 | ICHG | Charging Current Controlled by I_{CHARGE} Control Loop | Charging Current Not Controlled by I_{CHARGE} Control Loop | Charging |
| 2 | IBUS | I_{BUS} Limiting Charging Current | Charge Current Not Limited by I_{BUS} | Charging |
| 1 | VBUS_VALID | V_{BUS} Not Valid | V_{BUS} is Valid | $V_{BUS} > V_{BAT}$ |
| 0 | CV | Constant Current Charging | Constant Voltage Charging | Charging |

I²C Interface

The FAN54015's serial interface is compatible with Standard, Fast, Fast Plus, and High-Speed Mode I²C-Bus® specifications. The SCL line is an input and the SDA line is a bi-directional open-drain output; it can only pull down the bus when active. The SDA line only pulls LOW during data reads and signaling ACK. All data is shifted in MSB (bit 7) first.

Slave Address

Table 20. I²C Slave Address Byte

| Part Type | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|---|---|---|---|---|---|---|-----|
| FAN54015 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | R/W |

In hex notation, the slave address assumes a 0 LSB. The hex slave address for the FAN54015 is D4H and is D6H for all other parts in the family.

Bus Timing

As shown in Figure 42, data is normally transferred when SCL is LOW. Data is clocked in on the rising edge of SCL. Typically, data transitions shortly at or after the falling edge of SCL to allow ample time for the data to set up before the next SCL rising edge.

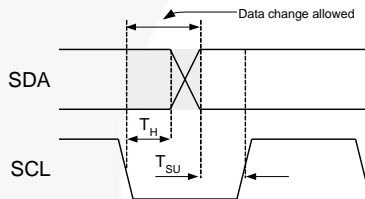


Figure 42. Data Transfer Timing

Each bus transaction begins and ends with SDA and SCL HIGH. A transaction begins with a START condition, which is defined as SDA transitioning from 1 to 0 with SCL HIGH, as shown in Figure 43.

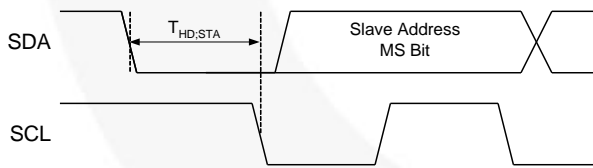


Figure 43. Start Bit

A transaction ends with a STOP condition, which is defined as SDA transitioning from 0 to 1 with SCL HIGH, as shown in Figure 44.

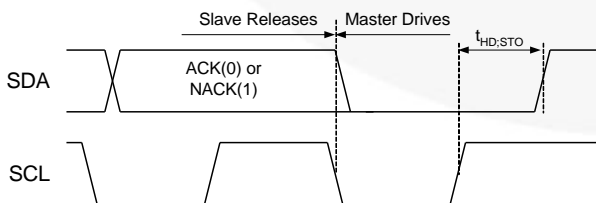


Figure 44. Stop Bit

During a read from the FAN54015 (Figure 46, Figure 47), the master issues a Repeated Start after sending the register address and before resending the slave address. The Repeated Start is a 1-to-0 transition on SDA while SCL is HIGH, as shown in Figure 45.

High-Speed (HS) Mode

The protocols for High-Speed (HS), Low-Speed (LS), and Fast-Speed (FS) Modes are identical except the bus speed for HS Mode is 3.4 MHz. HS Mode is entered when the bus master sends the HS master code 00001XXX after a start condition. The master code is sent in Fast or Fast Plus Mode (less than 1 MHz clock); slaves do not ACK this transmission.

The master then generates a repeated start condition (Figure 45) that causes all slaves on the bus to switch to HS Mode. The master then sends I²C packets, as described above, using the HS Mode clock rate and timing.

The bus remains in HS Mode until a stop bit (Figure 44) is sent by the master. While in HS Mode, packets are separated by repeated start conditions (Figure 45).

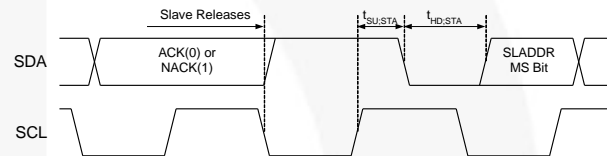


Figure 45. Repeated Start Timing

Read and Write Transactions

The figures below outline the sequences for data read and write. Bus control is signified by the shading of the packet, defined as Master Drives Bus and Slave Drives Bus. All addresses and data are MSB first.

Table 21. Bit Definitions for Figure 46, Figure 47, and Figure 48

| Symbol | Definition |
|----------------|---|
| S | START, see Figure 43 |
| A | ACK. The slave drives SDA to 0 to acknowledge the preceding packet. |
| \overline{A} | NACK. The slave sends a 1 to NACK the preceding packet. |
| R | Repeated START, see Figure 45 |
| P | STOP, see Figure 44. Figure 44 |

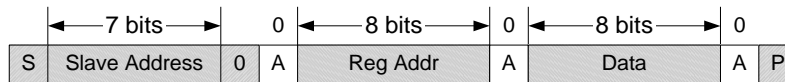


Figure 46. Write Transaction

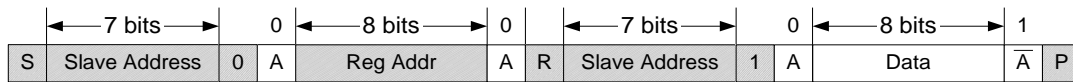


Figure 47. Read Transaction

Register Descriptions

The nine FAN54015 user-accessible registers are defined in Table 22.

Table 22. I²C Register Address

| Register | | Address Bits | | | | | | | |
|------------|-----------------|--------------|---|---|---|---|---|---|---|
| Name | REG# | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CONTROL0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CONTROL1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| OREG | 2 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| IC_INFO | 03 or 3BH | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| IBAT | 4 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| SP_CHARGER | 5 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| SAFETY | 6 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| MONITOR | 10h | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |

Table 23. Register Bit Definitions

This table defines the operation of each register bit for all IC versions. Default values are in **bold** text.

| Bit | Name | Value | Type | Description |
|-----------------|----------------|-------|------|---|
| CONTROL0 | | | | Register Address: 00 Default Value=X1XX 0XXX |
| 7 | TMR_RST OTG | 1 | W | Writing a 1 resets the t_{32S} timer; writing a 0 has no effect |
| | | | R | Returns the OTG pin level (1=HIGH) |
| 6 | EN_STAT | 0 | R/W | Prevents STAT pin from going LOW during charging; STAT pin still pulses to enunciate faults |
| | | 1 | | Enables STAT pin LOW when IC is charging |
| 5:4 | STAT | 00 | R | Ready |
| | | 01 | | Charge in progress |
| | | 10 | | Charge done |
| | | 11 | | Fault |
| 3 | BOOST | 0 | R | IC is not in Boost Mode |
| | | 1 | | IC is in Boost Mode |
| 2:0 | FAULT | | R | Fault status bits: <i>for Charge Mode, see Table 13; for Boost Mode, see Table 18</i> |

Continued on the following page...

Table 23. Register Bit Definitions (Continued)

| Bit | Name | Value | Type | Description | | |
|----------|------------------------|---------|------|---|--------------------------------|--------------|
| CONTROL1 | | | | Register Address: 01 Default Value=0011 0000 (30h) | | |
| 7:6 | I _{INLIM} | | R/W | Input current limit, <i>see Table 7</i> | | |
| 5:4 | V _{LOWV} | 00 | R/W | 3.4V | Weak battery voltage threshold | |
| | | 01 | | 3.5V | | |
| | | 10 | | 3.6V | | |
| | | 11 | | 3.7V | | |
| 3 | TE | 0 | R/W | Disable charge current termination | | |
| | | 1 | | Enable charge current termination | | |
| 2 | $\overline{\text{CE}}$ | 0 | R/W | Charger enabled | | |
| | | 1 | | Charger disabled | | |
| 1 | HZ_MODE | 0 | R/W | Not High-Impedance Mode | | See Table 16 |
| | | 1 | | High-Impedance Mode | | |
| 0 | OPA_MODE | 0 | R/W | Charge Mode | | |
| | | 1 | | Boost Mode | | |
| OREG | | | | Register Address: 02 Default Value=0000 1010 (0Ah) | | |
| 7:2 | OREG | | R/W | Charger output “float” voltage; programmable from 3.5 to 4.44V in 20mV increments; defaults to 000010 (3.54V) , <i>see Table 3</i> | | |
| 1 | OTG_PL | 0 | R/W | OTG pin active LOW | | |
| | | 1 | | OTG pin active HIGH | | |
| 0 | OTG_EN | 0 | R/W | Disables OTG pin | | |
| | | 1 | | Enables OTG pin | | |
| IC_INFO | | | | Register Address: 03 Default Value=10010100 (94h) | | |
| 7:5 | Vendor Code | 100 | R | Identifies Fairchild Semiconductor as the IC supplier | | |
| 4:2 | PN | | R | Part number bits, <i>see the Ordering Info on page 2</i> | | |
| 1:0 | REV | 00 | R | IC Revision, revision 1.X, where X is the decimal of these three bits | | |
| IBAT | | | | Register Address: 04 Default Value=1000 1001 (89h) | | |
| 7 | RESET | 1 | W | Writing a 1 resets charge parameters, except the Safety register (Reg6), to their defaults: writing a 0 has no effect; read returns 1 | | |
| 6:4 | IOCHARGE | Table 5 | R/W | Programs the maximum charge current, <i>see Table 5</i> | | |
| 3 | Reserved | 1 | R | Unused | | |
| 2:0 | ITERM | Table 6 | R/W | Sets the current used for charging termination, <i>see Table 6</i> | | |

Continued on the following page...

Table 23. Register Bit Definitions (Continued)

| SP_CHARGER | | | Register Address: 05 | | Default Value=001X X100 |
|-------------------|------------|-----------------|-----------------------------------|--|--------------------------------------|
| 7 | Reserved | 0 | R | Unused | |
| 6 | DIS_VREG | 0 | R/W | 1.8V regulator is ON | |
| | | 1 | | 1.8V regulator is OFF | |
| 5 | IO_LEVEL | 0 | R/W | Output current is controlled by IOCHARGE bits | |
| | | 1 | | Voltage across R_{SENSE} for output current control is set to 34mV (500mA for $R_{SENSE}=68m\Omega$ and 340mA for $100m\Omega$) | |
| 4 | SP | 0 | R | Special charger is not active (V_{BUS} is able to stay above V_{SP}) | |
| | | 1 | | Special charger has been detected and V_{BUS} is being regulated to V_{SP} | |
| 3 | EN_LEVEL | 0 | R | DISABLE pin is LOW | |
| | | 1 | | DISABLE pin is HIGH | |
| 2:0 | VSP | Table 8 | R/W | Special charger input regulation voltage, <i>see Table 8</i> | |
| SAFETY | | | Register Address: 06 | | Default Value=0100 0000 (40h) |
| 7 | Reserved | 0 | R | Bit disabled and always returns 0 when read back | |
| 6:4 | ISAFE | Table 9 | R/W | Sets the maximum $I_{OCHARGE}$ value used by the control circuit, <i>see Table 9</i> | |
| 3:0 | VSAFE | Table 10 | R/W | Sets the maximum V_{OREG} used by the control circuit, <i>see Table 10</i> | |
| MONITOR | | | Register Address: 10h (16) | | <i>See Table 19</i> |
| 7 | ITERM_CMP | See Table 19 | R | ITERM comparator output, 1 when $VRSENSE > ITERM$ reference | |
| 6 | VBAT_CMP | | R | Output of VBAT comparator | |
| 5 | LINCHG | | R | 30mA linear charger ON | |
| 4 | T_120 | | R | Thermal regulation comparator; when=1 and $T_{145}=0$, the charge current is limited to 22.1 mV across R_{SENSE} | |
| 3 | ICHG | | R | 0 indicates the ICHARGE loop is controlling the battery charge current | |
| 2 | IBUS | | R | 0 indicates the IBUS (input current) loop is controlling the battery charge current | |
| 1 | VBUS_VALID | | R | 1 indicates VBUS has passed validation and is capable of charging | |
| 0 | CV | | R | 1 indicates the constant-voltage loop (OREG) is controlling the charger and all current limiting loops have released | |

PCB Layout Recommendations

Bypass capacitors should be placed as close to the IC as possible. In particular, the total loop length for CMID should be minimized to reduce overshoot and ringing on the SW, PMID, and VBUS pins. All power and ground pins must be

routed to their bypass capacitors, using top copper whenever possible. Copper area connecting to the IC should be maximized to improve thermal performance if possible.

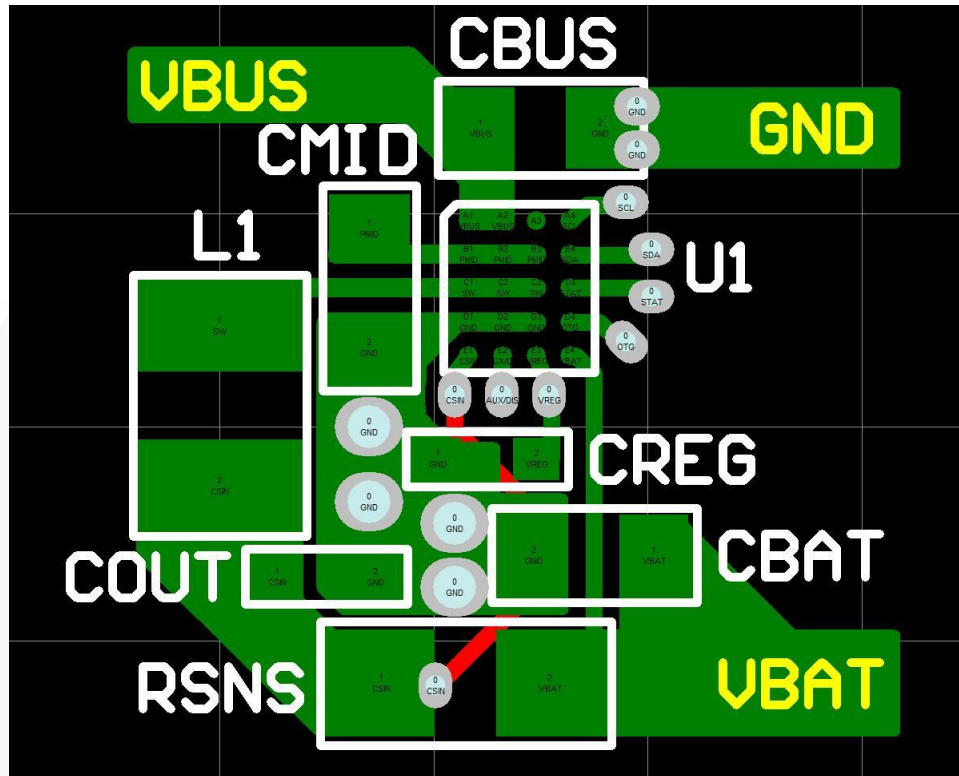


Figure 48. PCB Layout Recommendations

Physical Dimensions

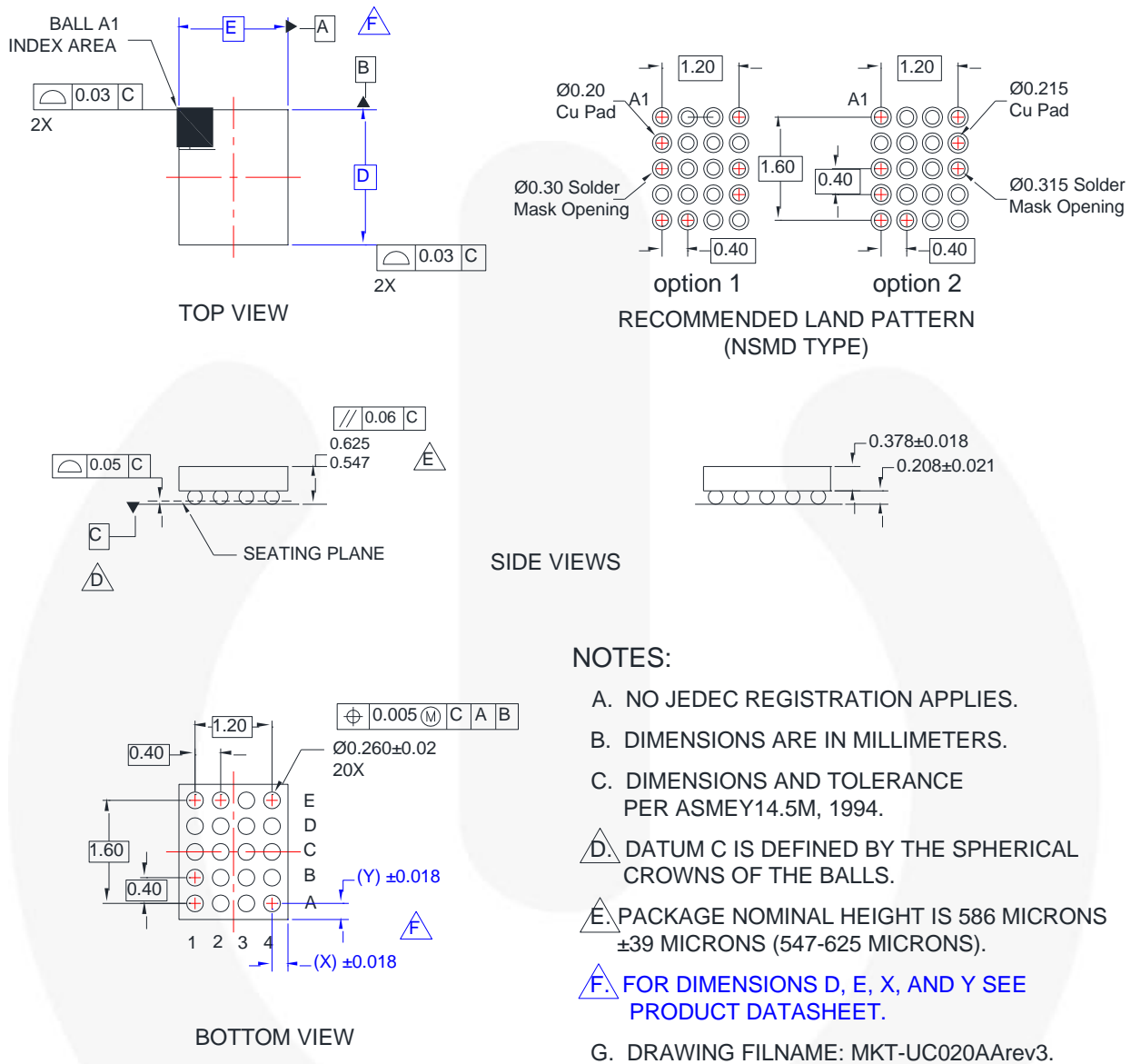


Figure 49. 20-Ball WLCSP, 4X5 Array, 0.4 mm Pitch, 250 µm Ball

Product-Specific Dimensions

| Product | D | E | X | Y |
|--------------|-----------------|-----------------|----------|----------|
| FAN54015UCX | 1.960 ±0.030 mm | 1.870 ±0.030 mm | 0.335 mm | 0.180 mm |
| FAN54015BUCX | 1.960 ±0.030 mm | 1.870 ±0.030 mm | 0.335 mm | 0.180 mm |






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