



DMN3067LW

N-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

V _{(BR)DSS}	R _{DS(ON)}	I _D T _A = +25°C
30V	$67m\Omega$ @ V_{GS} = $4.5V$	2.6A
	70mΩ @ V _{GS} = 4.0V	2.5A
	98mΩ @ V _{GS} = 2.5V	2.2A

Description

This new generation MOSFET has been designed to minimize the on-state resistance (RDS(ON)) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

- Switching
- **Power Management Functions**







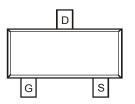
Top View

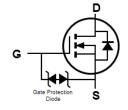
Features and Benefits

- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Small Surface Mount Package
- **ESD Protected Gate**
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 Standards for High Reliability

Mechanical Data

- Case: SOT323
- Case Material: Molded Plastic. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Matte Tin Finish annealed over Alloy 42 leadframe (Lead Free Plating). Solderable per MIL-STD-202, Method 208
- Terminal Connections: See Diagram
- Weight: 0.006 grams (approximate)





Top View Pin Configuration

Equivalent Circuit

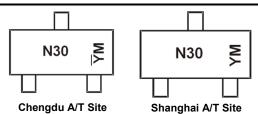
Ordering Information (Note 4)

Part Number	Case	Packaging
DMN3067LW-7	SOT323	3000/Tape & Reel
DMN3067LW-13	SOT323	10000/Tape & Reel

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- 2. See http://www.diodes.com/quality/lead free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + CI) and <1000ppm antimony compounds.</p>
 4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information



N30 = Product Type Marking Code

YM = Date Code Marking for SAT (Shanghai Assembly/ Test site) YM = Date Code Marking for CAT (Chengdu Assembly/ Test site) Y or \overline{Y} = Year (ex: A = 2013)

M = Month (ex: 9 = September)

Date Code Key

Year	201	1	2012		2013	20	14	2015		2016		2017
Code	Υ		Z		Α	ŀ	3	С		D		E
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	0	N	D



Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Units
Drain-Source Voltage	V_{DSS}	30	V
Gate-Source Voltage	V_{GSS}	±12	V
Continuous Drain Current (Note 6) V _{GS} = 4.5V	I _D	2.6 2.1	А
Pulsed Drain Current (10µs pulse, duty cycle = 1%)	I _{DM}	10	Α

Thermal Characteristics

Characteristic		Symbol	Value	Units	
Total Power Dissipation	(Note 5)	р	0.5	W	
Total Fower Dissipation	(Note 6)	P_{D}	1.1		
Thermal Resistance, Junction to Ambient	(Note 5)	В	241	°C/W	
Thermal Resistance, Junction to Ambient	(Note 6)	$R_{ heta JA}$	130		
Operating and Storage Temperature Range		T _{J,} T _{STG}	-55 to +150	°C	

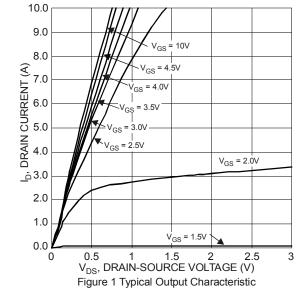
Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

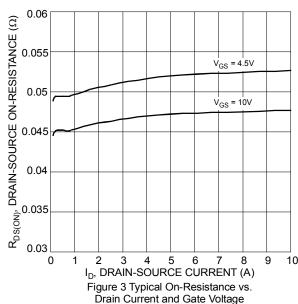
Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 7)							
Drain-Source Breakdown Voltage	BV _{DSS}	30	_	_	V	$V_{GS} = 0V, I_D = 250\mu A$	
Zero Gate Voltage Drain Current	I _{DSS}	_	_	1	μA	$V_{DS} = 30V, V_{GS} = 0V$	
Gate-Body Leakage	I _{GSS}	_	_	±10	μA	$V_{GS} = \pm 12V, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 7)							
Gate Threshold Voltage	V _{GS(th)}	0.5		1.5	V	$V_{DS} = V_{GS}, I_D = 250 \mu A$	
			48	67		V _{GS} = 4.5V, I _D = 2.5A	
Static Drain-Source On-Resistance	R _{DS} (ON)	_	50	70	-	V _{GS} = 4.0V, I _D = 2.5A	
		_	70	98		$V_{GS} = 2.5V, I_D = 2.5A$	
Diode Forward Voltage	V_{SD}			1.2	V	$V_{GS} = 0V, I_S = 0.6A$	
DYNAMIC CHARACTERISTICS (Note 8)							
Input Capacitance	C _{iss}		447	_			
Output Capacitance	Coss		54	_	pF	$V_{DS} = 10V, V_{GS} = 0V, f = 1.0MHz$	
Reverse Transfer Capacitance	C _{rss}	_	41	_			
Gate Resistance	R_G	_	23	_	Ω	$V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz$	
Total Gate Charge	Q_g	_	4.6	_		4500	
Gate-Source Charge	Q_{gs}	_	1.0	_	nC	$V_{GS} = 4.5V, V_{DS} = 15V,$ $I_{D} = 2.5A$	
Gate-Drain Charge	Q_{gd}	_	1.0	_		ID - 2.5A	
Turn-On Delay Time	t _{D(on)}	_	3.8	_			
Turn-On Rise Time	t _r	_	5.2	_	nS	V _{DD} = 15V, I _D = 1.25A, V _{GEN} = 4.5V,	
Turn-Off Delay Time	t _{D(off)}	_	15	_	1110	R_{GEN} = 10Ω	
Turn-Off Fall Time	t _f		6.1	_			

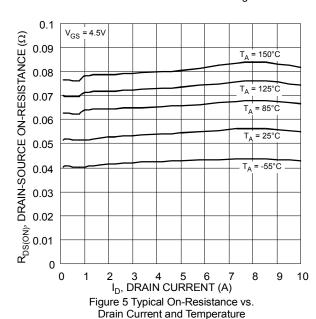
Notes:

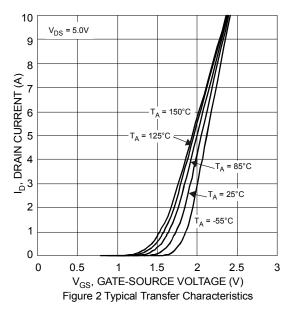
- 5. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper pad layout
- 7 .Short duration pulse test used to minimize self-heating effect.
 8. Guaranteed by design. Not subject to production testing.

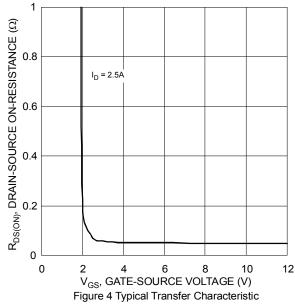












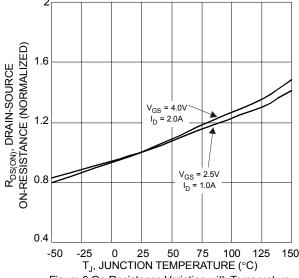
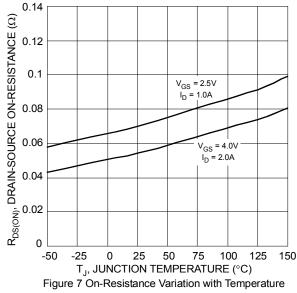
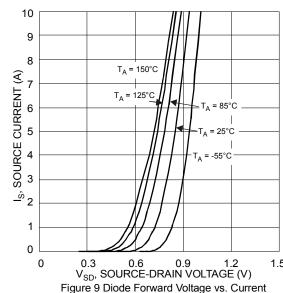
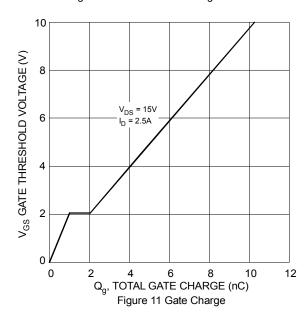


Figure 6 On-Resistance Variation with Temperature









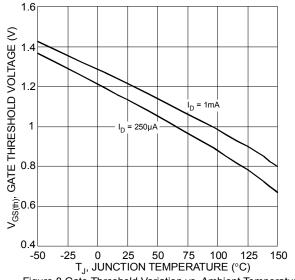
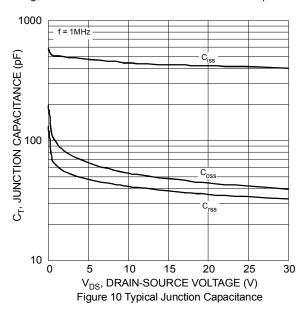


Figure 8 Gate Threshold Variation vs. Ambient Temperature



100
R_{DS(on)}
Limited

10
P_W = 10s
P_W = 10ms

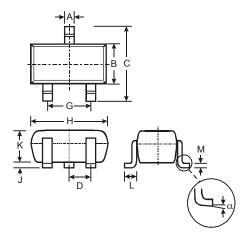
0.01
T_A = +25°C
V_{GS} = 4.5V
Single Pulse
DUT on 1 * MRP Board

0.001
V_{DS}, DRAIN-SOURCE VOLTAGE (V)
Figure 12 SOA, Safe Operation Area



Package Outline Dimensions

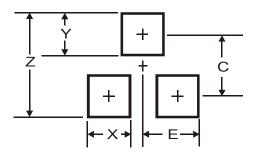
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for latest version.



SOT323							
Dim	Min	Max	Тур				
Α	0.25	0.40	0.30				
В	1.15	1.35	1.30				
С	2.00	2.20	2.10				
D	-	-	0.65				
G	1.20	1.40	1.30				
Н	1.80	2.20	2.15				
J	0.0	0.10	0.05				
K	0.90	1.00	0.95				
L	0.25	0.40	0.30				
M	0.10	0.18	0.11				
α	0°	8°	-				
All	All Dimensions in mm						

Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.



Dimensions	Value (in mm)
Z	2.8
Х	0.7
Υ	0.9
С	1.9
E	1.0



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Contact Us:

> Address:

401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd Minhang District, Shanghai , China

> Sales:

Direct +86 (21) 6401-6692

Email amall@ameya360.com

QQ 800077892

Skype ameyasales1 ameyasales2

Customer Service :

Email service@ameya360.com

Partnership :

Tel +86 (21) 64016692-8333

Email mkt@ameya360.com